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# **Charging effects in niobium nanostructures**

Torsten Henning

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## **Abstract**

Three types of metallic nanostructures comprising niobium were investigated experimentally; in all three types, electric transport at very low temperatures was governed by Coulomb blockade effects.

1. Thin film strips of niobium could be tuned into resistor strips by an electrochemical anodisation process, using microfabricated masks and *in situ* resistance monitoring. These resistors showed a transition from superconducting to insulating behaviour with increasing sheet resistance, occurring at a value approximately equal to the quantum resistance for Cooper pairs,  $h/(4e^2)$ .
2. Combining the anodisation technique with lateral size minimisation by shadow evaporation, devices in a single electron transistor-like configuration with two weak links and a small island between these were made. Direct evidence for the Coulomb blockade in the anodisation thinned niobium films was found when the transport characteristics could be modulated periodically by sweeping the voltage applied to a gate electrode placed on top of the structure.
3. ‘Conventional’ single electron transistors with Al base electrodes,  $\text{AlO}_x$  barriers formed *in situ* by oxidation, and Nb top electrodes were made by angular evaporation. The output current noise of such a transistor was measured as a function of bias voltage, gate voltage, and temperature. The low frequency noise was found to be dominated by charge input noise. The dependence of the noise on the bias voltage is consistent with self-heating of the transistor activating the noise sources.

## **Sammanfattning**

Tre typer av metalliska nanostrukturer innehållande niob har undersöks experimentellt. I alla tre typerna bestämdes den elektriska transporten vid mycket låga temperaturer av Coulomb-blockad-effekter.

1. Tunnfilmstrådar av niob kan förvandlas till resistorstrådar genom en elektrokemisk anodiseringprocess med mikrotillverkade masker och övervakning av resistansvärdet *in situ*. Dessa resistorer visar en övergång från supraleddande till isolerande beteende när ytresistansen ökar. Övergången uppträder vid ett värde i närheten av kvantresistansen för Cooperpar,  $h/(4e^2)$ .
2. Genom att kombinera anodiseringsteknik med lateral förminskning genom skuggförångning, tillverkades element med enelektrontransistor-lik geometri med två tunna länkar och en ö längre mellan. Bevis för Coulomb-blockad i dessa filmer som uttunnats genom anodisering, kunde direkt påvisas eftersom transportkarakteristikerna kunde moduleras periodiskt genom att svepa spänningen som lades på en grindelektron placerad ovanpå strukturen.
3. 'Konventionella' enelektrontransistorer med Al-baselektroder,  $\text{AlO}_x$ -barriärer framställda genom oxidering *in situ*, och Nb-toppelektroner har tillverkats med skuggförångning. Utgångsströmbruset av en sådan transistor har uppmäts som funktion av biasspänning, grindspänning och temperatur. Lågfrekvensbrusets var domineras av laddningsingångsbrus. Brusets beroende av biasspänningen kan förklaras med en aktivering av bruskällorna genom transistorns självuppvärmning.

## Zusammenfassung

Drei Typen von metallischen Nanostrukturen, die jeweils Niob enthielten, wurden experimentell untersucht; in allen drei Typen wurde der elektrische Transport bei sehr tiefen Temperaturen durch Coulomb-Blockade-Effekte bestimmt.

1. Dünnfilmstreifen aus Niob konnten mit einem elektrochemischen Anodisierungsprozeß zu Widerstandsstreifen getrimmt werden; dabei wurden mikrofabrizierte Masken verwendet und der Widerstand *in situ* kontrolliert. Diese Widerstände zeigten einen Übergang von supraleitendem zu isolierendem Verhalten bei zunehmendem Flächenwiderstand, der bei einem Wert nahe des Quantenwiderstandes für Cooperpaare,  $h/(4e^2)$ , auftrat.
2. Durch Kombination der Anodisierungstechnik mit Minimierung der lateralen Abmessungen mittels Schattenverdampfung wurden Elemente in Einzelelektronentransistor-Geometrie, mit zwei Schwachstellen und einer Insel dazwischen, hergestellt. Ein direkter Beleg für die Coulomb-Blockade in den anodisations-ausgedünnten Niob-Filmen wurde gefunden als es gelang, die Transportkennlinien periodisch mit einer an eine Gatterelektrode, die sich auf der Struktur befand, angelegten Spannung zu verändern.
3. 'Konventionelle' Einzelelektronentransistoren mit unteren Elektroden aus Al, durch *in situ*-Oxidation erzeugten  $\text{AlO}_x$ -Barrieren, und oberen Elektroden aus Nb wurden mittels Schattenbedampfung hergestellt. Der Ausgangsrauschstrom eines solchen Transistors wurde als Funktion der Vorspannung, der Gatterspannung und der Temperatur gemessen. Das niederfrequente Rauschen wurde dominiert von Eingangsladungsrauschen. Die Abhängigkeit des Rauschens von der Vorspannung ist konsistent mit einer Aktivierung der Rauschquellen durch die Selbstaufwärmung des Transistors.

## Résumé

Trois types de nanostructures métalliques comprenant du niobium ont été étudiés. Dans toutes les structures, le transport électrique aux très basses températures est gouverné par les effets de blocage de Coulomb.

1. Des lignes très fines de niobium ont été obtenues par lithographie électronique. Par la suite elles ont été affinées par un procédé d'anodisation électrochimique en contrôlant *in situ* la résistance des lignes. Leur comportement présente une transition entre un état supraconducteur et isolant lorsque leur « résistance carré » augmente. Cette transition se produit à une valeur environ égale à la résistance quantique par paire de Cooper,  $h/(4e^2)$ .
2. La combinaison des techniques d'anodisation et de réduction latérale de la ligne par évaporation inclinée a permis de réaliser des dispositifs comparables aux transistors à un seul électron ayant une petite île reliée à l'extérieur par deux liaisons faibles. La modulation de la tension appliquée à une grille placée au sommet de la structure génère une modulation des caractéristiques de transport. Cet effet met en évidence l'effet de blocage de Coulomb dans ces circuits de niobium obtenus par anodisation.
3. Des transistors « classiques » à un seul électron, avec des électrodes de base en Al, des barrières en  $\text{AlO}_x$  formées par oxydation *in situ*, et des électrodes supérieures en Nb ont été réalisés par évaporation inclinée. Le bruit du courant à la sortie de ces transistors a été mesuré en fonction de la tension de polarisation, de la tension de la porte et de la température. Les mesures ont montré que le bruit à basse fréquence est dominé par le bruit d'entrée de la charge. La dépendance du bruit de la tension de polarisation est compatible avec l'auto-échauffement du transistor qui active les sources de bruit.

# Contents

<b>List of Figures</b>	<b>13</b>
<b>Preface</b>	<b>15</b>
<b>1. Overview</b>	<b>19</b>
1.1. What is this thesis about? . . . . .	19
1.2. History of and motivation for this work . . . . .	21
<b>2. Background topics</b>	<b>25</b>
2.1. Tunnelling and superconductivity . . . . .	25
2.1.1. Tunnelling . . . . .	25
2.1.2. Superconductivity . . . . .	27
2.1.3. Superconductive tunnelling . . . . .	28
2.2. Charging effects . . . . .	29
2.2.1. Charging effects in very small tunnel junctions . . .	30
2.2.2. Charging effects in films and arrays . . . . .	32
2.2.3. Superconductor-insulator transition in thin films .	33
2.3. The single electron transistor (SET) . . . . .	35
2.4. Noise . . . . .	37
2.4.1. Noise nomenclature . . . . .	38
2.4.2. Low frequency noise . . . . .	40
2.5. Niobium . . . . .	41
2.5.1. Properties . . . . .	41
2.5.2. Niobium and its oxides . . . . .	42
<b>3. Nanofabrication with niobium</b>	<b>43</b>
3.1. Definition of nanosize patterns . . . . .	43
3.1.1. Lithographic and pattern transfer techniques . . .	43
3.1.2. Lithography and processing overview . . . . .	46
3.1.3. Computer aided design of nanostructures . . . . .	49
3.2. Fabrication methods . . . . .	51

## *Contents*

3.2.1. Criteria for a Nb nanofabrication technique . . . . .	51
3.2.2. Other fabrication techniques in single electronics . .	52
3.2.3. Techniques for the fabrication of multigranular systems	54
3.2.4. The Niemeyer-Dolan technique . . . . .	56
3.2.5. Competing Nb nanojunction fabrication techniques .	58
3.3. Shadow evaporation patterning of niobium . . . . .	59
3.3.1. Resists for the Niemeyer-Dolan technique . . . . .	59
3.3.2. Four layer resist . . . . .	62
<b>4. Anodised niobium nanostructures</b>	<b>67</b>
4.1. Anodic oxidation . . . . .	67
4.1.1. Principle and History . . . . .	67
4.1.2. Micro- and nanofabrication by anodisation . . . .	68
4.2. Microanodised niobium resistors . . . . .	69
4.2.1. Physical setup . . . . .	69
4.2.2. Electrical setup . . . . .	72
4.2.3. Anodisation dynamics . . . . .	73
4.3. Measurement setup and procedures . . . . .	75
4.3.1. Cryogenics . . . . .	76
4.3.2. Amplifier electronics . . . . .	76
4.3.3. Shielding and filtering . . . . .	77
4.4. Resistor samples . . . . .	77
4.4.1. Sample geometry and characterisation . . . . .	77
4.4.2. Superconductor-insulator transition . . . . .	81
4.4.3. Onset of the Coulomb blockade . . . . .	84
4.4.4. No gate effect . . . . .	87
4.5. Samples in SET-like geometry . . . . .	88
4.5.1. Fabrication technique . . . . .	88
4.5.2. IVC and gate effect . . . . .	92
4.5.3. Temperature dependence of the gate effect . . . .	96
4.6. Conclusion: anodised niobium nanostructures . . . . .	97
<b>5. Noise in a single electron transistor</b>	<b>99</b>
5.1. Noise model . . . . .	99
5.2. Sample fabrication and characterisation . . . . .	102
5.2.1. Fabrication . . . . .	102
5.2.2. DC characterisation . . . . .	105
5.3. Noise measurement setup . . . . .	108
5.3.1. Transimpedance amplifier . . . . .	109
5.3.2. Amplifier noise . . . . .	110
5.4. Measurement results . . . . .	111

## *Contents*

5.4.1. Gain determination . . . . .	111
5.4.2. Current noise spectral density . . . . .	111
5.4.3. Gain dependence of the current noise . . . . .	113
5.4.4. Resistance fluctuations . . . . .	116
5.5. Deviations from ideal charge noise behaviour . . . . .	117
5.5.1. Bias dependence . . . . .	117
5.5.2. Temperature dependence . . . . .	118
5.5.3. Model calculation of the self-heating . . . . .	120
5.5.4. Zero gain noise . . . . .	121
5.6. Conclusion: noise in a single electron transistor . . . . .	121
<b>6. Conclusion</b>	<b>125</b>
6.1. What's new? What's useful? What's not? . . . . .	125
6.2. Suggestions for future research . . . . .	126
<b>Bibliography</b>	<b>127</b>
<b>A. Symbols and notation</b>	<b>147</b>
<b>B. Glossary and abbreviations</b>	<b>151</b>
<b>C. Recipes</b>	<b>159</b>
C.1. Substrate preparation . . . . .	159
C.1.1. Photomask making (positive resist process) . . . . .	159
C.1.2. Photomask making (negative resist process) . . . . .	160
C.1.3. Gold pad photolithography (carrier chips) . . . . .	160
C.2. Niobium nanofabrication . . . . .	161
C.2.1. Four layer resist preparation . . . . .	161
C.2.2. Four layer resist exposure . . . . .	162
C.2.3. Four layer resist proximity correction . . . . .	162
C.2.4. Parameters for SET fabrication . . . . .	162
C.2.5. Four layer resist processing . . . . .	162
C.3. Niobium microanodisation . . . . .	163
C.3.1. Anodisation window mask . . . . .	163
C.3.2. Electrolyte for Nb anodisation . . . . .	163
<b>D. Measurement data handling</b>	<b>165</b>
<b>E. Selected publications 1994–1998</b>	<b>175</b>

*Contents*

# List of Figures

2.1.	Tunnelling between two metallic conductors . . . . .	26
2.2.	SET: IVC and modulation curves; R-bias and V-bias . . . . .	36
3.1.	Etch patterning vs. liftoff patterning . . . . .	45
3.2.	Nanofabrication process steps . . . . .	47
3.3.	CAD/CAM for nanostructure EBL . . . . .	50
3.4.	Niemeyer-Dolan technique for the fabrication of SET . . . . .	57
3.5.	Four layer resist processing . . . . .	63
3.6.	Surface contamination after etch processing . . . . .	66
4.1.	Niobium microanodisation setup . . . . .	70
4.2.	Anodisation voltage and sample resistance . . . . .	74
4.3.	Slow anodisation process at constant voltage . . . . .	75
4.4.	Dilution refrigerator with filters . . . . .	78
4.5.	Anodisation mask and geometry of resistor samples . . . . .	79
4.6.	Magnetic field effect on resistor sample IVC . . . . .	80
4.7.	IVC of three resistor samples . . . . .	82
4.8.	Arrhenius dependence of the zero bias differential resistance . . . . .	83
4.9.	Definition of $V_{\text{off}}^0$ . . . . .	85
4.10.	Onset of CB in resistor samples . . . . .	86
4.11.	Anodised Nb wire with top gate (no gate effect) . . . . .	87
4.12.	Double anodisation sample (no gate effect) . . . . .	88
4.13.	Shadow evaporation and anodisation technique for the fabrication of SET-like structures . . . . .	89
4.14.	Mask for fabrication of SET-like devices by angular evaporation . . . . .	90
4.15.	Variable thickness weak links in Nb wire . . . . .	90
4.16.	IVC for gate leakage . . . . .	91
4.17.	Coulomb blockade in an SET-like anodised structure . . . . .	93
4.18.	Control curves for an SET-like anodised structure . . . . .	94
4.19.	IVC of an SET-like anodised structure with gate modulation	95

*List of Figures*

4.20. Temperature dependence of gate modulation . . . . .	96
5.1. C-SET: Input and output quantities, parameters, noise sources	100
5.2. SET with Nb leads and Al island . . . . .	103
5.3. AFM image of an array of SET test structures . . . . .	104
5.4. IVC and noise measurement points . . . . .	107
5.5. Setup for SET noise measurements . . . . .	109
5.6. Input referred noise at maximum gain . . . . .	112
5.7. Current noise and gain as a function of gate charge . . . . .	114
5.8. Current noise as function of gain . . . . .	115
5.9. Current noise as function of gain for several bias points . .	117
5.10. Differential charge equivalent noise as function of bias for three different temperatures . . . . .	119
5.11. Zero gain (extrapolated) noise . . . . .	122
C.1. Geometric design parameters for shadow evaporated SET .	162
D.1. ADP organisation . . . . .	166

# Preface

This thesis is the result of work that I have done in the years 1994 to 1998 in the Applied Solid State Physics group at Chalmers and Göteborg University, and at the Swedish Nanometre Laboratory.

Experimental results have been published in the following conference contributions and papers:

- Torsten Henning, D. B. Haviland, and P. Delsing. Transition from supercurrent to Coulomb blockade tuned by anodization of Nb wires. *Czech. J. Phys.*, 46(Suppl. S4):2341–2342, 1996. Proc. 21st Int. Conf. on Low Temperature Physics, Prague, August 8–14, 1996.
- Torsten Henning, D. B. Haviland, and P. Delsing. Fabrication of Coulomb blockade elements with an electrolytic anodization process. *Electrochemical Society Meeting Abstracts*, 96-2:561, 1996. Fall Meeting San Antonio, Texas, October 6-11.
- Torsten Henning, D. B. Haviland, and P. Delsing. Charging effects and superconductivity in anodised niobium nanostructures. In H. Koch and S. Knappe, editors, *ISEC'97. 6th International Superconductive Electronics Conference. Extended Abstracts*, volume 2, pages 227–229, Berlin, June 1997. Physikalisch-Technische Bundesanstalt.
- Torsten Henning, D. B. Haviland, and P. Delsing. Coulomb blockade effects in anodized niobium nanostructures. *Supercond. Sci. Technol.*, 10(9):727–732, September 1997. [cond-mat/9706302](#).
- Torsten Henning, B. Starmark, T. Claeson, and P. Delsing. Bias and temperature dependence of the noise in a single electron transistor. accepted by *Eur. Phys. J. B* 1998-10-12, [cond-mat/9810103](#).
- B. Starmark, Torsten Henning, A. N. Korotkov, T. Claeson, and P. Delsing. Gain dependence of the noise in the single electron transistor. [cond-mat/9806354](#).

The *monografiavhandling* style was chosen with the best intentions of reader friendliness [1].

There are so many people that I am indebted to after these years, and I will try to name them here with no particularly deep thoughts about the order. First of all (and here order is intentional), I would like to thank Tord Claeson for giving me the chance to work in his excellent [2] group, and for his continued interest in the progress. And for paying me for having all this fun, of course. Another big Thank You to Per Delsing, whose Single Electron Tunnelling group I joined and who has supported me in every way from day one, and to David Haviland, who got me on the niobium anodisation track. I fondly remember the extensive and inspiring lunch time discussions with Per and David and Yuichi Harada, ChiiDong Chen, Magnus Persson, Joakim Pettersson and Peter Wahlgren. From Per Davidsson, I learned a lot about low temperature physics in general and Old Dil in particular. The work during the last year has profited very much from the cooperation with Björn Starmark, whose amplifier was not only well-designed, but absolutely physicist-proof. My other fellow PhD students contributed in one way or another, not least by creating a very pleasant atmosphere at the workplace: Tobias Bergsten, Karin Andersson, Denis Chouvaev, Linda Olofsson, our *exjobbare* Pål Dahle, and all the High- $T_c$  students that I will not enumerate more for the fear of forgetting one than out of space concerns. Edgar Hürfeld and Oliver Kuhn were welcome additions to our Little Germany in the SET group, and always good for a discussion or two.

Experimental physics is twice the fun if you are blessed with a technical staff like ours: Staffan Pehrson can build anything, and Henrik Fredriksen installed the niobium system and kept it alive at working hours that would be considered odd even for a student. Alex Bogdanov did the same thing for the JEOL lithography, and I learned much about nanofabrication from him. Of the people I met in the nanolab, Julie Gold was particularly helpful. Ann-Marie Frykestig taught me that less bureaucracy is better, something you can only appreciate fully when you have experienced the opposite.

Bengt Nilsson deserves a paragraph of his own.

On second thought, make that two. We all know why, and I won't say it here, because we would not want another laboratory to hire him away from us, right?

During these five years overseas, I have made some very dear new friends, and kept old ones. I think that these acknowledgements should be restricted to contributions that are directly related to this thesis, so sorry, being a friend gets you a place in my heart, but not on these pages. Andreas Klinkmüller might meet the contribution criterion, though, for

helping me when he found me clueless at something that was obviously called a “tc-shell prompt”. Things have developed a little, and this thesis is proudly made with Linux.

Starting in 1995, I have had much fun during some incredibly active (and productive) weeks in the nanolab, digging trenches in semiconductor heterostructures with my best friend, Peter Klar. Where is the connection with this thesis, one may ask? There is appendix E.

Finally, let’s talk about money again. My first year here was financed by the German Academic Exchange Service (DAAD), and I am very grateful to the German taxpayers for risking this investment. The taxpayers of Europe have subsequently fed me via several programmes, and deserve my heartfelt thanks as well.

Göteborg, 24th of January, 1999  
Torsten Henning



# 1. Overview

This chapter contains, first, a brief orientation on where the subject of this thesis is located within physics. This may be skipped immediately by anyone who can interpret the thesis' title without help. Secondly, there is a summarising overview that casts light on the motivation for and the connections between the different parts of this work.

## 1.1. What is this thesis about?

It is about **solid state physics**, predominantly about the electronic properties of the solid state. This encompasses phenomena which can be understood in terms of the Fermi Liquid Theory, which tells us that the behaviour of interacting electrons can be understood in terms of independent electrons with slightly modified properties, as well as phenomena that can only be understood as the consequence of collective effects (e.g. superconductivity).

It is about **electronics**, the science and art of designing solid state systems in which the laws governing the motion of electrons are exploited to produce or manipulate useful electrical, usually time dependent, quantities that we call signals.

It is about **three terminal devices**, the bread and butter of electronics. In a three terminal device, an electrical current between two terminals is influenced by the potential applied to, or the current sent into, the third terminal. In digital electronics, three terminal devices are used as switches opening or closing a current path. The classical three terminal devices are the thermionic tube, the bipolar transistor and the field effect transistor. A lot of novel three terminal devices are under development [3].

It is about **miniaturisation**. Electronics have experienced a series of booms when new three terminal devices were introduced and quickly became dominant in most applications. This progress is intimately linked to the continuing miniaturisation of devices and the consequent integration and complexity that these devices make possible.

## 1. Overview

It is about **single electronics**. In each new generation of three terminal devices, fewer and fewer electrons are needed per switching process. On the horizon, we now see a limit where only a single electron is needed to switch a device completely. The device still contains bazillions of electrons, but the presence or absence of just one electron makes all the difference! We will have to come back to that.

It is about **tunnel junctions**. One of the first applications of quantum mechanics, tunnelling has been understood since the 1920s. Basically, tunnelling means that a particle that has been on one side of a region that it cannot enter (because it does not have enough energy) can, after a certain time and with a certain probability, be found on the other side of that forbidden region (*barrier*).

It is about **very small capacitors** with very small capacitances. Tunnel junctions can be made with such small capacitances that the energy associated with charging them with a single elementary charge (the *characteristic charging energy*) gives rise to a substantial voltage over the capacitor.

It is about **the Coulomb blockade**. Said 'substantial voltage' can be so high that it prevents the tunnelling of further electrons until the tunnelled charge has been removed to the environment of the junction.

It is about **very low temperature physics**. To observe the Coulomb blockade, the thermal energy of the electrons must be considerably below the characteristic charging energy. We will do the calculations later, but suffice it to say that contemporary single electronics usually involves advanced cryogenics, typically with a dilution refrigerator that can cool samples to millikelvin temperatures continuously.

It is about **nanostructures**. Calculations will show that the critical sample dimensions for the Coulomb blockade to be observable are in the range of one hundred nanometres, where deep submicron technology gets dubbed *nanotechnology*.

It is about **mesoscopic physics**. On this length scale, not all of the laws of solid state physics, often derived assuming infinite system size, are valid without modification. On the other hand, the behaviour of such small systems is still different from that of single atoms and molecules. The twilight zone between solid state physics (*macroscopic physics*) and atomic and molecular physics (*microscopic physics*) is where *mesoscopic physics* happens. This is one of the most interesting areas of solid state physics because almost everything we know about the solid state in bulk may need to be reexamined at small length scales.

It is about **single electron transistors**, the first useful single electronics device invented. Their current-voltage characteristics depend on

## *1.2. History of and motivation for this work*

the number of electrons on a small island separated from two terminals by very small tunnel junctions, and are switched between extremal characteristics when the charge of the island is varied by half an elementary charge.

It is about **electrometry**. With another small capacitor as the third terminal, the single electron transistor can be used as a very sensitive measurement instrument for electrical charges.

It is about **noise**. Noise, that is unwanted signals following along with and adding to the useful signals, limits the performance of any electronic device. In single electronics, noise can limit the accuracy of the current standard, or the possibility to store bits of information represented by single electrons. An understanding of the noise is slowly emerging.

It is about **superconductivity**. Operating single electronics devices in the superconducting state is interesting from the physical basic research point of view, and may even be beneficial for some applications. Most single electronics materials become superconducting at the typical operation temperatures.

It is about **niobium**. Niobium is an interesting material because it has the highest superconducting transition temperature of all elements, which, together with its durability, made it the standard material of established low temperature electronics (which is practically synonymous to Josephson electronics). It is hard to handle, though, due to its metallurgical properties that we will examine in detail later.

It is about **a superconductor-insulator transition**. Increasing the disorder in thin superconducting films, an indicator of which is the resistance, can cause a transition between superconducting and insulating behaviour at low temperatures.

And last, but not least, it is about a fair amount of **nanofabrication techniques**, or “technology”. There are no industrial standard techniques for single electronics and no commercial foundries, so if one wants to examine the properties of a single electronics device, one has to fabricate it first. Especially with the introduction of relatively new materials like niobium, figuring out the right fabrication process may be more time and resource consuming than the actual measurements on the device.

## **1.2. History of and motivation for this work**

The work documented in this thesis started out with a project aiming at developing a new method for the fabrication of very small, high ohmic resistors. Such resistors would have a very small stray capacitance and should

## 1. Overview

be of interest for experiments on the effect of the electromagnetic environment on the behaviour of single electron transistors or single ultrasmall junctions [4, 5]. They were expected to play a role in the attempt to raise the operating frequency of the SET by integrating it with a HEMT [6, and references therein].

The fabrication method we chose to explore was the controlled anodic oxidation of nanofabricated niobium wires. We later found that the idea of raising and tuning the resistance value of thin film resistors by anodic oxidation was not exactly brand new [7].

The technological challenge could be broken up into three parts:

1. Definition of deep-submicron niobium wires and electrical connections by a suitable process,
2. Definition of a microfabricated anodisation mask laterally confining the region to be anodised, and
3. Implementation of a resistance monitoring setup and anodisation voltage control procedure.

Since some previous knowledge about niobium nanofabrication by liftoff processing was available locally [8], and it was obvious that this technique would be useful for tunnel junction device fabrication [9], we chose to employ liftoff processing already at this stage (as opposed to an etching process starting from predeposited niobium). Chapter 3 will treat the nanofabrication issues in detail as far as they are relevant for all parts of this work.

The anodisation mask and processing details are the subject of section 4.2. The samples produced were characterised by very low temperature transport measurements, described in section 4.3. This section will also be important for the subsequent chapter 5 on noise measurements, since the same measurement equipment was used for all very low temperature experiments.

While characterising the resistor samples, we found that they showed a Coulomb blockade when the sheet resistances exceeded a few kilohm (see 4.4). We then tried to modulate this blockade like in the experiments of Chandrasekhar and Webb [10, 11], to demonstrate its charging effect nature, and in the hope of building some kind of device. It turned out, however, that the anodised niobium wires were such a fine grained system that gating them failed to produce a modulation of their current-voltage characteristics. It was not until we modified the deposition process into a shadow evaporation process, producing sub-100 nm lateral structures,

## *1.2. History of and motivation for this work*

that we were able to show the electric field effect in an anodised niobium variable thickness wire system. Section 4.5 elaborates on these processes and measurements.

By this time, the interest in the resistors as such had declined. Resistors consisting simply of arrays of relatively large tunnel junctions worked nicely for the purposes of the SET-HEMT integration project [6].

Since the resistors now seemed only useful in combination with niobium based junctions, it was decided to proceed with fabrication and characterisation of the latter. Special attention was paid to their low frequency noise properties, since there were (and still are) considerable gaps in our understanding of this noise that is severely limiting the operation of single electronics devices. Chapter 5, elaborating these investigations, is outlined as follows. The specific details on the fabrication process, not covered in the general fabrication background of chapter 3, are given in section 5.2. We were in the fortunate situation of having a very low noise current amplifier (see 5.3), which allowed us not only to corroborate previous findings about the gain dependence of the low frequency noise [12,13] (see 5.4), but also gave new insight into its bias and temperature dependence (5.5).

*1. Overview*

## 2. Background topics

### 2.1. Tunnelling and superconductivity

Effects associated with tunnelling have been observed early in the twentieth century, and tunnelling has been one of the first cases where quantum mechanics was essential for the understanding of experimental findings. Superconductivity had already been discovered by that time, but it had not yet been recognized as a new thermodynamic state. Both phenomena are closely linked not only because both can only be explained in quantum mechanical terms, but also because much of our knowledge about superconductivity comes from tunnelling experiments.

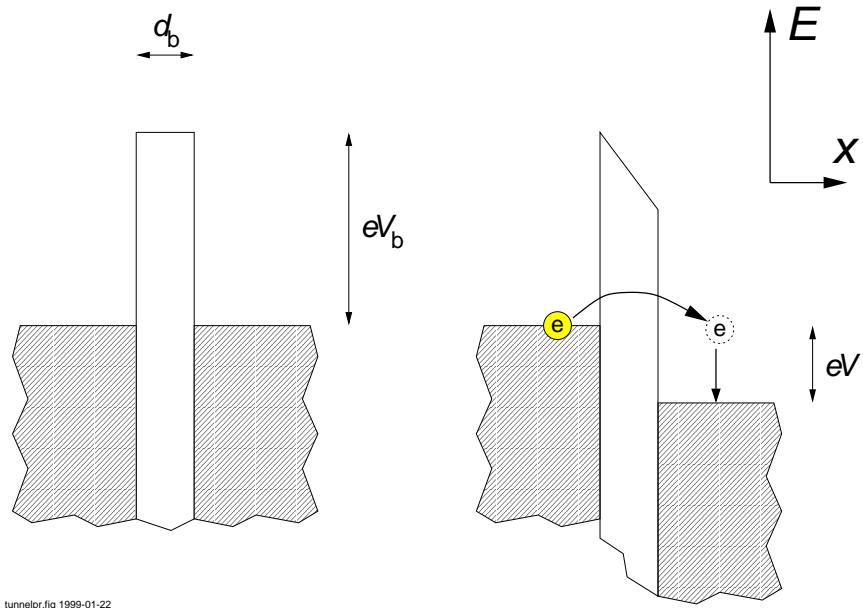
#### 2.1.1. Tunnelling

Consider a conduction electron with energy  $E$  near the Fermi surface in a region that we call ‘left electrode’, and an adjacent region called ‘barrier’ where the conduction band edge lies at a higher energy. On the other side of the barrier we have the ‘right electrode’. Even if the Fermi energy in the right electrode is different from that in the left electrode, classical physics would prohibit the transmission of the electron. Quantum mechanics, however, predicts a nonvanishing transmission through the barrier as long as it is finite in height (energetic) and width (in real space).

A voltage applied between left and right electrode results in a current flow. For small voltages, the current-voltage characteristics are linear and define a tunnelling resistance  $R_T$ . Tunnelling processes are classified as elastic, if the energy of the tunnelling particle is conserved, or inelastic. In the latter case, dissipation occurs through excitations in the barrier, the electrodes, or the electrode-barrier interfaces. Figure 2.1 is a schematic representation of the tunnelling between two metallic conductors.

Two examples of systems showing tunnelling are metallic tips producing field emission, and structures with a thin insulator separating two conductors. In the first case, the ‘left electrode’ is the metal tip, and the

2. Background topics



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**Figure 2.1.:** Tunnelling between two metallic conductors separated by a barrier of height  $eV_b$  and width  $d_b$ . In the right picture, the junction is biased with a voltage  $V$ , favouring tunnelling of electrons from the left to the right electrode. Dissipation will occur in the right electrode after the tunnelling, bringing the tunnelled electron closer to the Fermi level again.

## 2.1. Tunnelling and superconductivity

barrier is created by the work function, i. e. the energy needed to move an electron from the conductor to infinity. An electric field tilts the vacuum level, resulting in a triangular shaped barrier that allows the emission of electrons into vacuum ('right electrode'). This effect is not only of historical interest as an early verification of quantum mechanics (observed by Lilienfeld in 1922 and explained by Fowler and Nordheim in 1928), it is also of technological importance as the working principle of advanced electron guns in electron beam lithography machines. The second example, conductor-insulator-conductor structures in different varieties, is the main subject of this thesis.

### 2.1.2. Superconductivity

Below a critical temperature  $T_c$  and critical magnetic field  $H_c$ , certain materials are in a thermodynamic state called the 'superconducting state'. It manifests itself in a number of effects. The first effect discovered was the vanishing of the electrical resistance, which gave the phenomenon its name [14]. Of at least equal importance is the fact that superconductors (type I, the only superconductors known at that time) expel magnetic fields, the Meissner-Ochsenfeld effect [15].

We will in this report only be dealing with so-called 'low temperature' superconductors. These materials are rather well understood theoretically, much better than the 'high temperature' superconductors that were discovered just more than a decade ago [16]. A microscopic theory that is well confirmed experimentally is that of Bardeen, Cooper and Schrieffer (BCS, [17]). Pairs of electrons in time reversed states (opposite spin and wave vector) interact by exchange of virtual phonons, leading to an attractive interaction and the formation of so-called 'Cooper pairs'. A collective effect results in the formation of a ground state that has a lower energy than the electron-filled Fermi sphere, and a gap in the density of states opening up around the Fermi energy. The energetic width of this gap is  $2\Delta$ , the energy required to break up a Cooper pair and create an excitation.

The density of states has a singularity at the gap edges. It was measured by Giaever [18] in tunnelling experiments which gave a direct verification of the BCS theory.

Characteristic material parameters are the gap (at zero temperature)  $\Delta(0)$ , the London penetration depth  $\lambda$ , the characteristic length over which a magnetic field drops at the superconductor surface, and the coherence length  $\xi$ , over which the Cooper pair density varies. The critical temperature is related to the gap at zero temperature, and the gap energy vanishes at the critical temperature. Niobium is the element with the highest criti-

## 2. Background topics

cal temperature (at ambient pressure),  $T_c \approx 9.2$  K in bulk, corresponding to a gap of  $2\Delta \approx 3$  mV. The gap is reduced in thin films, considerably below 50 nm thickness [19]. The London penetration depth of niobium is  $\lambda = 32$  nm [20], and the coherence length  $\xi = 39$  nm [20].

### 2.1.3. Superconductive tunnelling

By *superconductive tunnelling*, we mean tunnelling between two electrodes, of which at least one is in the superconducting state, via an insulating barrier. This type of system is usually denoted as an SIS junction (both electrodes consist of the same superconducting material), SIN junction (one electrode is normal conducting), SIS' junction (two different superconductors), and so on. Two types of tunnelling are of particular importance, namely Giaever tunnelling [18] and Josephson tunnelling [21].

#### Giaever tunnelling

The net quasiparticle (electron) current  $I$  between the two electrodes under consideration is proportional to the densities of states  $\varrho_i$  on both sides, a transition matrix element  $M$ , and the difference in occupation of the Fermi distributions. Assuming a constant  $M$ , a sharp edge of the Fermi distributions  $f_i$  (that is, low temperature), and assuming that the difference in Fermi levels is equal to the voltage  $V$  between the electrodes, one can probe the densities of states on both sides. If one of the electrodes is normal conducting, one can assume  $\varrho_N = \text{const.}$ , and the current-voltage characteristics directly reflect the superconducting energy gap. The IVC of an NIS junction has a zero current branch between the voltages  $\pm \frac{\Delta}{e}$ , and current flow sets in at these voltages. Farther away from the origin, the IVC approach an ohmic asymptote.

For an SIS' junction, there is a zero current branch between  $\pm (\frac{\Delta_1 + \Delta_2}{e})$ , except for small current peaks at  $\pm (\frac{\Delta_2 - \Delta_1}{e})$ . At  $\pm (\frac{\Delta_1 + \Delta_2}{e})$ , strong current flow sets in, again with asymptotically ohmic behaviour. We use this feature in 5.2.2, where we consider SIS' junctions with S=Nb and S'=Al.

#### Josephson tunnelling

While in the processes considered so far, Cooper pairs are first broken by applying some finite voltage, before their constituting electrons tunnel, Cooper pairs can also tunnel without breaking. This results in a current-voltage characteristic with a zero voltage branch, called the *supercurrent*. Every junction has a characteristic maximum supercurrent, and once this

## 2.2. Charging effects

maximum is exceeded, the IVC jump to a stable state at finite voltage and current. Josephson tunnelling is only observed in junctions with sufficiently transparent barriers.

The maximally possible supercurrent (Josephson pair current) has the following dependence on the phase difference  $\gamma = \phi_r - \phi_l$  between the wavefunctions of the condensates in the two electrodes [22]:

$$I_c = I_{c0} \sin \gamma. \quad (2.1)$$

The coupling between the superconductors is often expressed in terms of a coupling energy

$$E_J = \frac{\hbar}{2e} I_{c0}. \quad (2.2)$$

In many respects, the described (DC) Josephson effect is a dual analog to the Coulomb blockade [23] that will be discussed below. By combining two SIS Josephson junctions in parallel, forming a loop, one can build a device called a DC SQUID, whose critical current is very sensitively dependent on the magnetic flux penetrating the loop, with a periodicity of only one flux quantum. The DC SQUID is the basis for the most advanced magnetometers available today.

Another Josephson effect is the generation of high frequency electromagnetic radiation in a junction. By locking external microwaves to the radiation in an array of junctions, this AC Josephson effect is exploited metrologically by linking the representation of the voltage unit to a frequency standard.

## 2.2. Charging effects

In this section, we will give some background on a group of phenomena known as charging effects, the most important of which is the Coulomb blockade. Though some charging effects have been suggested almost half a century ago [24], it was not after they had been observed in purposely designed systems that the word *Coulomb blockade* was coined [25, 26] (a close predecessor is *Coulomb suppression*, [27]). We will not proceed historically, but roughly reverse chronologically, starting with the relatively well understood single and few junction systems and ending with thin films that are still much more of an open field.

## 2. Background topics

### 2.2.1. Charging effects in very small tunnel junctions

In the previous section 2.1, we introduced metal-insulator (oxide)-metal junctions with a tunnel resistance  $R_T$ . This structure is reminiscent of a parallel plate capacitor with the barrier oxide as dielectric, and in fact, investigations have shown that the formula for the parallel plate capacitor's capacitance,

$$C = \frac{1}{\varepsilon_0 \varepsilon} \frac{A}{d}, \quad (2.3)$$

where  $A$  is the area and  $d$  the distance between the plates (that is the thickness of the oxide), holds down to very small dimensions.

Whenever an electron tunnels through the junction, the capacitor's charge changes by the amount of an elementary charge, and accordingly, its charging energy

$$E_{\text{ch}}(Q) = \frac{Q^2}{2C} \quad (2.4)$$

changes by

$$\Delta E_{\text{ch}} = E_{\text{ch}}(Q) - E_{\text{ch}}(Q \pm e) \in [-E_c, +E_c], \quad (2.5)$$

with the characteristic charging energy

$$E_c = \frac{e^2}{2C}. \quad (2.6)$$

Suppose we miniaturise the junction so much that  $C \lesssim 1 \text{ fF}$ , then the characteristic charging energy will be of the order of  $100 \mu\text{eV}$ , which in turn corresponds to a characteristic temperature  $T_c = E_c/k_B$  of about 1 K. At very low temperatures, those attainable with a dilution refrigerator for example, this characteristic charging energy is non-negligible.

Making such junctions, however, was a technological challenge not solved until well into the 1980's, because the lateral dimensions have to be rather small. Suppose we have a dielectric permeability  $\varepsilon = 10$  and an oxide thickness of 1 nm, then the area for the junction to give  $C \lesssim 1 \text{ fF}$  must be less than approximately 100 nm squared. Nowadays, making such small junctions is a known technology thanks to the progress in deep submicron processing, especially in electron beam lithography.

If a junction of the kind described above, which we will refer to as a *very small junction*, is charge neutral initially, tunnelling of an electron would increase the charging energy by the characteristic charging energy and is thus prohibited; this is the phenomenon called *Coulomb blockade*. If we could increase the charge on the electrodes steadily by moving the electron

## 2.2. Charging effects

cloud in the circuit with respect to the lattice, we would reach a point where tunnelling would suddenly decrease the charging energy at which an electron would actually tunnel. Continuing to displace the charge, we would reach the initial state again half a cycle later, and everything would start all over again. The charging energy would cause a time correlation of the tunnelling events [28] and a voltage oscillation (*SET-oscillation*) [25] with a frequency

$$f = \frac{I}{e}. \quad (2.7)$$

Metrologists love an equation like (2.7), because it relates a quantity that is defined in a cumbersome way and hard to measure ( $I$ ) to a quantity that is relatively easily defined in the laboratory ( $f$ ) via nothing but a natural constant.

Nature is not that kind, though.

Steadily displacing the charge means biasing the junction with a current. Unlike an electrochemical potential, a current is not a thermodynamic variable of state. Fixing a potential, i.e. voltage biasing a sample, is much more natural than current biasing.

In this special case, the key to understanding lies in the environment of the junction. The minimalist circuit involving a very small tunnel junction contains at least a source of some kind and two leads from the source's ports to the junction electrodes.

Speaking in electrotechnical terms now: even if we had a perfect current source, the stray capacitance of the leads would still act as a shunt and introduce a voltage bias component, and since the junction capacitance we are talking about is so small, even a few millimeters of lead are enough to destroy the charging effects.

The effect of the electromagnetic environment on very small tunnel junctions has been an important part of the research ever since the first such junctions were made [29–33], and it is a field still evolving both experimentally and theoretically. A proposed type I perpetuum mobile [34] demonstrates the importance of always considering the environment together with a very small junction.

To observe the Coulomb blockade, and SET oscillations, one has to protect the very small tunnel junctions against the shunting influence of the environment. This can be done by surrounding it with thin film resistors [4, 35, 36], or even easier, with other junctions, producing a one or two dimensional array. The special (and simplest) case of the two junction one dimensional array leads us to the device called the single electron transistor, discussed in 2.3.

## 2. Background topics

### 2.2.2. Charging effects in films and arrays

The other extreme way of surrounding a junction with other junctions is to include it in a large, possibly irregular, two dimensional array. Lithographically made arrays of this kind have been investigated for some time now [37, and references therein]. Small superconducting arrays consisting of just a few junctions and holes have given new insight into the interplay between charges (Cooper pairs) and vortices [38–40]. Large arrays, however, still pose considerable lithographical problems, namely in getting them homogeneous, and there are gaps in our understanding of phenomena such as the Hall effect [41, and references therein].

#### Granular films: discovery of the charging effect

Already in 1951, Gorter [24] suggested that the observed increase of the resistance in thin films at low temperatures and low bias might be due to a granular structure of these films and to charging effects, by virtue of which the charge transfer (by tunnelling) between the grains is impeded. This paper is generally regarded as the beginning of single electronics.

A decade later, Neugebauer and Weller [42] made transport measurements on ultrathin metal films prepared by evaporation. These films had a granular structure, as was demonstrated by TEM imaging. An Arrhenius type dependence of the resistance on temperature was found, and explained within a model of the film as a planar array of small islands connected by tunnel junctions and affected by charging effects.

Intentionally created small particles, made with the aim of studying superconductivity at small dimensions, were used in another classical experiment by Giaever and Zeller [43, 44]. They made Al-AlO<sub>x</sub>-Al junctions ( $T_{c,Al} = 1.2\text{ K}$ ) and embedded tin particles ( $T_{c,Sn} = 3.7\text{ K}$  in bulk) in the oxide. The finite size of the grains caused a finite spacing of energy levels in them, so that the Fermi levels in the grains and in the electrodes would not line up. Nonlinear current-voltage characteristics, with a feature we today call the Coulomb blockade, were observed and could be explained assuming a distribution of grain sizes. As a byproduct, these measurements indicated that superconductivity in small Sn particles persisted down to the smallest particle sizes of 5 nm.

The third experiment that lay the foundation to single electronics was made by Lambe and Jaklevic [45, 46]. They made a sandwich structure consisting of a base electrode, an oxide layer transparent for tunnelling electrons, a layer of small particles, another oxide layer, but much thicker than the first one and opaque to tunnelling electrons, and a top electrode.

## 2.2. Charging effects

The top electrode provided a capacitive coupling to the grains, and in modern terminology, we would describe their system as a parallel coupling of (inhomogeneous) *single electron boxes* [47–49]. Capacitance measurements showed that with increasing voltage, the small particles were charged stepwise by tunnelling through the thinner barrier. By applying an external field, the energy levels in the grains could be modulated. This field effect device is the ancestor of modern three terminal charging effect devices like multiple tunnel junction systems (see 3.2.3) or the single electron transistor (see 2.3).

### Development after 1975: from theory to devices

The theory of the charging effect started with a 1975 paper by Kulik and Shekhter [50], giving a quantum mechanical treatment with a charging Hamiltonian and a tunnelling Hamiltonian. They calculated the current-voltage characteristics for tunnelling through a small grain, that is, for a double junction system, and predicted a step structure in the characteristics in the case of asymmetric junctions. This effect has been verified experimentally, e.g. by Wilkins et al. [51] using an STM, and is known as the *Coulomb staircase* [52].

In 1982, Widom et al. [53] pointed out the duality between the Josephson effect and the *current bias frequency effect* we know today by the name of *Bloch oscillations*. The theory of these oscillations was worked out by Likharev and Zorin in 1984/1985 [54, 55].

Oscillations occurring even in junctions with normal conducting electrodes were predicted by Ben-Jacob et al. [56], and a theory of the *SET oscillations* was presented soon thereafter by Averin and Likharev [25].

The single electron transistor was introduced as a dual analog to the DC SQUID by Likharev in 1987 [57] (the more general name *charging effect transistor* or CHET [52] never got popular). Kuzmin and Likharev found single electron charging experimentally in granular junctions [58]. With the observation of charging in lithographically made junctions by Fulton and Dolan [59], the science of single electron devices took off in 1987, moving away from granular films to more well-controlled systems with a few junctions.

### 2.2.3. Superconductor-insulator transition in thin films

While the entry into the superconducting state below a critical temperature  $T_c$  is a thermodynamic phase transition, the superconductor-insulator

## 2. Background topics

transition (S-IT) we will consider in this subsection is (or ‘may be interpreted as’) an example of a quantum phase transition (QPT) [60]. QPT take (in principle) place at zero temperature, and the S-I phase boundary is crossed by varying a parameter other than the temperature in the system’s Hamiltonian. This can be the charging energy in a Josephson-junction array [38, 61] or the amount of disorder in a metal undergoing a metal-insulator transition (M-IT). Superconducting thin films have similarities with both disordered metallic films and arrays of Josephson junctions [62]. The small grain size generally means that even charging effects are important in these films.

Experimental studies have been performed on quench condensed films, that are films deposited from the vapour phase onto a very cold surface. This technique allows to grow amorphous or nanocrystalline films. Experimental studies on a variety of materials show that the parameter governing the behaviour seems to be the sheet resistance of the thin films. White et al. [63] have measured the superconducting energy gap with tunnelling experiments and found that the broadening of the gap edges became comparable to the gap itself, and hence superconductivity disappeared, when the sheet resistance at high temperature reached  $(10\dots 20)\text{ k}\Omega/\square$ .

Jaeger et al. [64] found that gallium films became globally superconducting when the sheet resistance was below about  $6\text{ k}\Omega/\square$ . Experiments [65, 66] suggest that the threshold for the superconductor-insulator transition is a sheet resistance of one-fourth the Klitzing resistance, the so-called quantum resistance for pairs

$$R_Q = \frac{\hbar}{(2e)^2} = \frac{R_K}{4} \approx 6.45\text{ k}\Omega. \quad (2.8)$$

There is no conclusive agreement to date [67] on whether this value is a universal sheet resistance for the S-IT [68] or not [69], and whether thin films actually better be modelled as junction arrays or disordered metals [70, 71].

In all these experiments, the sheet resistance depended very sensitively on the film thickness; in most cases, a difference of one nominal monolayer can change the sheet resistance over the entire range of the S-IT [62]. This problem was addressed by Wu and Adams [72], who used the same technique we used for the experiments described in this thesis (chapter 4): the films (Al in their case, Nb in our experiments) were deposited with a certain (relatively high) thickness and then thinned by controlled anodic oxidation [73].

### 2.3. The single electron transistor (SET)

The simplest device that bases its operation entirely on the charging effect is the double junction system known as the *single electron [tunnelling] transistor* or SET. It consists of two very small tunnel junctions, preferably with approximately equal tunnel resistances  $R_1 \approx R_2 \gtrsim R_K$ , and a metallic island between them. The island carries an integer number of (excess) electric charge carriers, and is furtherfore polarised with a certain displacement charge. In the simplest case, the island is capacitively coupled to a gate electrode. The gate voltage  $V_g$  then induces the displacement charge

$$Q_g = V_g C_g, \quad (2.9)$$

which is a continuous quantity.

The operation of the SET is based on the fact that on one hand, the gate charge  $Q_g$  can be varied continuously, whereas on the other hand, transport through the island via the tunnel barriers always involves an integer number of electrons.

In addition to the gate charge  $Q_g$ , there is an offset charge charge  $Q_0$  which results from other sources than the gate coupling capacitively to the island, namely background charges in the vicinity of the island. For the following discussions, we can absorb the offset charge into the gate charge. The distinction will become important later, especially when we consider the noise properties of the SET in chapter 5.

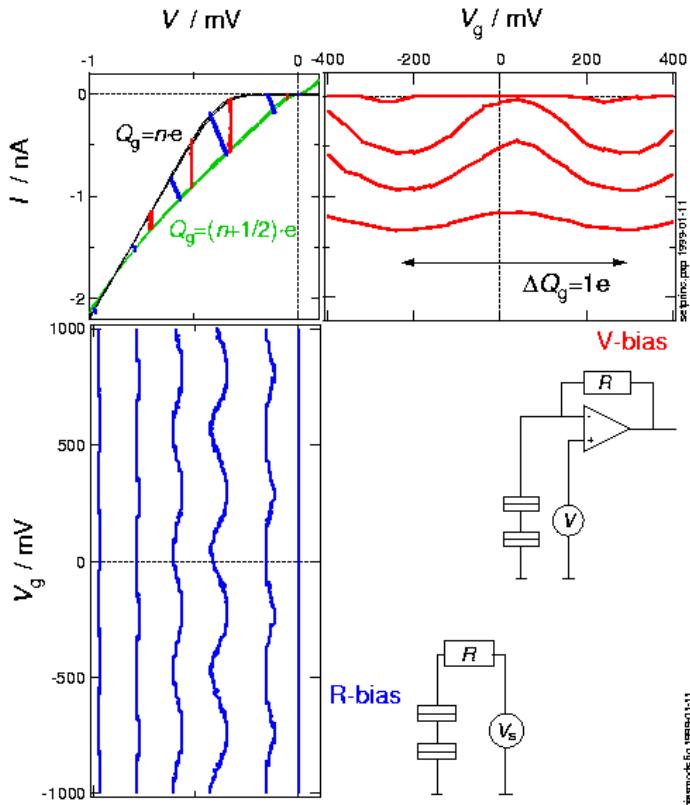
If the initial gate charge  $Q_g$  is an integer multiple of the elementary charge  $e$ , tunnelling of an electron onto the island increases the electrostatic energy of the system. Therefore, a threshold voltage

$$V_{\text{th}} = \frac{e}{C_{\Sigma}} \quad (2.10)$$

has to be overcome before the tunnelling process can occur and current can flow through the transistor. This is the state of maximum Coulomb blockade, shown in the current-voltage characteristic (IVC) of fig. 2.2 (top left) as the trace labelled “ $Q_g = n \cdot e$ ”.

The other extremal IVC is obtained when the gate charge is changed by half an elementary charge. Here, the initial state and the state after tunnelling of an electron are energetically equal, and no threshold voltage for current flow exists. The current-voltage characteristic in this case is not ohmic, though, as it might appear from the IVC in the limited range shown in fig. 2.2. Rather, there is an offset voltage from the ohmic characteristic which, at high bias, becomes independent of the island charge. We will

## 2. Background topics



**Figure 2.2.:** Current-voltage characteristics of a single electron transistor showing maximum and minimum blockade (top left), and modulation curves for two different bias schemes. In R-bias (left bottom), the SET is biased from a voltage source via a high ohmic resistor, whose value determines the inclination of the trace in the IVC (the load line) as the gate voltage is varied. In V-bias (top right), the voltage across the SET is held constant by an operational amplifier setup (causing a vertical trace in the IVC), and the current is modulated with a periodicity in the gate voltage corresponding to a difference of one elementary charge induced on the gate.

## 2.4. Noise

re-address the topic of the offset voltage again later. Suffice it here to say that the offset voltage has been the subject of extensive study in our group [33, 74–76].

Figure 2.2 also shows how to exploit the characteristics of the single electron transistor for purposes of electrometry. In the simpler case (circuitwise) of resistive bias or *R-bias*, shown in the lower part of the figure, the double junction system is biased via a high ohmic resistor from a voltage source. The gate has been omitted from the sketches. As the gate voltage  $V_g$  and thus the induced polarisation charge according to eq. (2.9) are varied, the voltage drop across the SET is modulated periodically. One period corresponds to a difference of the gate charge of exactly one elementary charge. Also the current, which can be measured via the voltage drop over the bias resistor, is modulated e-periodically. In the current-voltage diagram, the trace of  $(I, V)(V_g)$  for fixed source voltage  $V_s$  falls on a line whose inclination is given by the bias resistance, the so-called *load line*.

A perfectly vertical load line is attained in the voltage bias or *V-bias* mode depicted on the right in fig. 2.2. Here, an operational amplifier circuit keeps the voltage across the double junction constant, and the current, which can be measured via the voltage drop over the feedback resistor, is e-periodic with the gate charge.

In either bias mode, electrometry is done by biasing the SET at such a transport voltage  $V$  or source voltage  $V_s$  and gate voltage  $V_g$  that the gain

$$\eta = \frac{dI}{dV_g} \quad (2.11)$$

is maximised to optimise the sensitivity (in chapter 5 we will relativise this statement slightly). Small variations of the gate charge  $\Delta Q_g$  will then result in measurable variations of the current  $\Delta I$  or voltage  $\Delta V$  (in R-bias), and the resolution limit of the SET electrometer is set by its noise properties [77–79] (see also the following section). We will discuss this in more detail in chapter 5.

## 2.4. Noise

The purpose of electronics is the handling and processing of some time dependent electrical quantity (e.g. a current) whose variation we call *signal*. Unfortunately, in a real world scenario, not only does the signal get distorted, but it may also get drowned in a mess of other, unwanted signals that we call *noise*. In the time domain, noise manifests itself in fluctuations of the signal quantity. Since most electronics involve some kind of

## 2. Background topics

frequency selection, it is useful and customary to think about noise in the frequency domain. The noise spectral density of the current  $I$ , for example, is the Fourier transform

$$S_I(f) = \int_{-\infty}^{+\infty} dt R_I(t) e^{i\omega t} \quad (2.12)$$

of the current autocorrelation function

$$R_I(t) = \lim_{T \rightarrow \infty} \frac{1}{T} \int_{-T/2}^{+T/2} dt' I(t') I(t' - t), \quad (2.13)$$

that is the properly normalised convolution of the current with itself.  $S_I(f)$  gives us a measure of the noise power in a certain bandwidth. The larger the bandwidth in the measurement, the more noise power will be present.

The noise spectral densities of uncorrelated noise sources add up:

$$S_{I,\Sigma}(\omega) = \sum_j S_{I,j}(\omega). \quad (2.14)$$

Noise sources are uncorrelated when the processes causing the respective fluctuations are stochastically independent.

### 2.4.1. Noise nomenclature

When considering a device, we can attribute the noise measured at the output of the device as coming from two groups of sources. First, there is noise already present at the device's inputs that proliferates through the device and eventually gets transformed in the way the output quantity depends on this input quantity (e.g. amplified). The result of this transformation of the noise present at the input of the system is called *input noise*. Observe the unfortunate use of the word *input* here: input noise is the noise at the output of the device that is the direct result of the noise present at the input.

Second, the device itself will add some noise to the output quantity. This contribution is called *output noise*, another unlucky word coining. Output noise should better be called *internal noise*, but since it cannot be detected before it has reached the output, it received its name. Since input noise and output noise are uncorrelated by definition, the measurable noise spectral density at the output is the arithmetic sum of the spectral densities of input noise and output noise.

If the noise present at the input triggers some process in the device that adds noise, we absorb this contribution into the input noise by stating that

## 2.4. Noise

the transfer function for the noise present at the input need not be identical to the transfer function for the input quantity.

Instead of working with separate numbers for input noise and output noise, in engineering these two are often combined into yet another quantity, the *input referred noise*. If the transfer function is known, e.g. as a simple gain  $\eta$ , one can take the measured noise at the output, which is the sum of input noise and output noise, and divide it by the transfer function to calculate the input referred noise. More general, the input referred noise is the noise at the input of a system that would cause the observed noise at the output of the system under the assumption that the system just transforms the input quantity without adding noise by itself. In chapter 5, we will encounter such a quantity in our discussion of the noise in the single electron transistor, where all measured noise is referred to the input quantity charge.

Another real life complication is that we often cannot measure the output quantity of the device directly, but have to use an amplifier. This amplifier itself is a device that adds (output) noise, which we call *amplifier noise*. The noise measured at the output of the whole system, consisting of the device under test (DUT) and the amplifier, is then the sum of amplifier noise, amplified input noise of the DUT, and amplified output noise of the DUT.

Noise with a frequency independent spectral density is called *white noise*. Of course, white noise must be limited by some cutoff frequency since the energy of the system is finite. Typical white noise contributions in electrical systems are the thermal noise of the currents in resistors, and shot noise. Thermal current noise in a resistor is known as *Nyquist* or *Johnson noise*, its spectral density is

$$S_{I,\text{th}} = \frac{4k_B T}{R}, \quad (2.15)$$

where  $R$  is the resistance value and  $T$  the resistor's temperature.

Since electric current is carried by discrete electrons, statistics of the number of electrons per unit time lead to an inevitable noise term known as shot noise [80], with a spectral density of

$$S_{I,\text{e}} = 2eI \quad (2.16)$$

in a single junction.

## 2. Background topics

### 2.4.2. Low frequency noise

The noise spectral density of many systems shows a pronounced increase at low frequencies, often with a dependence of the form

$$S_X(f) = S_X(f_0) \left( \frac{f}{f_0} \right)^{-\alpha}, \quad \alpha \approx 1. \quad (2.17)$$

This noise is known as *1/f noise*, *flicker noise* or *excess noise*, however, we prefer the more general term *low frequency noise* (LFN). Among the systems that show this LFN are such distinct ones as metal films [81], nerve fibres, the human heartbeat period, semiconductor field effect transistors, SQUID magnetometers, and the SET electrometers described in 2.3. Since single electrons transistors are in many respects analogous to SQUIDs [23, 57], this parallel deserves some more attention in chapter 5.

Despite years of effort, the physics of LFN is not completely understood. A model that seems to reach quite far, at least for semiconductor structures, is that of charge traps. These charge traps, which are located in the silicon oxides covering devices, and in gate oxides, can catch an electron for an average lifetime  $\tau$ . A single such trap would then give rise to a current spectral noise density with a Lorentzian shape [82],  $S_I \propto (1 + \beta f^2)^{-1}$ , and an ensemble of many such traps with lifetimes distributed evenly over a certain interval  $[\tau_1, \tau_2]$  would lead to an approximate  $1/f$  dependence of the resulting spectral noise density over the frequency interval  $[(2\pi\tau_2)^{-1}, (2\pi\tau_1)^{-1}]$  [83].

At very low frequencies, the noise becomes very hard to measure accurately because of the long integration times required. On the high frequency side, there appears a *corner frequency* where the LFN crosses over to a noise floor set by some kind of more or less white noise, e.g. by amplifier noise. Stating the frequency range of the LFN is, therefore, quite difficult.

Low frequency noise is detrimental to all potential applications of single electron tunnelling. In logic devices, it can cause computing (bit) errors. Since realistic logic applications seem to lay in the more distant future, this may not be a top priority concern. Proposed analog-to-digital converters (ADC) [84] certainly work better without LFN and the need for background charge re-trimming it imposes.

In metrological devices, LFN limits the accuracy [85] by causing random errors. However, even with quite noisy devices measured by the state of the art, metrologically sufficient accuracy could be achieved [86, 87].

In single electron memory (SETRAM), the primary industrial scale application envisioned today, LFN will limit the lifetime of a single bit.

## 2.5. Niobium

With the recent invention of the radio frequency single electron transistor (RF-SET) [88, 89], it has become possible to conduct electrometry at such high frequencies that the contribution from low frequency noise becomes negligible.

### 2.5. Niobium

Niobium was discovered by Charles Hatchett in the year 1801 and originally named Columbium. In the following years, it became confused with Tantalum, discovered 1802, with which it occurs mostly in nature, and was finally isolated and rediscovered in 1844 by Rose and named Niobium (after Niobe, the daughter of Tantalos). Both names were used until element 41 was officially named Niobium by IUPAC in 1950, but the name Columbium is to date still used occasionally by the American metallurgical community and e.g. the United States Geological Survey. In metallic form, niobium was isolated for the first time by Bolton in 1905.

Early work on niobium anodisation was inspired by potential applications in electrolytic capacitors [90, 91]. Today, niobium oxides are often studied because they form the surface of superconducting accelerator cavities, and since acceleration is a high frequency application, the surface is very important to the cavity quality. Such cavities used to be made of sheet niobium, but are nowadays also produced from copper covered with sputter deposited niobium.

#### 2.5.1. Properties

The superconducting critical temperature  $T_c$  of BCS superconductors is known to depend on the density of states  $N(E_F)$  at the Fermi energy. For niobium,  $E_F$  lies on the flank of a narrow peak in the density of states [92]. This explains the pronounced sensitivity of niobium's critical temperature to crystal lattice imperfections, since these tend to smear out the DOS peak, thus lowering  $N(E_F)$  and  $T_c$ .

The influence of gaseous impurities on the superconducting properties of niobium has been investigated by DeSorbo at General Electric in 1963 [93]. He found that the addition of oxygen reduced the  $T_c$  of wire samples to as low as 5.8 K for an oxygen content slightly below four atomic percent. Interestingly enough, the addition of more oxygen raised  $T_c$  again, and finally lead to the inclusion of oxide phases as the solubility limit was exceeded. Nitrogen showed the same tendency of first lowering, then raising

## 2. Background topics

$T_c$ , but its effect was much weaker. Note that this refers to the solution of N in Nb, not to the stoichiometric compound NbN.

### 2.5.2. Niobium and its oxides

There exist three stable oxides, niobium pentoxide  $\text{Nb}_2\text{O}_5$ , niobium dioxide  $\text{NbO}_2$ , and niobium monoxide  $\text{NbO}$ , and the solution of oxygen [94] in niobium notated as  $\text{Nb}(\text{O})$ , with up to one weight percent of oxygen at high temperatures. Niobium pentoxide occurs as  $\text{NbO}_x$  with  $x \in [2.4 \dots 2.5]$ , the dioxide and monoxide only in narrower stoichiometry [95].  $\text{Nb}_2\text{O}_5$  is the principal constituent of anodic oxide films on niobium [96, 97]. Its density in bulk amorphous form is  $\varrho = 4360 \text{ kg/m}^3$ , and its dielectric constant  $\varepsilon \approx 41$  [97]; values for thin films might deviate from this value, though.  $\text{Nb}_2\text{O}_5$  is an insulator,  $\text{NbO}$  a superconductor with  $T_c \approx 1.4 \text{ K}$ .

The microstructure of an anodic oxide film on niobium is rather complicated. The outermost layer is  $\text{Nb}_2\text{O}_5$ , followed by a thin layer of  $\text{NbO}_2$  followed in turn by  $\text{NbO}$ . This sequence was determined by Gray et al. using ion scattering spectroscopy [95]. It is noteworthy that they found a more gradual falloff in stoichiometric oxygen content from  $\text{Nb}_2\text{O}_5$  to Nb on anodised foils than in natural oxide layers. A thin layer of  $\text{NbO}$  seems to always appear between the metal and the pentoxide, independent of the preparation details [98]. Halbritter [99, 100] points out that the interface between niobium and its oxides is not even but serrated [101]. This serration is stronger for ‘bad’ niobium as measured by the residual resistance ratio (RRR), the ratio of the resistivities at room temperature and at 4.2 K or just above the transition. Niobium deposited by thermal evaporation is, compared to sputter deposited material, always worse, but evaporation in conjunction with a liftoff mask offers more flexible patterning techniques.

The reason for the serration of the interface is the volume expansion from Nb to  $\text{Nb}_2\text{O}_5$  by a factor of about 3 [102] in combination with the mechanical properties of the compounds involved. Nb (density  $\varrho = 8570 \text{ kg/m}^3$  at room temperature) is relatively soft, and niobium pentoxide microcrystallites cut into the metal. This serration does not occur on the metals NbN and NbC that are harder than Nb; carbon inclusion in the interface is known to improve the quality of Nb based tunnel junctions [103].

As a consequence of the complicated interface structure, niobium oxide on niobium is a bad choice for a tunnel junction material [104]. To form good homogeneous junctions with relatively high transparency, one uses other insulators to create barriers between niobium electrodes. A good choice is aluminium oxide [105].

# 3. Nanofabrication with niobium

## 3.1. Definition of nanosize patterns

Compared to the processes encountered in modern industrial semiconductor processing, producing metallic nanostructures is in principle very simple indeed. There are basically two kinds of process steps, viz. lithographic steps and pattern transfer steps, which we will discuss in 3.1.1. After that, we will give an overview over the lithographic techniques used for the various types of samples presented in this thesis (3.1.2) and mention how patterns are produced with the help of computers (3.1.3).

### 3.1.1. Lithographic and pattern transfer techniques

Lithography is the creation of a physical pattern on some surface with the aim of transferring this pattern to another structure that could not have been patterned directly, i. e. without the lithography in between. The oldest application of lithography is the (mass) reproduction of drawings by creating the pattern on the surface of a flat stone (hence the name, “lithos” is greek for stone), and then copying it by inking the stone, and transferring the graphic to paper. Some time after the invention of silver halogenide photography, photosensitive organic materials were found and used to reproduce photographic images for printing. Such an organic material, a *resist*, is at the heart of any lithographic process. Apart from visible light, any sufficiently energetic radiation source can be used to modify a suitable resist. The semiconductor industry uses (deep ultraviolet) light for all mass fabricated circuits, because X-ray techniques are too expensive in almost every respect. The masks for this photolithography, in turn, as well as nanopatterns for research purposes, are usually produced by electron beam lithography (EBL).

Resists come in two basic flavours, called *positive* and *negative*, depending on their behaviour under exposure and development.

Positive resists consist of some kind of macromolecules that are broken

### 3. Nanofabrication with niobium

down by the radiation during exposure. The development is done with a suitable kind of weak solvent. Provided that the cracked (exposed) and unexposed resist molecules differ sufficiently in their respective solubilities, the former will be removed completely from the exposed regions of the sample.

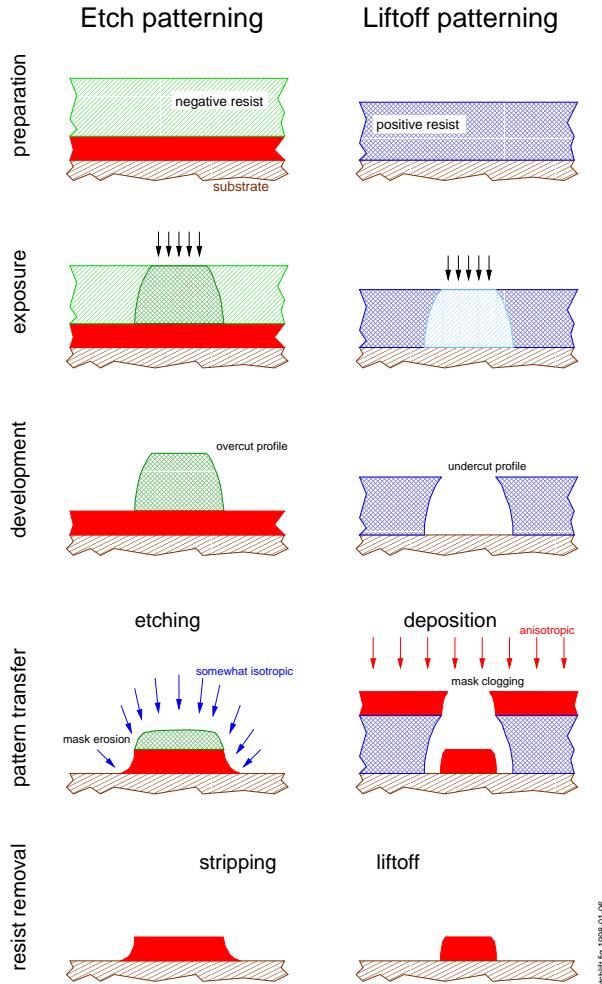
Negative resists, on the other hand, consist of small molecules with functional groups. The irradiation removes some atoms from these groups, making them reactive and the molecules susceptible to chemical bonding, so-called crosslinking. Upon development, once again in a weak solvent, the unlinked molecules are removed, and the resist stays where the sample has been exposed.

The choice of resist is governed by two considerations, speed and required profile. Speed is dependent on the area where resist is needed to be, or be removed, and on the sensitivity of the available resists. It used to be that positive resists were much less sensitive than negative resists and thus needed higher doses, resulting in lower resolution (higher beam diameter) and/or longer exposure times. With the introduction of ZEP 7000B, however, one now has a high resolution positive e-beam resist with a sensitivity comparable to negative resists. A recipe for photomask making with ZEP 7000B can be found in C.1.1.

Before discussing the resist profile issue, we should look at the techniques used for the pattern transfer steps, so that we can understand the demands. The two fundamental types of pattern transfer processes are the etching process and the liftoff technique, both illustrated in fig. 3.1. Etching processes are dominating for the metallisation in contemporary industrial lithography, and came long before the liftoff processing was introduced [106]. In a pattern transfer by etching, the material that is to be patterned is deposited on the substrate as a first step. Since no organic materials are present at this stage, rather extreme conditions regarding temperature, vacuum etc. can be created, allowing the optimisation of material properties to a certain degree. Then, a layer of resist is prepared on top of the material and patterned by lithography. After development, the material not covered by resist is removed by some kind of etching process, be it reactive ion etching (RIE), ion beam etching (IBE), or wet chemical etching (WCE).

A resist profile with perfectly vertical sidewalls is very, very hard to attain. Under this premise, for the etching process one will prefer to err on the side of the bell shape or *overcut profile* indicated in fig. 3.1, to prevent etchant from sipping under the resist. Such an overcut profile is almost automatically generated in negative resist, either by light diffraction behind a photomask in the case of a photo resist, or, in the case of EBL,

### 3.1. Definition of nanosize patterns



**Figure 3.1.:** Patterning process types relevant for nanofabrication: etching and liftoff. Note the widening of the exposure profile due to scattering of the irradiating particles and the resulting resist profiles, overcut in negative and undercut in positive resists. Isotropy of etching and mask erosion lead to a concave, clogging of the liftoff mask on the other hand to a convex profile of the patterned material in the respective processes.

### 3. Nanofabrication with niobium

by scattering of the electron beam in the resist (forward scattering) and the materials below (backscattering). Hence, etching processes normally use negative resists.

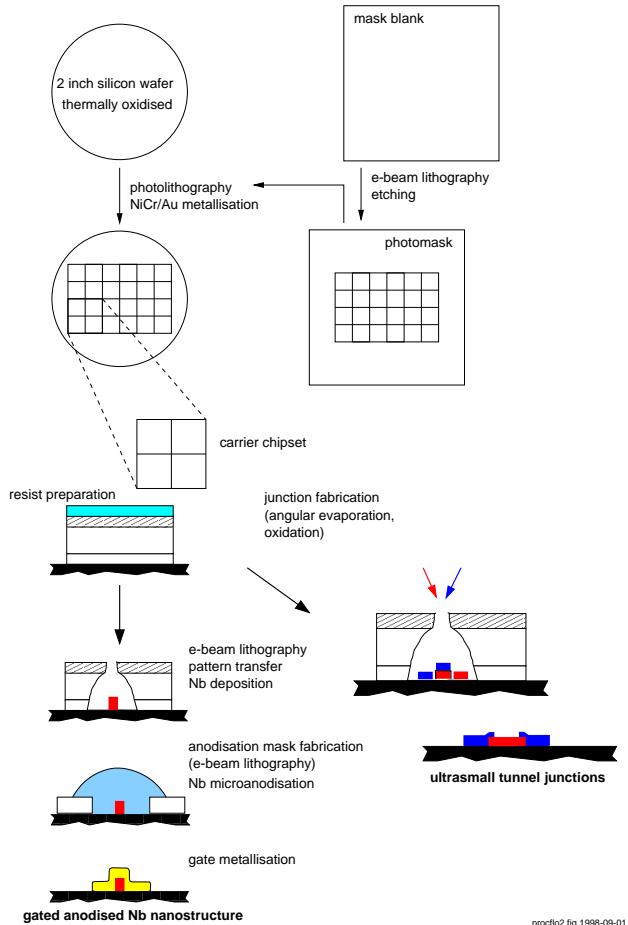
Liftoff processing, on the other hand, does not start with pre-deposited material, but with resist prepared directly on the substrate. The resist is then lithographed into a stencil, and the material is deposited on the substrate through the holes in the stencil. This obviously limits the ranges of suitable materials, available deposition techniques, and possible environmental parameters, but on the other hand, allows to deposit material on substrates that are not suitable for etching. The biggest advantages of liftoff processes, however, are the resolution and the ability to make more complex patterns by nonvertical evaporation techniques. Liftoff deposition cannot create structures with aspect ratios as high as strongly anisotropic etch processes can. High energetic IBE or chemically and energetically well balanced RIE can be used to make structures with aspect ratios of 10 in suitable materials, while liftoff masks clog and thereby limit the amount of material that can be deposited. After the deposition of the material on and through the stencil, the resist with the stencil and superfluous material on top is removed (*lifted off*) in a strong solvent. To allow this liftoff, the metal film must not cover the resist sidewalls, but tear cleanly at the edges of the stencil holes. This is achieved by creating an undercut profile as drawn in fig. 3.1. By virtue of the same diffraction or scattering mechanisms mentioned above, such an undercut profile is almost automatically created in positive resists. The effect can be enhanced by using multilayer resist systems, and the extreme form of this line of evolution are the resist systems for shadow evaporation described in 3.2.4.

#### 3.1.2. Lithography and processing overview

For the various parts of work documented in this thesis, a number of lithographic or lithography related techniques were used and will be discussed in the remainder of this chapter and in specific sections of chapters 4 and 5. To provide an orientation, fig. 3.2 gives an illustrative flow scheme.

Any sample fabrication started with the preparation of the substrate chips. We used two inch wafers in (100) orientation with a thickness of about 0.25 mm that had been thermally oxidised to a depth of approximately 1  $\mu\text{m}$ . Oxidised silicon has the advantages that it allows the testing of samples at room temperature, and anodisation without current leakage through the substrate. Its disadvantages are that it makes the samples more prone to damage from electrostatic discharges, and possibly, that it makes SET electrometers more noisy (see chapter 5).

### 3.1. Definition of nanosize patterns



**Figure 3.2.:** Nanofabrication process steps for anodised niobium nanostructures (chapter 4) and ultrasmall tunnel junctions (chapter 5).

### 3. Nanofabrication with niobium

To save exposure time, only an area of  $160 \times 160 \mu\text{m}^2$  on each chip was actually patterned with electron beam lithography (this area corresponds to four *fields* of the system in highest resolution mode). From this EBL writing field in the centre of the chips, sixteen gold leads went to contact pads. Electrical contact to the samples was made by means of spring-loaded probes (*pogo pins*) in a distance of about 2.5 mm from the chip centre. This gold lead and pad pattern was most economically produced by photolithography, the photomask in turn by electron beam lithography (see recipes C.1.1 and C.1.2 in the recipe appendix C).

A documented process for the lead and pad pattern photolithography [107, appendix to chapter 4] had to be abandoned to comply with environmental regulations restricting the use of toxic and carcinogenic chemicals. Therefore, a new process, described in C.1.3, was developed. This process not only eliminated the use of chlorobenzene, but also required fewer chemicals and treatment steps and less time while producing good resolution. This issue was especially important to ensure proper detection of fiducials integrated in the pattern that were later used to align patterns in various layers of electron beam lithography.

After the photolithography, the wafers were scribed by pre-sawing them from the back. Resist was prepared on the whole wafer, and subsequently, the wafer was divided into typically six carrier chipsets of two by two chips, each chip measuring  $7 \times 7 \text{ mm}^2$ . Processing started with these sets of four, later continued with individual chips.

Figure 3.2 shows the two different fabrication lines for the anodised niobium nanostructures described in chapter 4, and for the ultrasmall tunnel junction systems used for the measurements that are the subject of chapter 5. Both lines started with the preparation and patterning of four layer resist (see 3.3.2). Niobium was then deposited by vertical evaporation for the anodised wire samples (4.4), or by a special kind of angular evaporation for the anodised samples in SET-like geometry (4.5), followed by liftoff. On both kinds of samples for anodisation, a mask was produced that defined the anodised areas (4.2.1). The anodisation mask could later serve as a liftoff mask for the fabrication of a top gate on the anodised structures, especially on the SET-like samples (4.4.4).

For the fabrication of the more conventional single electron transistors, that is the noise measurement samples, aluminium and niobium were used in a shadow evaporation à la Niemeyer [108] and Dolan [109] as described in 3.2.4.

### 3.1. Definition of nanosize patterns

#### 3.1.3. Computer aided design of nanostructures

Computer aided design (CAD) is an excellent tool for rapid prototyping, and in nanostructure research, each and every device is a prototype.

Since there are no complex design rules to be observed, CAD of nanostructure is mainly a drawing and programming aid for the researcher with whom the responsibility for the design rests. It is not comparable to the design of complex semiconductor electronics that would be completely impossible with paper and pencil.

Figure 3.3 gives an overview of the pattern data flow. The nanostructures described in this thesis were designed (drawn) using AutoCAD version 10 on an old, slow and very reliable VAXSTATION P3100 minicomputer, not least because the DXF output of this old programme was compatible with all following handling stages.

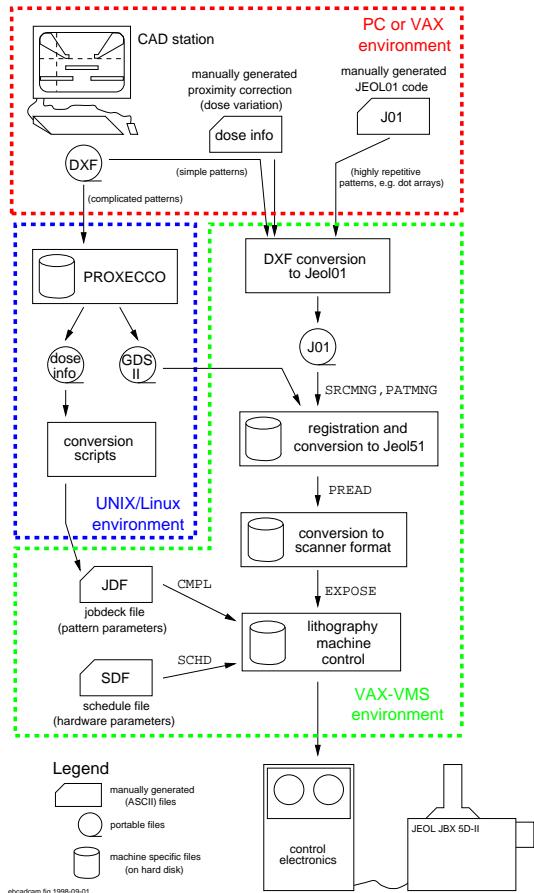
AutoCAD 10 has a rudimentary support for three dimensions that allows to assign an *elevation* to every drawing object. This ability was used to implement a manual proximity correction by trial and error. Features of the design were drawn with different elevations, increasing with decreasing feature size. During compilation of the lithography machine job, an assignment of doses (*shot modulation*) to the elevations (*shot ranks*) was made, iterating from initial dead reckoning to a rather stable set of values.

This method works for single electronics systems with few junctions, whose drawings consist mainly of scarce lines and rectangles. It fails for complex structures like two dimensional arrays of tunnel junctions. For these patterns (which were made, though they did not enter this thesis), proximity correction [111] was done using the commercial software PROXECCO [110]. Its output was, on one hand, a pattern file in the industry standard GDS II (Calma stream) format. On the other hand, PROXECCO generates a dose variation table that was converted to a JEOL jobdeck file shot modulation table by a homebrewn script that was written as an exercise in tclsh, but should be easily portable to other languages.

Manually proximity corrected patterns were converted to the JEOL 01 format by a noncommercial programme and subsequently underwent a number of conversions, as did the PROXECCO-generated patterns in GDS II format.

In addition to the pure pattern data, two files completed the information required by the lithography system. The jobdeck file (JDF) detailed the placement of various patterns and the specifics of the fiducials needed for this placement. It also contained the shot modulation table. The schedule file (SDF) gave hardware parameters like autoloader levels and origins of the coordinates for the JDF in absolute (machine) coordinates, and the

### 3. Nanofabrication with niobium



**Figure 3.3.: CAD/CAM for nanostructure EBL.** Patterns were designed on a CAD station (mini- or microcomputer) and rendered as DXF files. Depending on the necessity of elaborate proximity correction, they were either processed with PROXECCO [110], or a shot modulation was entered manually as a variation of elevation in the drawing. PROXECCO-corrected patterns were delivered in stream format (GDS II), manually corrected patterns in JEOL 01 format. For simple, highly repetitive patterns, JEOL 01 code was generated manually.

### *3.2. Fabrication methods*

base dose (resist sensitivity) that was then multiplied by the factors in the modulation table.

## **3.2. Fabrication methods**

In this section, we will first state what we expect from a fabrication technique for niobium nanojunctions. After an introduction to the state of the art in metallic junction and multigranular system fabrication techniques, we will take a closer look at the shadow evaporation technique we used in this thesis, and compare it to its main competitors. The wide field of semiconductor-based single electronics, including all systems involving gated two-dimensional electron gases, is intentionally left out, although there are some very interesting developments concerning memory applications based on semiconductor technology [112, 113].

### **3.2.1. Criteria for a Nb nanofabrication technique**

Techniques for nanostructure fabrication will, in the academic research environment, be judged by the quality of the product, while factors like simpleness and cost effectiveness play hardly any role. In the present stage of very low scale integration in single electronics, flexibility of design is also a criterion of minor relevance. This leaves us with the following criteria for a good nanofabrication technique, in the special case of single electronics devices based on tunnel junctions:

1. The junctions should be as small as possible, to minimise their capacitances and thus maximise their characteristic charging energy and the operating temperature of the device.
2. In the case of niobium, the quality of the metal should be such that a maximal superconducting energy gap  $\Delta$  is attained, as close as possible to the bulk value of 1.5 meV.
3. The barrier resistances should be tunable to a value that maximises the signal and, consequently, optimises the signal-to-noise ratio. For a single electron transistor, this means a target value of the order of  $25\text{ k}\Omega$  combined junction resistance, depending on the biasing scheme.
4. The junctions should be as homogeneous and equal as possible, both in capacitance as in resistance values. The latter criterion is more stringent, since the tunnel resistance of an oxide barrier depends

### 3. Nanofabrication with niobium

**Table 3.1.:** Criteria for good single electronics niobium junctions and strong points (■) of the competing fabrication techniques. ND: Niemeyer-Dolan, SOG: Spin-on glass, SAIL: Self-aligned in-line technique.  $T_{\text{dil}}$  means a typical dilution refrigerator attainable temperature. References in the text (3.2.5).

	$E_C \gg k_B T_{\text{dil}}$	$\Delta_{\text{Nb}} \approx 1.5 \text{ meV}$	$R_i \approx R_K$	$R_1 \approx R_2$
ND	■		■	■
SOG		■	■	■
SAIL	■	■		?

more strongly (viz. exponentially) on the barrier thickness than the capacitance.

No single technique known today fulfills all of these criteria equally well, so, depending on the intended application, certain trade-offs will have to be made in choosing a technique.

Table 3.1 compares the three techniques that can be regarded as so far established that they are presently competing in the field of fabrication of ultrasmall single junctions involving niobium:

1. the Niemeyer-Dolan or shadow evaporation technique, which will be described in 3.2.4 since it is the technique we chose for the work described here,
2. the various trilayer processes developed at PTB, represented by the one that makes use of a planarising spin-on glass (SOG), and
3. the self-aligned in-line technique (SAIL).

Before comparing these techniques in more detail in 3.2.5, where references will be given, we will review other techniques for the fabrication of charging effect devices that were excluded from this comparison, either because they are not suitable for niobium or because they cannot fulfill more than two of the criteria enumerated. Techniques for the fabrication of more or less controlled multigranular systems will be treated extra in 3.2.3, and chapter 4 deals with our own special technique in this field.

#### 3.2.2. Other fabrication techniques in single electronics

Over the last decade, numerous techniques for single electron charging effect devices have been conceived and developed. Many of these aim pri-

### 3.2. Fabrication methods

marily at maximising the charging energy in order to achieve a Coulomb blockade at 4.2 K, 77 K, or even room temperature. A few even allow for operation at these elevated temperatures (as opposed to those merely producing a blockade that cannot be modulated). Often, though, the high charging energy is bought at the expense of a certain degree of randomness in the structure, and very often a high resistance and consequently low signal levels.

**Direct writing** A thin, lithographically defined metal line is deposited by a liftoff process. During and after the liftoff process, the metal is exposed to atmosphere, and a native oxide coating is formed. Oxide formation may be enhanced by heating or a plasma treatment. A second thin line crossing the first one is then fabricated in a second lithography process, requiring a certain alignment precision in the lithography. This process worked for chromium [114], but is applicable neither to aluminium, which would oxidise too heavily for reasonable resistance values, nor to niobium due to the complicated structure of niobium oxides formed in atmosphere (see 2.5.2).

**Membrane-with-hole** To study superconductivity in ultrasmall aluminium particles, Ralph et al. [115, 116] etched a groove into a silicon nitride membrane, ending in a tiny hole to the other side. Covering both sides of the membrane with aluminium, using a discontinuous film on the flat side first and oxidising before evaporating a continuous film, they were able to obtain structures in which tunnelling occurred through a single, very small grain. This technique can be combined with non-vertical evaporation on the grooved side and vertical evaporation through the hole from the flat side [117], creating a single particle with the cross section of the hole and a length determined by the membrane thickness and the evaporation angle on the grooved side. This type of structure has been used to study tunnelling in a very low impedance environment [117].

**Nanoparticle assembly** A variety of methods exploit the fact that it is perhaps not so difficult to produce fairly homogeneous nanoparticles or clusters by themselves (especially for chemists). Then, a pair of electrodes is made by lithography, and one or more of the prefabricated particles are assembled in the gap between the electrodes. Electrostatic trapping can be used to place single particles [118] or assemble chains of particles [119] between the electrodes. Other schemes use bifunctional linker molecules [120, 121]

### 3. Nanofabrication with niobium

to chemically *self-assemble* [122] metal clusters in the gap. Also, some SPM techniques (see below) fall into this category.

**SPM techniques** The methods involving scanning probe microscopy can be divided into STM measuring techniques on single grains in granular systems on one side, and STM/AFM fabrication techniques on the other side.

In STM measurements [51, 123], the tip is brought close to a grain that is separated from the conducting substrate by an oxide coating. This grain then forms the island of an SET. Of course, the junctions are quite dissimilar, one consisting of a dielectric and the other of a vacuum gap. By actually scanning the tip over the sample, locally resolved Coulomb blockade spectroscopy can be performed, e.g. near the percolation threshold of a granular film [124].

SPM-based fabrication techniques come in a large number of variations. An AFM tip can be used to assemble metallic disks with atomic precision, forming an SET with at least partly vacuum gap tunnel junctions [125, 126]. Such devices are of potential interest for comparing noise characteristics, helping to assess the barriers' contribution to transistor noise. These devices are limited to resistance values above  $1\text{ M}\Omega$ , though, because of the limited tip placement accuracy. Other approaches use SPM to create barriers in thin films, be it by nanoanodisation of thin films with an STM [127] or by scratching grooves (*ploughing*) with an AFM tip [128, 129]. Even an AFM can be used to induce local oxidation [130].

#### 3.2.3. Techniques for the fabrication of multigranular systems

Following the discovery of the charging effect by Giaever and Zeller [43, 44], using an aluminium oxide matrix with embedded tin particles, researchers have striven to produce granular systems in which the grain size is much smaller than typical lithographic resolutions. Ideally, the grains are so small that they show charging effects at room temperature. In recent years, the ambition has again been to laterally nanostructure these systems, to reduce the number of parallel current paths that contribute to the measured characteristics, as in the 1987 experiments by Kuzmin et al. [58].

Since every metal thin film has granular structure, ultrathin films below the threshold for complete coverage (but above the electric transport percolation threshold) can be suitable systems. The incrementally evaporated quench-condensed films in which Haviland et al. [65] observed a

### 3.2. Fabrication methods

superconductor-insulator transition (see 2.2.3) are an example. Recently, Kubatkin et al. [131] have combined quench condensation with lateral miniaturisation by angular evaporation, and they were able to observe the Coulomb blockade at room temperature and its gate modulation [132].

The step edge cut-off technique, SECO [133, and references therein] should be classified as a granular system fabrication method. In SECO, grooves with sharp edges, etched into the substrate, are filled with metal by evaporation under normal incidence almost up to the brim. The idea is that then the metal in the groove and the film on top of the unetched substrate will come so close that a tunnel junction is created, with a barrier consisting partly of the substrate dielectric, partly of vacuum. It must be assumed that metal granularity, step rounding and other imperfections in general lead to the creation of multigranular systems. Charging effects have been observed in these structures at 77 K, and gate modulation was possible.

Multigranular systems can be combined with SPM methods, as in the experiments of Nejoh et al. [134], who observed Coulomb blockade at room temperature in a system of metal grains connected by liquid crystals.

Choosing a material other than metal has been the approach of many groups. One of the classic experiments, and the one we tried to follow with our niobium anodisation experiments, was the observation of charging effects in short, highly resistive wires of indium oxide,  $\text{In}_2\text{O}_3$ , by Chandrasekhar and Webb [10, 11]. Indium oxide is a strange material behaving in some respects like a semiconductor. For example, irradiation with light can change the conductivity significantly [135].

Another superconductor material used in a number of experiments is niobium nitride, NbN. Coulomb blockade has been observed in nanobridges made by ion beam etching and using the shadow of a silicon dioxide step [136], and the gate effect has been demonstrated in NbN nanobridges at 4.2 K [137].

Other semiconductor multiple tunnel junction (MTJ) systems have been made by ionised beam deposition of particles in a gap between electrodes [138], and by side gating of semiconductor mesa narrows [139] and wires [140]. Such MTJ have been discussed as a possible element of single electron tunnelling RAM applications [141, 142].

Our own niobium nanoanodisation process for MTJ fabrication is described in detail in chapter 4.

### 3. Nanofabrication with niobium

#### 3.2.4. The Niemeyer-Dolan technique

Getting it small is not even half the battle in nanoelectronics. Making electrical contacts that allow measurements on a structure is often as complicated as making the objects themselves. In multilayer structures, there is the additional problem of properly placing the different layers, a process known as *alignment*. The angular evaporation technique, pioneered by Niemeyer [108] and implemented in the form described below by Dolan [109], addresses not only the problem of aligning the two electrodes forming a junction. It also permits forming the barrier *in situ*, i.e. without breaking vacuum and moving the sample to atmosphere (which would produce too thick and opaque barriers).

The essential feature in an angular evaporation process is a narrow structure suspended above and shadowing part of the substrate. In the original technique of 1973, a thin glass wire was placed over a groove in the substrate. We will here describe the angular evaporation technique as it was introduced by Dolan, using masks lithographically patterned first by photolithography, now regularly by electron beam lithography. Figure 3.4 gives three views of a double junction made by angular evaporation, as we fabricated them for the noise measurements described in chapter 5.

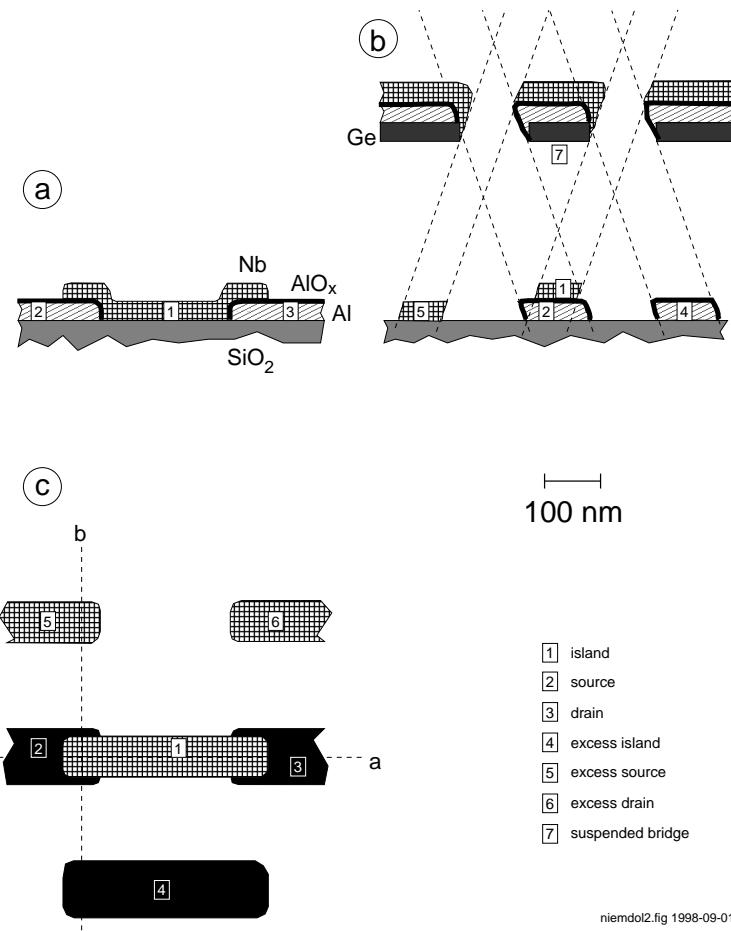
To produce the suspended bridge, a resist system with at least two, often three layers is used that can generate the extreme undercut profile required. We will refer the discussion of resists to 3.3.1.

The first step after development and processing of the mask is the deposition of the base electrode material, aluminium in our case shown in fig. 3.4. The oxide layer is then created by exposing the sample to oxygen under low pressure, either inside the evaporation system chamber or, in more advanced systems, in a separately pumped load lock. After the oxidation, and once again under UHV conditions, the top electrode material (here: niobium) is deposited under another tilt angle between the source direction and the substrate normal. In practice, both evaporations will be carried out under approximately oppositely equal tilt angles.

The tilting causes the mask pattern to be shifted, as we see in the bottom drawing of fig. 3.4. Designing the pattern accordingly, one can create overlap regions between the island and the source and drain electrodes, respectively, where the junctions are formed.

If the barrier material requires a separate evaporation, care must be taken to avoid any electrical shorts between base and top electrode. This requires much greater precision in angle control than the shown process involving just two evaporations, and a fine grained structure of the barrier material.

### 3.2. Fabrication methods



**Figure 3.4.:** Niemeyer-Dolan (angular evaporation) technique for the fabrication of single electron transistors. **a:** Side view, cut along the current path. **b:** Side view, cut perpendicular to the current path, and showing the resist mask and the layers deposited on it during the evaporation. Note how these depositions change the cross section of the openings in the mask. **c:** Top view, indicating the cut planes for views a and b. Drawings are approximately to scale in all dimensions.

### 3. Nanofabrication with niobium

The deposition of excess material is an unavoidable drawback of the angular evaporation technique, as is the fact that design flexibility is limited by defining one fixed direction and amount of pattern shift for the whole chip. Since single electronics today, however, is still in the stage of very low scale integration, we felt that adapting the Niemeyer-Dolan technique according to our needs was preferable over developing a completely new process.

A variation of the shadow evaporation technique that we used for the definition of very short thin weak links in a niobium wire is described in 4.5.1.

#### 3.2.5. Competing Nb nanojunction fabrication techniques

As described in the last subsection, the Niemeyer-Dolan technique is a self-aligned technique for the fabrication of planar (overlap) junctions. Its design flexibility is limited by the definition of one shift direction for the whole chip, and by the deposition of superfluous material. Addressing these limitations while pursuing a more “natural” way to size reduction is the self-aligned in-line technique (SAIL) [143].

Instead of planar junctions, SAIL creates vertical edge junctions. Since one of the junction dimensions is a film thickness, which is usually much smaller than lithographically defined line sizes, SAIL made junctions tend to have nice large characteristic charging energies.

SAIL consists of two lithography steps. A thin line of the island material is deposited first. An etch mask then defines the island position. The metal line is removed in the vicinity of the island, and the barrier layer generated by oxidation or sputtering. The same mask then serves as a liftoff mask for the deposition of both electrodes.

Since both island and source/drain materials can be sputter deposited, junctions with niobium electrodes can be made very small and still have a critical temperature and superconducting gap close to the bulk optimum. Junction capacitances of the order of  $10^{-16}$  F have been reported [144]. Though there does not seem to be an inherent limitation, junction resistances have been rather high so far ( $\approx 1\text{ M}\Omega$ ), and the future will have to show how far this can be reduced.

The three layer techniques under development by the collaboration between PTB Braunschweig and Moscow SU exploit the fact that no in situ fabricated junction has ever been as good as those made from a prefabricated sandwich. The electrodes can be made quite thick with this technique, up to 200 nm [145], which helps to improve the superconducting properties even more. This improvement is bought at the price of larger

### *3.3. Shadow evaporation patterning of niobium*

junctions than made with SAIL or shadow evaporation. The latest reported values [146] are  $(0.4 \times 0.4) \mu\text{m}^2$  for the “cross-strip” and  $(0.3 \times 0.3) \mu\text{m}^2$  for the “etching-anodisation” and “SOG” techniques, respectively. The SOG or spin-on-glass technique appears to have come farthest in the development of charging device fabrication techniques that are compatible with the old Josephson junction processes and facilities known from SQUID technology and the voltage standard. It uses multiple electron beam lithography and etching steps. After an etching step that leaves pillars with the cross section of the junctions, the sample is covered with a planarising resist called spin-on glass. An island between two junctions is then formed by covering the whole sample with niobium, which again can be done by sputtering or evaporation and to sizeable thicknesses, and by etching the niobium after the island has been defined by EBL with negative resist. A more detailed description can be found in [145].

Deviations of the etch profile from perfect verticality seem to produce effective junction sizes down to  $(0.2 \times 0.2) \mu\text{m}^2$  [146], but at the same time point to a limitation of the cross sections ultimately attainable with this technique. If one is satisfied with a charging energy corresponding to a few hundred mK, the SOG technique fulfills all the criteria for a good niobium nanojunction technique.

An aspect that we have not mentioned so far is the quality of the  $\text{AlO}_x$  barrier. The main reason is that we know very little about our barriers, for example, how homogeneous they are and how much of the conductance actually is via pinholes or other kinds of defects. One can only assume that prefabricated sandwich barriers will be at least as good as in situ produced ones since much larger parameter spaces can be explored in their making.

## **3.3. Shadow evaporation patterning of niobium**

### **3.3.1. Resists for the Niemeyer-Dolan technique**

The suspended bridge is usually generated in two or three layer resist systems patterned by electron beam lithography. Table 3.2 gives an overview of some resist systems that can be used to produce nanosize patterns with the shadow evaporation technique:

- Two layer resists consist of an e-beam sensitive top layer and usually a more sensitive bottom layer. The difference in sensitivity, ideally in combination with selective developers, leads to the removal of bottom layer material at larger distances from the exposing beam than in the

### 3. Nanofabrication with niobium

**Table 3.2.: Some resist systems for EBL and shadow evaporation. References in the text.**

layer sequence	Two layer systems undercut mechanism
PMMA / P(MMA-MAA)	sensitivity difference, non- or moderately selective developers
ZEP 520 / PMGI	sensitivity difference, highly selective developers
layer sequence	Three layer systems pattern transfer; remarks
PMMA / Ge / P(MMA-MAA)	development of e-beam sensitive bottom layer resist
PMMA / Ge / S1813,PMMA	reactive ion etching; called “four layer resist” here
PMMA(?) / Si <sub>3</sub> N <sub>4</sub> / SiO <sub>2</sub>	wet chemical etching with HF; no liftoff
PMMA / Si or Ge / PES	solvent

### 3.3. Shadow evaporation patterning of niobium

top layer and to the creation of the undercut profile with the Dolan bridge.

- Three layer resists have an e-beam patterned top layer, a mask or stencil layer (usually inorganic), and a supporting bottom layer. The pattern is transferred from the top layer to the mask by some kind of etching process (often RIE or IBE, sometimes WCE). The four layer resist we used (3.3.2) is really a special form of three layer resist.

#### Conventional multilayer resist systems

The combination of PMMA and CP, copolymer P(MMA-MAA), has been the working horse of (aluminium based) single electronics for the last dozen years. Exploiting the sensitivity difference between both resists, that can be enhanced by preexposing the CP prior to PMMA coating, its disadvantage is that there are no highly selective developers for the different layers available. This narrows the parameter ranges for doses, developer concentrations, and development time(s), and can make the fabrication of high density patterns [147–149] quite arduous. A recently introduced combination of a ZEP 520 top layer and a polyimide bottom layer [150] allows for the use of highly selective developers (xylene and Shipley MF322, respectively), gives good resolution, and can even be baked to higher temperatures than PMMA and CP.

#### Resist considerations for Nb evaporation

The problems in the deposition of niobium by evaporation are twofold:

1. The intense heat in the evaporation system tends to melt organic resists, resulting in distorted patterns or seriously sagging or damaged Dolan bridges. PMMA for example starts flowing at about 110°C, and the substrate temperature should not exceed 100°C [151].
2. The deposited niobium generally shows a suppression of the critical temperature and residual resistance ratio. Inclusion of gaseous impurities emanating from the resist is generally held responsible for this problem, which is affectionately known as the “stinking resist” problem.

The first complex has been addressed by the introduction of three layer resist systems with sturdy inorganic (metallic) stencils supported by a resist layer. Table 3.2 shows a selection of these.

### 3. Nanofabrication with niobium

Inserting a germanium layer between the PMMA top and P(MMA-MAA) bottom layer of conventional two layer resist was an early approach to creating a three layer mask for liftoff nanopatterning. The pattern can in principle be transferred to the bottom layer by development, though reactive ion etching seems to be more common. This system is still not completely satisfactory for niobium deposition, where substrate temperatures can reach 150°C [152]. The stability is improved by depositing the germanium on a layer of hard baked photo resist, which brings us to the four layer resist [9] described in 3.3.2.

At present, the focus of interest is shifting from the first problem, that is getting niobium deposited in nanopatterns at all, to the second, improving the quality. Two parallel trends can be noted. One trend is to find organic resists that can be baked to higher temperatures, to outgas as much as possible before entering a deposition system. These resists are then also expected to outgas less under the actual evaporation conditions. An example for such a resist is polyethersulfone (PES), known in France under the band name Vitrex. In collaboration with CNRS-CRTBT Grenoble, we have patterned niobium wires with this resist. Due to a very limited number of samples, however, statistics about the resulting Nb quality are not conclusive yet.

The second trend is that towards completely inorganic resists. Hoss et al. have very recently reported [153] using a Si<sub>3</sub>N<sub>4</sub> mask supported by an SiO<sub>2</sub> layer over a silicon substrate. Since the undercut in this system is generated by wet chemical etching with hydrofluoric acid, the choice of materials is somewhat limited, and liftoff after the deposition is hardly an option. The remaining metal would cause a certain shunting by introducing additional stray capacitances, but it is possible to measure on single electronics devices without doing liftoff [74]. Therefore, such inorganic resists definitely are an interesting development for certain applications demanding good superconducting niobium.

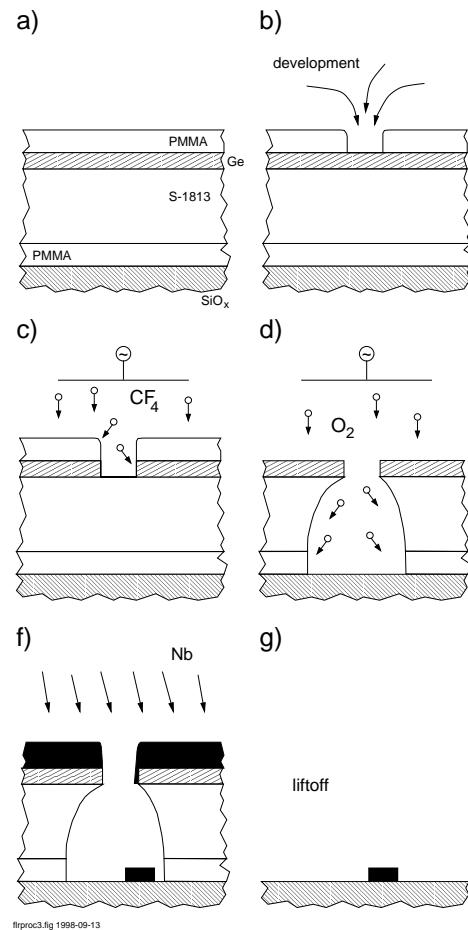
For the preparation of very thin niobium films, a suitable surface cleaning must be allowed prior to the deposition [154].

#### 3.3.2. Four layer resist

##### Preparation and pattern transfer

The structure of four layer resist we used can be seen in the top left of fig. 3.5. From the top it consists of a 50 nm PMMA layer that is patterned by electron beam lithography, a 20 nm germanium mask, and the support layers. These support layers in turn are 200 nm of hard baked Shipley S-

### 3.3. Shadow evaporation patterning of niobium



**Figure 3.5.: Four layer resist processing: overview of processing steps for Nb liftoff nanopatterning. After exposure and development of the PMMA top layer, the pattern is transferred to the germanium mask by reactive ion etching (RIE) with carbon tetrafluoride CF<sub>4</sub>. Subsequent oxygen RIE creates the undercut profile necessary for a liftoff mask, especially if intended for the angular evaporation technique.**

### 3. Nanofabrication with niobium

1813 photo resist and 50 nm of PMMA. Details on the process are given in C.2.1. It should be emphasized here that keeping the right baking temperatures is very important. Baking a higher layer at a too high temperature can lead to warped masks, cracks due to tensile stress in the germanium layer, or problems with liftoff.

A simple developer for PMMA is a mixture of isopropanole and water. As soon as possible after exposure, the patterns were developed using the concentration, times etc. given in C.2.5. The openings in the EBL-patterned PMMA top layer were transferred to the germanium layer by reactive ion etching (RIE). RIE is a combination of chemical etching and physical sputtering. The sample is placed inside a low pressure reaction chamber on an insulated electrode, and a reactive gas ('process gas') is let into the reaction chamber. A radio frequency cold plasma discharge is then ignited in the chamber. The process gas becomes partially cracked by the discharge, creating highly reactive radicals that can reach the sample because their mean free path is long enough in the low pressure. These radicals provide the chemical etching, which is essentially isotropic. Additionally, molecules accelerated in the electric field have a sputtering effect. The lower the chamber pressure, the higher is the anisotropy of this sputtering. Near the electrode on which the sample is placed, a DC bias voltage occurs between the electrode and the plasma potential due to different mobilities of positive and negative ions. The anisotropy of the etching increases with this DC bias.

A suitable reactive gas for germanium etching is carbon tetrafluoride  $\text{CF}_4$ . Our RIE system was not equipped with an etch end detection, so that the required etching time had to be estimated based on experience, allowing some extra margin since reactive ion etching processes tend to be somewhat irreproducible. Etch rates may vary depending on contaminations present in the chamber, or on the size of the sample areas, just to name a few factors. Overdoing this etch step resulted in a slight increase in linewidths, but this increase was considered tolerable.

Successful etching of the germanium layer is clearly visible by optical microscope inspection. While developed PMMA areas appear just slightly brighter than their surroundings in an optical microscope, the etched Ge areas are much darker.

Both the hardbaked photoresist and the PMMA bottom layers were etched with RIE using oxygen as reactive gas. A higher pressure than in the Ge etch step was used to increase the anisotropy of the etch rate to create the desired undercut profile. Another advantage of higher pressure is that the physical sputtering, leading to damage of the suspended Ge mask parts, is reduced.

### 3.3. Shadow evaporation patterning of niobium

Other than in the Ge etch step, the lack of an etch end detection is rather unfavourable here, because unnecessarily long etching causes damage of the Ge mask that could otherwise have been avoided. Figure 4.14 on page 90 is a scanning electron micrograph of an etched four layer resist mask. The undercut is clearly visible if one uses acceleration voltages of  $(5\dots8)\text{ kV}$ . The suspended bridge in this picture is damaged in the form of a tiny crack. More careful timing of the oxygen etch step and use of Teflon pedestals to adjust the position of the sample in the reaction chamber can reduce the risk of such damage.

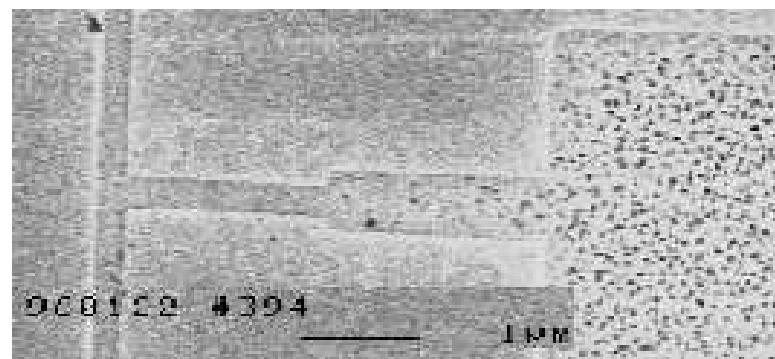
#### Niobium deposition and quality problems

For the niobium resistor samples, we deposited the metal in a non-bakable multipurpose HV system. During evaporation, the pressure rose to typically  $(3\pm1)\cdot10^{-5}\text{ Pa}$ , which gave niobium films of 20 nm thickness with a  $T_c$  of about 1.5 K. Later we used a bakable UHV system with a usual background pressure of  $3\cdot10^{-7}\text{ Pa}$ . In films of 40 nm thickness deposited with four layer resist masks, we obtained residual resistance ratios between 1.3 and 1.9, and critical temperatures between 1.5 K and just below 4 K, depending on the individual conditions.

At a deposition rate of between 2 nm/s and 4 nm/s, and without either substrate heating or cooling, we had a niobium grain size so small that we could not distinguish grains in an SEM. From an AFM analysis, we obtained a niobium surface roughness of between 5 nm and 7 nm (root-mean-square), which should indicate a grain size of a few nanometres.

Figure 3.6 illustrates another quality problem with four layer resist: on large open areas, grainy contaminants occurred after the reactive ion etching pattern transfer steps. Their density depended sensitively and not completely reproducibly on the conditions during the oxygen etching step. Since the fine structures were spared from these contaminations, we decided to tolerate them.

### 3. Nanofabrication with niobium



**Figure 3.6.:** Scanning electron micrograph of niobium patterned by the four layer process, showing grainy contaminants whose density increases with the width of the structure.

## 4. Anodised niobium nanostructures

### 4.1. Anodic oxidation

#### 4.1.1. Principle and History

In an anodic oxidation or *anodisation*, a metal is brought into contact with an electrolyte, and negatively charged ions containing oxygen are driven into the metal by an externally applied electrical field. The ions react with the metal to form an oxide. The process is not reversible, i.e., the oxide layer does not decrease when the polarity is reversed. This “one way only” behaviour in mind, the metals suitable for such a process were called *valve metals*.

Transforming metal into an oxide, anodisation can be viewed either as a technique to create an oxide layer, or to remove metal. The former application is dominant, and anodic oxidation is used at an industrial scale today for the surface treatment of metals, e.g. aluminium. While in this example, a certain porosity of the surface that allows the inclusion of colour pigments is desirable, the application most important for the development of anodisation techniques had just the opposite aim, namely the creation of pinhole-free oxide layers in electrolytic capacitors [90, 155]. A fair amount of development, especially regarding electrolytes, was conducted behind closed doors in industry, and since many decades have passed and modern analysis techniques had not been invented at that time, much know-how associated with electrolyte recipes today gives an impression of black magic. A standard reference for early developments in electrolytic capacitors and anodisation is the 1937 book by Güntherschulze and Betz [90], in which numerous metals are treated. The most important metal for capacitors, still today, is tantalum, to which niobium is closely related in its physico-chemical properties.

A standard reference on anodisation is the 1961 book by Young [156].

#### 4. Anodised niobium nanostructures

The behaviour of niobium has been covered in a 1993 series of review papers by d'Alkaine [157–159].

##### 4.1.2. Micro- and nanofabrication by anodisation

For purposes of micro- and nanofabrication, anodic oxidation basically serves as a means to remove metal. Since in most cases, however, the oxide is not dissolved in the electrolyte or at all removable without affecting the other structures, the oxide layers usually become an integral part of the device design.

Commercially, anodisation of niobium is used for the production of small Josephson junctions from prefabricated three layer ( $\text{Nb}/\text{AlO}_x/\text{Nb}$ ) sandwiches through a process called selective niobium anodisation process (SNAP) [102]. The top layer metal is oxidised where a photolithographically defined resist mask exposes it to the electrolyte, and then suitable contacts are made to the bottom layer and the unoxidised top layer regions. Sandwiches for such a *three layer technique* can be fabricated under extreme conditions and give the best niobium and interface quality (for their application in single electronics, see 3.2.5). The top layer is anodised all the way through, and the proper etch end can be detected by driving a constant current through the anodisation cell and monitoring the voltage; a discontinuity in the voltage increase rate indicates that the  $\text{AlO}_x$  layer has been reached.

Anodisation can also be used to not completely remove a metal, but just thin it out very much. Apart from the resistor fabrication process, which was patented [7] long before SNAP was devised, several processes were developed in the last decades.

Ohta et al. [160] used anodisation to thin out a weak link of niobium between two thick and large niobium pads. In the temperature dependence of the critical current, they observed a transition from weak link Josephson junction behaviour to tunnel Josephson junction behaviour with decreasing residual thickness of the linking metal. Goto et al. [161, 162] produced a silicon monoxide mask over a niobium strip with a long ( $\approx 10 \mu\text{m}$ ) and narrow ( $\approx 200 \text{ nm}$ ) slit, created by shadow evaporation at the edge of a resist strip. They then anodised the niobium through this small slit and found a transition from the behaviour of a continuous superconductor to that of a Josephson junction, manifesting itself in the occurrence of Shapiro steps under microwave irradiation.

In neither experiment was the resistance or thickness of the remaining metal monitored during the anodisation. Instead, the assumption of a niobium consumption directly proportional to the anodisation voltage [102]

## 4.2. Microanodised niobium resistors

was made, which is an oversimplification [163], as we will see in 4.2.3.

Nakamura et al. [164] used anodisation to thin out the top electrodes, and thereby the cross sections, of Al-AlO<sub>x</sub>-Al single electron transistors made by the conventional shadow evaporation process. By this technique [164], which they called anodisation controlled miniaturisation enhancement (ACME), they were able to raise the operating temperature of individual samples, and observed a modulation of the source-drain current with the gate voltage up to temperatures of 30 K. In these experiments, the resistances of the SET were monitored *in situ* and could be increased by about two orders of magnitude. A drawback with this technique, as with all anodisation techniques, is that preexisting asymmetries are enhanced, causing most of the samples to show a Coulomb staircase in their current-voltage characteristics.

## 4.2. Microanodised niobium resistors

### 4.2.1. Physical setup

Figure 4.1 is a sketch of the experimental setup for resistor fabrication by anodisation with *in situ* resistance monitoring. It corresponds very much to the scheme given in Western Electric's 1959 patent [7], except that our length scales are much smaller, that we specify the nature of the monitoring device, and that we include the cathode on the sample (see 4.2.1).

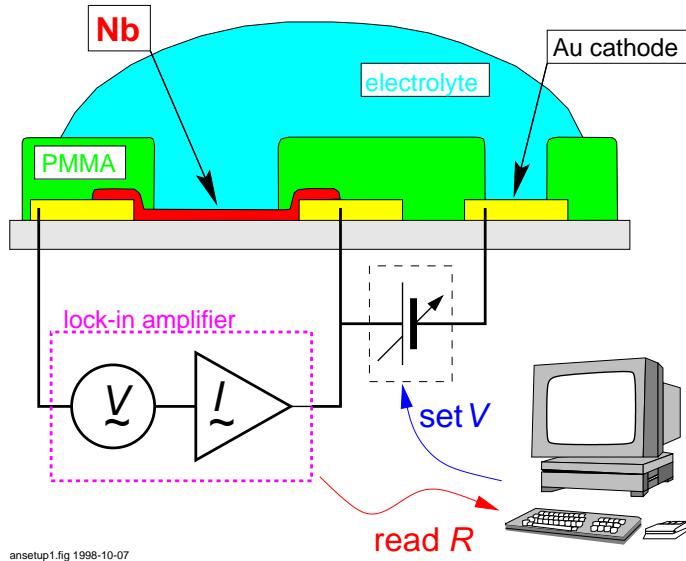
The areas of niobium that are to be anodised are exposed to the electrolyte (see 4.2.1) by windows in the anodisation mask (see 4.2.1). The cell voltage is controlled according to the resistance measurement (see 4.2.2).

#### Anodisation mask

Had only the size resolution been a criterion, photolithography would have been completely sufficient for the creation of the anodisation window mask. We wanted, however, to have an absolute window placement accuracy better than 1 μm, which was impossible with our photolithographic equipment. It appeared therefore most feasible to exploit the electron beam lithography system's fiducial detection and pattern alignment capabilities for the definition of the anodisation mask. In addition, the electron scattering in an electron beam resist material would automatically give the undercut profile required for the deposition of top gates with the same mask.

As material for the anodisation mask, we chose a highly viscous solution of PMMA, spin coating the wafer to a thickness of ca. 1.8 μm (for

#### 4. Anodised niobium nanostructures



**Figure 4.1.:** Niobium microanodisation setup (schematic, not to scale). In reality, the leads to the resistance monitoring and voltage control electronics were situated on the chip perimeter, away from the electrolyte droplet.

## 4.2. Microanodised niobium resistors

more technical details, see the recipe in C.3.1 on page 163). This thickness was necessary to prevent dielectric breakthrough of the PMMA under the anodisation voltages of up to 25 V.

The exposure and development of the anodisation mask were straightforward, except maybe for the very long development time of 15 minutes that was necessary to completely open the windows. Images of anodisation mask windows can be seen in figs. 4.5 on page 79 and 4.11 on page 87.

### Electrolyte

As mentioned before, a lot of the development of electrolytes for anodisation processes is poorly documented in the scientific literature. Many recipes are based on experience rather than on a deep understanding of the underlying process details. Demands for a good electrolyte are stability and a low vapour pressure. The latter eliminates the need for hermetically sealed encapsulations in capacitors, and is a very welcome property for our application since any significant change in the electrolyte composition during the anodisation (with the electrolyte droplet being directly exposed to atmosphere) is undesirable.

We could trace back the recipe for the electrolyte we used to a 1967 paper by Joynson et al. [165], but cannot rule out that it might have been published elsewhere earlier. The electrolyte consists of an aqueous solution of ammonium pentaborate mixed with ethylene glycol (see C.3.2 for the details).

Originally intended to be used at 120°C, this electrolyte can be used at room temperature if it is regenerated by heating to about 100°C under stirring for a few minutes not more than two days prior to use. After two days, precipitations occur. The prepared solution can be used for at least one year without any significant change in properties. Niobium is a well-behaved metal in respect to anodisation inasmuch as it works with many different electrolytes, and is insensitive to contaminations [90].

The addition of ethylene glycol is an old, empirically founded practice. In 1990, Bairachnyi et al. published a short article [166] in which they investigated the glycol's role. They found that it improves the stoichiometry of the oxide film, and thus the stability of the electric properties.

The long-time stability of our anodised wire samples might at least partially be attributed to the beneficial effect of the glycol. In Nb<sub>2</sub>O<sub>5</sub>-Nb bilayers, degradation is known to change the interface between metal and oxide with time [167]. Anodisation-trimmed resistors with very high sheet resistances would be especially prone to ageing by interface degradation. Luckily, in this application there are no field strengths to be expected that

#### 4. Anodised niobium nanostructures

would run as high as those across an electrolytic capacitor dielectric, and that promote interface degradation [168]. Nevertheless, for real resistor applications, some kind of protective coating might be necessary [169].

##### Cathode

The first anodisations were made with a tungsten wire as cathode, inserted into the electrolyte droplet. It was later replaced by the stainless steel needle of the syringe that was used to apply the electrolyte droplet to the chip. This needle allowed to correct the droplet size, and its wedged tip reduced the risk of accidental damage to the sample or mask during repeated manual insertions of the cathode.

Obviously, these designs would have required some kind of holder mechanism for continuously monitored and executed anodisations. The problem of droplet size reduction by evaporation during long anodisations would have required a droplet size overhead in excess of a (generous) safety distance between mask and electrode. These problems were instantly remedied by integration of the cathode on the chip.

The cathode material does not appear to matter on this small scale. Of course, a valve metal like niobium is a non-optimal choice since any (unintentional) reversal of polarity would build an oxide layer on the cathode. The simplest solution was to use one of the gold contact leads on the prefabricated substrate chip as cathode. Such an on-chip cathode can be seen on the left in fig. 4.5.

In any case, careful grounding of the electrolyte (syringe needle), sample, and cathode during insertion and connection was found to be essential. Due to the very small areas of niobium exposed by the anodisation mask window, electrostatic charge would generate enough current to drive the anodisation process far, even to pinchoff, in an instant.

##### 4.2.2. Electrical setup

Our requirements for a resistance monitoring device were:

1. a certain precision,
2. the ability to work in spite of the large potential difference between the sample and the cathode, which went up to almost 30 V, and
3. a negligibly small distortion of the electric field along the sample.

The last requirement was of particular importance. Measuring the resistance with a DC ohmmeter would introduce a considerable potential drop

## 4.2. Microanodised niobium resistors

along the sample, and since very small anodisation voltage differences can result in large differences of the sheet resistance of the anodised film, this approach would result in an uneven film thickness. When we tried such a method initially, the same strip resistance value was reached at significantly lower cell voltages than with a “proper” resistance measurement. Obviously, the films had begun to pinch off at the side with the higher anodisation voltage.

All three named requirements were met by using a lock-in technique. We used a Stanford SR850DSP amplifier in current measuring mode. A sine shaped voltage excitation with an rms amplitude of typically 4 mV, and up to 32 mV for highly resistive samples, was applied. With a sufficiently long time constant, an accuracy of the resistance measurement of a few percent was achieved. Since the wiring of the sample holder was quite open and pickup therefore non-negligible at low frequencies, we used a lock-in frequency of 3 kHz in the vast majority of cases.

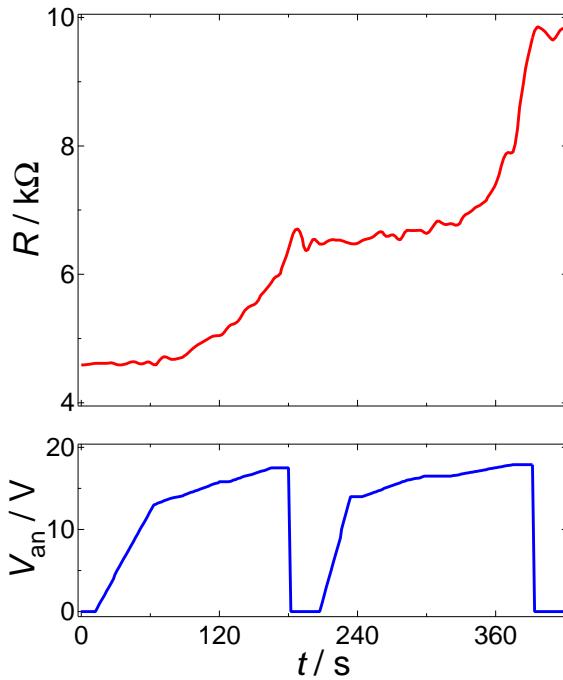
The voltage and resistance readings were fetched by a control computer and logged. A control programme with a graphical user interface allowed the experimentalist to modify the anodisation voltage ramping rate and, with a little smooth touch, tune the resistance to a desired value. The anodisation currents were not accessible to measurement since the anodised areas were too small and the currents thus too weak.

### 4.2.3. Anodisation dynamics

As expected, the sample resistance increased irreversibly as the anodisation voltage was applied. For a given voltage and ramping rate, the rate of resistance increase is a complicated function of voltage, metal thickness, and time itself. In fig. 4.2, the time evolution of the resistance and the voltage causing it are plotted as functions of time. The resistance values are rather low here since this was a sample in single electron transistor-like geometry (see 4.5). Typical features seen in fig. 4.2 are:

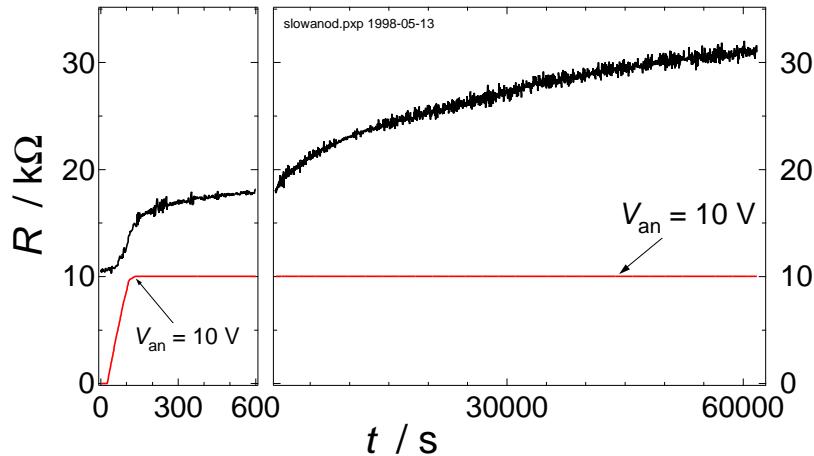
- It takes a certain voltage to cause any measurable impact on the resistance at all. Once that voltage is reached, the resistance reading climbs at an increasing pace.
- At high resistance values (small remaining film thicknesses), small differences in voltage cause big differences in resistance.
- Zeroing the voltage promptly and safely holds the resistance at its maximum value.

4. Anodised niobium nanostructures



**Figure 4.2.:** Anodisation voltage and sample resistance. The resistance  $R$  along the wire sample, measured *in situ*, increases irreversibly. By adjusting the cell voltage  $V_{an}$ , the rate of increase of  $R$  can be controlled. Zeroing  $V_{an}$  holds  $R$  at its current value. Note that  $dR/dT$  is not only a function of  $V_{an}$ , but of the time  $t$  as well.

### 4.3. Measurement setup and procedures



**Figure 4.3.:** Slow anodisation process at constant anodisation voltage. The resistance of the sample (a  $10\mu\text{m}$  long wire) continued to increase with time.

As mentioned before, the popular notion of an anodisation constant, i. e. a strictly linear dependence between the anodisation voltage and the amount of oxide created, does not hold. This is directly visible in fig. 4.3. In the anodisation shown here, the voltage was ramped up quickly to 10 V and then held constant for more than sixteen hours. During the whole time, the resistance continued to increase measurably. The resistance rate decreased, but nevertheless, under these constant voltage conditions the oxide would continue to grow until the metal were completely anodised.

This effect can be exploited for the high precision tuning of resistors: by stopping the voltage ramping well before the desired resistance value has been reached, and by simply waiting, one can reach the target resistance with a precision only limited by the resistance measurement, and then zero the voltage once that value has been reached. The slow dynamics allow for improved precision by using longer integration times on the lock-in amplifier.

## 4.3. Measurement setup and procedures

#### 4. Anodised niobium nanostructures

##### 4.3.1. Cryogenics

The first measurements were performed in a noncommercial dilution refrigerator that reached temperatures down to 95 mK. The temperature could be measured with a resistance thermometer calibrated over the whole accessible temperature range. Most measurements documented in this report were, however, done in a commercial dilution refrigerator of type TLE 200 from Oxford Instruments. A germanium resistance thermometer was calibrated down to 45 mK, and the base temperature of the cryostat was below 20 mK, as estimated from a preliminary measurement with nuclear orientation thermometry. A magnetic field up to 5 Tesla could be applied perpendicular to the sample. With a ramp rate of 0.1 T/min, the sample was warmed to approximately 40 mK by eddy currents.

##### 4.3.2. Amplifier electronics

From the sample, the DC leads went via filters (described below) and multiply thermally anchored wires to an amplifier box on top of the cryostat at room temperature. The bias voltage was symmetrised with respect to ground and fed to the samples via high ohmic resistors in the mentioned amplifier box. Voltage drops over the sample and over the bias resistors (proportional to the current) were picked up by low noise amplifiers, and the amplified voltages sent outside the shielded room for registration. Details about the measurement electronics can be found in Delsing's PhD thesis [23].

Signals were measured with digital voltmeters, initially with DMM of type Tektronix DM5520 with a buffer capacity of 500 points, later with Keithley 2000 DMM storing 1024 data points. The measurement times were synchronised with a Keithley 213 voltage source providing the bias voltage, which was stepped rather than swept continuously. Gate voltages were either generated with a second port on this Keithley 213 source, or with a Stanford Research Systems DS 345 signal generator.

Unless explicitly mentioned otherwise, the sweep of the bias or the gate voltage was always bidirectional, starting and ending at one of the edges of the swept voltage region.

All data were registered electronically with the help of a GPIB equipped Macintosh. For historical and practical reasons, the measurement software was written in various versions of LabVIEW (see appendix D).

The special amplifier used for the noise measurements that are the subject of chapter 5 will be described separately in 5.3.

#### 4.4. Resistor samples

##### 4.3.3. Shielding and filtering

The cryostat was placed in a steel enclosure ('shielded room'). Inside this enclosure, all electronics were analog. Leads into the shielded room were passed through filters in its wall. Inside the cryostat, the leads were multiply filtered against high frequency radiation. Figure 4.4 shows the dilution refrigerator insert with two types of filters mounted: the leads coming from room temperature are heat sunk at the various stages and passed through a copper powder filter [170] at the mixing chamber stage. From there to the connector at the bottom of the insert, the DC leads are formed by 500 mm Thermocoax [171], a commercial coaxial cable with very good damping properties [172]. More information about the cryostat and the filter design and properties can be found in [173].

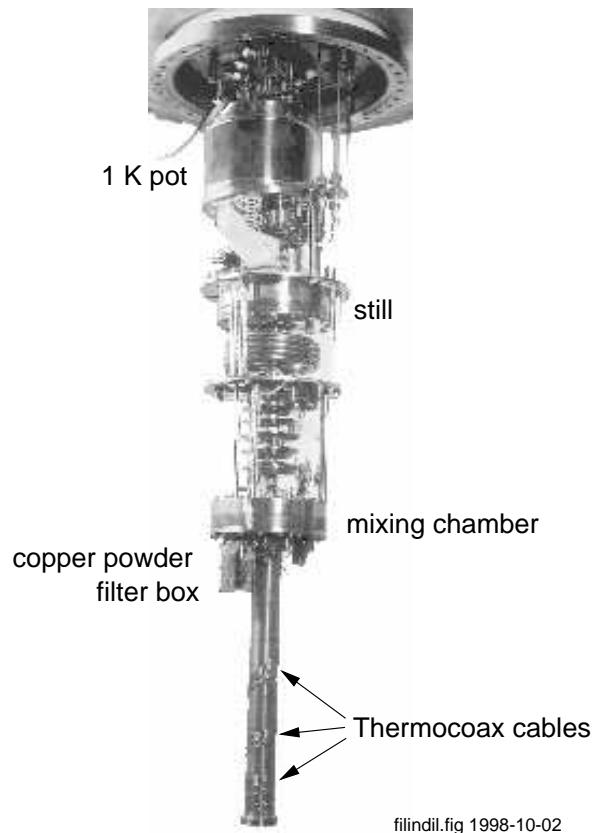
## 4.4. Resistor samples

### 4.4.1. Sample geometry and characterisation

The layout of the resistor samples is shown in fig. 4.5. The standard geometry were strips of  $10\ \mu\text{m}$  length,  $20\ \text{nm}$  thickness and a width limited by the lithography and pattern transfer techniques. At the time these samples were made, linewidths between  $120\ \text{nm}$  and  $180\ \text{nm}$  were the limit, caused by the pattern transfer to the germanium mask (this improved later, when a better RIE machine was taken into operation). The wires were either single, and attached to wider niobium pads for four probe measurements, or grouped into a  $120\ \text{nm}$  long wire as in fig. 4.5. These long wires had probe leads spaced at  $10\ \mu\text{m}$  distance from each other, and allowed the measurement of the resistance of each segment in a four probe configuration.

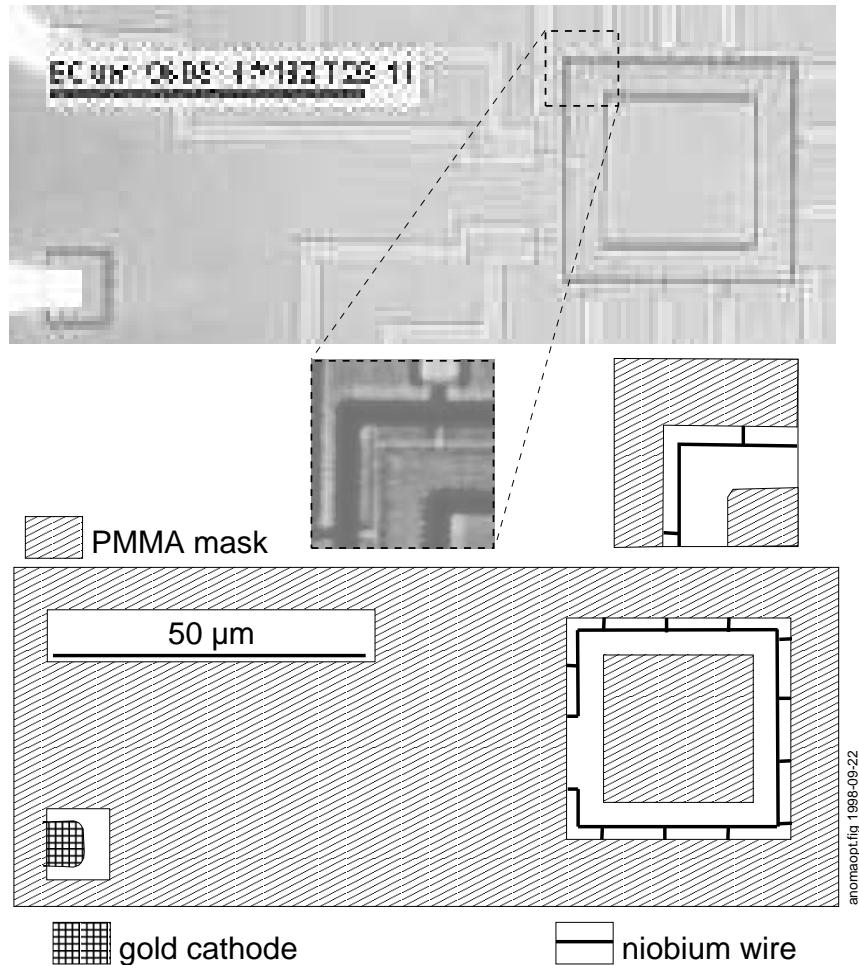
The anodised samples were characterised by low temperature magneto-transport measurements. For a highly resistive sample, fig 4.6 shows the current-voltage characteristics in different magnetic fields. There is an obvious Coulomb blockade, whose threshold is reduced in an external magnetic field. Another characteristic feature in the  $0\ \text{T}$  trace in fig. 4.6 is the telegraph noise pattern, that is the switching of the IVC between two curves along the load line. This telegraph noise was often observed in our samples, especially at high resistances. The generally accepted explanation of this pattern is that charge traps [77] upon charging and discharging induce charge differences on one grain that is important in the current path, in the sense of acting like a single electron transistor coupled in series with the rest of the film. The fluctuation of the charge in one trap between the two states 'charged' and 'discharged' creates telegraph noise. Several such

4. Anodised niobium nanostructures



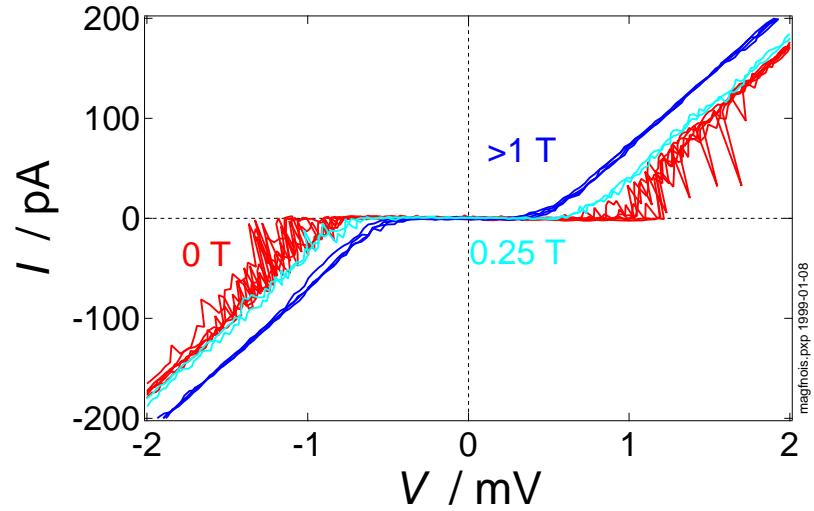
**Figure 4.4.:** Dilution refrigerator insert with low temperature filters. DC leads are formed as 500 mm Thermocoax cables near the sample at dilution refrigerator temperatures, and passed through a copper powder filter box.

#### 4.4. Resistor samples



**Figure 4.5.:** Optical micrograph of resistor samples and its artistic interpretation. The Nb wire, divided into twelve sections of  $10\text{ }\mu\text{m}$  length each, is barely visible through the window in the PMMA anodisation mask. The small window on the left exposes a gold contact used as on-chip-cathode to the electrolyte.

4. Anodised niobium nanostructures



**Figure 4.6.:** Effect of an external magnetic field on the current-voltage characteristics of a highly resistive samples. The threshold voltage is reduced by about half. Telegraph noise affecting the IVC in the field free state is smoothed out in the external field. Several traces have been superimposed in each case.

#### 4.4. Resistor samples

two level fluctuators (TLF) may be in effect simultaneously.

Telegraph noise is also encountered in single electron transistors made by conventional techniques. If it is seen, the sample is often dismissed as “infected by a TLF”. Sometimes the sample can be “cured” by thermally cycling it and thereby changing the population of defects. Interestingly enough, applying a magnetic field on an “infected” SET usually does not suppress the telegraph noise. Noise similar to that seen in fig. 4.6 has been seen in one-dimensional regular arrays of small junction SQUIDs [173].

We do not have a satisfactory explanation for the observed noise pattern and can only state that here it seems to be directly related to the superconducting properties of the samples (see also 4.4.2). To add to the confusion, one might add that while here the sample is noisier in the superconducting state, Wahlgren has observed that arrays were more noisy in the normal conducting state [89, ch. 7, fig. 4]. Very similar telegraph noise has been observed by Fujii et al. in completely normal conducting composite films [174].

##### 4.4.2. Superconductor-insulator transition

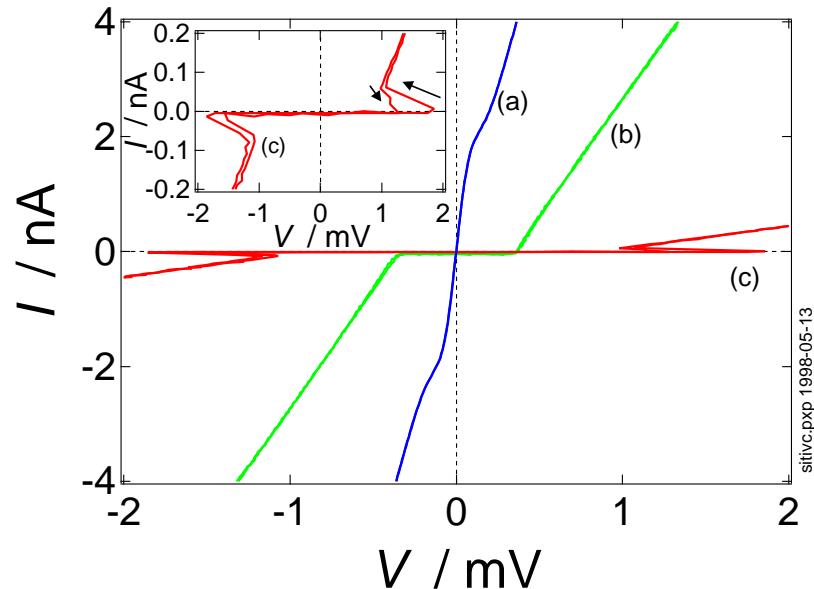
Figure 4.7 collects the types of current-voltage characteristics we observed in the resistor samples. The data presented here were taken on strips on three different chips. The strips had equal dimensions, but were anodised for different times and to different final voltages. The measurements were taken in a four probe configuration, at temperatures between below 50 mK and 200 mK, and in the absence of an externally applied magnetic field.

For the samples with lowest resistance, like in trace (a), we found a remnant of the supercurrent, visible as a region of reduced differential resistance for currents up to about 2 nA. The sample whose IVC is shown as (a) in fig. 4.7 had a sheet resistance of approximately  $1.5 \text{ k}\Omega/\square$ . For samples anodised to greater depth, we observed an increase of the differential resistance around zero bias that we have already referred to as the “Coulomb blockade” (which will be finally justified in 4.5).

Trace (b) in fig. 4.7 is a typical example of a sharp Coulomb blockade with a well-defined threshold voltage. This sample had a sheet resistance of about  $8 \text{ k}\Omega/\square$ . In samples with very high sheet resistances, we observed not only a sharp blockade, but even a backbending of the IVC (trace (c) and inset in fig. 4.7).

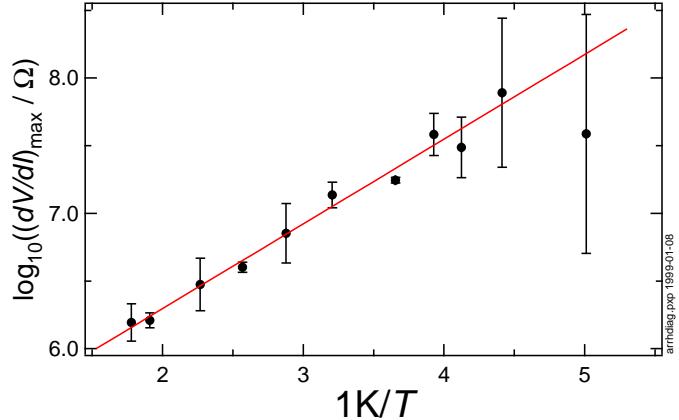
The backbending in the sweep direction from low bias outwards could be explained by heating of the sample at the onset of current flow, where the relatively high voltage leads to power dissipation even at low currents. On the other hand, this would not explain a backbending in both sweep

4. Anodised niobium nanostructures



**Figure 4.7.:** Current-voltage characteristics (IVC) of three resistor samples. With increasing sheet resistance (measured at high bias and/or at high temperature), the IVC changed from a supercurrent remnant ((a)  $1.5 \text{ k}\Omega/\square$ ) to a sharp Coulomb blockade ((b)  $8 \text{ k}\Omega/\square$ ). Samples with very high sheet resistance showed a backbending IVC ((c)  $40 \text{ k}\Omega/\square$ ). Sample dimensions in each case were  $10 \times 0.15 \mu\text{m}^2$ , the data were taken at temperatures of about  $200 \text{ mK}$  (a) or at base temperature below  $50 \text{ mK}$  (b,c), respectively, without applying an external magnetic field.

#### 4.4. Resistor samples



**Figure 4.8:** Temperature dependence of the zero bias differential resistance. The Arrhenius type dependence indicates a thermal activation behaviour. Values have been determined from numerical differentiation of measured current-voltage characteristics. No external field was applied during these measurements.

directions. The backbending IVC show a remarkable similarity with the IVC observed in arrays of ultrasmall Josephson junctions by Geerligs et al. [38] and Chen et al. [61].

Even the observed telegraph noise fits into the picture of the resistor strips behaving as an array of superconducting junctions. Haviland et al. [173] have observed it accompanying the superconductor-insulator transition in one-dimensional SQUID arrays, and gave an explanation for the observed hysteresis by analogy to the resistively shunted model for Josephson junctions [175].

The temperature dependence of the resistance is a usual criterion for classifying a material as insulating or undergoing a superconducting transition. Since our samples had such nonlinear IVC, one cannot assign a global resistance value but looks instead, for example, at the differential resistance at zero bias. A dedicated measurement would have to involve a carefully devised biasing scheme and a sensitive detection, preferably involving a lock-in technique [107]. Even from the measured raw IVC one can, however, extract some information about the zero bias differential resistance. For one sample, values gathered from the numerical differentiation of IVC are plotted as a function of inverse temperature in fig. 4.8. The

#### 4. Anodised niobium nanostructures

errors indicated here were estimated from the curvature around the maximum in the differential resistance. For the temperature range of fig. 4.8, before the sample went into a full Coulomb blockade, we see that the zero bias resistance follows an Arrhenius law

$$R_0(T) = R^* \cdot e^{\frac{E_a}{k_B T}}, \quad (4.1)$$

which suggests a thermally activated behaviour [107]. From fig. 4.8, we extract an activation energy corresponding to a temperature of about 0.6 K, or to a voltage of  $50 \mu\text{V}$ . This is of the same order of magnitude as the voltage swing and the temperature of its disappearing in our samples in the SET-like geometry (see 4.5). More quantitative statements are complicated since the sample might have been inhomogeneous; this one had a sheet resistance of about  $4 \text{k}\Omega/\square$ .

##### 4.4.3. Onset of the Coulomb blockade

Defining a quantitative measure of the Coulomb blockade is an old problem. Threshold voltages are hardly ever well-defined due to rounded current-voltage characteristics, and since these IVC are also nonlinear over many decades in bias voltage, extrapolating their tangent at the end of an arbitrarily chosen voltage range would produce ambiguous results. A solution to this problem was found by Wahlgren [33, 76], who has shown the usefulness of the *offset voltage* analysis when studying environmental effects on the Coulomb blockade.

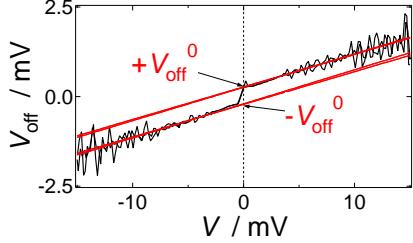
The local offset voltage  $V_{\text{off}}(V)$  is computed numerically by extrapolating the tangent to the  $I(V)$  curve and taking its intersection with the voltage axis:

$$V_{\text{off}}(V) = V - I(V) \left. \frac{dV'}{dI} \right|_V. \quad (4.2)$$

Figure 4.9 shows a calculation of  $V_{\text{off}}(V)$  for a resistor sample. We see that  $V_{\text{off}}(V)$  has a jump at zero bias and varies with approximately constant slopes in the vicinity. The intersection of the extrapolation here with the  $V_{\text{off}}$ -axis, which we call  $V_{\text{off}}^0$ , is therefore well-defined (see fig. 4.9).

This value has been shown to be of particular interest in the case of the Coulomb blockade in double junctions, where it gives the limit for the blockade in the so-called *global rule* for low environment impedances, where the whole electromagnetic environment influences the Coulomb blockade [76]. It is not surprising that  $V_{\text{off}}^0$  is useful in the case of our resistor samples. Since we assume that we have a very large number of grains, probably

#### 4.4. Resistor samples



**Figure 4.9.:** Definition of  $V_{\text{off}}^0$ . Extrapolation of  $V_{\text{off}}(V)$ , calculated from the tangent to the  $I(V)$  curve, to zero bias gives  $V_{\text{off}}^0$ , a measure of the Coulomb blockade.

several thousand in a  $10 \mu\text{m}$  strip, the voltage drop per intergranular junction is small, and according to the horizon picture of tunnelling [89, and references therein], the global rule should then apply.

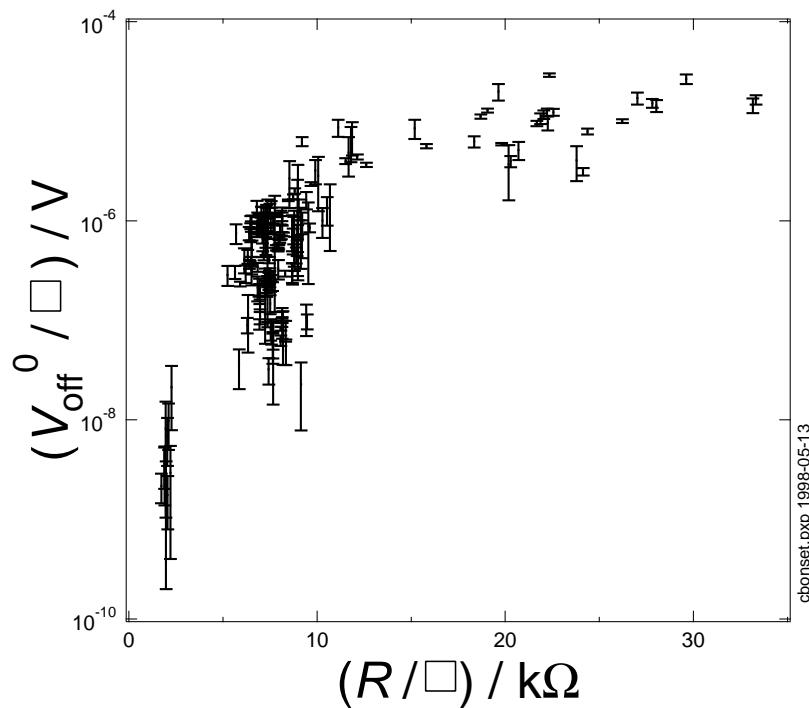
For each IVC, which was taken bidirectionally by ramping the bias up and down, we made four independent extrapolations of  $V_{\text{off}}$ . Figure 4.10 shows the results of this analysis for a set of 187 strips from four different batches with lengths between  $10 \mu\text{m}$  and  $120 \mu\text{m}$ . The errors have been estimated as the standard deviations of the four  $V_{\text{off}}^0$  values per IVC. The correlation between extrapolated zero bias offset voltage  $V_{\text{off}}^0$  and sample resistance  $R$  is obvious here where both quantities have been normalised to the number of squares in the films.

Inhomogeneities may be responsible for the significant spread in the data, but the trend is clear: the Coulomb blockade is appreciable for all samples with a sheet resistance of more than  $10 \text{k}\Omega/\square$ , and at least three orders of magnitude less for all samples with less than  $5 \text{k}\Omega/\square$ . In the intermediate region, there is some clutter due to measurement uncertainties. There is also an uncertainty in the determination of the number of squares. The sample widths were estimated from scanning electron microscope inspection of samples produced under nominally identical conditions, and the error in the measurement of the film area (not indicated in fig. 4.10) may very well be up to 20%.

Within this measurement accuracy, the superconductor-insulator transition we observed here in an unconventional way set in at a sheet resistance that is compatible with  $h/(4e^2) \approx 6.4 \text{k}\Omega$ . It has been suggested from studies on ultrathin metal films [68, 176] that there should be a universal sheet resistance for the superconductor-insulator transition and that it might well be just  $h/(4e^2)$ . Values that agree with this, by a factor of two or three at worst, have not only been found in studies of quench-condensed films [62, 64, 65], but also in regular arrays of ultrasmall Josephson junctions [38, 61].

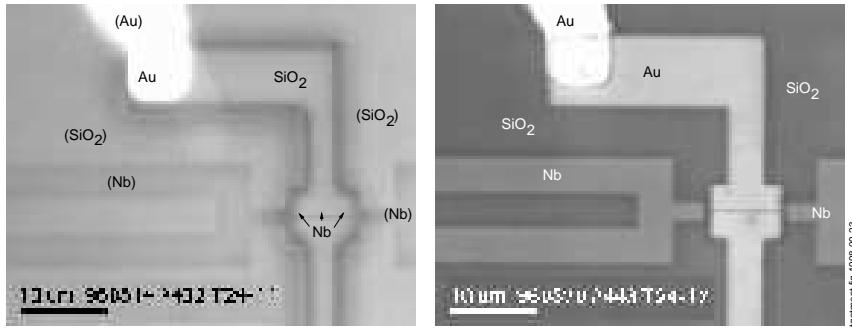
Our resistor samples are of course not regular arrays of Josephson junc-

4. Anodised niobium nanostructures



**Figure 4.10.:** Onset of the Coulomb blockade (CB) in resistor samples. Both  $V_{\text{off}}^0$  and the resistance  $R$  are normalised to the number of squares. The CB is suppressed below  $6 \text{ k}\Omega/\square$ . Errors were estimated from the standard deviation of four independent extrapolations per data set (bidirectionally swept IVC, extrapolated below and above zero, respectively).

#### 4.4. Resistor samples



**Figure 4.11.:** Anodised wire with top gate, one of the geometries that we tried and that did not give a gate effect. The optical micrographs show a sample after preparation of the anodisation mask (left) and after evaporation of the gate and lift-off (right). Materials in parentheses are seen through the PMMA mask.

tions, and definitely not homogeneous, but granular. The average grain size is supposedly a few nanometres (see 3.3.2). The superconducting coherence length, on the other hand, should be around 40 nm for niobium [20], and since this is much larger than the grain size, the distinction between an homogeneous and a granular film should vanish [66].

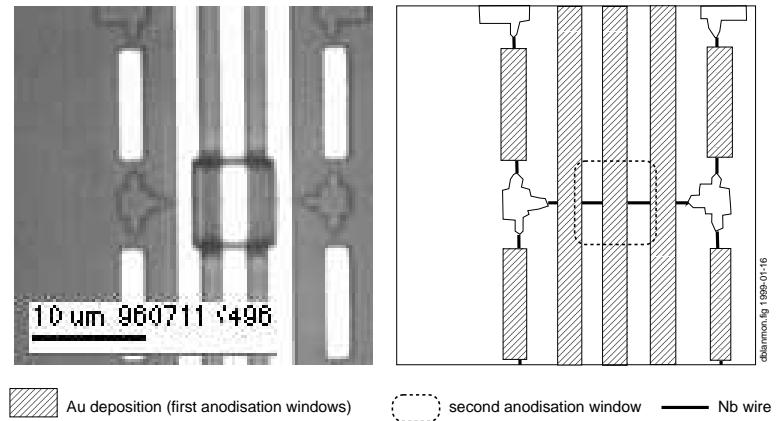
##### 4.4.4. No gate effect

At this point in the investigations, it remained to show that the observed feature that we have boldly called “Coulomb blockade” so far actually was caused by charging effects. To prove this, one has to be able to modify the current-voltage characteristics with the voltage on a capacitively coupled gate. In Chandrasekhar’s experiment [11], side gates close to their short wires were sufficient to produce a gate effect. The indium oxide they used showed “the presence of large grains” [10], and they noted that “only one or perhaps two segments (...) [were] present” in their samples.

Since we expect to have many more segments, due to a smaller initial grain size and the additional serration of the interface between niobium and the oxide, it is not surprising that we did not see a gate effect with side gates. Even top gates, with a much better capacitive coupling to the strips, did not give a gate effect. Figure 4.11 shows a top gated sample before anodisation and after evaporation of the gates.

We also tried an approach with two anodisation processes, which can

#### 4. Anodised niobium nanostructures



**Figure 4.12.:** Sample with a double anodisation mask, another device developed in pursuit of a gate effect (yet another failure). In a first step, the niobium wires had been anodised where the subsequently deposited gold marks the windows. After removal of the first mask, a second mask was created and opened as shown, for anodisation of the two pieces of niobium wire exposed in the window and between the gold strips. The sample's current-voltage characteristics could **not** be influenced with a gate voltage applied to the central gold strip.

be seen as a step towards the samples in SET-like geometry. Even at the length scales of a few micrometres, which can be seen in fig. 4.12, there was no gate effect detectable.

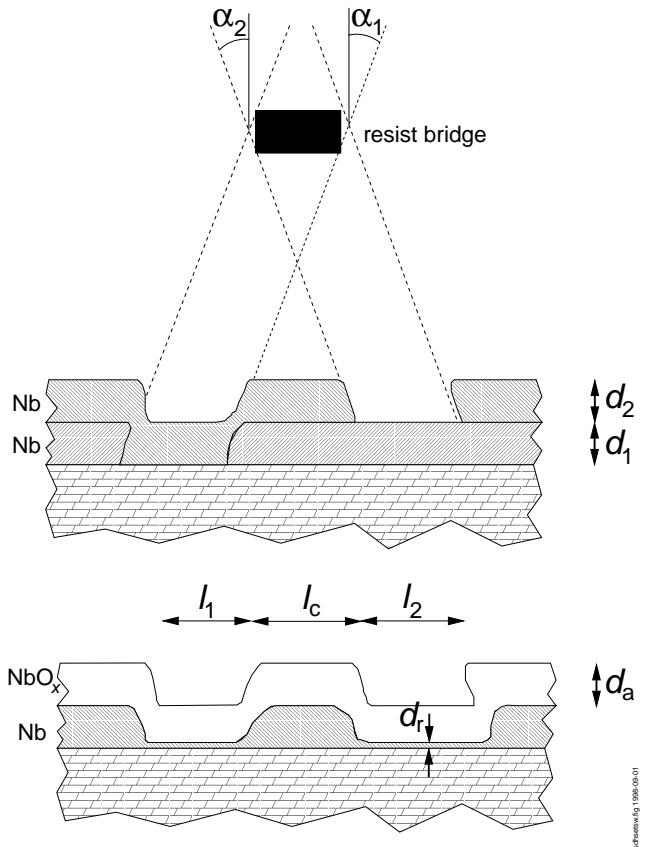
## 4.5. Samples in SET-like geometry

### 4.5.1. Fabrication technique

In order to reduce the number of grains participating in the electrical transport and giving rise to the Coulomb blockade, we used the combined shadow evaporation and anodisation technique illustrated in fig. 4.13. The corresponding mask is shown in fig. 4.14, and a niobium film patterned by this technique in fig. 4.15.

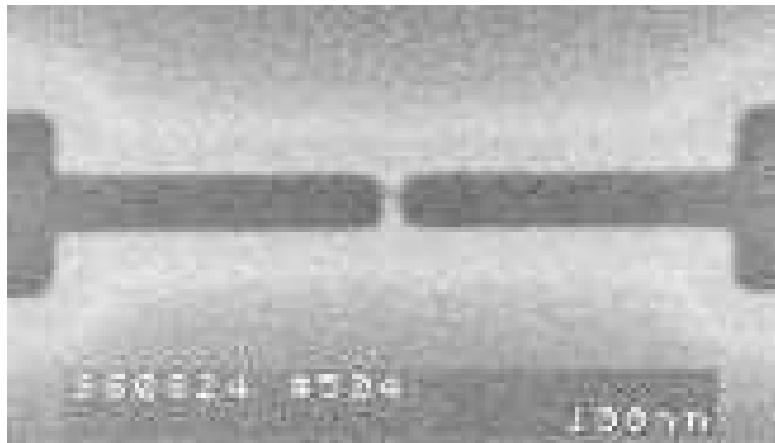
The lengths  $l_1 \approx l_2$  of the weak links are defined by the lithography as the width of the suspended bridge, while the island length  $l_c$  is determined by the pattern overlap, and can be made very small. In two subsequent

#### 4.5. Samples in SET-like geometry

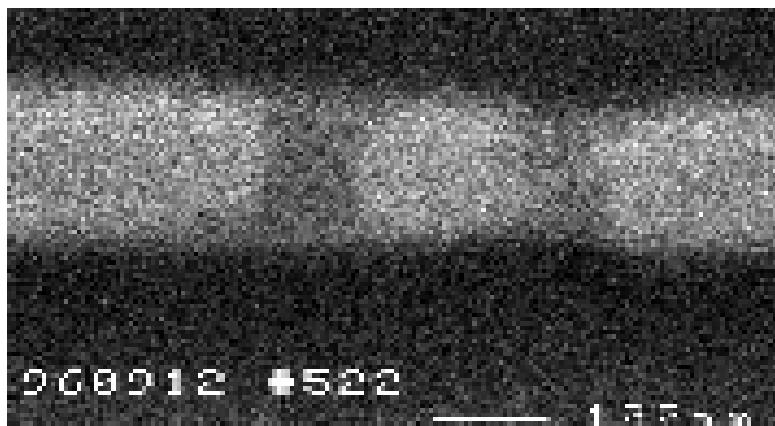


**Figure 4.13.:** Shadow evaporation and anodisation technique for the fabrication of SET-like structures. Anodisation creates an oxide layer of thickness  $d_a$ , thinning the weak links to a thickness  $d_{rl}$ . Neglected in this sketch are the deposition of material on the bridge during the two evaporation, and the swelling of the oxide film during anodisation.

#### 4. Anodised niobium nanostructures

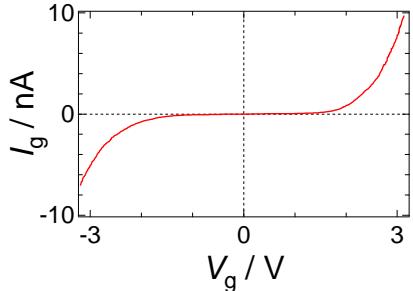


**Figure 4.14.:** Mask for fabrication of samples in SET-like geometry, after pattern transfer. The darkest areas are the substrate, oxidised silicon. Adjacent light areas show where the organic resist support layers have been underetched by oxygen RIE. The suspended germanium bridge in the centre is here damaged by a tiny crack.



**Figure 4.15.:** Variable thickness weak links in a niobium wire made by double angle evaporation. Scanning electron micrograph taken after Nb deposition and liftoff and before further processing (anodisation).

#### 4.5. Samples in SET-like geometry



**Figure 4.16.:** Current-voltage characteristic for the leakage current between an anodised double weak link structure and its top gate, taken at about 30 mK.

niobium evaporation, film thicknesses  $d_1 \approx d_2$  are deposited. It is critical to have the difference between  $d_1$  and  $d_2$  as small as possible, so that both thin spots are further thinned out to the same residual film thickness  $d_r$ . In the simplified sketch of fig. 4.13, we have neglected the deposition of material that leads to an asymmetry in the shape of both weak links, and the swelling of the film during anodisation (in reality,  $d_a \approx 3 \cdot (d_1 + d_2 - d_r)$ ).

The scanning electron micrograph of the mask (fig. 4.14) shows a problem encountered occasionally with four layer resist, namely tensile stress in the germanium layer that can lead to cracks if only a few individual bridges are created at large distances from each other. If the pattern design allows it, additional holes can be made in the mask near the intended bridge to release some of the stress. Also, increasing the Ge thickness can remedy a lot of these problems.

Figure 4.15 shows the two niobium thin spots before anodisation and deposition of the gate electrode on top of the structure.

The samples were rinsed carefully with deionised water immediately after the anodisation. Ultrasonic excitation at this stage appeared to destroy many samples. A gentle surface ashing made with oxygen RIE provided sufficient adhesion of the gold gates to the samples. 50 nm of gold were evaporated to guarantee a continuous film even where it ran over the strip edges. These gates had a two terminal resistance of about  $60 \Omega$  at a length of  $160 \mu\text{m}$  and a width of  $8 \mu\text{m}$ , narrowing down to  $3 \mu\text{m}$  in the immediate vicinity of the anodised area.

We tested the gate insulation by measuring the current-voltage characteristics between gate and source, as shown in fig. 4.16. In most samples, the insulation was found to be this good. Up to a gate voltage of about 1.5 V, the gate current was too small to be measured, which translates to an insulation resistance of at least  $30 \text{ G}\Omega$ . For higher gate voltages, a measurable leak current set in. In some samples, this current flow started

#### 4. Anodised niobium nanostructures

at voltages as low as 0.5 V. The leakage was easily detected by the shift of the measured IVC, and these samples were dismissed.

##### 4.5.2. IVC and gate effect

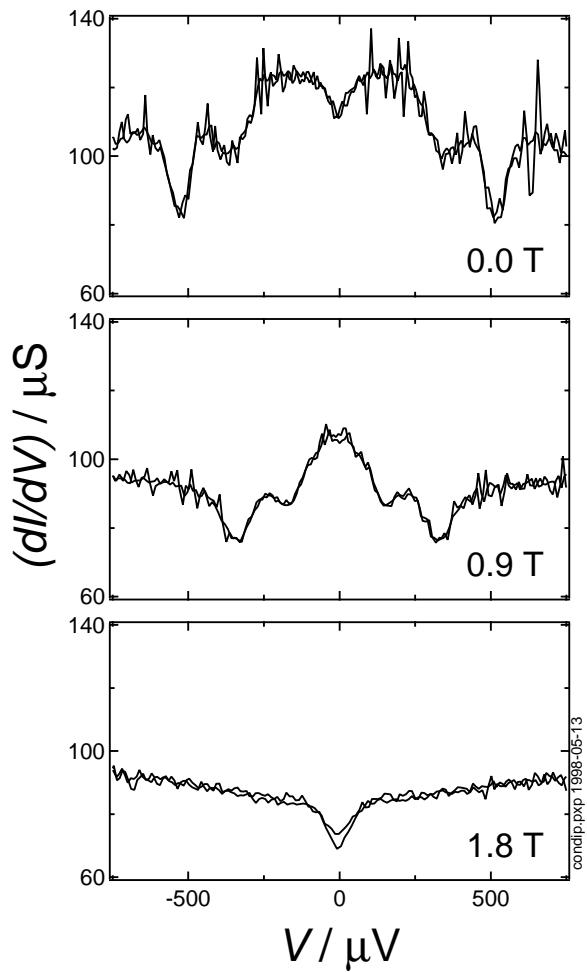
All sufficiently anodised samples showed a Coulomb blockade at millikelvin temperatures. Sometimes it manifested itself just as a hardly perceptible dip in the differential conductivity at zero bias. In other samples, we observed a rather sharp blockade, in several samples even at 4.2 K. In neither of these cases, very weak or very strong blockade, did we manage to modulate the IVC with a gate voltage. Only when the IVC in the case without external field had a more complicated structure, as in the top panel of fig. 4.17, was there a measurable gate effect. As an external magnetic field was ramped up, the series of conductivity dips and peaks moved towards zero bias and finally merged into a single conductance dip there, obviously resulting from the Coulomb blockade of single electron tunnelling. The off-zero-bias structures are probably related to the superconducting properties, and the zero bias conductance dip in the field-free case may be indicating the Coulomb blockade of Cooper pair tunnelling [4].

To measure the gate response of the sample's IVC, we biased it at a number of practically constant currents and swept the gate voltage up and down with a frequency of about 8 mHz. The voltage between drain and source was registered in the usual way with the low noise amplifiers in the cryostat top box. The gate voltage was applied via a voltage divider, and diagnostic leads made it possible to verify that the gate voltage was actually present on the sample.

In the superconducting state, no gate modulation was discernible from all noise without further analysis. For the measurement shown in fig. 4.18, we suppressed superconductivity completely by applying an external field of 2 T. The causal influence of the gate voltage is obvious. These control curves are far from the almost perfect sine curves a single electron transistor gives, but are typical for systems of multiple tunnel junctions (MTJ). The large period of the oscillations of about 50 mV in gate voltage is also typical for an MTJ system. If we just had a two junction SET, this period would indicate an unreasonably low total island capacitance of only 3 aF.

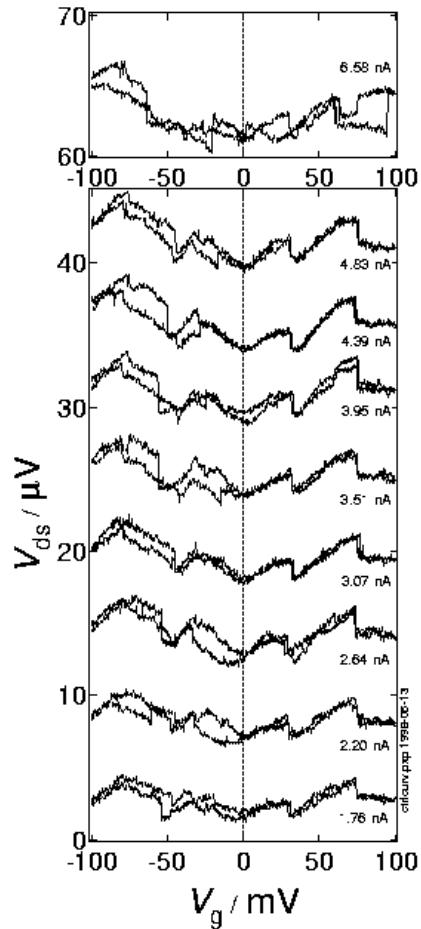
Instead of showing the gate effect by recording modulation curves at fixed bias points, one can map out the whole modulation range of the current-voltage characteristics at once [59] by recording the IVC while simultaneously oscillating the gate voltage at a higher frequency. This is very useful for a quick verification, and for a gate leak test. If the gate is leaking current, the IVC will be shifted as a whole by the oscillating

4.5. Samples in SET-like geometry



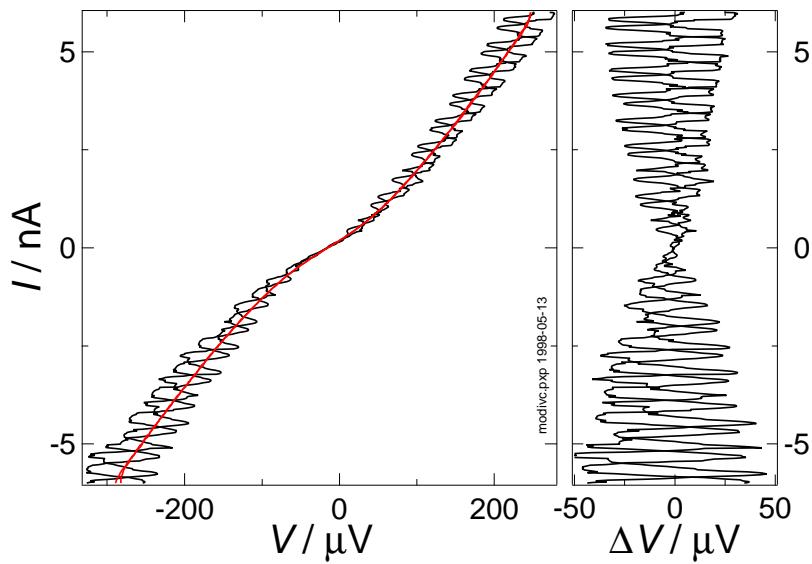
**Figure 4.17.:** Coulomb blockade in an SET-like anodised structure. As superconductivity was suppressed by an external magnetic field, the off-zero-bias conductance peaks disappeared, and a Coulomb blockade for single electrons remained. Data were taken at  $T \approx 40 \text{ mK}$ .

4. Anodised niobium nanostructures



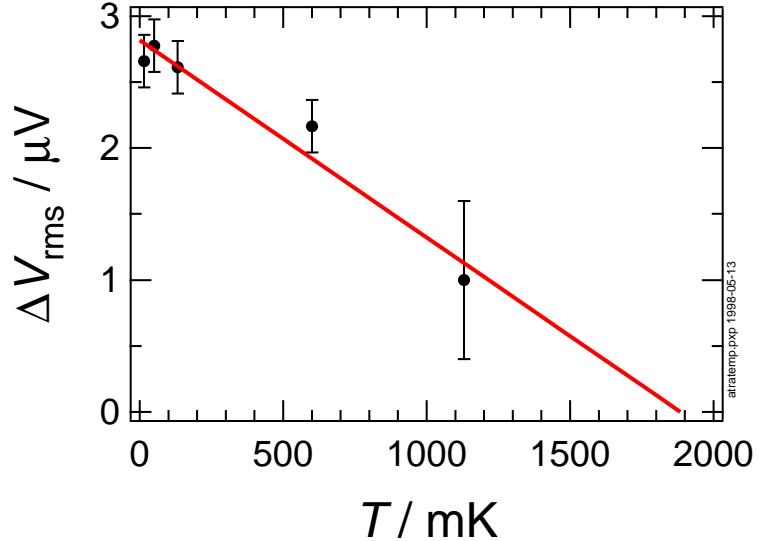
**Figure 4.18.:** Control curves for an SET-like anodised structure. The drain-source voltage  $V_{ds}$  at different current bias points oscillated as the voltage  $V_g$  applied to the gate on top of the structure was ramped up and down (once per each bias point). Data were taken at dilution refrigerator base temperature below 30 mK, and superconductivity was suppressed by an external field of 2 T.

#### 4.5. Samples in SET-like geometry



**Figure 4.19.:** IVC of an SET-like anodised structure with gate modulation. The rms value of the sine-modulated gate voltage was 120 mV and its frequency 40 times that of the bias sweep. The right panel shows the deviation of  $V$  from the unmodulated IVC in the left panel. Data were taken at a temperature below 50 mK, and no external magnetic field was applied.

#### 4. Anodised niobium nanostructures



**Figure 4.20.:** Temperature dependence of the voltage swing in an anodised weak link sample with SET-like geometry.

gate voltage, whereas a true gate effect is indicated by a behaviour as in fig. 4.19. The voltage swing  $\Delta V$  vanishes at zero bias. In the right panel,  $\Delta V$  is plotted separately. It has been calculated as the difference between the modulated IVC in the left panel and an IVC recorded in the same configuration with the gate voltage amplitude zeroed.

#### 4.5.3. Temperature dependence of the gate effect

An important parameter for a single electron device is the temperature  $T^*$  at which the gate effect vanishes. It should give information on the energy scale at which the Coulomb blockade occurs. For single electron transistors made by angular evaporation, Wahlgren [74] gives the approximate relation between  $T^*$  and the maximum voltage swing  $\Delta V_{\text{max}}$

$$e\Delta V_{\text{max}} \approx 4k_B T^*. \quad (4.3)$$

This relation seems to hold even for the very small SET made by Nakamura et al. [177] that had a  $T^*$  of more than 100 K. In both these cases, the junction resistances were considerably above  $R_K$ .

#### 4.6. Conclusion: anodised niobium nanostructures

The temperature dependence of the voltage swing in one of our samples in SET geometry is shown in fig. 4.20. For the low temperature values up to 600 mK, the swing  $\Delta V$  between gate modulated and unmodulated IVC was analysed in the bias region between  $-7.5$  nA and  $7.5$  nA, and the root-mean-square value is plotted together with the estimated uncertainty. The high temperature value at 1130 mK was determined by comparison of the voltage swings at  $\pm 7.5$  nA in two measurements with a square shaped gate signal, and by normalisation to the low temperature amplitude.

As expected, the amplitude of the modulation decreased with temperature. A simple extrapolation of the few data points in fig. 4.20 gives a  $T^*$  somewhere between 2 K and 3 K.

Instead of a maximum voltage swing of about  $100\ \mu\text{V}$  at low temperature, we would have expected a value several times higher for the measured  $T^*$  according to eq. (4.3). The comparatively low resistance of these samples may be responsible for the suppression of the IVC modulation amplitude.

### 4.6. Conclusion: anodised niobium nanostructures

We have demonstrated that anodic oxidation of nanofabricated niobium thin film wires can be used to produce resistors of several hundred kiloohms on a length of ten micrometres. This technique is intrinsically limited by the onset of a Coulomb blockade when the sheet resistance per square exceeds the quantum resistance  $6\ \text{k}\Omega/\square$ . The anodised wires show transport properties typical of an array of ultrasmall Josephson junctions, where superconducting effects coexist with charging effects. The low temperature current-voltage characteristics of these samples show a superconductor-insulator transition where the degree of anodisation is the tuning parameter.

Placing short anodised areas with the aid of lithographic techniques, one can fabricate transistor-like samples whose current-voltage characteristics can be modulated by a gate voltage. This gate effect disappears, however, already at a temperature of a few Kelvin, which might turn out to be the limiting factor for potential applications.

4. *Anodised niobium nanostructures*

## 5. Noise in a single electron transistor

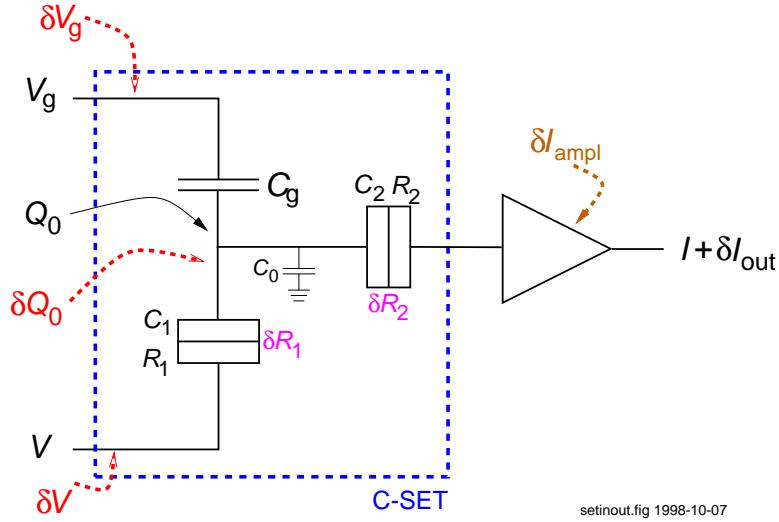
### 5.1. Noise model

The model we use for the single electron transistor's input and output noise is laid out in fig. 5.1. The capacitively coupled SET has three input quantities, all of which might be affected by noise: the bias voltage  $V$ , the gate voltage  $V_g$ , and the background charge  $Q_0$ . However, due to careful filtering of the leads (see 4.3.3), we can neglect the noise in both bias and gate voltages, which leaves the background charge as the only noisy input quantity.

Background charge noise is generally associated with charge traps [178, 179]. Their exact nature and location is still disputed, they may actually be at some distance from the island [180, 181]. Whenever these traps, located sufficiently close to the C-SET's island, change their charge state, the offset charge of the island is changed, and the transport characteristics of the SET are modified. This is analogous to the situation in SQUIDs, where background fluxons frozen in the superconductor are responsible for a large portion of the low frequency noise. Like in the SQUID analog, the background charge noise in SET appears to be largely a materials problem. However, no significant improvements have been made yet by varying the materials for SET [182, 183]. Whereas in SQUID, the low frequency noise contribution from background fluxons can be eliminated by a bias reversal scheme [184], no such scheme has yet been devised for SET, making improvements on the materials and circuitry more urgent than ever.

The second contribution to LFN in SQUIDs comes from fluctuations of the junction resistances  $R_{1,2}$ . It appears obvious that such a fluctuation could also occur in an SET and contribute as an output noise source. The observation of LFN caused by resistance fluctuations has been reported recently [185]. Speculative to date is a correlation between background charge noise and junction resistance fluctuations [13], which might be caused by

5. Noise in a single electron transistor



setinout.fig 1998-10-07

**Figure 5.1.:** Schematic diagram of a capacitively coupled single electron transistor (C-SET), consisting of two junctions with resistances  $R_1$ ,  $R_2$  and (very low) capacitances  $C_1$ ,  $C_2$ , and of a gate capacitor with  $C_g$ . In a voltage biased configuration, the input quantities voltage  $V$ , gate voltage  $V_g$  and offset charge  $Q_0$  due to background charges result in a current  $I$  at the output of the amplifier. Its noise  $\delta I$  is the result of noise at the input of the SET, especially fluctuations in the background charge  $\delta Q_0$ , of the amplifier noise  $\delta I_{\text{ampl}}$ , and of fluctuations in the junction resistances  $\delta R_i$ . In this simplification, the triangular symbol stands for any generic amplifier. The output signal can actually be a voltage that is proportional to the current being measured, and in that case, the noise added by the amplifier will be a voltage noise.

### 5.1. Noise model

charged defects in the tunnel barriers, affecting both the barrier transparency and the island charge upon charging.

Any combination of bias voltage  $V$ , gate voltage  $V_g$  and offset charge  $Q_0$  defines an operating point of the SET with a certain output current  $I$  and gain  $\partial I / \partial Q_g$ . Background charge fluctuations with spectral noise density  $S_{Q_g}(\omega)$  and resistance fluctuations with spectral noise densities  $S_{R_i}(\omega)$  will then add up, taking the former's contribution up to the second order in the gain and neglecting correlation, to a current noise

$$S_{I_{Q,R}}(\omega) = \left( \left( \frac{\partial I}{\partial Q_g} \right)^2 + \frac{\alpha}{4} \left( e \frac{\partial^2 I}{\partial Q_g^2} \right)^2 \right) S_{Q_g}(\omega) + \sum_{i=1}^2 \left( \frac{\partial I}{\partial R_i} \right)^2 S_{R_i}(\omega), \quad (5.1)$$

where  $\alpha$  is an expansion coefficient describing contributions in second order in gain that we will come back to below (see page 116).

Another fundamental noise source is shot noise [80] generated in the tunnel junctions. In our case, it is negligible up to bias voltages well above the Coulomb blockade threshold, so that the noise generated by both junctions can be regarded as uncorrelated [186]. For linear arrays with  $n \gg 2$  junctions, the shot noise suppression resulting from this uncorrelation has recently been measured [89]. The shot noise of our single electron transistor at high bias is then

$$S_{I_e}(I) = \frac{2eI}{2} = eI. \quad (5.2)$$

Measurements on an SET require an amplifier that inevitably adds noise to the output signal. The total noise measured at the output of the amplifier is the sum of the amplifier noise, the amplified shot noise, the amplified SET output noise caused by resistance fluctuations, and the amplified background charge input noise of the SET.

Mind the consistently inconsistent use of the term *charge noise* in the literature. We will try to be stringent here and either speak of *background charge noise*, alias *input charge noise*, or of *input referred noise*, alias *charge equivalent noise*. The latter is defined in analogy to *flux noise* in SQUID, which is just the spectral density of input flux fluctuations that would cause the observed noise at the system's output under the assumption that no other noise contributions arise from the SQUID itself or the amplifier electronics, in other words, for an ideal system.

Similarly, charge equivalent noise is the measured noise at the output of the system (SET plus amplifier), divided by the amplifier gain and by the SET's gain. Since an SET is useless without an amplifier, there is a certain justification for using this quantity as a figure of merit. It is customary to

## 5. Noise in a single electron transistor

compare the noise of SET systems at the frequency  $f = 10\text{ Hz}$ , where the LFN is pronounced in almost all samples, yet measurement times are still reasonably short.

It appears that the evaluation at 10 Hz has no drawbacks over the approach regarding integrated quantities in the frequency band (50...100) Hz [13].

Having the lowest charge equivalent noise at 10 Hz is a matter of a chase between single electronics laboratories. The current record is held by the PTB-MSU collaboration that achieved  $2.5 \cdot 10^{-5} e/\sqrt{\text{Hz}}$  [185] in aluminium devices of stacked design that minimised the contact area between substrate and island. The previous record of  $7 \cdot 10^{-5} e/\sqrt{\text{Hz}}$  had also been set in a multilayer device [187].

Other characteristic figures one might like to compare are the corner frequency of the LFN and the white noise figure. These quantities, however, say more about the amplifier than about the SET, and since we regard the SET as the device under test and the amplifier as an unavoidable complication, we will not work with these figures.

In the evaluation of the measurements presented below, we introduce the *differential charge equivalent noise* (see 5.4), which is a quantity describing only properties of the SET without involving amplifier characteristics at all.

## 5.2. Sample fabrication and characterisation

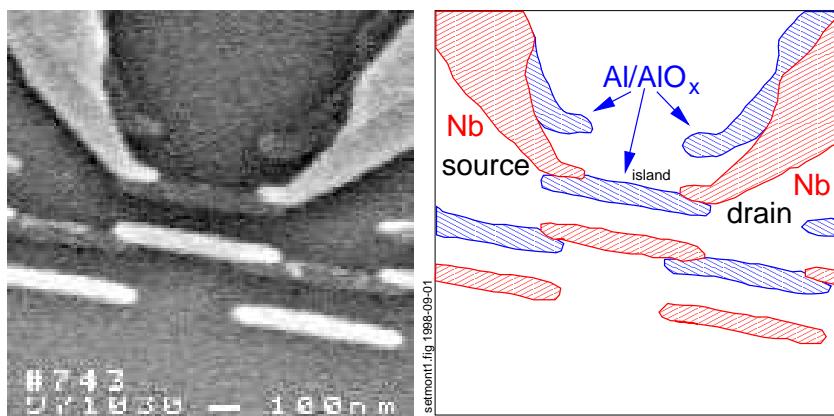
### 5.2.1. Fabrication

The sample, whose scanning electron micrograph is shown in fig. 5.2, was made by the shadow evaporation technique (see 3.2.4), using the four layer resist described in 3.3.2. Details about the fabrication process can also be found in the recipe appendix (C.2.1).

Substrate material was silicon from a two inch wafer, thermally oxidised to a depth of approximately  $1\mu\text{m}$ . The base material for the junction structure was aluminium, which here formed the island of the transistor. The aluminium can be seen constituting the structures with relatively poor contrast in fig. 5.2. The film thickness was 20 nm, and the deposition was carried out under an angle of  $-21^\circ$  to the substrate normal.

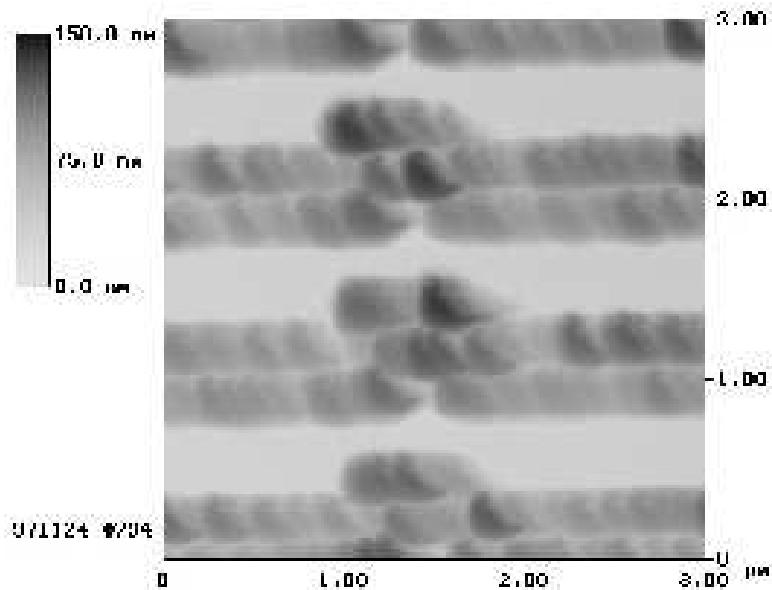
The primary reason for choosing aluminium as the base electrode material was the evaporation source available at this time, an effusion cell. This cell only delivered an evaporation rate of 3 nm per minute, so that the evaporation of the bottom metal layer took more than six minutes.

## 5.2. Sample fabrication and characterisation



**Figure 5.2.:** Single electron transistor with niobium leads and aluminium islands. Left: scanning electron micrograph, right: artistic interpretation.

5. Noise in a single electron transistor



**Figure 5.3.:** Atomic force micrograph (AFM) of an array of SET test structures, demonstrating the coarse grains of the aluminium film (upper strips) compared to the smoother niobium (lower) strips.

This resulted in a rather coarse grained structure of the aluminium film, as demonstrated by the atomic force micrograph of fig. 5.3. It would have been impossible to cover a niobium bottom layer with a sufficiently thin, yet homogeneous, aluminium layer as the fabrication of Nb-AlO<sub>x</sub>-Nb junctions would have required.

The aluminium layer, evaporated from a melt whose nominal purity was 5N, was oxidised after the first evaporation in the load lock of the UHV evaporation system, using non-dehumidified air at a pressure of 8.8 Pa for 20 minutes, and after two hours of pumping, the niobium counterelectrodes were deposited by electron gun evaporation from a melt of nominal purity 2N8.

In retrospect, it must be regarded as unfortunate that we evaporated the niobium right away without any pre-evaporations against the closed shutter. Such practice [9] might have improved the quality of the film by keeping the background pressure lower, due to the chemisorption pumping (*gettering*) by the fresh niobium layer. While the evaporation system had

## 5.2. Sample fabrication and characterisation

a standard background pressure of  $3 \cdot 10^{-7}$  Pa without pre-evaporations, it went as low as  $5 \cdot 10^{-8}$  Pa after the deposition of a fresh niobium layer and about an hour of cooling. During the niobium evaporation, the pressure indicator showed an increase to approximately one hundred times the base pressure. A further complication was that the niobium was not deposited in one continuous operation, but instead opening the shutter for two seconds and then closing it for eight seconds a total of five times, giving a total niobium film thickness of approximately 20 nm (with an accuracy of several nm due to the rate uncertainty and difficulty in exact shutter timing). This pulsed evaporation procedure was intended to minimise the heat load to the substrate and the resist, and thereby to minimise grain size and prevent resist damage. We had seen thermally damaged resist structures earlier in this series of experiments, but later found that we could attribute these problems to incorrect resist fabrication caused by a faulty baking temperature control (see 3.3.2 and C.2.1 for details on correct resist fabrication). The pulsed evaporation procedure was later abandoned.

Figure 5.2 shows the niobium film, deposited under an angle of  $+21^\circ$  to the substrate normal, as the structures giving much better contrast than aluminium in the scanning electron microscope. The excess island created by the shadow evaporation here happens to form part of a linear array of tunnel junctions not related to the investigations described here (as a matter of fact, it was broken). The gate electrode is situated far outside the imaged detail.

Since SEM inspection regularly damages ultrasmall, high ohmic tunnel junctions, fig. 5.2 in fact shows a transistor nominally identical to the sample characterised below. Two chips (with four SET structures each) on a contiguous piece of substrate were processed simultaneously, and the SEM image shows the structure on the second chip corresponding to the sample under consideration on the first chip.

Apart from samples with niobium electrodes and aluminium islands as shown in fig. 5.2, even such with aluminium electrodes and niobium islands were made. We have, however, no useful noise measurement data from these samples.

### 5.2.2. DC characterisation

Unless stated otherwise, the DC characterisation measurements of the sample were carried out in the dilution refrigerator mentioned in 4.3.1, at the base temperature of  $(30 \pm 5)$  mK which it reached at the time of these measurements. Contrary to the general statement in 4.3.3, the shielded room was partially dismounted during these measurements.

## 5. Noise in a single electron transistor

### Normal conducting state

The transistor's serial resistance, i. e. the sum of both junctions' resistances

$$R_T = R_1 + R_2, \quad (5.3)$$

was measured between room temperature and liquid helium temperature one week after the fabrication was completed (i. e. after removal of the sample from the UHV system). From the room temperature value of  $(125 \pm 5) \text{ k}\Omega$ ,  $R_T$  rose upon cooling to 4.2 K to  $(165 \pm 8) \text{ k}\Omega$  at high bias. Around zero bias, the differential resistance increased to about  $215 \text{ k}\Omega$  due to the Coulomb blockade.

The sample appeared to be rather stable against ageing and thermal cycling. A first set of measurements was started when the sample was one month old, the second measurement campaign, from which all data presented here stem, another two months later. During this time, no significant changes of the electrical characteristics were observed.

The  $I$ - $V$  characteristics in the normal conducting state, as shown in fig. 5.4, were taken in an externally applied magnetic field of 5 T. Absence of the Coulomb staircase in these characteristics indicates that the two junctions were quite similar. This is corroborated by the observation that the spread in transistor resistances among the four double junctions on the chip was less than 20%, even though they may have had slightly different dimensions due to the proximity effect and non-identical surroundings (the junction patterns themselves were nominally identical), and because two of them had aluminium islands, while the other two had niobium islands.

The total capacitance of the island, i. e. the sum of the junction capacitances  $C_{1,2}$ , the gate capacitance  $C_g$  and the capacitance to ground  $C_0$ ,

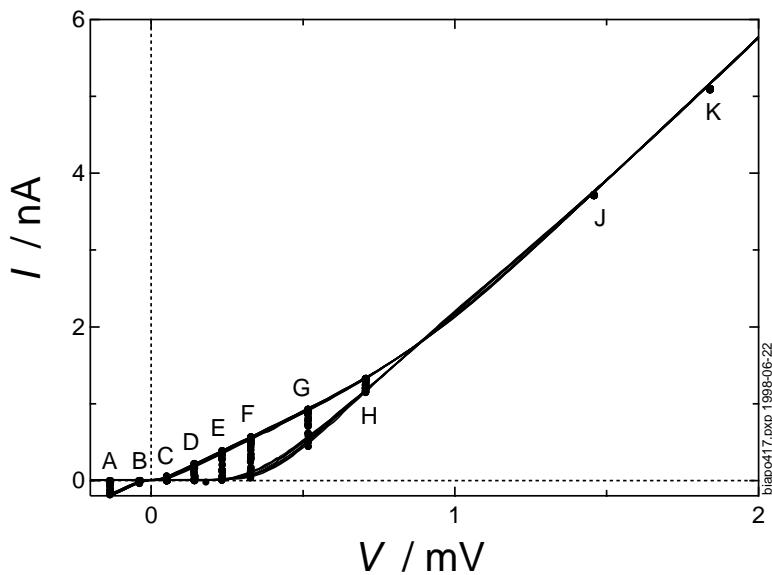
$$C_\Sigma = C_1 + C_2 + C_g + C_0, \quad (5.4)$$

was determined at dilution refrigerator base temperature using the offset voltage analysis method described by Wahlgren et al. [33, 76]. From an extrapolated offset voltage at zero bias of  $V_{\text{off}}^0 = (325 \pm 15) \mu\text{V}$ , we found an island capacitance

$$C_\Sigma = \frac{e}{V_{\text{off}}^0} = (0.49 \pm 0.02) \text{ fF}. \quad (5.5)$$

The gate capacitance was rather low because of the large distance to the gate (since a dedicated gate electrode was damaged, another contact had to substitute it). From a gate voltage period of the current at fixed bias

5.2. Sample fabrication and characterisation



**Figure 5.4.:** Current-voltage characteristics of the single electron transistor at base temperature ( $\approx 30$  mK) in the normal conducting state, for minimum and maximum Coulomb blockade. The letters indicate the voltage bias points for the noise measurements.

## 5. Noise in a single electron transistor

voltage of  $V_p = (0.512 \pm 0.008)$  V, we found a gate capacitance

$$C_g = \frac{e}{V_p} = (0.313 \pm 0.003) \text{ aF}. \quad (5.6)$$

See fig. 2.2, top right, where the original data from this measurement were used to illustrate the principle of SET operation.

### Superconducting state

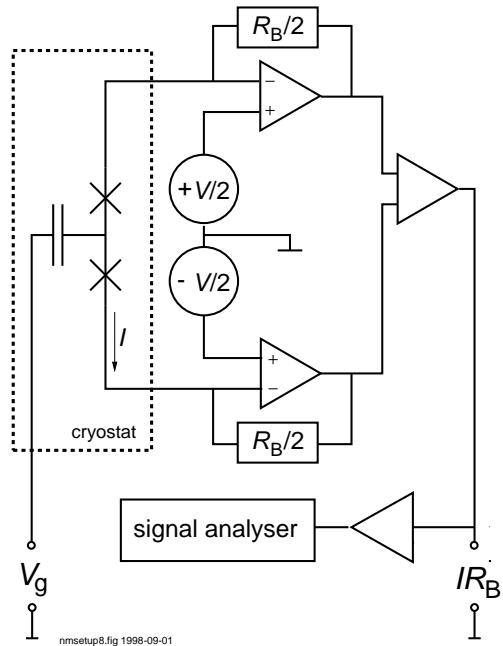
In the superconducting state, at base temperature without any external magnetic field applied, twice the superconducting energy gaps of both the island and the source/drain materials are added to the Coulomb gap. An analysis is best done by looking at the peaks in the differential conductance plotted versus bias voltage. Upon variation of the gate voltage, we found a minimum distance of the peaks of  $2\Delta_{Al} + 2\Delta_{Nb} = (850 \pm 20)$   $\mu\text{eV}$ . Assuming  $\Delta_{Al} = (190 \pm 10)$   $\mu\text{eV}$ , this means  $\Delta_{Nb} = (235 \pm 15)$   $\mu\text{eV}$ . While clearly suboptimal, this nevertheless constitutes an improvement in gap value over an aluminium top layer of 25%, even under the non-optimised deposition conditions as described above.

In this tunnelling experiment, we probed the niobium's superconducting energy gap  $\Delta$  in the electrodes near the junctions. We did not measure the critical temperature of this sample directly since we did not have a suitable setup for measurements between approximately 1 K and 4.2 K, i. e. between the ranges of a dilution refrigerators and an unpumped Helium-4 bath. Though the critical temperature would have been a nice figure of merit, the quantity really relevant for the performance of a superconducting Coulomb blockade device is just the energy gap, and it is known that very disordered niobium films no longer show the BCS dependence of  $T_c$  on  $\Delta$ . For high disorder, the ratio  $2\Delta(T = 0)/(k_B T_c)$  falls below the BCS value of 3.53 [188]. One should thus keep in mind that our mentioning of  $\Delta$  is somewhat more humble and relevant than quoting a critical temperature.

## 5.3. Noise measurement setup

For the measurements of the current and its spectral noise density, we used an amplifier designed and built by Björn Starmark. Detailed [189] and very detailed [12] information about this amplifier is available, and we will restrict ourselves to summarising the amplifier properties here as far as they are relevant to our investigations.

### 5.3. Noise measurement setup



**Figure 5.5.:** Setup for noise measurements on a single electron transistor (schematic, simplified). The sample is voltage biased symmetrically with respect to ground, and the resulting current measured with help of a transimpedance amplifier placed on top of the cryostat, inside a shielded enclosure. A signal analyser performs a real time fast Fourier transform on the current signal and calculates the noise spectral density.

#### 5.3.1. Transimpedance amplifier

The basic principle is that the amplifier translates an input current into a relatively simply measurable output voltage. The amplifier's gain has the dimension of an impedance, hence the name transimpedance amplifier. Figure 5.5 shows a simplified schematic of the noise measurement setup. The sample, situated inside the cryostat, is voltage biased via two operational amplifiers. Using the sketched biasing scheme, namely symmetrical bias with respect to ground, reduced the effect of pickup from external noise sources in the leads near the amplifier [12, 3.5.6]. The output of the differential preamplifier is actually the sum of the bias voltage  $V$  and the amplified current, which in turn is in very good approximation  $R_B I$ .

## 5. Noise in a single electron transistor

All amplifier parts were located at room temperature on top of the cryostat, inside the (not completely) shielded room. The current signal, i. e. the amplifier output from which the bias voltage has been subtracted by virtue of a circuit element omitted from fig. 5.5, was fed to a digital voltmeter outside the measurement cabin and to an HP 35565 dynamic signal analyser. Unlike in all the DC measurements described so far, this signal was not fed through shielded room feedthrough filters, but directly with a coaxial cable.

The HP 35565 performed a real time FFT and calculated the noise spectral density of the current signal. We covered the frequency range from 1 Hz to 300 Hz, averaging 25 spectra ending at 10 Hz and 100 spectra each ending at 100 Hz and 1 kHz (evaluated up to 300 Hz), respectively, trading off accuracy against speed in the lowest frequency region.

We made noise measurements at the bias voltage points labelled A to K in fig. 5.4. At each bias point, a series of 21 different gate voltages was applied, spanning about 1.6 modulation periods or elementary charges induced on the island by the gate (see the top right graph of fig. 2.2 on page 36). At any bias and gate voltage pair, the noise measurements took about five minutes, and though it would have been better to have more data, the total measurement time was limited to about eighteen hours by the lifetime of amplifier batteries.

### 5.3.2. Amplifier noise

Over the relevant frequency range from 1 Hz to 300 Hz, the amplifier noise was due to two contributions, the thermal noise of the feedback resistors  $R_B$  at (room) temperature  $T_B$ , and the input equivalent voltage noise  $e_n$  of the operational amplifiers. With  $r_0 = dV/dI$ , the output impedance of the SET, the amplifier noise reads

$$i_{n,\text{ampl}}(T, f) = \sqrt{2k_B \frac{T_B}{R_B} + \frac{e_n^2(f)}{2r_0^2}}. \quad (5.7)$$

The Analog Devices AD 743 ultralow noise BIFET op-amp had an  $e_n$  of 5.5 nV/ $\sqrt{\text{Hz}}$  (at 10 Hz) [190], and thus we could, thanks to the relatively high impedance of this particular sample, neglect the second contribution. This left us with an amplifier noise entirely due to the thermal noise in the feedback resistors, for which we used  $i_{n,\text{ampl}} = (28 \pm 2) \text{ fA}/\sqrt{\text{Hz}}$  over the whole frequency range in the following.

## 5.4. Measurement results

### 5.4.1. Gain determination

The single electron transistor's small signal gain can be expressed via its transconductance and gate capacitance as

$$\frac{dI}{dQ_g} = \frac{dI}{dV_g} \frac{dV_g}{dQ_g} = \frac{dI}{dV_g} \frac{1}{C_g}. \quad (5.8)$$

We determined the transconductance  $dI/dV_g$  by numerical differentiation of current and gate voltage data taken simultaneously with the noise measurements. The sparsity of the gate voltage points (21 per bias point) introduced the dominating uncertainty in the determination of the gain. Nevertheless, we preferred this random uncertainty over introducing a systematic error by fitting some analytical expression to the data.

In the early first measurement campaign mentioned earlier, we had attempted to measure the gain directly. For this purpose, a small AC component had been superimposed on the gate voltage, and the resulting AC component of the current signal had been read out with a lock-in amplifier. However, in order to attain a useful signal level, we had to increase the gate AC component so much that the spectra were blurred by numerous peaks at harmonics, subharmonics, and beat frequencies of the AC signal and of 50 Hz mains. Crosstalk between the leads in the cryostat appears to be responsible, abetted by the low gate capacitance.

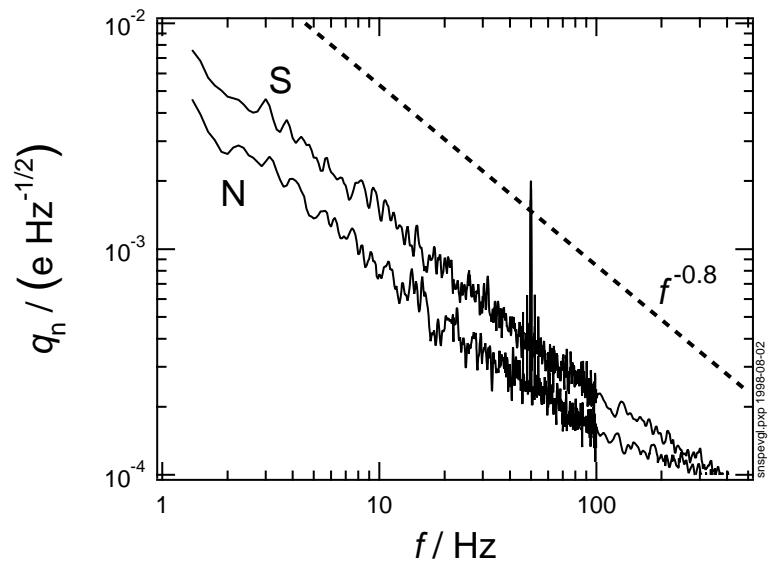
### 5.4.2. Current noise spectral density

In fig. 5.6, the input referred (charge equivalent) noise of the SET is shown as a function of frequency at those two (bias and gate voltage) points that gave the highest gains in the superconducting and normal state, respectively. In both cases, the total current noise at the output  $i_n$ , including the amplifier noise  $i_{n,ampl}$  (see 5.3.2), has been divided by the respective gains:

$$q_n = i_n \left( \frac{dI}{dQ_g} \right)^{-1}. \quad (5.9)$$

Though the maximum gain in the superconducting state was twice as high as in the normal conducting state (3.4 nA/e and 1.7 nA/e, respectively), the input referred noise does not differ significantly between the two states. This is a first rough indication for the dominating influence of input noise on the overall noise, which we shall quantify below.

5. Noise in a single electron transistor



**Figure 5.6.:** Input referred (charge equivalent) noise, at the bias and gate voltage points giving maximum gain, for the normal conducting state ( $N$ , cf. fig. 5.4, point  $F$ ) and superconducting state ( $S$ ), respectively. The dashed line indicates the frequency dependence  $i_n \propto f^{-0.8}$ .

## 5.4. Measurement results

We further see the same frequency dependence  $q_n \propto f^{-0.8}$ , corresponding to a dependence  $S_q \propto f^{-1.6}$  of the spectral power density, in both the superconducting and normal state. This same frequency dependence had been observed in a number of all-aluminium SET on substrates from the same batch [13].

At 300 Hz, we see the crossover from input dominated to output dominated, namely amplifier (white), noise. Since the same amplifier noise is divided by the higher gain in the superconducting case, the input referred noise for the superconducting sample is lower than for a normal conducting one; this is a consequence of the input referral. The engineer's justification is that a higher gain means a better signal-to-noise ratio, and this is exactly what the lower input referred noise indicates.

In the following, we will concentrate on evaluating the noise at the frequency  $f = 10$  Hz. Instead of simply reading the spot value for the noise spectral density from the measured raw data, we improved the accuracy by producing linear fits to the bilogarithmic noise density and frequency data in the ranges 3 Hz to 10 Hz and 10 Hz to 30 Hz, respectively, and taking the average of the two fits at 10 Hz (after a plausibility check) as the measured noise value. The ranges were chosen to stay above the region of data inaccuracy due to the limited measurement time, and below the 50 Hz mains peak.

When speaking of the net current noise  $i_{n,\text{net}}$ , as we will do in the following, we mean the measured current noise  $i_n(f)$  from which the amplifier noise  $i_{n,\text{ampl}}$  (flat) and the shot noise  $i_{n,e} = \sqrt{eI}$  have been subtracted, the latter only being significant for the two highest bias points well above the Coulomb blockade threshold:

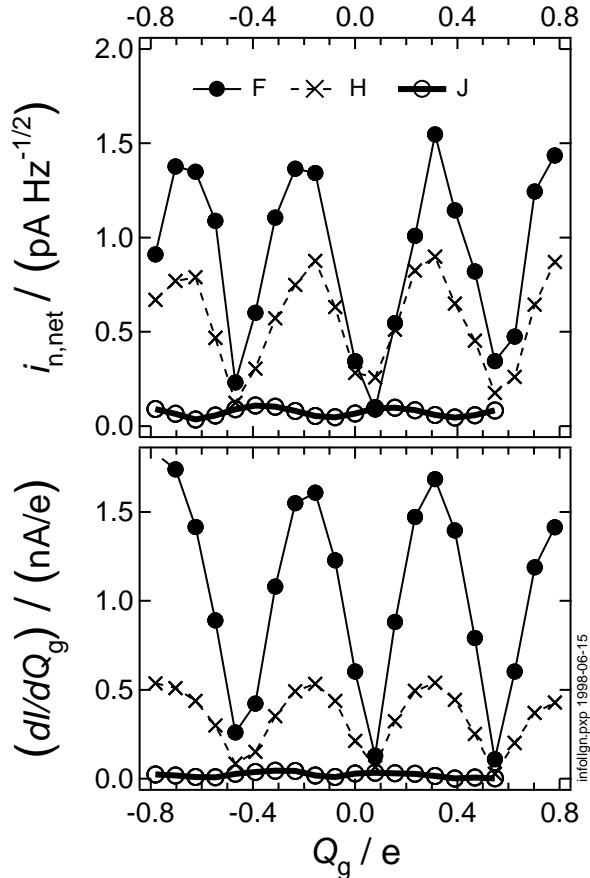
$$i_{n,\text{net}} = \sqrt{i_n^2 - i_{n,\text{ampl}}^2 - eI}. \quad (5.10)$$

### 5.4.3. Gain dependence of the current noise

In fig. 5.7, the net current noise at 10 Hz (top panel) and the SET's gain (bottom) are plotted, respectively, as a function of the gate charge, for three bias points (cf. fig. 5.4; an amplifier battery ran empty near the end of the measurement J). It is immediately obvious (and comes as no surprise [13]) that the noise follows the gain, or in other words, that the noise has dominantly input noise character.

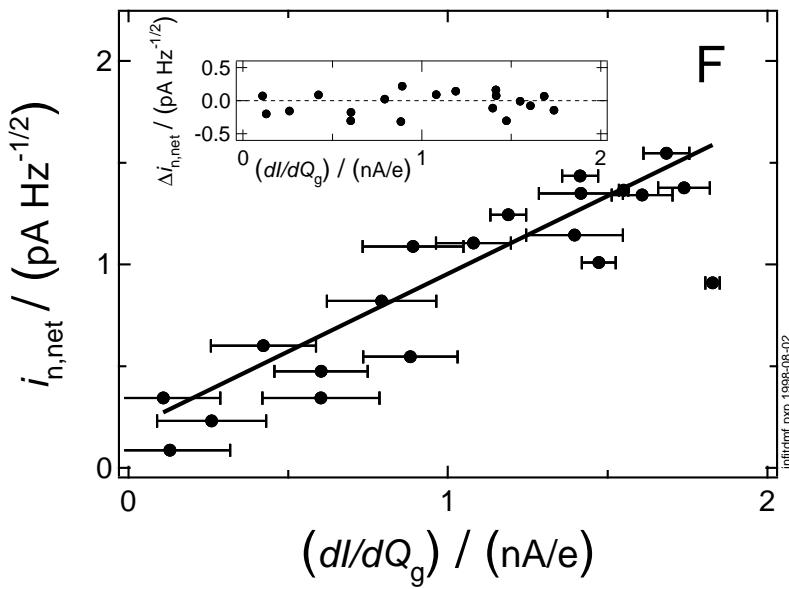
For a more quantitative analysis, we plotted the net current noise as a function of the gain in fig. 5.8. At each bias point, the gain dependence of the net current noise could well be described by a linear relation, as the graph in fig. 5.8 exemplifies for bias point F. The figure's inset shows

5. Noise in a single electron transistor



**Figure 5.7.:** Net current noise at 10 Hz  $i_{n,\text{net}}$  and gain  $dI/dQ_g$  as a function of the charge induced on the gate of the SET. Amplifier noise and shot noise have been subtracted from the measured noise to calculate the net noise. Bias points are labelled as in fig. 5.4. Measurements were taken at 30 mK with the sample driven into the normal conducting state.

#### 5.4. Measurement results



**Figure 5.8.:** Dependence of the net current noise at 10 Hz on the gain. The thick line shows a linear least squares fit to the data points, and the fit residuals are shown in the inset. The error margin on the gain is relatively large due to the small number of gate voltage points per bias point. These data were taken in bias point F (cf. fig. 5.4), at 30 mK and in the normal conducting state.

## 5. Noise in a single electron transistor

that the residuals to a least squares linear fit spread non-systematically. This means that within our measurement accuracy, we cannot identify any other gain dependent noise component apart from charge input noise. Specifically, we do not see evidence for charge-resistance correlation noise, for which the square of the current noise,  $S_{I_{R,\text{corr}}} = i_{n_{R,\text{corr}}}^2$ , should depend linearly on the gain [13].

We will refer to the slope

$$q_n^{\text{fit}} = \langle di_n/d(dI/dQ_g) \rangle \quad (5.11)$$

in the diagrams exemplified by fig. 5.8 as *differential charge equivalent noise*. To our knowledge, this quantity has not been studied systematically before.

An upper limit for the contribution to the noise in second order in the gain, described by the term proportional to  $\alpha$  in eq.(5.1), can be given. The coefficient  $\alpha$  can be evaluated as [13]

$$\alpha(f) = \frac{1}{e^2 S_{Q_g}(f)} \int_{-\infty}^{+\infty} S_{Q_g}(f') S_{Q_g}(f - f') df'. \quad (5.12)$$

We found that  $\alpha \lesssim 10^{-4}$ , practically independent of frequency, and that thus we could neglect the noise effect of second order input charge noise.

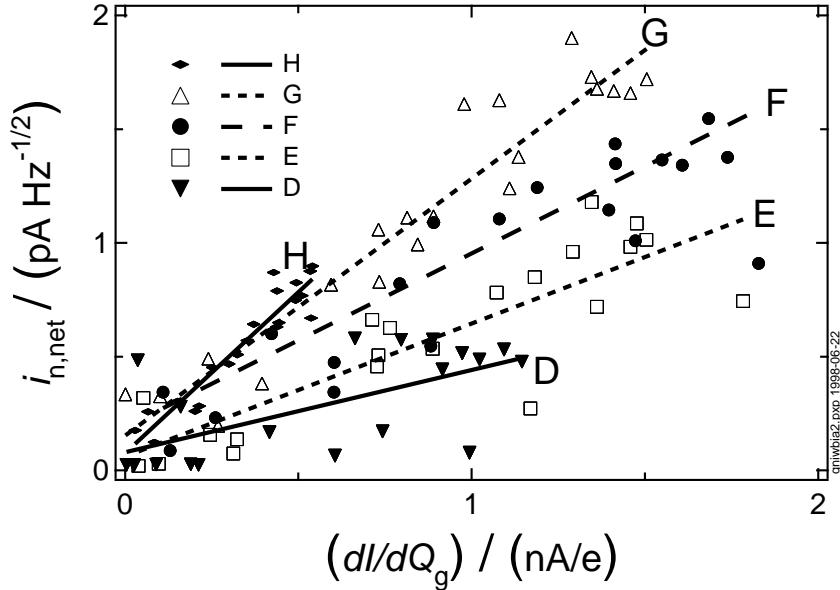
### 5.4.4. Resistance fluctuations

An upper estimate for the resistance fluctuations can be given within the phenomenological low frequency noise model [13]. Details on the calculations can be found in [12, section 2.3.3]. A number of rather strong assumptions have to be made:

1. The estimation is only applicable for bias voltages well above the blockade (threshold) voltage, where the dynamic junction resistance is approximately constant.
2. The junctions are identical in their DC as well as in their noise properties.
3. The background charge noise  $S_{Q_g}$  is not dependent on anything other than possibly the bias voltage.

In the frequency band between 50 Hz and 100 Hz, the total SET resistance  $R_1 + R_2 = (165 \pm 8) \text{ k}\Omega$  did, under the above assumptions, not fluctuate by more than  $31 \Omega$ .

## 5.5. Deviations from ideal charge noise behaviour



**Figure 5.9.:** Gain dependence of the net current noise (amplifier noise and shot noise have been subtracted) at 10Hz (base temperature, normal conducting state). With increasing bias ( $D \dots H$ , cf. fig. 5.4), the slope of the noise-gain relation increases, from  $0.36 \cdot 10^{-3} e/\sqrt{\text{Hz}}$  at bias point  $D$  to  $1.42 \cdot 10^{-3} e/\sqrt{\text{Hz}}$  at point  $H$ . These slopes have been calculated by a least squares fit to the data as illustrated in fig. 5.8, error bars have been omitted to reduce clutter.

## 5.5. Deviations from ideal charge noise behaviour

### 5.5.1. Bias dependence

In the model presented in 5.1, a constant charge input noise independent of any transistor back action would produce a constant differential charge equivalent noise, independent of the bias voltage for example. This is, however, not the case we find experimentally.

For the five bias points around that with maximum gain, the plots used for the determination of the differential charge equivalent noise (as demonstrated in fig. 5.8) have been superimposed in fig. 5.9. It is immediately

## 5. Noise in a single electron transistor

evident that the differential charge equivalent noise increases systematically with the bias voltage, roughly by a factor of four when the bias voltages increases fivefold.

This bias dependence of the noise at low temperatures has immediate consequences for the optimal operating point of an SET electrometer. While maximising the gain maximises the signal, an optimisation of the signal-to-noise ratio may be achieved by sacrificing some gain against reduced noise by biasing on the lower flank of the gain-vs.-bias curve.

### 5.5.2. Temperature dependence

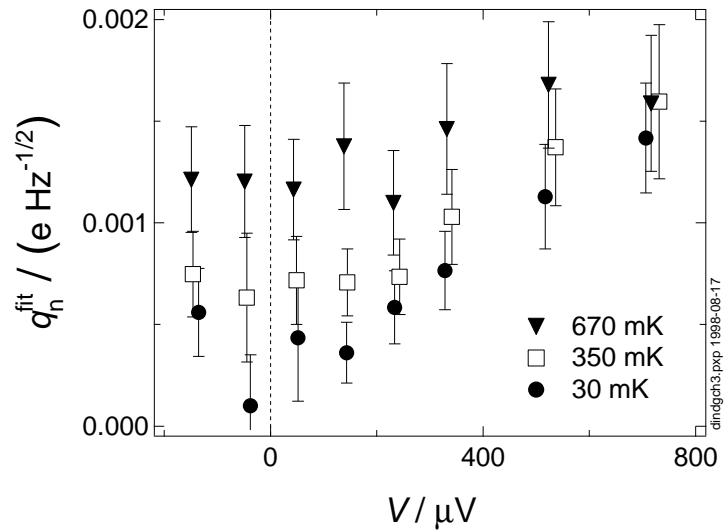
The simplest back action mechanism by which the bias voltage could influence the noise sources is heating of the electrons or phonons in the barriers, the island and leads, and the surfaces in their vicinity, by the dissipation near the junctions. Wolf et al. [191] observed a weak dependence of the low frequency noise on the transport current, with a proportionality to the fourth root of the current, and suggested self-heating as an explanation. For a single two level fluctuator, Kenyon et al. [192] observed a bias dependence of the noise. Under the general assumption, that  $1/f$ -like low frequency noise results from the superposition of many such TLF, these experiments corroborate the self-heating hypothesis.

To test this hypothesis, we repeated the set of measurements described so far at elevated temperatures of 350 mK and 670 mK. The evaluation results for the differential charge equivalent noise as a function of bias are plotted in fig. 5.10.

Within the error margin, which we estimated from the average amplitude of the current noise-vs.-gain fits, the noise at low bias rose significantly with temperature, while at higher bias of about twice the threshold voltage, noise were independent of the ambient temperature. At even higher bias, gains were so low at all temperatures that zero gain noise (see 5.5.4) masked the differential charge equivalent noise. Nevertheless, the trend in fig. 5.10 is clear: at temperatures of approximately a little less than two thirds of a Kelvin, the bias dependence of the differential charge equivalent noise vanished.

The implications for high sensitivity electrometry are obvious. If one is forced to operate an SET electrometer at temperatures approaching that corresponding to the charging energy, the signal-to-noise ratio can be optimised by simply maximising the signal, which in turn means biasing the SET at the point giving the global maximum in gain.

## 5.5. Deviations from ideal charge noise behaviour



**Figure 5.10.:** Differential charge equivalent noise (proportionality constant relating gain increase to increase in net current noise), as a function of bias voltage and at different temperatures. Data values were determined as the slopes of the linear fit curves in the noise current versus gain diagrams (cf. fig. 5.8). The error margins were estimated from the average amplitude of the fit residuals. While the increase of the differential charge equivalent noise with bias is evident at 30 mK, it is masked by temperatures of about half a Kelvin.

## 5. Noise in a single electron transistor

### 5.5.3. Model calculation of the self-heating

If it is self-heating of the transistor that activates the noise sources, we should expect an equilibrium temperature of about half a Kelvin, since this is the temperature at which the bias dependence of the noise saturated (see 5.5.2).

At very low temperatures, the thermal coupling between different subsystems in the solid state becomes weak. Energy is transported into the electronic system of the SET island via the junctions. Due to their relatively high resistance, we can neglect their thermal conductivity and thus their cooling effect [193]. Heat transfer from the electrons in the island goes only to the phonon system of the island. In equilibrium, the temperatures of the electron system  $T_{\text{el}}$  and of the island phonon system  $T_{\text{ph}}$  are related by [193]

$$T_{\text{el}} = \sqrt[5]{T_{\text{ph}}^5 + \frac{P}{\Sigma\Omega}}, \quad (5.13)$$

where  $\Omega$  is the island's volume,  $P$  the power dissipated in the island of the SET, and  $\Sigma \approx 1 \cdot 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  [194] a coefficient describing the electron-phonon coupling. Values for  $\Sigma$  in the literature vary by about one order of magnitude between  $0.3 \cdot 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  [195] and  $2.4 \cdot 10^9 \text{ W m}^{-3} \text{ K}^{-5}$  [196].

Determining the island's phonon temperature is not as straightforward. In thick films one could use the model of the island's phonon system coupled to the substrate's phonon system via the area  $A$  with the *Kapitza resistance*  $\alpha$ . For thick film samples at very low temperatures, this can lead to significant temperature differences between the different phonon systems. In thin films, however, this model does not apply at very low temperatures [196], and the phonon population of the film and the substrate can no longer be clearly separated.

If we calculate the temperature of the phonon system under the assumption that the usual relation [193]

$$T_{\text{ph}} = \sqrt[4]{\frac{P}{A\alpha} + T_{\text{substrate}}^4} \quad (5.14)$$

holds, where  $\alpha = 100 \text{ W m}^{-2} \text{ K}^{-4}$  [193], we find a  $T_{\text{ph}}$  of the order of 500 mK. For a film thickness of 40 nm, this is just about the temperature below which eq. (5.14) loses relevance [196].

The electron temperature is not affected much by the phonon temperature, and at the upper edge of our bias range ( $800 \mu\text{V}$ ), we find values for  $T_{\text{el}}$  between 800 mK (neglecting any heating of the phonon system) and 1100 mK (assuming that eq. (5.14) is fully applicable).

## 5.6. Conclusion: noise in a single electron transistor

Stretching the model represented by eq. (5.14) to its limits, we can motivate a heating of the phonons of the island to about half a Kelvin. Thus, all of the noise increase with bias could be attributed to ohmic self-heating.

Another bias dependence could have been caused by the noise sources being activated by fluctuations of the island potential, that should increase with the potential differences to the electrodes. If this mechanism had been more dominant, we would have found more bias dependence of the noise than had been possible to explain with self heating, but since we obtain temperatures of about 0.5 K from the model calculations with conservative parameter estimates, such a contribution by island potential fluctuations cannot be detected within the accuracy of these measurements.

### 5.5.4. Zero gain noise

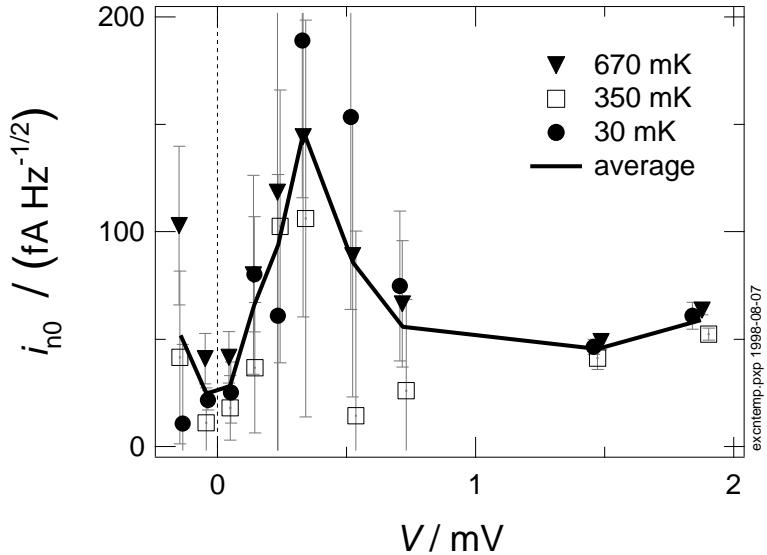
Another deviation from the ideal input charge noise behaviour is the gain independent component that we call *zero gain noise*. It readily presents itself as the offset along the noise axis in the fit procedure used to determine the differential charge equivalent noise. Zero gain noise also spooks around the literature as *excess noise* [13], which is unfortunate inasmuch this term is a historical synonym [197] for low frequency noise (see 2.4.2).

Figure 5.11 shows that the zero gain noise clearly was a function of bias, with a dependence roughly resembling that of the maximum gain on the bias, i. e. peaking slightly above the threshold voltage. While the maximum gain, however, dropped by about one half upon raising the temperature from 30 mK to 670 mK, the zero gain noise was temperature independent within our measurement accuracy. We do not have a model explaining the observed zero gain noise at the present time, and it is apparent that more numerous and especially more precise data are needed here.

## 5.6. Conclusion: noise in a single electron transistor

We studied the low frequency current noise of a voltage biased single electron transistor in the normal conducting state and found it dominated by input charge noise. Introducing a technique that analyses the differential charge equivalent noise, that is the coefficient relating an increase in bias to the resulting increase in noise, we found a second order effect, namely a bias and temperature dependence of the noise. Both dependences can be reduced to a temperature dependence when the self-heating of the electron

5. Noise in a single electron transistor



**Figure 5.11.:** Zero gain noise at 10 Hz (normal conducting state) as a function of bias voltage, for the same temperatures as in fig. 5.10. The values were calculated from the vertical axis intersection in the fit procedure illustrated in fig. 5.8, the errors have been estimated from the ratio between the average amplitude of the fit residuals and the gain range. Within this accuracy, no temperature dependence is visible. The zero gain noise has a maximum close to the threshold voltage of the SET.

### *5.6. Conclusion: noise in a single electron transistor*

gas in the transistor is taken into account. Within our measurement accuracy, a bias dependence of the noise due to island potential fluctuations cannot be detected. The details of the mechanism and the exact location of the noise sources, however, remain unknown.

5. *Noise in a single electron transistor*

# 6. Conclusion

## 6.1. What's new? What's useful? What's not?

In this thesis, we have investigated new fabrication methods for resistors and charging effect devices, and a new evaluation technique for low frequency noise measurements of single electron transistors.

Anodisation-made resistors allow us to pack large resistances on fairly short lengths. The limitation is not set by fabrication issues, but is rather inherent due to the onset of the Coulomb blockade at high sheet resistances. It can be imagined that useful applications for such resistors should exist.

Exploiting the Coulomb blockade for devices is not equally straightforward. The process suffers from asymmetry in the residual metal thicknesses, which is a problem common to all anodisation miniaturisation schemes. The fine grained structure gives us a multiple tunnel junction system with a gate effect vanishing at only a few Kelvin. Given that practically the only application area envisioned today for (random)multiple tunnel junctions is memory, these anodised niobium systems are facing a tough competition.

Noise, namely low frequency noise, has not been considered enough in the modelling of single electronics devices, especially regarding high temperature operation. Our measurements indicate that low frequency noise may become worse with higher temperatures. These measurements have of course only scratched the surface of all that is to be discovered about low frequency noise. Now that the equipment and an evaluation technique are at hand, extensive measurements should be done soon to establish causal dependencies between fabrication and sample parameters on one hand and noise data on the other hand. It should then be possible to obtain reasonable estimates on how detrimental low frequency noise will be on the road towards room temperature single electronics.

## 6. Conclusion

### 6.2. Suggestions for future research

(...) [W]e can do that, too,  
some time.

Monica S. Lewinsky [198]

Although experiments reported by other groups indicate that there is no dramatic improvement of the low frequency noise properties of C-SET to be expected from the use of other substrate materials, some more systematic research on the materials influence might be worthwhile.

Korotkov's model for the low frequency noise in SET [13] came after the measurements presented here were made. With this model in hand, we would have concentrated on more (and that means better) measurements at low gain. This should allow for improved conclusions about many aspects of the LFN, be it resistance fluctuations, charge-resistance-correlation noise, and the nature of the zero gain noise.

With very small high-ohmic resistors and junctions with oxide barriers, we have the two key components of a resistively coupled single electron transistor. It should be possible to combine both components on a single chip, in just one angular evaporation step. Prototypes exist, but all dozen or so of them had at least one of the junctions destroyed or a pinchoff in the resistor strip. The idea of integrating the Nb based junctions into an R-SET was the main reason to limit the film thicknesses to 20 nm that are so unfavourable for the superconducting properties. By adding some halide contaminants to the anodisation electrolyte, it should be possible to anodise only the niobium line to the SET island into a resistor, while simultaneously destroying the parallel line of aluminium inevitably generated in the shadow evaporation deposition.

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## A. Symbols and notation

	meaning (numerical value) [199]	SI unit
$\alpha$	expansion coefficient	1
$\alpha$	Kapitza resistance	$\text{kg s}^{-3} \text{K}^{-4}$
$\Delta$	superconducting energy gap	$\text{m}^2 \text{kg s}^{-2}$
$\Delta V$	voltage swing (modulation)	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$\gamma$	phase difference over Josephson junction	1
$\eta$	gain	depends on ampl. type
$\varepsilon$	relative dielectric permittivity	1
$\varepsilon_0$	dielectric permittivity of vacuum $(8.854 \dots 10^{-12})$	$\text{m}^{-3} \text{kg}^{-1} \text{s}^4 \text{A}^2$
$\lambda$	London penetration depth	m
$\mu_0$	permeability of vacuum $(1.256 \dots 10^{-6})$	$\text{m kg s}^{-2} \text{A}^{-2}$
$\xi$	coherence length	m
$\varrho$	density	$\text{m}^{-3} \text{kg}$
$\Sigma$	electron-phonon interaction constant	$\text{m}^{-1} \text{kg s}^{-3} \text{K}^{-5}$
$\tau$	lifetime	s
$\phi$	phase of multiparticle wavefunction	1
$\Omega$	volume	$\text{m}^3$
$A$	area	$\text{m}^2$
$B$	magnetic flux density	$\text{kg s}^{-2} \text{A}^{-1}$
$C$	capacitance	$\text{m}^{-2} \text{kg}^{-1} \text{s}^4 \text{A}^2$
$C_0$	stray capacitance	$\text{m}^{-2} \text{kg}^{-1} \text{s}^4 \text{A}^2$
$C_g$	gate capacitance	$\text{m}^{-2} \text{kg}^{-1} \text{s}^4 \text{A}^2$
$C_\Sigma$	total island capacitance	$\text{m}^{-2} \text{kg}^{-1} \text{s}^4 \text{A}^2$
$d$	thickness	m
$d_b$	barrier width	m

### A. Symbols and notation

$e$	elementary charge ( $1.602 \dots \cdot 10^{-19}$ )	s A
$e_n$	op amp input equivalent noise	$m^2 \text{ kg s}^{-3.5} \text{ A}^{-1}$
$E$	energy	$m^2 \text{ kg s}^{-2}$
$E_a$	activation energy	$m^2 \text{ kg s}^{-2}$
$E_c$	characteristic charging energy $e^2/(2C)$	$m^2 \text{ kg s}^{-2}$
$E_{ch}$	charging energy	$m^2 \text{ kg s}^{-2}$
$E_F$	Fermi energy	$m^2 \text{ kg s}^{-2}$
$E_J$	Josephson (coupling) energy	$m^2 \text{ kg s}^{-2}$
$f$	frequency	$\text{s}^{-1}$
$G$	conductivity	$\text{m}^{-2} \text{ kg}^{-1} \text{ s}^3 \text{ A}^2$
$H$	magnetic field	$\text{m}^{-1} \text{ A}$
$h$	Planck's constant ( $6.626 \dots \cdot 10^{-34}$ )	$\text{m}^2 \text{ kg s}^{-1}$
$\hbar$	Planck's constant divided by $2\pi$ ( $1.054 \dots \cdot 10^{-34}$ )	$\text{m}^2 \text{ kg s}^{-1}$
$i_n$	current noise	$\text{s}^{-1/2} \text{ A}$
$I$	current	A
$I_c$	critical current	A
$I_{c0}$	maximum critical current	A
$I_s$	supercurrent	A
$k_B$	Boltzmann constant ( $1.380 \dots \cdot 10^{-23}$ )	$\text{m}^2 \text{ kg s}^{-2} \text{ K}^{-1}$
$l$	length	m
$P$	power	$\text{m}^2 \text{ kg s}^{-3}$
$q_n$	charge noise	$\text{s}^{1/2} \text{ A}$
$Q$	charge	s A
$Q_0$	offset charge	s A
$Q_g$	gate charge	s A
$r_0$	output impedance	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$
$R$	resistance	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$
$R^*$	resistance constant	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$
$R_0$	zero bias (dynamic) resistance	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$
$R_I$	current autocorrelation function	$\text{A}^2$
$R_K$	quantum resistance	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$
$R_{K-90}$	Klitzing resistance (25812.807)	$\text{m}^2 \text{ kg s}^{-3} \text{ A}^{-2}$

$R_Q$	'quantum resistance for pairs' $R_K/4$	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
$R_T$	tunnelling resistance	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-2}$
$S_I$	current spectral noise density	$\text{s A}^2$
$S_{I,e}$	current shot noise spectral density	$\text{s A}^2$
$S_{I,\text{th}}$	current thermal noise spectral density	$\text{s A}^2$
$S_{Q_g}$	background charge noise spectral density	$\text{s}^3 \text{A}^2$
$S_R$	resistance noise spectral density	$\text{m}^4 \text{kg}^2 \text{s}^{-5} \text{A}^{-4}$
$t$	time	s
$T$	temperature	K
$T^*$	temperature of vanishing gate effect	K
$T_c$	critical temperature	K
$T_{\text{el}}$	electron temperature	K
$T_{\text{ph}}$	phonon temperature	K
$V$	voltage, bias voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_{\text{an}}$	anodisation (cell) voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_b$	(tunnel) barrier height	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_g$	gate voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_{\text{off}}$	offset voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_{\text{off}}^0$	(extrapolated) zero bias offset voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$V_{\text{th}}$	threshold voltage	$\text{m}^2 \text{kg s}^{-3} \text{A}^{-1}$
$x$	spatial coordinate	m

*A. Symbols and notation*

## B. Glossary and abbreviations

**Ångström (Å):** Outdated unit of length.  $1 \text{ \AA} = 10^{-10} \text{ m}$ .

**ACME:** Anodization controlled miniaturization enhancement [164]

**ADC:** Analog-to-digital converter

**ADP:** Automated data processing

**AF:** Anodic film (more general than AOF, may incorporate inclusions from the electrolyte)

**AFM:** Atomic force microscope/microscopy/micrograph

**AIS:** Automated information system

**Ammonium pentaborate:**  $(\text{NH}_4)\text{B}_5\text{O}_8 \cdot x\text{H}_2\text{O}$  [200], where  $x$  gives the amount of crystal water. If undefined, we assume  $x \approx 4$  (APB tetrahydrate).

**AOF:** Anodic oxide film

**APB:** Ammonium pentaborate

**ASCII:** American Standard Code for Information Interchange

**Aspect ratio:** Ratio between height and width of a structure. Fabrication of structures with high aspect ratios requires very anisotropic etching or deposition techniques.

**BCS:** Bardeen-Cooper-Schrieffer (theory of superconductivity) [17, and references therein]

**BIFET:** Bipolar output FET input operational amplifier

**CAD:** Computer Aided Design

**CAM:** Computer Aided Manufacturing

*B. Glossary and abbreviations*

**Cb:** Chemical symbol for Columbium

**CB:** Coulomb blockade

**CBCPT:** Coulomb blockade of Cooper pair tunnelling

**CHET:** Charging effect transistor [52]

**Chip marks:** Alignment marks (JEOL EBL system) used for highest precision alignment. Three chip marks have to be situated within one field. In the work described here, wafer marks were used instead.

**Columbium (Cb):** old name for Niobium (Nb), used in the Angloamerican language space until about 1950 and in the American metallurgical community even later.

**Contrast:** Degree to which the physicochemical properties exploited in resist development differ in exposed areas compared to unexposed areas

**Corner frequency:** Frequency above which low frequency noise becomes negligible compared to white noise

**CP:** Copolymer P(MMA-MAA)

**DAQ:** Data acquisition

**DMM:** Digital multimeter

**DMS:** Dilute magnetic semiconductor

**DOS:** Density of states

**DSA:** Dynamic signal analyser

**DUT:** Device under test

**DVM:** Digital voltmeter

**DXF:** Drawing Exchange Format

**EBL:** Electron beam lithography

**EOS:** Electron optical system

**Field:** Area that can be written by the EBL without the need of moving the stage,  $80 \times 80 \mu\text{m}^2$  in highest resolution mode. At the edges of the fields, stitching error occurs, so fine structures should not cross field boundaries.

**FFT:** Fast Fourier transform

**Forming:** The process of growing an anodic [oxide] film

**Gauss (G):** Hopelessly outdated unit of magnetic flux density in one of the various CGS systems. Corresponds to (but is not equal to) 0.1 mT.

**GDS-II:** Stream format, a.k.a. Calma Stream. The industry standard for lithographic pattern data.

**GLP:** Good Laboratory Practice, a set of rules that define the proper conduct and documentation of scientific experiments [201].

**GPIB:** General purpose interface bus (IEEE-488)

**HEMT:** High electron mobility transistor

**IBE:** Ion beam etching (milling)

**Inch:** Outdated unit of length. 1 in=25.4 mm

**Igor:** A data evaluation and graphing programme for scientists and engineers from WaveMetrics

**IUPAC:** International Union of Pure and Applied Chemistry

**IVC:** Current-voltage characteristic

**JEOL:** Japanese manufacturer of electron optical research instrumentation

**JJ:** Josephson junction

**JJA:** Josephson junction array

**Jobdeck file (JDF):** Text file in the JEOL EXPRESS system that describes which patterns (chips) are to be exposed and where they are to be positioned relative to each other, and that contains the definition of the shot modulation and the alignment (mark detection) parameters. It also points to a calibration sequence of the electron optical system that will be carried out at the beginning of the exposure and eventually during the exposure.

## B. Glossary and abbreviations

**LabVIEW:** A graphical programming language for data acquisition and experiment control from National Instruments

**LFN:** Low frequency noise

**LIA:** Lock-in amplifier

**Linux:** The best operating system for small computers

**MEK:** Methyl ethyl ketone

**Microfabrication:** Fabrication of devices with typical linear dimensions below  $1\text{ }\mu\text{m}$

**M-IT:** Metal-insulator transition

**ML:** Monolayer

**MSU:** Moscow State University

**NaN:** Not a number

**Nanofabrication:** The art and science of producing non-random structures with typical linear dimensions less than  $100\text{ nm}$

**Negative resist:** Resist that is removed during development where it has *not* been exposed. Example is SAL 601 (e-beam resist).

**PMGI:** Poly(dimethyl glutarimide), a positive e-beam and deep UV resist

**PMMA:** Polymethylmethacrylate, a positive e-beam resist [202]

**P(MMA-MAA):** Copolymer poly(methylmethacrylate-methacrylic acid), a positive e-beam resist, more sensitive than PMMA

**Positive resist:** Resist that is removed during development where it has been exposed. Examples are PMMA (e-beam resist) or S-1813 (photoresist).

**PROXECCO:** A commercial computer programme for proximity correction [110].

**Proximity correction:** Increasing the exposure dose for narrow and/or isolated features to compensate for the proximity effect.

**Proximity effect:** Additional exposure of pixels with many neighbouring exposed pixels due to scattering of the electron beam in the resist and substrate and to secondary electrons.

**PTB:** Physikalisch-Technische Bundesanstalt

**QPT:** Quantum phase transition

**RAM:** Random access memory

**RIE:** Reactive ion etching

**Rotation:** Angular misorientation of the sample relative to the sample holder and consequently the whole electron beam lithography machine. Rotation has to be compensated by the EOS, increasing inaccuracies (stitching error) and pattern distortions. A limit on allowed rotation is set in the internal configuration files of the JEOL system.

**RRR:** Residual resistance ratio, between the resistances at room temperature and just above the resistive transition or at 4.2 K; a measure for the quality often used for Nb.

**S-1813:** A positive photoresist

**SAIL:** Self-aligned in-line technique, developed in Jena [143]

**SAL 101:** A developer for PMGI

**SAL 601:** A negative e-beam resist

**Schedule file (SDF):** Text file in the JEOL EXPRESS system that describes where the arrangement of patterns defined in the jobdeck file is to be placed relative to the machine and what the reference dose for the shot modulation is. It also contains information on hardware settings and definitions for the alignment mark detection.

**SECO:** Step-edge cut-off technique [133]

**Selectivity:** Ratio of the solubilities of different resists exposed simultaneously, important for the resolution in processes involving two layer resist systems

**SEM:** Scanning electron microscope

**Sensitivity:** Reciprocal of the irradiation dose required to produce the physicochemical modifications in a resist needed for development

**SET:** (“ess-eeh-tee”) Single electron tunnelling, alt. single electron (tunnelling) transistor

## B. Glossary and abbreviations

**Shadow evaporation technique:** also known as Dolan technique, Niemeyer-Dolan technique, nonvertical evaporation technique etc. A method of forming very small overlap junctions in the shadowed area underneath a suspended bridge on the substrate. Self-aligning, involves only one lithography step. Introduced by Niemeyer [108], in its present form with resist mask by Dolan [109].

**Shot modulation:** JEOL-specific implementation of handling the assignment of doses to pattern parts (to compensate the proximity effect). Each primitive is assigned a shot rank (an integer number) that corresponds to a certain dose enhancement factor (a floating point number). This assignment is called the shot modulation.

**S-IT:** Superconductor-insulator transition

**SNAP:** Selective niobium anodization process [102]

**SnL:** Swedish Nanometre Laboratory, Göteborg.

**SPM:** Scanning probe microscopy. AFM and STM are both SPM techniques.

**SQUID:** Superconducting quantum interference device

**Stitching error:** Misalignment of parts of the electron beam exposed pattern at the boundaries of fields and subfields. Stitching error increases with sample rotation.

**STM:** Scanning tunnelling microscopy

**Subfield:** Area that can be written by the EBL without switching digital-to-analog converters,  $10 \times 10 \mu\text{m}^2$  in highest resolution mode. At subfield boundaries, slight stitching error occurs, so the finest nanostructures should not cross them.

**Tear-off technique:** A special form of angular evaporation technique where some material is deposited on resist sidewalls and removed during liftoff. Requires good control over the undercut and the evaporation angles.

**TEM:** Transmission electron microscopy

**TLF:** Two level fluctuator

**UHV:** Ultra high vacuum, below  $10^{-6}$  Pa

**Vector scan:** EBL mode where the beam is swept only over the areas that are to be exposed, as opposed to raster scan, where it is swept over the whole sample and simply blanked from non-exposure areas. Requires faster electron optics and makes systems more expensive, but can save a lot of exposure time.

**VI:** Virtual Instrument, a LabVIEW programme

**VTB:** Variable thickness bridge

**Wafer marks:** Alignment marks (JEOL EBL system) that can be placed almost anywhere on the sample. Of course, precision of alignment improves when the marks are as close to the writing area as possible.

**WCE:** Wet chemical etching

**White noise:** Noise with a frequency independent spectral density, usually occurring at some intermediate frequency range

**ZEP 520:** A positive e-beam resist

**ZEP 7000B-97:** A positive e-beam resist with high sensitivity

*B. Glossary and abbreviations*

# C. Recipes

All recipes assume that reactive ion etching (RIE) is done in a Plasmatherm Batchtop 70 with a seven inch electrode (area  $248\text{ cm}^2$ ), an electrode distance of 60 mm and a working frequency of 13.56 MHz.

The contact printer operates in the wavelength range (320...420) nm<sup>2</sup>.

Electron beam lithography was done with a JEOL JBX 5D-II system with CeB<sub>6</sub> cathode.

## C.1. Substrate preparation

### C.1.1. Photomask making (positive resist process)

1. Clean a Cr mask with RIE. Process gas oxygen, pressure 67 Pa, flow  $36\text{ }\mu\text{mol/s}$ , rf power 250 W, time 120 s.
2. Spin ZEP 7000B-97, solvent chlorobenzene, at 2000 rpm, to a thickness of approximately 500 nm.
3. Bake in an oven for 20 min at 180°C.
4. Expose using 4th lens, 3rd aperture, 10 nA beam current, with a dose of  $10\text{ }\mu\text{C/cm}^2$ .
5. Develop for (6...8) min in a 1:1 mixture (by volume) of MEK and Ethylmalonate.
6. Rinse in Ethylmalonate.
7. Blow dry with nitrogen (not quite easy).
8. Ash the surface with RIE. Process gas oxygen, pressure 13 Pa, flow  $36\text{ }\mu\text{mol/s}$ , rf power 50 W, time 30 s.
9. Wet etch in Balzers Chrome Etch #4 as long as necessary, about 2 min when the solution is fresh.

### C. Recipes

10. Rinse with deionised water.
11. Strip the resist with RIE. Process gas oxygen, pressure 67 Pa, flow  $36 \mu\text{mol/s}$ , rf power 250 W, time 120 s.

#### **C.1.2. Photomask making (negative resist process)**

1. Rinse a Cr mask with deionised tap water.
2. Ash the surface with RIE. Process gas oxygen, pressure 33 Pa, flow  $36 \mu\text{mol/s}$ , rf power 50 W, time 30 s.
3. Spin Microposit Primer.
4. Spin Shipley SAL-601 at 4000 rpm, giving a thickness of about 800 nm.
5. Preexposure bake for 20 min at  $90^\circ\text{C}$  in an oven.
6. E-beam expose in the JEOL JBX 5D-II. Design dose  $10 \mu\text{C/cm}^2$ , acceleration voltage 50 kV, fourth lens (working distance 39 mm), third aperture (diameter  $300 \mu\text{m}$ ), current 5 nA.
7. Postexposure bake for 20 min at  $110^\circ\text{C}$  in an oven.
8. Develop in Microposit MF322 for about 6 min, inspect in the microscope.
9. Ash the surface in the RIE (see above) and immediately thereafter
10. Etch in Balzers No. 4 chromium etch (composition: 200 g cerium ammonium nitrate, 35 mL 98% acetic acid, filled with deionised water to 1000 mL).
11. Remove the resist by stripping with RIE. Process gas oxygen, pressure 66 Pa, flow  $7 \mu\text{mol/s}$ , rf power 250 W, time 120 s.

#### **C.1.3. Gold pad photolithography (carrier chips)**

1. Strip the surface of an oxidised two inch Si wafer with RIE. Process gas oxygen, pressure 66 Pa, flow  $7 \mu\text{mol/s}$ , rf power 250 W, time 120 s.
2. Spin Shipley S-1813 at 5500 rpm, giving a thickness of about 1000 nm.
3. Bake for 7:30 min at  $110^\circ\text{C}$  on a hotplate.

## C.2. Niobium nanofabrication

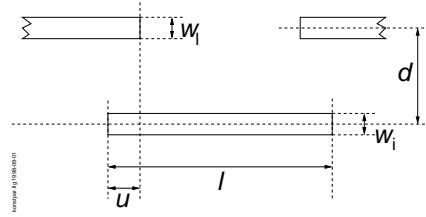
4. Expose for 12 s at an intensity of  $10 \text{ mW/cm}^2$ , correspondingly longer or shorter for different intensities.
5. Develop in a 1:1 mixture (by volume) of Microposit Developer and deionised water for 60 s, rinse thoroughly with deionised water from the tap. **Or:**
6. Develop in pure MF 322 developer for 15 s and rinse.
7. Ash the surface with RIE. Process gas oxygen, pressure 33 Pa, flow  $36 \mu\text{mol/s}$ , rf power 50 W, time 30 s. Immediately thereafter
8. evaporate 20 nm of  $\text{Ni}_{0.6}\text{Cr}_{0.4}$  at  $0.1 \text{ nm/s}$  and
9. 80 nm Au at  $0.2 \text{ nm/s}$ .
10. Liftoff in slightly warmed acetone.
11. Presaw from the back to a depth of about  $50 \mu\text{m}$ . When cutting alignment edges from the front side, try to preserve a  $\text{C}_4$  symmetric circumference shape of the wafer; this facilitates later resist preparation.

## C.2. Niobium nanofabrication

### C.2.1. Four layer resist preparation

1. Ash the surface of a wafer with gold chip patterns with RIE. Process gas oxygen, pressure 33 Pa, flow  $36 \mu\text{mol/s}$ , rf power 50 W, time 30 s.
2. Spin 350k PMMA (1.8 %, in xylene) at 2500 rpm to a thickness of about 50 nm.
3. Bake for 12 min at  $170^\circ\text{C}$  on a hotplate.
4. Spin Shipley S-1813, diluted 1:1 by volume with Shipley P-Thinner, at 3000 rpm, giving a thickness of about 200 nm.
5. Bake for 12 min at  $160^\circ\text{C}$  on a hotplate.
6. Evaporate 20 nm Ge at  $0.2 \text{ nm/s}$ .
7. Spin 350k PMMA (1.8 %, in xylene) at 2500 rpm to a thickness of about 50 nm.
8. Bake for 10 min at  $150^\circ\text{C}$  on a hotplate.
9. Break into suitable chip sets for further handling.

### C. Recipes



**Figure C.1.:** Geometric design parameters for SET made by shadow evaporation.

#### C.2.2. Four layer resist exposure

Acceleration voltage 50 kV, first aperture (diameter 60  $\mu\text{m}$ ), fifth lens (working distance 14 mm), current 20 pA for the fine patterns (1 nA for the coarser leads). Area doses

- 1120  $\mu\text{C}/\text{cm}^2$  for 20 nm wide lines.
- 400  $\mu\text{C}/\text{cm}^2$  for 100 nm wide lines.
- 280  $\mu\text{C}/\text{cm}^2$  for all wider lines and areas.

#### C.2.3. Four layer resist proximity correction

(for PROXECCO:) double Gaussian with  $\alpha = 0.02 \mu\text{m}$ ,  $\beta = 10 \mu\text{m}$  and  $\eta = 0.5$ . The low  $\eta$ , the ratio between exposure by backscattered and by directly impacting electrons, is due to the Ge layer that absorbs a large fraction of the backscattered electrons. Number of doses 32, output quality fine, physical fracturing.

#### C.2.4. Parameters for SET fabrication

See fig. C.1 for definition of geometric parameters. Linewidths  $w_l \approx w_i \approx 100 \text{ nm}$ , pattern shift  $d = 240 \text{ nm}$ , island length  $l = 600 \text{ nm}$ , overlap  $u = 100 \text{ nm}$ .

#### C.2.5. Four layer resist processing

1. Expose in the EBL machine (see C.2.2).
2. Develop in a mixture of 10 volume parts isopropanole and 1 volume part deionised water for 60 s under ultrasonic excitation.
3. Reactive ion etching: pattern transfer to the Ge mask. Process gas  $\text{CF}_4$ , pressure 1.3 Pa, flow 7.5  $\mu\text{mol}/\text{s}$ , rf power 14 W, time 120 s.

### *C.3. Niobium microanodisation*

4. RIE of the support layers. Process gas O<sub>2</sub>, pressure 13 Pa, 15  $\mu\text{mol/s}$  flow rate, rf power 20 W, time 15 min.
5. Evaporate Nb with e-gun heating. Deposition rate about 0.5 nm/s.
6. Liftoff in slightly warmed acetone, spraying chip centres directly with a syringe.

## **C.3. Niobium microanodisation**

### **C.3.1. Anodisation window mask**

1. Spin 950k PMMA (8 %, in chlorobenzene) at 5000 rpm, giving a thickness of about 1.8  $\mu\text{m}$ .
2. Bake for 12 min at 170 °C on a hotplate.
3. E-beam expose with an area dose of 280  $\mu\text{C/cm}^2$ . Acceleration voltage 50 kV, first aperture (diameter 60  $\mu\text{m}$ ), fifth lens (working distance 14 mm), current 1 nA.
4. Develop in a mixture of 10 volume parts isopropanole and 1 volume part deionised water under ultrasonic excitation for 8 min.

### **C.3.2. Electrolyte for Nb anodisation**

Downscaled from the recipe of Joynson [165]: 8.3 g ammonium pentaborate, 60 mL ethylene glycol and 40 mL distilled water to be stirred and heated to about 100 °C. The solution has to be regenerated by heating and stirring before using since the ammonium pentaborate precipitates.

*C. Recipes*

## D. Measurement data handling

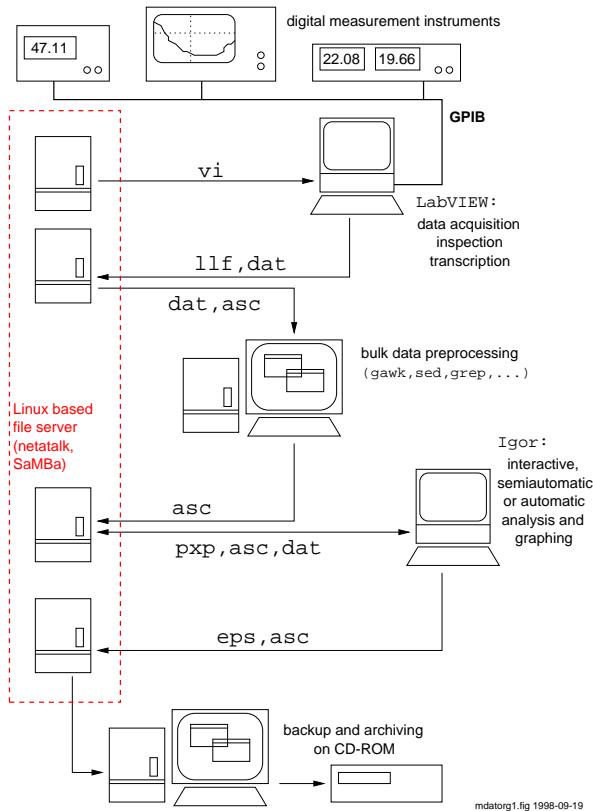
Modern physics is hardly imaginable without automatic data processing (ADP). A disadvantage of ADP is that the handling of the data largely takes place in volatile machine memory, and that the evaluation leaves much less of a paper trail than it used to only about a decade ago. Moreover, caused by the rapid changes in data storage, both in file formats and in physical media, original data as well as evaluation results can become inaccessible within a few years. While this may basically be desirable, as a mechanism that prevents us with overburdening ourselves with useless data garbage, it is at the brink of violating one of the principles of our profession. Data acquisition and evaluation must be reconstructable over a reasonable period of time; this is a matter of Good Laboratory Practice.

This chapter outlines how the data gathered for and used in this thesis were taken and stored, and how the electronic evaluation is documented. We are now in the fortunate situation that storage technologies have advanced so far that it has become feasible to keep the entire body of original data on inexpensive media. With the information in this appendix, it should be possible to understand and, if necessary, use the original data that will accompany at least some of the electronic versions of this work.

### ADP infrastructure

Figure D.1 gives an overview over the flow of measurement data. Digital measurement instruments, like multimeters, signal analysers or lock-in amplifiers, were connected, usually via a GPIB, to the measurement computer, which happened to be a succession of Macintoshes over the years. Experiment control and data acquisition programmes were written in LabVIEW, a graphical programming language that in its current version is available for and compatible between MacOS, various Windows versions and a few commercial UNIX flavours. Data were stored in a LabVIEW binary format that changed at least once during the course of this work. The data were quickly transcribed to an ASCII form that is documented in detail in the

#### D. Measurement data handling



**Figure D.1.:** Automatic data processing: organisation and flow of measurement data. All measurement instruments were digital and delivered raw data via GPIB to a Macintosh computer running LabVIEW. Inspection of the data during the measurement and the transcription to ASCII files were also done under LabVIEW. The data files were organised and preprocessed on a Linux workstation, and the final analysis and graphical presentation was carried out on other Macintoshes and Windows NT workstations using the Igor software. Files were kept on a Linux file server and backed up and archived via the Linux system.

following section D. All data evaluation was then based on these ASCII files that are to be considered the original data. The simple preprocessing of large amounts of data, such as screening and extraction of specific quantities, was done with a number of GNU tools like awk, sed and grep on a Linux workstation.

For the final evaluation and graphical presentation of the data, the (proprietary) software Igor from WaveMetrics was found most suitable, for a number of reasons. Igor has a powerful scripting language that allows easy handling of large sets of data, and file input/output. By breaking up long evaluation sequences into short programmes, using ASCII files as interface for the exchange of intermediate data, Igor can be employed in a way that optimises traceability. All evaluation steps are documented as instructions in the Igor procedures, which can be exported and stored or printed as human-readable ASCII files. Like LabVIEW, the latest version of Igor is available for Macintosh and 32 bit-Windows systems with Intel processors. Unfortunately, there is no UNIX/Linux version.

Data were kept on a Linux file server interfaced to the Macintosh world with netatalk and to the Windows network with SaMBa. The measurement data, photographs, and scanned documents are stored on compact discs.

## Measurement data file formats

### Definitions

A **logbook** is a book with a sturdy cover and paginated blank pages in which circumstances of experiments are noted with a nondelible pen immediately as they occur. Entries made at a later date than the date of the measurement, usually in the form of additional remarks, are clearly marked as such.

A **measurement** is completed when data from an instrument have been read either into AIS memory or by a human observer, independently of whether these data have been recorded on storage media.

An **experiment** is an ensemble of measurements logically belonging together, usually carried out with essentially unchanged apparatus and a variation of typically one parameter. Every experiment is identified by a three-digit numerus currens and must be described in a logbook entry. The last digit of the year and the hexadecimal digit for the month are prepended to this three digit number, giving a five alphanumeric character long **experiment identification number**.

Every experiment consists of a number of **logs**, that is a set of measure-

#### *D. Measurement data handling*

ments with unchanged parameters. Usually, one independent variable is changed ('swept'), and recorded along with at least one dependent variable and the relevant parameters. Logs within each experiment are numbered with a three digit decimal number, starting from 000 for each experiment. The concatenation of experiment identification number and this three digit log number gives the **log identification number**. Individual logs need not have a corresponding entry in the logbook, if parameters have been varied and recorded automatically; in this case, a summary entry in the logbook is sufficient.

A **LabVIEW log file** records the data of exactly one experiment in a National Instruments proprietary binary format.

**Transcription** is the process of translating the information contained in a LabVIEW log file into ASCII files suitable for both human and automatic reading and processing, and for archiving.

A **log file** is the ASCII translation of exactly one log. Its name consists of the log identification number and the extension **.dat** (note the compliance with ISO 9660 and DOS restrictions on filenames). Log files are only generated automatically from the LabVIEW log file and never modified afterwards.

### **Types of information**

By semantical content, information contained in every log of an experiment falls into one of the following categories.

**Parameters** are recorded as pairs of parameter names and parameter values. They give settings of experimental apparatus, and setpoints and measured actual values of physical quantities.

**Data** consist of usually at least two, fairly large streams of numerical data.

**Free formatted text** is text information given manually to the programme writing the LabVIEW log files, describing hardware settings, sample characteristics etc. It is used to back up the logbook entries and to make information accessible to ADP.

**Other info** like timestamps either in name-value-pair format like parameters, or as free formatted text.

According to into which of these categories information fall, their formatting in the ASCII transcription will vary.

## Implementation in LabVIEW

Every log in a LabVIEW log file consists of

- a timestamp,
- a free formatted comment text and
- a number of ('an array of' in LabVIEW notation) clusters, each consisting in turn of
  - a name string,
  - a parameter string and
  - a value array.

The information contained in each cluster falls into exactly one of two of the categories described in D:

For *parameter clusters*, the name string is arbitrary yet descriptive, and the parameter string contains exactly as many lines (separated by newline characters dependent on the OS LabVIEW runs under) as there are values in the value array. Each line in the parameter name string then gives the name of the parameter whose value is recorded in the corresponding cell of the value array.

In *data clusters*, the name string contains the name of the variable, chosen consistently across as many experiments as possible (see table D.1). The parameter has either less or more lines than there are values in the value array, usually less. In the parameter string, keywords and parameters are recorded that the measuring and recording programme might use to derive measured quantities from raw data, for example a bias resistance value used to compute the transport current from a voltage measurement.

## Format of ASCII transcript

In this section, the rules for the translation of LabVIEW log files into log files are described and the characteristic patterns making these log files accessible to ADP are defined. As an example, we show the transcript of the first log (number 000) of the experiment with the numerus currens 394, registered in December 1997. According to the naming conventions outlined above, this file must have the name `7c394000.dat`. The transcript starts with some information intended for its identification in case the file should change its name (like in a recovery action after a file system corruption):

#### D. Measurement data handling

**Table D.1.:** Variable names (non-exhaustive compilation) and generic “wave” names for Igor use. Unless indicated specifically, quantities are recorded in the appropriate SI units, except for temperatures, which are recorded in mK for historical reasons.

variable name	description
<i>i</i> <i>logIDnr</i>	transport current
<i>isrbdclogIDnr</i>	current times bias resistance (DC)
<i>v</i> <i>logIDnr</i>	voltage
<i>vblogIDnr</i>	bias voltage
<i>vglogIDnr</i>	gate voltage
<i>vguaclogIDnr</i>	voltage before divider on gate (AC)
<i>vgudclogIDnr</i>	voltage before divider on gate (DC)
<i>vsdclogIDnr</i>	voltage over sample (DC)
... <i>mv</i> ...	mean value
... <i>std</i> ...	standard deviation
<i>inv</i> ...	inverse ( $1/x$ )
<i>ln</i> ...	natural logarithm of ...
<i>log</i> ...	decadic logarithm of ...
... <i>mv</i>	... in mV
... <i>ua</i>	... in $\mu$ A
... <i>ko</i>	... in k $\Omega$

```
MEASUREMENT DATA TRANSCRIPT FILE
COPYRIGHT henning@fy.chalmers.se
SOURCE_FILE_(LABVIEW_LOG) 7c394
FILENAME 7c394000.dat
```

Then, the free formatted text is included, surrounded by characteristic lines:

```
--- BEGIN_COMMENT ---
SAMPLE T47-34
completely Per's box
sweeping I-V
MAGN 05.000 T
base temperature
PINS 1-1-16-16
GATEPIN 3
stepping gate
--- END_COMMENT ---
```

Even without consulting the logbook, one can now see that this file contains a current-voltage characteristic of the device between pins 1 and 16 on chip T47-34, measured in a magnetic field of 5 Tesla at cryostat base temperature, and that the parameter varied in this experiment is the gate voltage applied to pin 3 on the chip.

The next brief section of the log file is the time stamp, both in a machine friendly and a human readable format:

```
TIMESTAMP 2964497225
DATE_TIME 1997-12-09 08:27
```

This *I-V* characteristic was logged at 08:27 hours local time on 9th December, 1997.

The following is the transcription result of three parameter clusters:

```
SWEET cluster
BUFSIZ 1.024000E+3
LORAMP -1.000000E+1
HIRAMP 1.000000E+1
SWPORT 3.000000E+0
TRPORT 2.000000E+0
SWMODE 1.000000E+0
ACCURACY cluster
DELAY 2.000000E+1
```

#### D. Measurement data handling

```
NPLC      1.000000E+0
AUTOCAL   0.000000E+0
DISPLAY   1.000000E+0
TEMPERATURE cluster
T_INIT    1.500000E+3
R_INIT    0.000000E+0
T_FINAL   1.500000E+3
R_FINAL   0.000000E+0
SENSOR    5.000000E+0
```

Most of this should be self-explanatory. If applicable, “1” represents the Boolean “true” or “on”, “0” represents “false” or “off”. BUFSIZ gives the number of data points in a sweep, SWMODE equal 1 indicates bidirectional sweep (0 would have been unidirectional). The implausible values for initial and final temperature are due to a bug in the temperature measurement software: since our thermometer is not calibrated below what we believe to be 15 mK, an appropriate output would have been ‘NaN’, as a synonym for ‘below 15 mK’.

The next cluster is a data cluster for the variable named *i*:

```
--- BEGIN DATACOMMENTS i ---
i_R_BIAS 2E4
i_GAIN 1E3
--- END DATACOMMENTS i ---
--- BEGIN DATA i ---
i7c394000
-1.990785E-8
-1.984932E-8
          {1020 lines of text deleted here}
-1.979642E-8
-1.984588E-8
--- END DATA i ---
```

The variable name is prepended to the lines of the parameter string, separated by an underscore. Here, the current was computed by measuring the voltage drop across the bias resistor of  $20\text{ k}\Omega$ , amplified with a gain of 1000. Similarly, the voltage across the sample *v* and the gate voltage *vg* are recorded.

Immediately preceding the actual numerical data is one line that contains a name uniquely identifying the data stream. The name consists of the variable name and the log identification number. When handling the data with Igor, this becomes the “wave” name.

```

--- BEGIN DATACOMMENTS v ---
v_GAIN 1E2
--- END DATACOMMENTS v ---
--- BEGIN DATA v ---
v7c394000
-2.734458E-3
-2.723223E-3
{1020 lines of text deleted here}
-2.718614E-3
-2.729049E-3
--- END DATA v ---
--- BEGIN DATACOMMENTS vg ---
vg_GAIN 4E1
vg_FIX_RANGE 9 VOLT
--- END DATACOMMENTS vg ---
--- BEGIN DATA vg ---
vg7c394000
9.926481E-7
9.704308E-7
{1020 lines of text deleted here}
1.125952E-6
1.092626E-6
--- END DATA vg ---

```

Finally, the last cluster is a parameter cluster again, giving the gate voltage setpoint. If the gate voltage had not been measured in every point of the sweep, one measurement of the actual value would have been included here:

```

SHELL_VOLTAGE cluster
V_SHELL_SETPOINT      0.000000E+0
V_SHELL_MEASURED      NaN

```

The log file is concluded by a human readable line that also helps to verify the completeness of the log file:

```
END OF MEASUREMENT DATA TRANSCRIPT FILE
```

## **Applicability**

The above scheme was used for all low temperature and very low temperature experiments from the beginning of 1996, starting with experiment

#### D. Measurement data handling

**Table D.2.:** File name extensions and file types

extension	file type
.txt	text (ASCII), generic
.asc	text (ASCII), intermediate data
.dat	text (ASCII), original data (not to be altered)
.pdf	Portable Document Format, often scanned material
.bmp	Windows bitmap, e.g. SEM original photos
.tif	TIFF images, e.g. optical microscope photographs
.jpg	JPEG/JFIF, compressed photographs
.vi	LabVIEW Virtual Instruments (programmes)
.bdat	LabVIEW log file, versions $\leq 3$
.llf	LabVIEW log file, versions $\geq 5$
.pxp	Igor packed experiment
.eps	Encapsulated Postscript (graphics)
.tar	GNU tape archive
.gz	GNU gzip compressed file
.html	HTML (for navigation)
{none}	executable scripts

number 62236 on 1996-02-20. Data taking during the anodisation of samples were recorded directly in ASCII in another, linewise constructed, column oriented format, since these data had to be yanked to the hard disk during the process.

#### Other file formats

The most important of those data formats, identified by the file name extension, that will be encountered in the electronic material relating to this work, are given in table D.2.

## **E. Selected publications 1994–1998**

### **Superconductor physics and single electronics**

- Torsten Henning, B. Starmark, T. Claeson, and P. Delsing. Bias and temperature dependence of the noise in a single electron transistor. accepted by Eur. Phys. J. B 1998-10-12, [cond-mat/9810103](#).
- B. Starmark, Torsten Henning, A. N. Korotkov, T. Claeson, and P. Delsing. Gain dependence of the noise in the single electron transistor. [cond-mat/9806354](#).
- T. Henning, B. Starmark, and P. Delsing. Stromrauschen eines Einzelektronentransistors. Talk at Tagung Kryoelektronische Baulemente Kryo '98, Braunschweig, 1998-10-11–13. Published in summary form only.
- Torsten Henning. Coulomb blockade effects in anodised niobium nanostructures (Coulomb-blockad-effekter i anodiserade Nb-nanostrukturer). Licentiate thesis, Institutionen för Mikroelektronik och Nanovetenskap, Chalmers Tekniska Högskola AB och Göteborgs Universitet, Göteborg, May 1997. [cond-mat/9710037](#).
- Torsten Henning, D. B. Haviland, and P. Delsing. Coulomb blockade effects in anodized niobium nanostructures. *Supercond. Sci. Technol.*, 10(9):727–732, September 1997. [cond-mat/9706302](#).
- Torsten Henning, D. B. Haviland, and P. Delsing. Charging effects and superconductivity in anodised niobium nanostructures. In H. Koch and S. Knappe, editors, *ISEC'97. 6th International Superconductive Electronics Conference. Extended Abstracts*, volume 2, pages 227–229, Berlin, June 1997. Physikalisch-Technische Bundesanstalt. ISBN 3-9805741-0-5.

#### E. Selected publications 1994–1998

- Torsten Henning, D. B. Haviland, and P. Delsing. Fabrication of Coulomb blockade elements with an electrolytic anodization process. *Electrochemical Society Meeting Abstracts*, 96-2:561, 1996. Fall Meeting San Antonio, Texas, October 6–11. Published in summary form only.
- Torsten Henning, D. B. Haviland, and P. Delsing. Transition from supercurrent to Coulomb blockade tuned by anodization of Nb wires. *Czech. J. Phys.*, 46(Suppl. S4):2341–2342, 1996. Proc. 21st Int. Conf. on Low Temperature Physics, Prague, August 8–14, 1996.
- T. Henning, D. B. Haviland, P. Delsing, and T. Claeson. Widerstände für Einzelladungstunnelemente. *Verhandl. DPG (VI)*, 30:1751, 1995. DPG-Frühjahrstagung Berlin 1995. Published in summary form only.
- Torsten Henning, David B. Haviland, and Per Delsing. Nanofabrikation von Widerständen aus anodisierten Nb-Drähten. *Verhandl. DPG (VI)*, 31:1966–1967, 1996. DPG-Frühjahrstagung Regensburg 1996. Published in summary form only.
- T. Henning, D. B. Haviland, P. Delsing, and T. Claeson. Nb resistors for single electronics. *Bull. APS (II)*, 40(1):205, March 1995. APS March Meeting San Jose 1995. Published in summary form only.
- Torsten Henning, H. Kliem, A. Weyers, and W. Bauhofer. Characterization of high-temperature superconductor ceramics from their resistive transition. *Supercond. Sci. Technol.*, 10(9):721–726, September 1997. [cond-mat/9707165](#).

## Semiconductor physics

- P. J. Klar, D. Wolverson, J. J. Davies, W. Heimbrodt, M. Happ, and T. Henning. Photoluminescence and photoluminescence excitation studies of lateral size effects in  $Zn_{1-x}Mn_xSe/ZnSe$  quantum disc samples of different radii. *Phys. Rev. B*, 57(12):7114–7118, March 1998. [cond-mat/9803208](#).
- Ivan J. Griffin, Peter J. Klar, Daniel Wolverson, J. John Davies, Bernard Lunn, Duncan E. Ashenford, and Torsten Henning. Magneto-photoluminescence studies of  $Zn_{1-x}Mn_xTe/ZnTe$  multiple quantum-well and quantum-dot structures. *J. Crystal Growth*, 184/185:325–329, 1998. [cond-mat/9805079](#).

- P. J. Klar, D. Wolverson, D. E. Ashenford, B. Lunn, and Torsten Henning. Comparison of  $Zn_{1-x}Mn_xTe/ZnTe$  multiple-quantum wells and quantum dots by below-bandgap photomodulated reflectivity. *Semicond. Sci. and Tech.*, 11:1863–1872, 1996. [cond-mat/9710008](#).
- Peter J. Klar, Daniel Wolverson, J. John Davies, Bernard Lunn, Duncan E. Ashenford, and Torsten Henning. Spin-flip Raman scattering in quantum dots based on  $Cd_{1-x}Mn_xTe/CdTe$  quantum well structures. In Matthias Scheffler and Roland Zimmermann, editors, *Proc. 23rd Int. Conf. on the Phys. of Semicond., Berlin, 21–26 July 1996*, volume 2, pages 1485–1488. World Scientific, June 1996. ISBN 981-02-2777-9 (set), 981-02-2946-1 (vol. 2).