Mutual Compensation of Mobility and Threshold Voltage Temperature Effects with Applications in CMOS Circuits

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***Abstract*—Mutual compensation of mobility and threshold voltage temperature variations may result in a zero temperature coefficient bias point of a MOS transistor. The conditions under which this effect occurs, and stability of this bias point are investigated. Possible applications of this effect include voltage reference circuits and temperature sensors with linear dependence of voltage versus temperature. The theory is verified experimentally investigating the temperature behavior of a simple voltage reference circuit realized in 0.35-μm CMOS process.**

***Index Terms*—Device characterization, mobility, MOSFETs, threshold voltage, temperature effects, temperature sensors, voltage references.**

I. Introduction

MUTUAL compensation of mobility and threshold voltage temperature effects in field-effect transistors is well known [1]–[4]. Yet, the detailed investigation of this compensation resulting in the so-called zero temperature coefficient (ZTC) point in MOS transconductance characteristics was never done. In early MOS technologies, this ZTC point was observed for high gate-source voltages [5] that exceed power-supply voltages of modern circuits, and this may be an explanation of the fact that the compensation has not obtained proper attention. Yet, the exact behavior of transistor transconductance characteristics in the vicinity of ZTC bias point is important for design of circuits operating in a wide temperature range [5].

Recently, [6] it was confirmed that the ZTC point exists for a series of industrial CMOS technologies. It was shown that, using an external constant current source for biasing a diode-connected MOS transistor at ZTC point, one obtains a temperature-stable voltage. The reported stability was 13 ppm/°C in the range of 0–125 °C. It was suggested that these results could be employed to develop a reference voltage circuit. Other authors [7] have doubts on applications of the compensation effect, and consider that the circuits will not be reproducible.

This work considers the conditions of mutual compensation of mobility and threshold voltage temperature effects in MOS transistors. The ideal compensation requires that the transistor threshold voltage is a linear function of temperature, T, and that the mobility is proportional to T^{-2}. These two conditions, in general, were known [5]. But if the first condition is approximately satisfied (say, in the temperature range −20 to 120 °C), the second is not satisfied in practice. It is shown here that the exponent in the mobility temperature dependence may be different from −2, and is also a weak function of temperature. Yet, this exponent determines the temperature stability of current or voltage reference circuits using ZTC bias point.

We investigated the behavior of transistor transconductance characteristics at ZTC point and the vicinity. To verify the proposed theory, we designed a simple voltage reference and tested it in operating as a reference, and as a temperature sensor.

To provide some background, Section II of this paper presents the conditions of compensation required to obtain ZTC point. Section III discusses temperature behavior of threshold and mobility in more detail than usual. Section IV describes the transistor gate-source voltage and drain current drifts in the vicinity of ZTC point. Section V describes the design of a simple voltage reference circuit using combination of mutual compensation of mobility and threshold voltage temperature effects, and resistor temperature compensation effect that is also available in 0.35 μm CMOS n-well technology. The experimental results for this circuit are also given in this section. All results are summarized in the Discussion and Conclusions section.

II. Compensation of Mobility and Threshold Voltage Temperature Effects

Following [8] let us write the n-channel transistor drain current equation

$$I_d = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)(V_{\rm gs} - V_T)^2. \tag{1}$$

The carrier mobility, μ_n, and the threshold voltage, V_T decrease with temperature [9], and for a given temperature, T_1, one can find the bias voltage

$$V_{\rm GS} = V_T(T_1) + \left[2\mu_n \frac{\partial V_T/\partial T}{\partial \mu_n/\partial T}\right]\Bigg|_{T=T_1} \tag{2}$$

such that the drain current I_d, at T_1, satisfies the condition $(\partial I_d)/(\partial T)|_{T=T_1} = 0$. It is usually assumed [9] that V_T depends on temperature as

$$V_T(T) = V_T(T_0) + \alpha_{\rm VT}(T - T_0) \tag{3}$$

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where T_0 is the reference temperature, and $\partial V_T/\partial T = \alpha_{\rm VT}$ is a negative constant. The mobility depends on temperature as [10]

$$\mu_n(T) = \mu_n(T_0)(T/T_0)^{\alpha_\mu}. \tag{4}$$

Let us assume, for now, that α_μ is a constant. When (3) and (4) are substituted in (2) one obtains that the required bias voltage is

$$V_{\rm GS} = V_T(T_0) + \alpha_{\rm VT}T_1\left(1+\frac{2}{\alpha_\mu}\right) - \alpha_{\rm VT}T_0. \tag{5}$$

If, in addition, $\alpha_\mu = -2$, then there exists also a temperature independent voltage

$$V_{\rm GS} = V_{\rm GSF} = V_T(T_0) - \alpha_{\rm VT}T_0 \tag{6}$$

biasing the transistor to an also temperature independent drain current $I_{\rm DF}$. If (6) and (3) are substituted into (1), one obtains

$$I_D = \frac{\mu_n(T)C_{ox}}{2}\left(\frac{W}{L}\right)(\alpha_{\rm VT}T)^2. \tag{7}$$

If the temperature dependence (4) is substituted in (7) with $\alpha_\mu = -2$ one obtains

$$I_D = I_{\rm DF} = \frac{\mu_n(T_0)T_0^2C_{ox}}{2}\left(\frac{W}{L}\right)\alpha_{\rm VT}^2. \tag{8}$$

In this case the temperature decrease of mobility indeed compensates the temperature decrease of the threshold voltage, and the transistor biased by the voltage $V_{\rm GSF}$ has a temperature independent drain current $I_{\rm DF}$.

A diode-connected transistor can be biased by a current source. Rewriting (1) as

$$V_{\rm gs} = V_T + \sqrt{\frac{2I_d}{\mu_nC_{ox}(W/L)}} \tag{9}$$

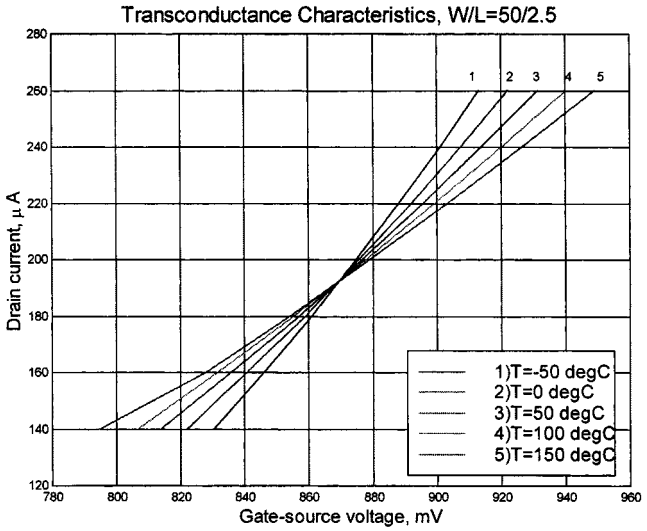
one can find, for a given temperature, T_2, the drain current, I_D, that provides the condition $(\partial V_{\rm gs})/(\partial T)|_{T=T_2} = 0$. For this current, the voltage $V_{\rm gs}$ becomes equal

$$V_{\rm GS} = V_T(T_2) + \frac{2\alpha_{\rm VT}T_2}{\alpha_\mu} = V_{\rm GSF} + \alpha_{\rm VT}T_2\left(1+\frac{2}{\alpha_\mu}\right). \tag{10}$$

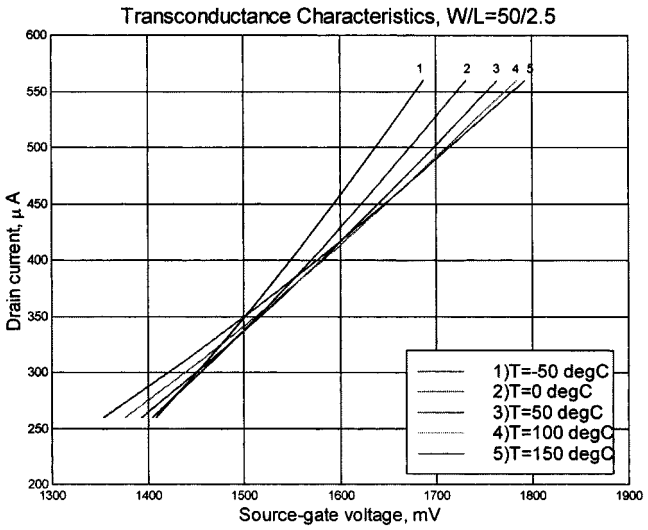
When $\alpha_\mu = -2$, this voltage has the same value as in (6), and the required I_D is given by (8).

If this point ($V_{\rm GSF}$, $I_{\rm DF}$) exists, the transistor transconductance characteristics obtained at different temperatures have a common intercept point. As it follows from (3) and (6), for $V_{\rm gs} = V_{\rm GSF}+\Delta V_{\rm GS}$ and an arbitrary temperature T, $V_{\rm gs}-V_T = \Delta V_{\rm GS} - \alpha_{\rm VT}T$. The drain current becomes

$$I_d = \frac{\mu_n(T_0)(T/T_0)^{-2}C_{ox}}{2}\left(\frac{W}{L}\right)(\Delta V_{\rm GS} - \alpha_{\rm VT}T)^2 \approx I_{\rm DF}\left(1-\frac{2}{\alpha_{\rm VT}T}\Delta V_{\rm GS}\right). \tag{11}$$



(a)



(b)

Fig. 1. Transconductance characteristics in the vicinity of ZTC bias point (a) n-channel transistor (b) p-channel transistor.

Fig. 1(a) shows, as an example, the simulated transconductance characteristics (with T as a parameter) for an n-channel device in 0.35 μm CMOS technology. They have a common intercept point ($V_{\rm GSF} \approx 869$ mV, $I_{\rm DF} \approx 192$ μA), and, indeed, can be approximated as pieces of straight lines with the slope that is inversely proportional to temperature.

If $\alpha_\mu \neq -2$, the point ($V_{\rm GSF}$, $I_{\rm DF}$) does not exists. Then, for $V_{\rm gs} = V_{\rm GSF} + \Delta V_{\rm GS}$, as it follows from (5), at an arbitrary temperature $V_{\rm gs} = V_{\rm GSF} + \Delta V_{\rm GS} + \alpha_{\rm VT}T(1+2/\alpha_\mu)$. The drain current becomes

$$I_d = \frac{\mu_n(T_0)(T/T_0)^{\alpha_\mu}C_{ox}}{2}\left(\frac{W}{L}\right)\left(\Delta V_{\rm GS} + \frac{2\alpha_{\rm VT}T}{\alpha_\mu}\right)^2 \approx I_{\rm DF}\left(\frac{2}{\alpha_\mu}\right)^2\left(\frac{T}{T_0}\right)^{2+\alpha_\mu}\left(1+\frac{\alpha_\mu}{\alpha_{\rm VT}T}\Delta V_{\rm GS}\right). \tag{12}$$

The characteristics are again pieces of straight lines with the slope that is inversely proportional to the temperature. Yet, they

do not have a common intercept point, they have a "bottleneck" only. The initial point of each characteristic (obtained for $\Delta V_{\rm GS} = 0$) depends on temperature. Such characteristics [Fig. 1(b)] were obtained for p-channel transistors of the same technology. Introducing $\Delta T = T - T_0$ one can approximate $(T/T_0)^{2+\alpha_\mu} \approx 1 + (2+\alpha_\mu)(\Delta T/T_0)$. Then, the drain current in the vicinity of the "bottleneck" can be rewritten as

$$I_d \approx I_{\rm DF}\left(\frac{2}{\alpha_\mu}\right)^2\left[1+(2+\alpha_\mu)\frac{\Delta T}{T_0}\right] \cdot\left[1+\frac{\alpha_\mu}{\alpha_{\rm VT}}\frac{\Delta V_{\rm GS}}{(T_0+\Delta T)}\right]. \tag{13}$$

When $\alpha_\mu = -2$, the result (13) coincides with (11).

III. Temperature Dependencies of $\alpha_{\rm VT}$ and α_μ

In the previous section, it was assumed that $\alpha_{\rm VT}$ and α_μ are temperature independent. In general, this is not valid for a wide range of temperatures neither for $\alpha_{\rm VT}$, nor for α_μ.

One usually [9] approximates V_T as a linear function of temperature

$$V_T(T) = V_T(T_0) + \alpha_{\rm VT}(T - T_0) \tag{14}$$

repeated here for convenience. The values of $\alpha_{\rm VT}$ vary [9], [10] from -1 mV/°C to -4 mV/°C, and the most frequently used figure is -2 mV/°C. These figures are difficult to use in design: $\alpha_{\rm VT}$ is an extracted parameter [11] in BSIM3v.3 and others, more advanced (BSIM3v.3.1 in our case) models. Nothing stipulates that $\alpha_{\rm VT}$ should be constant.

The evaluation of $\alpha_{\rm VT}$ can be found in [1], [12]–[15]. We found that the procedure described in [15] gives the values of $\alpha_{\rm VT}$ coinciding well with the experimental ones [16]. In accordance with [15], for long channel transistors without substrate bias, V_T can be expressed in the general form

$$V_T = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} + 2\phi_F + \Delta V_T(N_i) + \gamma(N_s, t_{ox}, L, W) \cdot\sqrt{2\phi_F + V_o}. \tag{15}$$

Here, ϕ_{ms} is the contact potential difference between gate and substrate, Q_{ss} is the surface-state charge density per unit area, ϕ_F is the Fermi potential of substrate, $\Delta V_T(N_i)$ is the threshold shift owing to a channel implant N_i with depth d_i. Then, γ is the body-effect constant that depends on the substrate doping N_s, the gate oxide thickness t_{ox}, the channel length L, and width W. Finally, $V_o(N_i, N_s, d_i)$ is a correction term owing to the threshold shift implant. For enhancement devices with a ΔV_T shifting implant of the same type as the substrate, V_o has a sign opposite to that of ϕ_F. When a usual n-type doped silicon gate is applied, CMOS n-channel devices belong to the described type.

The only factors which may cause a temperature dependence of V_T are ϕ_{ms} and ϕ_F. Therefore, the temperature coefficient of V_T is given by

$$\frac{\partial V_T}{\partial T} = \frac{\partial \phi_{ms}}{\partial T} + 2\frac{\partial \phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\phi_F + V_o}}\frac{\partial \phi_F}{\partial T}. \tag{16}$$

For the devices of 0.35 μm CMOS technology, the gate doping is of the opposite type as that of substrate, and $\phi_{ms} = (kT/q)\ln(N_s N_g/n_i^2)$. Here, N_g is the gate doping level. Assuming [13], [14], that $n_i^2 = 1.5 * 10^{33} T^3 \exp[-E_{G0}/kT]$, where $E_{G0}/q = 1.21$ V is the extrapolated zero-degree band gap, one can find that for an n-type doped gate

$$\frac{\partial \phi_{ms}}{\partial T} = \frac{1}{T}\left[\phi_{ms} + \frac{E_{G0}}{q} + \frac{3kT}{q}\right]. \tag{17}$$

The temperature coefficient of $2\phi_F = [2kT/q]\ln(N_s/n_i)$is given by

$$2\frac{\partial \phi_F}{\partial T} = \frac{1}{T}\left[2\phi_F - \left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right)\right]. \tag{18}$$

Hence, the temperature coefficient of the threshold voltage becomes

$$\frac{\partial V_T}{\partial T} = \frac{\phi_{ms}}{T} + 2\frac{\phi_F}{T} + \frac{\gamma}{\sqrt{2\phi_F + V_o}}\frac{\partial \phi_F}{\partial T}. \tag{19}$$

For numerical calculation it was decided to take $N_s = 1 * 10^{17}$ cm^{-3} and $N_g = 1 * 10^{19}$ cm^{-3}. The typical value of the oxide thickness for 0.35 μm CMOS technology is $7.3{*}10^{-7}$ cm. Then, one finds that $\phi_{ms} = -0.931$ V and $2\phi_F = 0.811$ V. Evaluating the body effect coefficient as [8] $\gamma \approx 1.67{*}10^{-3} t_{ox}\sqrt{N_s}$ V$^{1/2}$ (here t_{ox} is in cm, and N_s is in cm^{-3}) one obtains that $\gamma = 0.385$ V$^{1/2}$. These values are reasonably close to that used in [15] and to the parameters of the process used for circuit manufacturing. Then, for $T = T_0 = 300$ °K one finds that the first term in (19) is -3.10 mV/°C, and the second one is 2.70 mV/°C.

The last term in (19) depends on the value of V_o and the temperature range. For $V_o = -0.2$ V, this term is still practically constant, and is approximately equal to -0.43 mV/°C. It was decided to use this value of V_o. One finds that the resulting $\alpha_{\rm VT} = -0.83$ mV/°C. In the 0.35 μm CMOS technology $V_T(T_0) = 0.6$ V, and one obtains that $V_{\rm GSF} = 0.849$ V. This voltage is, from one side, close to the results obtained in simulations [see Fig. 1(a)] and, from the other side, still allows one to assume $\alpha_{\rm VT}$ constant.

Let us consider now the temperature dependence of mobility. As it was used in (4)

$$\mu(T) = \mu(T_0)(T/T_0)^{\alpha_\mu} \tag{20}$$

The parameter α_μ (also an extracted value) is considered independent on temperature [7], [10], and the most frequent figure used is -1.5. Indeed, for nonpolar semiconductors, such as silicon, the theoretical value of mobility from acoustic phonon interaction, μ_a, is given by [12]

$$\mu_a \propto (m_e)^{-5/2} T^{-3/2} \tag{21}$$

where m_e is the conductivity effect mass. Hence, $\alpha_\mu = -1.5$ is valid when this scattering mechanism is dominant. Yet, there are

other scattering mechanisms as well. As a result of these additional mechanisms, the mobility decreases not as it is predicted by (21). The experimental figures [12] for n- and p-type silicon are $T^{-2.42}$ and $T^{-2.20}$, respectively, for the dopant concentrations N_A, $N_D \leq 10^{12}$ cm^{-3}. When the concentrations increase above 10^{17} cm^{-3}, the mobilities become approximately proportional to $T^{-1.2}$ for n- and $T^{-1.9}$ for p-type of silicon. This means that $\alpha_\mu = -2$ is possible for n-channel devices for N_A, N_D of about 10^{15}–10^{16} cm^{-3} used in modern technologies. For p-channel devices, the chance to achieve $\alpha_\mu = -2$ is less. This can be a reasonable explanation that one observes the compensation in n-channel transistors [Fig. 1(a)] and does not observe it in p-channel ones [Fig. 1(b)].

The investigation of slopes for the plots of mobility versus temperature given in [12] shows that α_μ is not constant. We assumed that for n-channel transistors $\alpha_{\mu 0}$ and $\alpha_{\mu 1}$ are both negative, and $-2.1 \leq \alpha_{\mu 0} \leq -1.9$ and $-0.05 \leq \alpha_{\mu 1} \leq -0.01$. These values were confirmed in simulations and, afterwards, experimentation with manufactured circuits. As an approximation sufficient for design purposes, it was decided to use

$$\alpha_\mu = \alpha_{\mu 0} + \alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right). \tag{22}$$

If (22) is substituted in (13) the drain current becomes rather complicated function of temperature. Yet, a simplified expression

$$I_d \approx I_{\mathrm{DFC}}\left[1+\left(2+\alpha_{\mu 0}+\alpha_{\mu 1}\frac{\Delta T}{T_0}\right)\frac{\Delta T}{T_0}\right] \cdot\left[1+\frac{\alpha_{\mu 0}}{\alpha_{\mathrm{VT}}}\frac{\Delta V_{\mathrm{GS}}}{(T_0+\Delta T)}\right] \tag{23}$$

where $I_{\mathrm{DFC}} = I_{\mathrm{DF}}(2/\alpha_{\mu 0})^2$, is sufficient to take into account the temperature effects of both mobility and threshold voltage.

IV. Stability of Bias in ZTC Point and Vicinity

If $I_d \approx I_{\mathrm{DFC}} + \Delta I_D$, the stability of ZTC bias point, as it follows from (23) can be evaluated using

$$\Delta I_D = I_{\mathrm{DFC}}\left[(2+\alpha_{\mu 0})\frac{\Delta T}{T_0}+\alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right)^2+\frac{\alpha_{\mu 0}}{\alpha_{\mathrm{VT}}} \cdot\frac{\Delta V_{\mathrm{GS}}}{(T_0+\Delta T)}\right]. \tag{24}$$

When the transistor is biased to ZTC point by a constant voltage, then $\Delta V_{\mathrm{GS}} = 0$, and the drain current drift will be

$$\Delta I_D = I_{\mathrm{DFC}}\left[(2+\alpha_{\mu 0})\frac{\Delta T}{T_0}+\alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right)^2\right]. \tag{25}$$

If $\alpha_{\mu 0} = -2$, this drift becomes

$$\Delta I_D \approx I_{\mathrm{DFC}}\alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right)^2. \tag{26}$$

The current I_d for a constant $V_{\mathrm{GS}} = V_{\mathrm{GSF}} = 868$ mV was simulated [Fig. 2(a)]. It can be approximated as $I_d = 192.8\ \mu$A $+1.5 * 10^{-3}(T-27)\ \mu$A $-5 * 10^{-5}(T-27)^2\ \mu$A (here T and in all other numerical examples is in °C). Comparing this result with (25) one finds that $I_{\mathrm{DFC}} = 192.8\ \mu$A, $T_0 = 300$ °K, $\alpha_{\mu 0} \approx -1.998$, and $\alpha_{\mu 1} \approx -0.023$. One can also find that $I_{\mathrm{DF}} = 192.4\ \mu$A.

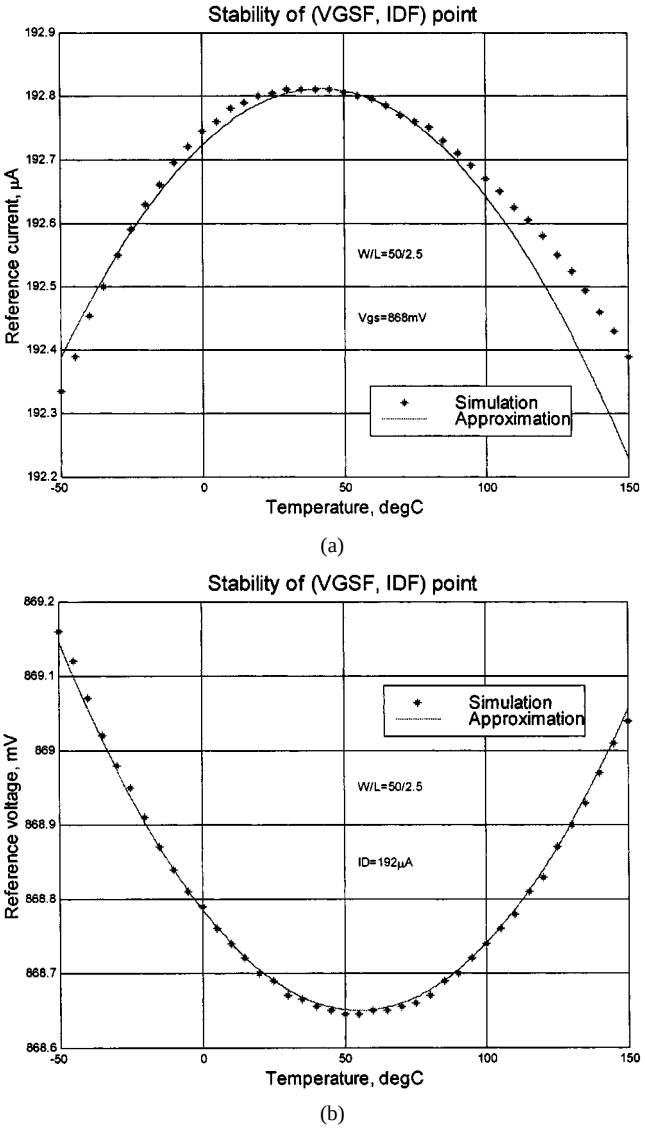


Fig. 2. Stability of ZTC bias point in simulations. (a) Constant gate-source voltage. (b) Constant drain current.

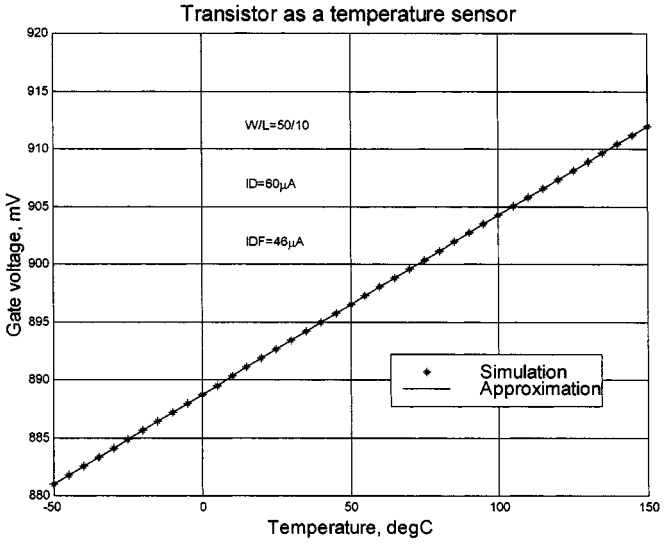
When the transistor is diode-connected, and biased to ZTC point by a current $I_D = I_{\mathrm{DFC}}$ then $\Delta I_D = 0$. The voltage drift of the gate-source voltage reference becomes

$$\Delta V_{\mathrm{GS}} \approx -\frac{\alpha_{\mathrm{VT}}T_0}{\alpha_{\mu 0}}\left[(2+\alpha_{\mu 0})\frac{\Delta T}{T_0}+(2+\alpha_{\mu 0}+\alpha_{\mu 1}) \cdot\left(\frac{\Delta T}{T_0}\right)^2\right]. \tag{27}$$

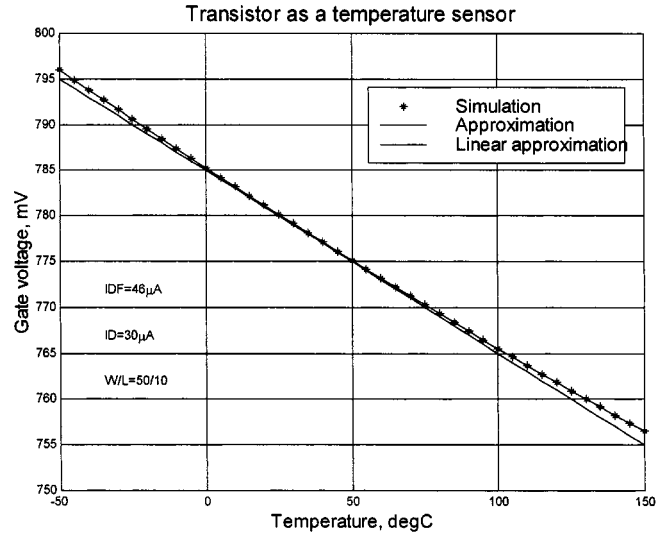
If $\alpha_{\mu 0} = -2$, the drift is reduced to

$$\Delta V_{\mathrm{GS}} \approx -\alpha_{\mu 1}\left(\frac{\alpha_{\mathrm{VT}}T_0}{\alpha_{\mu 0}}\right)\left(\frac{\Delta T}{T_0}\right)^2. \tag{28}$$

The voltage V_{gs} for a constant $I_D = I_{\mathrm{DF}} = 192\ \mu$A was simulated [Fig. 2(a)]. It can be approximated as $V_{\mathrm{gs}} = 868.65$ mV $+4.6 * 10^{-5}(T-55)^2$ mV. Comparing this result with (27) one



(a)



(b)

Fig. 3. Gate-source voltage temperature dependence for diode-connected transistor. (a) Positive slope. (b) Negative slope.

finds that $V_{\rm GSF} = 868.65$ mV, $T_0 = 328\,^{\circ}$K, $\alpha_{\mu 0} \approx -2$, and $\alpha_{\mu 1} \approx -0.036$.

Both simulations are in agreement and consistent with initial assumptions. Hence, (26) and (28) describe reasonably well the achievable stability of ZTC bias point.

In addition, using $\alpha_{\mu 0} = -2$ and neglecting the term $\alpha_{\mu 1}(\Delta T/T_0)^2$ in (24) one can find that

$$g_m = \frac{\Delta I_D}{\Delta V_{\rm GS}} = I_{\rm DFC}\,\frac{\alpha_{\mu 0}}{\alpha_{\rm VT}}\,\frac{1}{(T_0+\Delta T)}. \tag{29}$$

This result adequately represents the temperature dependence of transconductance at ZTC bias point.

Calculating $\Delta V_{\rm GS}$ from (25) one obtains that

$$\Delta V_{\rm GS} = \frac{\alpha_{\rm VT} T_0}{\alpha_{\mu 0}}\left(1+\frac{\Delta T}{T_0}\right) \cdot \left[\frac{\Delta I_D}{I_{\rm DFC}} - (2+\alpha_{\mu 0})\,\frac{\Delta T}{T_0} - \alpha_{\mu 1}\left(\frac{\Delta T}{T_0}\right)^2\right]. \tag{30}$$

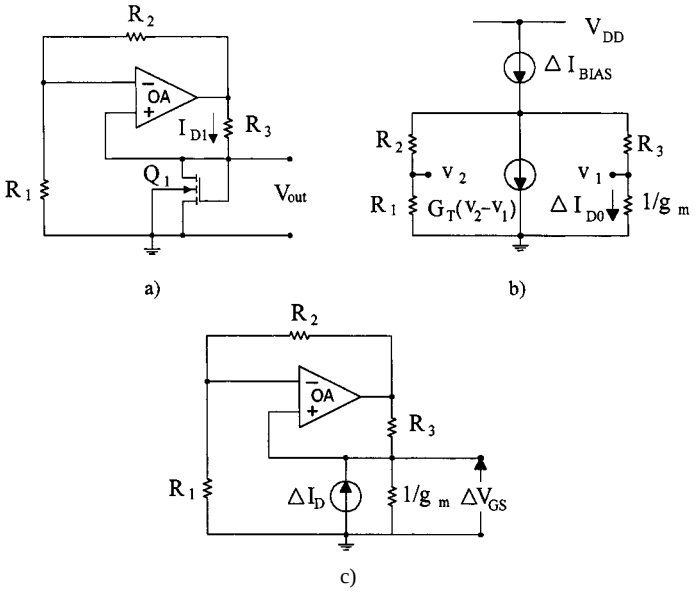


Fig. 4. (a) Voltage reference circuit. (b) Small-signal equivalent circuit for evaluation of bias variation effect. (c)Circuit for drift evaluation.

If a diode-connected transistor is biased by a current different from $I_{\rm DFC}$, and $\Delta I_D/I_{\rm DFC}$ is large in comparison with other terms in the square bracket of (30), then the voltage $\Delta V_{\rm GS}$ will change linearly with temperature as

$$\Delta V_{\rm GS} \approx \frac{\Delta I_D}{I_{\rm DFC}}\left(\frac{\alpha_{\rm VT} T_0}{\alpha_{\mu 0}}\right)\left(1+\frac{\Delta T}{T_0}\right). \tag{31}$$

Such a circuit can be used as a temperature sensor. This sensor, depending on the sign of ΔI_D, will have positive or negative slope of its temperature characteristic (Fig. 3). The device has $I_{\rm DF} \approx I_{\rm DFC} = 46$ μA and $V_{\rm GSF} \approx 844$ mV. When it is diode-connected and biased by a current of 60 μA [Fig. 3(a)], the simulated gate-source voltage temperature dependence is linear, and can be approximated as $V_{\rm gs} = 893$ mV $+0.155(T-27)$ mV. The theoretical dependence predicted by (30) should be $V_{\rm gs} \approx 882$ mV $+0.126(T-27)$ mV. For this case, the simulated and theoretical results are in a good agreement. When the transistor is biased by 30 μA [Fig. 3(b)] the simulated dependence is approximated as $V_{\rm gs} = 779$ mV $-0.22(T-27)$ mV $+1.125*10^{-4}(T+50)^2$ mV. The linear approximation to the simulated curve is $V_{gs} = 780$ mV $-0.200(T-27)$ mV. The theoretical dependence following from (30) should be $V_{\rm gs} = 806$ mV $-0.144(T-27)$ mV. Thus, for small bias currents the nonlinearity is more visible. This is explained, of course, by the nonlinearity of transconductance characteristics themselves near ZTC bias point [see Fig. 1(a)], the expression (31) is only an approximation. Note that the temperature sensor operation does not require that the compensation is present, the circuit works even if $\alpha_{\mu 0} \neq -2$.

V. Voltage Reference Circuit Design and Testing

To further verify the obtained results we designed a voltage reference circuit based on mutual compensation of mobility and threshold voltage temperature variations. The circuit is shown in Fig. 4(a) and it is similar to the circuit with Zener diode [17]. It was designed at the assumption that $\alpha_{\mu 0} = -2$, and

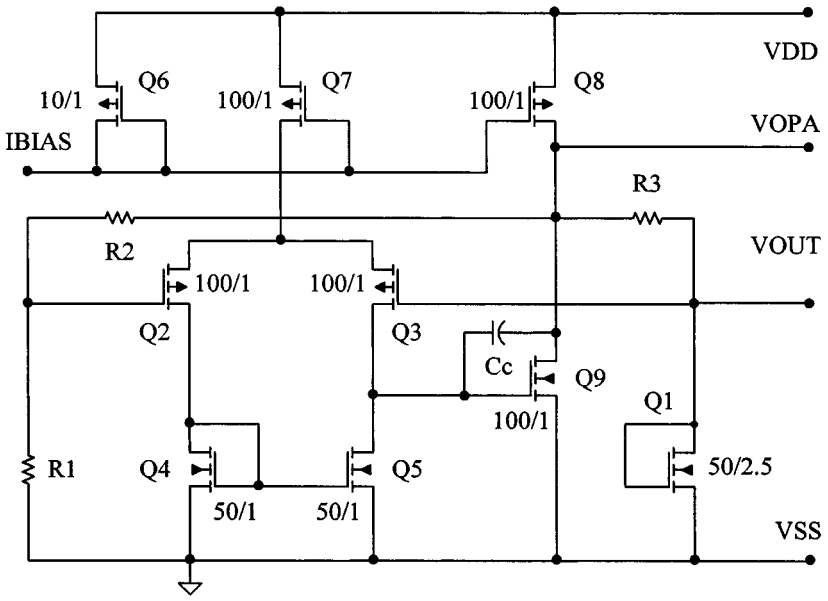


Fig. 5. Voltage reference circuit schematic.

$I_{\mathrm{DFC}} = I_{\mathrm{DF}}$. In this circuit, for transistor Q_1 the following design relationship should be satisfied

$$I_{\mathrm{D1}} = I_{\mathrm{DF}} = V_{\mathrm{GS1}} \frac{R_2}{R_1 R_3} = V_{\mathrm{GSF}} \frac{R_2}{R_1 R_3}. \tag{32}$$

One has to choose the resistors R_1, R_2, R_3 so that $I_{D1} = I_{\mathrm{DF}}$ and $V_{\mathrm{GS1}} = V_{\mathrm{GSF}}$. The values of $I_{\mathrm{DF}} = 192$ μA and $V_{\mathrm{GSF}} = 869$ mV obtained in simulations for the device with W/L =50 μm/2.5 μm were considered as the parameters of the ZTC bias point at $T = T_0 = 300$°K.

The full schematic is shown in Fig. 5. The aspect ratios shown are in microns. The technology parameters used for calculations were $\mu_n C_{ox} = 210$ μA/V^2 and $\mu_p C_{ox} = 70$ μA/V^2, $V_{TN} =$ 0.6 V, $V_{TP} = -0.7$ V. The operational amplifier is compensated by a capacitor $C_C = 10$ pF. The amplifier transconductance, G_T, is equal to 142 mA/V when the circuit is biased by the external bias current $I_{\mathrm{BIAS}} = 44$ μA applied to the terminal IBIAS. The transistor Q_1 in this case should have $I_{D1} =$ 193 μA and $V_{\mathrm{GS1}} = 870$ mV, the values close to the required ones. The resistors are $R_1 = 10$ kΩ, $R_2 = 5.8$ kΩ, and $R_3 =$ 2.6 kΩ. When the temperature changes, the resistor values also change so that $R_i = R_{i0}(1 + k_i \Delta T)$ (here $i = 1, 2, 3$). Substituting these dependencies into (32), one can find the variation, ΔI_D, of the I_{DF} current due to the resistor temperature variations

$$I_{\mathrm{DF}} + \Delta I_D \approx V_{\mathrm{GSF}} \frac{R_{20}}{R_{10} R_{30}} [1 + (k_2 - k_1 - k_3)\Delta T]. \tag{33}$$

This variation $\Delta I_D \approx 0$ when $k_2 = k_1 + k_3$. This condition for temperature coefficients is satisfied rather closely in 0.35 μm CMOS technology if R_1 and R_3 are designed using the polysilicon resistor layer ($k_1 = k_3 = 0.722 * 10^{-3}$1/°C), and R_2 using the n$^+$-diffusion layer ($k_2 = 1.473 * 10^{-3}$1/°C). Such design makes the condition (32) independent of resistor temperature variation, and allows one to better evaluate the influence of α_μ.

Evaluation of the voltage temperature drift at the output of this voltage reference, for the case of $\alpha_{\mu 0} \neq -2$, can be done the following way. An offset ΔI_{BIAS} of the external bias current allows one to introduce, if necessary, the offset current ΔI_{D0} in the drain current of Q_1. Using the small-signal circuit shown in Fig. 4(b) one can find that ΔI_{D0} is equal to

$$\Delta I_{D0} = \frac{\Delta I_{\mathrm{BIAS}}}{1 + \dfrac{1 + g_m R_3 + G_T(R_1 + R_2 - g_m R_1 R_3)}{g_m (R_1 + R_2)}}. \tag{34}$$

Here, g_m is the transconductance of Q_1. This current, in accordance with (30), will cause the first component of drift

$$\Delta V_{\mathrm{GS0}} = \left[\frac{\Delta I_{D0}}{I_{\mathrm{DFC}}} - (2 + \alpha_{\mu 0}) \frac{\Delta T}{T_0} - \alpha_{\mu 1} \left(\frac{\Delta T}{T} \right)^2 \right] \cdot \frac{\alpha_{\mathrm{VT}}}{\alpha_{\mu 0}} (T_0 + \Delta T). \tag{35}$$

The second component of the drift can be calculated from the system of two equations

$$\begin{cases} \Delta V_{\mathrm{GS1}} = \left[\dfrac{\Delta I_D}{I_{\mathrm{DFC}}} - (2 + \alpha_{\mu 0}) \dfrac{\Delta T}{T_0} - \alpha_{\mu 1} \left(\dfrac{\Delta T}{T} \right)^2 \right] \dfrac{\alpha_{\mathrm{VT}}}{\alpha_{\mu 0}} (T_0 + \Delta T) \\ \Delta V_{\mathrm{GS1}} = \Delta I_D \dfrac{R_1 R_3}{(g_m R_1 R_3 - R_2)}. \end{cases} \tag{36}$$

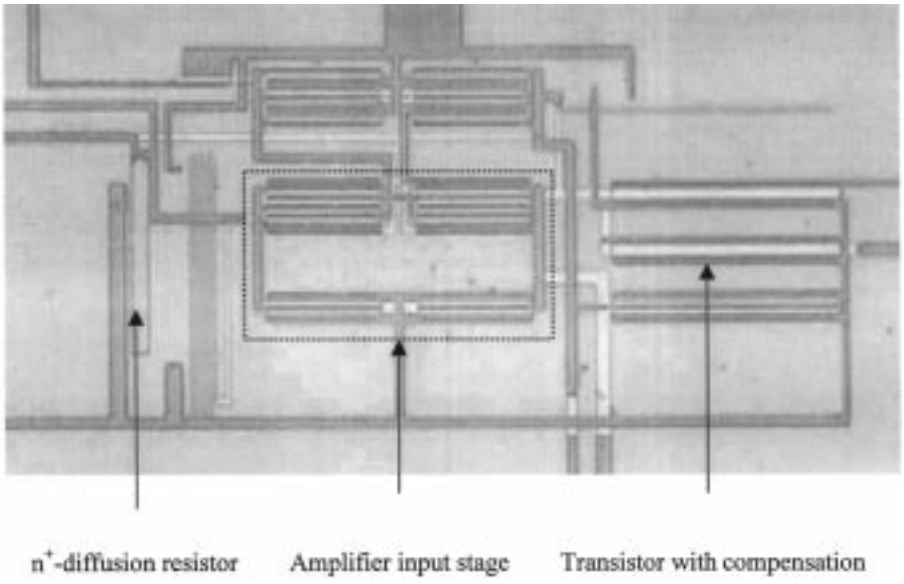


Fig. 6. Voltage reference circuit chip micrograph.

The second equation in this system is obtained considering the small-signal equivalent circuit of Fig. 4(c). Taking into consideration (30) and (32), one finds that

$$\Delta V_{\mathrm{GS1}} = -V_{\mathrm{GSF}} \left[(2+\alpha_{\mu 0}) \frac{\Delta T}{T_0} + \alpha_{\mu 1} \left(\frac{\Delta T}{T_0} \right)^2 \right]. \quad (37)$$

Then, the total voltage drift will be

$$\Delta V_{\mathrm{GS}} = V_{\mathrm{GS0}} + V_{\mathrm{GS1}} \approx A_0 + A_1 \frac{\Delta T}{T_0} + A_2 \left(\frac{\Delta T}{T_0} \right)^2 \quad (38)$$

where

$$A_0 = \frac{\Delta I_{D0}}{I_{\mathrm{DFC}}} \frac{\alpha_{\mathrm{VT}} T_0}{\alpha_{\mu 0}}$$

$$A_1 = \left[\frac{\Delta I_{D0}}{I_{\mathrm{DFC}}} \frac{\alpha_{\mathrm{VT}} T_0}{\alpha_{\mu 0}} - (2+\alpha_{\mu 0}) \left(\frac{\alpha_{\mathrm{VT}} T_0}{\alpha_{\mu 0}} + V_{\mathrm{GSF}} \right) \right]$$

$$A_2 = -\left[(2+\alpha_{\mu 0}) \frac{\alpha_{\mathrm{VT}} T_0}{\alpha_{\mu 0}} + \alpha_{\mu 1} \left(\frac{\alpha_{\mathrm{VT}} T_0}{\alpha_{\mu 0}} + V_{\mathrm{GSF}} \right) \right].$$

If ΔI_{BIAS} is chosen so that $A_1 = 0$, then the output voltage, V_{out}, at the terminal VOUT of the circuit, will be

$$V_{\mathrm{out}} = V_{\mathrm{REF}} + A_2 \left(\frac{\Delta T}{T_0} \right)^2 \quad (39)$$

where $V_{\mathrm{REF}} = V_{\mathrm{GSF}} + (2+\alpha_{\mu 0})((\alpha_{\mathrm{VT}} T_0/\alpha_{\mu 0}) + V_{\mathrm{GSF}})$. Hence, a circuit sample can be tuned, by the external bias current, to the same voltage, V_{REF}, so that the dependence of V_{out} from temperature will be quadratic. The voltage V_{REF} is different from V_{GSF} (it coincides with V_{GSF} for $\alpha_{\mu 0} = -2$), yet it should be the same for all circuit samples in the same run. Measuring V_{REF} and V_{GSF}, and using the calculated, as in Section III, value of α_{VT} one can find the experimental value of $\alpha_{\mu 0}$. The experimental temperature drift of V_{out} can be used to find the experimental $\alpha_{\mu 1}$.

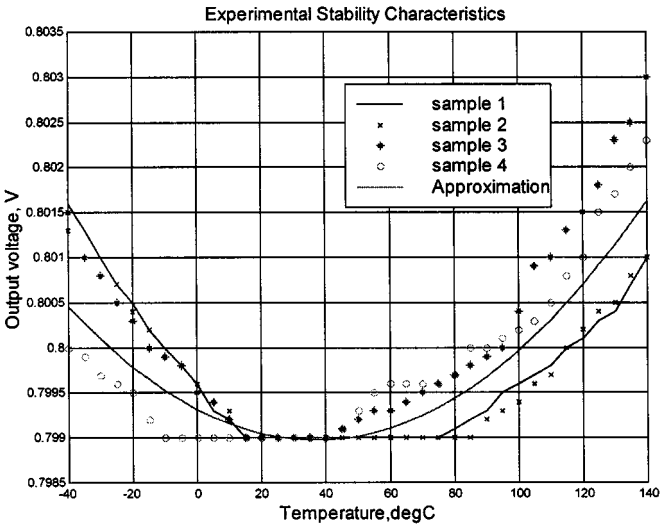


Fig. 7. Experimental temperature stability characteristics of voltage reference circuits.

The reference circuit was fabricated (Fig. 6). It occupies the area 170 μm by 120 μm. The compensation capacitor is not shown, it is located in an empty space between the circuit pads.

We had in our disposal four samples. Fig. 7 shows the test results for them. Changing the bias current of a sample by an external temperature stable resistor (TK 133 with temperature stability of 5 ppm/°C [18]) each sample was tuned to the same output voltage $V_{\mathrm{out}} = V_{\mathrm{REF}} = 799$ mV. The circuit was put, together with the external resistor, in the temperature cabinet. The average experimental temperature dependence of the output voltage for the samples can be approximated as $V_{\mathrm{out}} = 799$ mV $-5 * 10^{-6}(T-27)$ mV $+2.5 * 10^{-4}\,(T-27)^2$ mV where the temperature is in °C. The average temperature stability of these reference circuits is about 10 ppm/°C in the temperature range of −20°C–100 °C. The worst case stability is 15 ppm/°C in the same range. The power-supply voltage was 3.0–3.3 V in these experiments.

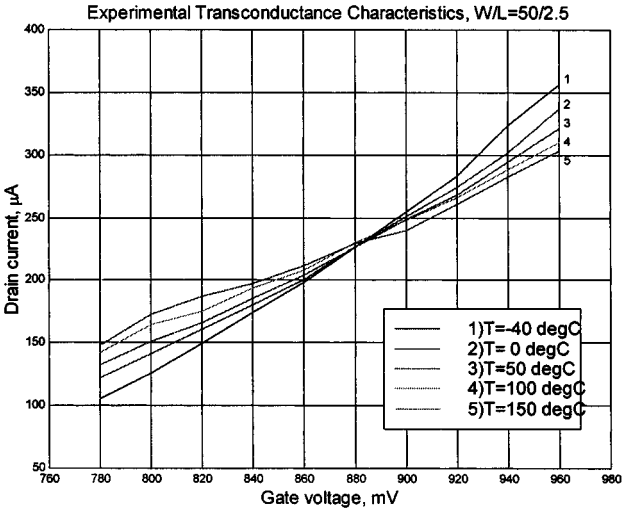


Fig. 8. Experimental transconductance characteristics in the vicinity of ZTC bias point.

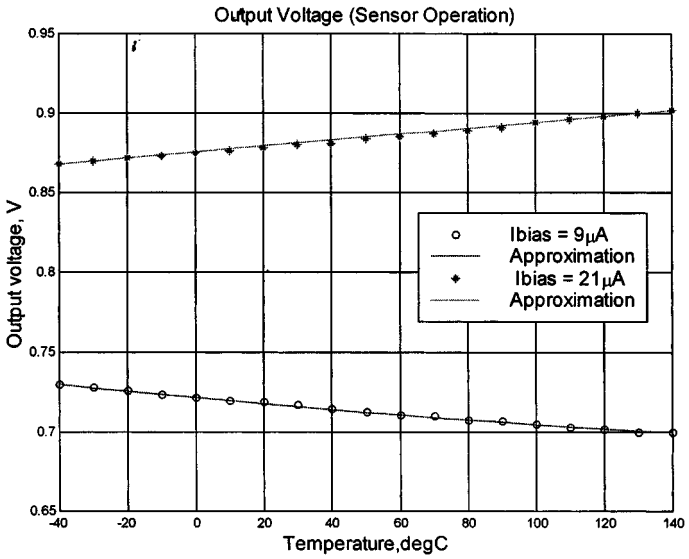


Fig. 9. Voltage reference circuit operating as temperature sensor.

The experimental transconductance characteristics of Q_1 obtained using VOUT and VOPA terminals confirmed the existence of ZTC point (Fig. 8) at $I_{\rm DFC} = 230\ \ \mu$A and $V_{\rm GSF} =$ 883 mV. The difference of 84 mV between $V_{\rm REF} = 799$ mV and this value of $V_{\rm GSF}$ allows one to find the experimental value of $\alpha_{\mu 0} = -2.084$, if we take $\alpha_{\rm VT} = -0.83$ mV/°C and $T_0 = 300$ °K. Then, one can find $\alpha_{\mu 1} \approx -0.012$. These experimental values of $\alpha_{\mu 0}$ and $\alpha_{\mu 1}$ are also in agreement with the values obtained from simulations of the device with the same aspect ratio.

One sample (sample No 1) was also biased to verify its operation as a temperature sensor. The results of this test are shown in Fig. 9. They confirmed that the circuit biased for a positive slope of $V_{\rm out}$ temperature dependence becomes a linear temperature sensor. This issue is not pursued further in this paper.

VI. Discussion and Conclusions

The design of MOS circuits for operation in a wide range of temperatures requires exact knowledge of temperature behavior of two important parameters, namely, threshold voltage and mobility. The threshold voltage temperature dependence is better known, in addition the existing circuits of threshold extractors (a list of references can be found in [19]) allows one to measure this dependence in practical circuits. The exact temperature dependence of mobility is less investigated, and the design exercise of the voltage reference circuit described in this paper provides a possible approach to better describe temperature dependence of mobility.

When a CMOS technology shows the presence of ZTC point, then the proposed approach may provide a new family of voltage reference circuits or, at least, can be used for temperature stabilization of bias currents and voltages.

The developed theory shows that the temperature behavior of transconductance characteristics in the vicinity of ZTC point allows one to design simple temperature sensors with linear dependence of the sensor voltage versus temperature.

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