Instruction Set Summary

Instr	Addressing Mode	Assembler Format	Operation	Op Code Hex	Op Code Dec	Bytes	Clock Cycles	Status Register - P (N V D I Z C)	Instr
ADC	Immediate	ADC #oper	.A + # + C → .A, C	69	105	2	2		**ADC**
	Zero Page	ADC addr	.A + [addr] + C → .A, C	65	101	2	3	✓ ✓ - - ✓ ✓	
	Zero Page, X	ADC addr, X	.A + [addr + .X] + C → .A, C	75	117	2	4		
	Absolute	ADC ADDR	.A + [ADDR] + C → .A, C	6D	109	3	4		
	Absolute, X	ADC ADDR, X	.A + [ADDR + .X] + C → .A, C	7D	125	3	4*		
	Absolute, Y	ADC ADDR, Y	.A + [ADDR + .Y] + C → .A, C	79	121	3	4*		
	(Indirect, X)	ADC (addr, X)	.A + [[addr + .X + 1, addr + .X]] + C → .A, C	61	97	2	6		
	(Indirect),Y	ADC (addr),Y	.A + [[addr + 1, addr] + .Y] + C → .A, C	71	113	2	5*		
AND	Immediate	AND #oper	.A ∩ # → .A	29	41	2	2		**AND**
	Zero Page	AND addr	.A ∩ [addr] → .A	25	37	2	3	✓ - - - ✓ -	
	Zero Page, X	AND addr, X	.A ∩ [addr + .X] → .A	35	53	2	4		
	Absolute	AND ADDR	.A ∩ [ADDR] → .A	2D	45	3	4		
	Absolute, X	AND ADDR, X	.A ∩ [ADDR + .X] → .A	3D	61	3	4*		
	Absolute, Y	AND ADDR, Y	.A ∩ [ADDR + .Y] → .A	39	57	3	4*		
	(Indirect, X)	AND (addr, X)	.A ∩ [[addr + .X + 1, addr + .X]] → .A	21	33	2	6		
	(Indirect),Y	AND (addr),Y	.A ∩ [[addr + 1, addr] + .Y] → .A	31	49	2	5*		
ASL	Accumulator	ASL A	.A (←) → .A ; 0 → bit 0, bit7 → C	0A	10	1	2	N V D I Z C	**ASL**
	Zero Page	ASL addr	[addr] (←) → [addr] "	06	6	2	5	✓ - - - ✓ ✓	
	Zero Page, X	ASL addr, X	[addr + .X] (←) → [addr + .X] "	16	22	2	6		
	Absolute	ASL ADDR	[ADDR] (←) → [ADDR] "	0E	14	3	6		
	Absolute, X	ASL ADDR, X	[ADDR + .X] (←) → [ADDR + .X] "	1E	30	3	7		
BCC	Relative	BCC oper	Branch on C = 0	90	144	2	2*	N V D I Z C	**BCC**
BCS	Relative	BCS oper	Branch on C = 1	B0	176	2	2*	- - - - - -	**BCS**
BEQ	Relative	BEQ oper	Branch on Z = 1	F0	240	2	2*	All Branches	**BEQ**
BNE	Relative	BNE oper	Branch on Z = 0	D0	208	2	2*	* - Add 1 if branch to same page	**BNE**
BMI	Relative	BMI oper	Branch on N = 1	30	48	2	2*	* - Add 2 if branch to diff page	**BMI**
BPL	Relative	BPL oper	Branch on N = 0	10	16	2	2*		**BPL**
BVS	Relative	BVS oper	Branch on V = 1	70	112	2	2*		**BVS**
BVC	Relative	BVC oper	Branch on V = 0	50	80	2	2*		**BVC**
BIT	Zero Page	BIT addr	.A ∩ [addr] ; bit7 → N, bit6 → V	24	36	2	3	N V D I Z C	**BIT**
	Absolute	BIT ADDR	.A ∩ [ADDR] "	2C	44	3	4	b_7 b_6 - - ✓ -	
BRK	Implied	BRK 1→B flag	PC + 2 ↓ P ↓, [FFFE]→PCL, [FFFF]→PCH	00	0	1	7	- - - 1 - -	**BRK**
CLC	Implied	CLC	0→C	18	24	1	2	N V D I Z C	**CLC**
CLD	Implied	CLD	0→D	D8	216	1	2	- - - - - 0	**CLD**
CLI	Implied	CLI	0→I	58	88	1	2	- - 0 - - -	**CLI**
CLV	Implied	CLV	0→V	B8	184	1	2	- - - 0 - -	**CLV**
								- 0 - - - -	
CMP	Immediate	CMP #oper	.A - #	C9	201	2	2	N V D I Z C	**CMP**
	Zero Page	CMP addr	.A - [addr]	C5	197	2	3	✓ - - - ✓ ✓	
	Zero Page, X	CMP addr, X	.A - [addr + .X]	D5	213	2	4		
	Absolute	CMP ADDR	.A - [ADDR]	CD	205	3	4		
	Absolute, X	CMP ADDR, X	.A - [ADDR + .X]	DD	221	3	4*		
	Absolute, Y	CMP ADDR, Y	.A - [ADDR + .Y]	D9	217	3	4*		
	(Indirect, X)	CMP (addr, X)	.A - [[addr + .X + 1, addr + .X]]	C1	193	2	6		
	(Indirect),Y	CMP (addr),Y	.A - [[addr + 1, addr] + .Y]	D1	209	2	5*		
CPX	Immediate	CPX #oper	.X - #	E0	224	2	2	N V D I Z C	**CPX**
	Zero Page	CPX addr	.X - [addr]	E4	228	2	3	✓ - - - ✓ ✓	
	Absolute	CPX ADDR	.X - [ADDR]	EC	236	3	4		
CPY	Immediate	CPY #oper	.Y - #	C0	192	2	2	N V D I Z C	**CPY**
	Zero Page	CPY addr	.Y - [addr]	C4	196	2	3	✓ - - - ✓ ✓	
	Absolute	CPY ADDR	.Y - [ADDR]	CC	204	3	4		
DEC	Zero Page	DEC addr	[addr] - 1 → [addr]	C6	198	2	5	N V D I Z C	**DEC**
	Zero Page, X	DEC addr, X	[addr + .X] - 1 → [addr + .X]	D6	214	2	6	✓ - - - ✓ -	
	Absolute	DEC ADDR	[ADDR] - 1 → [ADDR]	CE	206	3	6		
	Absolute, X	DEC ADDR, X	[ADDR + .X] - 1 → [ADDR + .X]	DE	222	3	7		
DEX	Implied	DEX	.X - 1 → .X	CA	202	1	2	N V D I Z C	**DEX**
DEY	Implied	DEY	.Y - 1 → .Y	88	136	1	2	✓ - - - ✓ -	**DEY**
EOR	Immediate	EOR #oper	.A ⊎ # → .A	49	73	2	2	N V D I Z C	**EOR**
	Zero Page	EOR addr	.A ⊎ [addr] → .A	45	69	2	3	✓ - - - ✓ -	
	Zero Page, X	EOR addr, X	.A ⊎ [addr + .X] → .A	55	85	2	4		
	Absolute	EOR ADDR	.A ⊎ [ADDR] → .A	4D	77	3	4		
	Absolute, X	EOR ADDR, X	.A ⊎ [ADDR + .X] → .A	5D	93	3	4*		
	Absolute, Y	EOR ADDR, Y	.A ⊎ [ADDR + .Y] → .A	59	89	3	4*		
	(Indirect, X)	EOR (addr, X)	.A ⊎ [[addr + .X + 1, addr + .X]] → .A	41	65	2	6		
	(Indirect),Y	EOR (addr),Y	.A ⊎ [[addr + 1, addr] + .Y] → .A	51	81	2	5*		
INC	Zero Page	INC addr	[addr] + 1 → [addr]	E6	230	2	5	N V D I Z C	**INC**
	Zero Page, X	INC addr, X	[addr + .X] + 1 → [addr + .X]	F6	246	2	6	✓ - - - ✓ -	
	Absolute	INC ADDR	[ADDR] + 1 → [ADDR]	EE	238	3	6		
	Absolute, X	INC ADDR, X	[ADDR + .X] + 1 → [ADDR + .X]	FE	254	3	7		
INX	Implied	INX	.X + 1 → .X	E8	232	1	2	N V D I Z C	**INX**
INY	Implied	INY	.Y + 1 → .Y	C8	200	1	2	✓ - - - ✓ -	**INY**
JMP	Absolute	JMP ADDR	[PC + 1] → PCL, [PC + 2] → PCH	4C	76	3	3	N V D I Z C	**JMP**
	Indirect	JMP (ADDR)	[ADDR] → PCL, [ADDR + 1] → PCH	6C	108	3	5	- - - - - -	
JSR	Absolute	JSR ADDR	PC + 2 ↓, [PC + 1] → PCL, [PC + 2] → PCH	20	32	3	6		**JSR**