Instr	Addressing Mode	Assembler Format	Operation	Op Code Hex	Op Code Dec	Bytes	Clock Cycles	Status Register - P N V D I Z C	Instr
LDA	Immediate	LDA #oper	# → .A	A9	169	2	2		**LDA**
	Zero Page	LDA addr	[addr] → .A	A5	165	2	3	✓ – – – ✓ –	
	Zero Page, X	LDA addr, X	[addr + .X] → .A	B5	181	2	4		
	Absolute	LDA ADDR	[ADDR] → .A	AD	173	3	4		
	Absolute, X	LDA ADDR, X	[ADDR + .X] → .A	BD	189	3	4*		
	Absolute, Y	LDA ADDR, Y	[ADDR + .Y] → .A	B9	185	3	4*		
	(Indirect, X)	LDA (addr, X)	[[addr + .X + 1, addr + .X]] → .A	A1	161	2	6		
	(Indirect),Y	LDA (addr),Y	[[addr + 1, addr] + .Y] → .A	B1	177	2	5*		
LDX	Immediate	LDX #oper	# → .X	A2	162	2	2		**LDX**
	Zero Page	LDX addr	[addr] → .X	A6	166	2	3	✓ – – – ✓ –	
	Zero Page, Y	LDX addr, Y	[addr + .Y] → .X	B6	182	2	4		
	Absolute	LDX ADDR	[ADDR] → .X	AE	174	3	4		
	Absolute, Y	LDX ADDR, Y	[ADDR + .Y] → .X	BE	190	3	4*		
LDY	Immediate	LDY #oper	# → .Y	A0	160	2	2		**LDY**
	Zero Page	LDY addr	[addr] → .Y	A4	164	2	3	✓ – – – ✓ –	
	Zero Page, X	LDY addr, X	[addr + .X] → .Y	B4	180	2	4		
	Absolute	LDY ADDR	[ADDR] → .Y	AC	172	3	4		
	Absolute, X	LDY ADDR, X	[ADDR + .X] → .Y	BC	188	3	4*		
LSR	Accumulator	LSR A	.A (→) → .A ; 0→bit7, bit0→C	4A	74	1	2		**LSR**
	Zero Page	LSR addr	[addr] (→) → [addr] "	46	70	2	5	0 – – – ✓ ✓	
	Zero Page, X	LSR addr, Y	[addr + .X] (→) → [addr + .X] "	56	86	2	6		
	Absolute	LSR ADDR	[ADDR] (→) → [ADDR] "	4E	78	3	6		
	Absolute, X	LSR ADDR, X	[ADDR + .X] (→) → [ADDR + .X] "	5E	94	3	7		
NOP	Implied	NOP	No OPeration	EA	234	1	2	– – – – – –	**NOP**
ORA	Immediate	ORA #oper	.A ∪ # → .A	09	9	2	2		**ORA**
	Zero Page	ORA addr	.A ∪ [addr] → .A	05	5	2	3	✓ – – – ✓ –	
	Zero Page, X	ORA addr, X	.A ∪ [addr + .X] → .A	15	21	2	4		
	Absolute	ORA ADDR	.A ∪ [ADDR] → .A	0D	13	3	4		
	Absolute, X	ORA ADDR, X	.A ∪ [ADDR + .X] → .A	1D	29	3	4*		
	Absolute, Y	ORA ADDR, Y	.A ∪ [ADDR + .Y] → .A	19	25	3	4*		
	(Indirect, X)	ORA (addr, X)	.A ∪ [[addr + .X + 1, addr + .X]] → .A	0i	1	2	6		
	(Indirect),Y	ORA (addr),Y	.A ∪ [[addr + 1, addr] + .Y] → .A	11	17	2	5*		
PHA	Implied	PHA	.A ↓, SP – 1 → SP	48	72	1	3		**PHA**
PLA	Implied	PLA	.A ↑, SP + 1 → SP	68	104	1	4	– – – – – –	**PLA**
PHP	Implied	PHP	.P ↓, SP – 1 → SP	08	8	1	3	All Push/Pulls xcpt PLP	**PHP**
PLP	Implied	PLP	.P ↑, SP + 1 → SP	28	40	1	4	from stack	**PLP**
ROL	Accumulator	ROL A	.A (←) → .A ; C→bit0, bit7→C	2A	42	1	2		**ROL**
	Zero Page	ROL addr	[addr] (←) → [addr] "	26	38	2	5	✓ – – – ✓ ✓	
	Zero Page, X	ROL addr, X	[addr + .X] (←) → [addr + .X] "	36	54	2	6		
	Absolute	ROL ADDR	[ADDR] (←) → [ADDR] "	2E	46	3	6		
	Absolute, X	ROL ADDR, X	[ADDR + .X] (←) → [ADDR + .X] "	3E	62	3	7		
ROR	Accumulator	ROR A	.A (→) → .A ; C→bit7, bit0→C	6A	106	1	2		**ROR**
	Zero Page	ROR addr	[addr] (→) → [addr] "	66	102	2	5	✓ – – – ✓ ✓	
	Zero Page, X	ROR addr, Y	[addr + .X] (→) → [addr + .X] "	76	118	2	6		
	Absolute	ROR ADDR	[ADDR] (→) → [ADDR] "	6E	110	3	6		
	Absolute, X	ROR ADDR, X	[ADDR + .X] (→) → [ADDR + .X] "	7E	126	3	7		
RTI	Implied	RTI	P ↑, PC ↑, SP + 3 → SP, PC + 1 → PC	40	64	1	6	from stack	**RTI**
RTS	Implied	RTS	PC ↑, SP + 2 → SP, PC + 1 → PC	60	96	1	6	– – – – – –	**RTS**
SBC	Immediate	SBC #oper	.A – # – C̄ → .A, C C̄ = Borrow	E9	233	2	2		**SBC**
	Zero Page	SBC addr	.A – [addr] – C̄ → .A, C	E5	229	2	3	✓ ✓ – – ✓ ✓	
	Zero Page, X	SBC addr, X	.A – [addr + .X] – C̄ → .A, C	F5	245	2	4		
	Absolute	SBC ADDR	.A – [ADDR] – C̄ → .A, C	ED	237	3	4		
	Absolute, X	SBC ADDR, X	.A – [ADDR + .X] – C̄ → .A, C	FD	253	3	4*		
	Absolute, Y	SBC ADDR, Y	.A – [ADDR + .Y] – C̄ → .A, C	F9	249	3	4*		
	(Indirect, X)	SBC (addr, X)	.A – [[addr + .X + 1, addr + .X]] – C̄ → .A, C	E1	225	2	6		
	(Indirect),Y	SBC (addr),Y	.A – [[addr + 1, addr] + .Y] – C̄ → .A, C	F1	241	2	5*		
SEC	Implied	SEC	1→C	38	56	1	2		**SEC**
SED	Implied	SED	1→D	F8	248	1	2	– – – – – 1	**SED**
SEI	Implied	SEI	1→I	78	120	1	2	– – 1 – – –	**SEI**
STA	Zero Page	STA addr	.A → [addr]	85	133	2	3	– – – 1 – –	**STA**
	Zero Page, X	STA addr, X	.A → [addr + .X]	95	149	2	4		
	Absolute	STA ADDR	.A → [ADDR]	8D	141	3	4		
	Absolute, X	STA ADDR, X	.A → [ADDR + .X]	9D	157	3	5		
	Absolute, Y	STA ADDR, Y	.A → [ADDR + .Y]	99	153	3	5		
	(Indirect, X)	STA (addr, X)	.A → [[addr + .X + 1, addr + .X]]	81	129	2	6		
	(Indirect),Y	STA (addr),Y	.A → [[addr + 1, addr] + .Y]	91	145	2	6		
STX	Zero Page	STX addr	.X → [addr]	86	134	2	3		**STX**
	Zero Page, Y	STX addr, Y	.X → [addr + .Y]	96	150	2	4	– – – – – –	
	Absolute	STX ADDR	.X → [ADDR]	8E	142	3	4		
STY	Zero Page	STY addr	.Y → [addr]	84	132	2	3		**STY**
	Zero Page, X	STY addr, X	.Y → [addr + .X]	94	148	2	4	– – – – – –	
	Absolute	STY ADDR	.Y → [ADDR]	8C	140	3	4		
TAX	Implied	TAX	.A → .X	AA	170	1	2		**TAX**
TXA	Implied	TXA	.X → .A	8A	138	1	2	✓ – – – ✓ –	**TXA**
TAY	Implied	TAY	.A → .Y	A8	168	1	2		**TAY**
TYA	Implied	TYA	.Y → .A	98	152	1	2	All Transfers xcpt TXS	**TYA**
TSX	Implied	TSX	SP → .X	BA	186	1	2		**TSX**
TXS	Implied	TXS	.X → SP	9A	154	1	2	– – – – – –	**TXS**