D	A	Task Mode	Task Name				Duration	Start	Finish	, 2018 5	3 8 11 14 17 20 23
1	•	Node	Initial Res	search			33 days	Mon 1/8/18	Wed 2/21/18	5	8 11 14 17 20 23
2		*	Arduin	o Research			33 days	Mon 1/8/18	Wed 2/21/18		
3		*	FPGA R	esearch			21 days	Wed 1/24/18	Wed 2/21/18		
4		*	Rese	arch Xilinx FPGAs			19 days	Wed 1/24/18	Sun 2/18/18		
5		*	Rese	earch Microsemiconductor FPGAs			19 days	Wed 1/24/18	Sun 2/18/18		
6		*	Rese	earch Lattice FPGAs			19 days	Wed 1/24/18	Sun 2/18/18		
7		*	Rese	earch Intel FPGAs			19 days	Wed 1/24/18	Sun 2/18/18		
8		*		Compare and choose FPGA for project (deper on success of prototype)			3 days	Mon 2/19/18	Wed 2/21/18		
9		*	Resrea	Resreach possible development boards			4 days	Mon 1/22/18	Thu 1/25/18		
10		*	Initial s	Initial software research				Fri 1/26/18	Wed 2/21/18		
11		*	Initial p	Initial popular AES algorithm research				Fri 2/2/18	Wed 2/21/18		
12		*	Detailed I	Detailed Research				Fri 2/9/18	Fri 3/30/18		
13		*	Develo	pment Board Researd		27 days	Fri 2/9/18	Mon 3/19/18			
14		*	Rese	esearch documentation on the Mojo v3			11 days	Fri 2/9/18	Fri 2/23/18		
15		*	Research documentation on the Papilio One 250k				11 days	Fri 2/9/18	Fri 2/23/18		
16		*	Rese	arch documentation	on the PulseRain M	110	11 days	Fri 2/23/18	Fri 3/9/18		
17		*	Choo	se a development bo	ard for prototypin	g	2 days	Fri 3/16/18	Mon 3/19/18		
18		-5	Specific	Software and Crypto	Resreach		28 days	Wed 2/21/18	Fri 3/30/18		
19		*	Cryp	tol software SAW soft	ware research		13 days	Wed 2/21/18	Fri 3/9/18		
20		*	Read	l Cryptol documentati	on		28 days	Wed 2/21/18	Fri 3/30/18		
21		-5	Develop F	irst Two Algorithms			53 days	Wed 2/21/18	Fri 5/4/18		
				Task		Inactive S	Summary		External Tasks		
				Split		Manual T	ask		External Milestor	ne	\Diamond
				Milestone	◆ Durat		-only		Deadline		•
	Project: Reconfigurable_Arduin Date: Tue 4/10/18			_Arduin Summary		Manual S	ummary Rollup		Progress		
Date.	rue 4	, 10/10				Manual Summary			Manual Progress		
				Inactive Task		Start-only	/	С	-		
				Inactive Milestone		Finish-on		3			
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)	0	Task Mode	Task Name				Duration	Start	Finish	/ 2018 5 8 11 14 17 20	
22		*		Resreach AES algorithm (1st Choosen Cryptogr Algorithm)			13 days	Wed 2/21/18	Fri 3/9/18		
23		*		Resreach SHA algorithm (2nd Algorithm)	•	nd Choosen Cryptog	raphic	13 days	Wed 2/21/18	Fri 3/9/18	
24		*	Run fur	nctions provided in A	AES-128 cryptograph	nic file	12 days	Fri 3/9/18	Sun 3/25/18		
25		*	Run fur	nctions provided in S	12 days	Fri 3/9/18	Sun 3/25/18				
26		- 5	Testing	& Prototype			31 days	Fri 3/23/18	Fri 5/4/18		
27		-	AES-	128 Testing & Proto	type		16 days	Fri 3/23/18	Sun 4/15/18		
28		*	Cr	eate benchmark for	the AES-128 c file		6 days	Fri 3/23/18	Fri 3/30/18		
29		*	Te	st AES-128 benchm	ark		6 days	Sat 3/31/18	Fri 4/6/18		
30		*	Up	oload the benchmar	k AES-128 to the Arc	oniuk	2 days	Fri 4/6/18	Sun 4/8/18		
31		*		Upload the benchmark AES-128 to a Developmen Board				Mon 4/9/18	Fri 4/13/18		
32		*	Cr	Create benchmark for the AES-128 verilog file				Mon 4/2/18	Fri 4/6/18		
33		*	Ge	Generate bitstream for the AES-128				Fri 4/6/18	Wed 4/11/18		
34		*	Up	Upload AES-128 bitstream to a FPGA board				Thu 4/12/18	Sun 4/15/18		
35		7?	Te	Test the AES-128 algorithm on the FPGA board							
36		-5	SHA-	1 Testing & Prototy	ре		10 days	Mon 4/16/18	Sun 4/29/18		
37		*	Cr	eate benchmark for	the SHA-1 c file		3 days	Mon 4/16/18	Wed 4/18/18		
38		*	Te	st SHA-1 benchmar	<		3 days	Wed 4/18/18	Fri 4/20/18		
39		*	Up	oload the benchmar	k SHA-1 to the Ardu	ino	2 days	Fri 4/20/18	Sun 4/22/18		
				Task		Inactive S	Summary		External Tasks		
				Split		Manual Ta	•		External Mileston	ne ♦	
				Milestone	♦	Duration-			Deadline	•	
-		_	ble_Arduin	Summary			Summary Rollup		Progress		
Jate:	rue 4	/10/18		Project Summary		Manual S	•		Manual Progress		
				Inactive Task		Start-only	•	Е	19 000		
				Inactive Milestone		Finish-onl	•	3			

D	0	Task Mode	Task Name				Duration	Start	Finish	, 2018 5		11 14	17	20	23
40		*		oload the benchmarl pard	SHA-1 to a Develo	pment	4 days	Sun 4/22/18	Wed 4/25/18						
41		*	Cr	eate benchmark for	the SHA-1 verilog fi	le	3 days	Fri 4/20/18	Tue 4/24/18						
42		*	Ge	enerate bitstream fo	2 days	Wed 4/25/18	Thu 4/26/18								
43		*	U	oload SHA-1 bitstrea	m to a FPGA board		2 days	Thu 4/26/18	Fri 4/27/18						
44		*	Te	st the SHA-1 algorithm on the FPGA board			2 days	Fri 4/27/18	Sun 4/29/18						
45		*	Chec	k benchmarks with sponser			5 days	Mon 4/30/18	Fri 5/4/18						
46		-	Develop I	Next Two Algorithms	s		1 day	Fri 2/9/18	Fri 2/9/18						
47		*?	Resrea	Resreach choosen asymmetic cryptographic algorithm											
48		*?	Resrea	ch random number g	generator algorithm										
49		**	Run asy NaCl (S	ymmetric algoritm p alt)	rovided or choosen										
50		*?		Run random number generator algorithm provided or choosen from NaCl											
51		-5	Benchma	rk & Test Next Two	1 day	Fri 2/9/18	Fri 2/9/18								
52		-5	C Progi	gramming			1 day	Fri 2/9/18	Fri 2/9/18						
53		*?		Create benchmark for the asymmetric cryptographic algorithm											
54		*?		te benchmark for the	e random number g	enerator									
55		**	Test	the benchmark asyn	nmetric cryptograph	nic									
56		*?		the benchmark rand	lom generator algor	ithm									
				Task		Inactive S	ummary		External Tasks						
				Split		Manual Ta	ask		External Mileston	ne	\Diamond				
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				Inactive Task		Start-only		Е							
				Inactive Milestone		Finish-onl		3							

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~?		oad the benchmark a rithm to the Arduino		aphic							
*?		oad the benchmark ra rithm to the Arduino	•	erator							
*?				aphic							
*?											
-5	Verilog	g Programming			1 day	Fri 2/9/18	Fri 2/9/18				
Create benchmark for the rando algorithm verilog file				generator							
*?		Generate bitstream for the asymmetric cyrptographic algorithm Generate bitstream for the random number generator algorithm									
*?											
*?			cryptographic algori	thm to							
**			ber generator algor	ithm to							
**			n on the								
*?			r generator algorithi	m on the							
		Task		Inactive S	ummary		External Tasks				_
		Split		Manual Ta	ask		External Milestor	ne	\Diamond		
Reconfic	aurable Arduin	Milestone	♦ Duration		only		Deadline		•		
_		Summary		Manual Su	ummary Rollup		Progress			-	
	- -	Project Summary		Manual Su	ummary		Manual Progress			-	
		Inactive Task		Start-only		Е					
		Inactive Milestone		Finish-onl	у	3					
	An A	Uplo algo Uplo algo Verilog Verilog Verilog Crea algo Crea algo Crea algo Crea algo Cyrp Gene cyrp Uplo the I	Upload the benchmark a algorithm to the Developm Upload the benchmark ralgorithm to a Developm Verilog Programming Create benchmark for the algorithm verilog file Create benchmark for the algorithm verilog file Generate bitstream for the cyrptographic algorithm Generate bitstream for the generator algorithm Upload the asymmetric of the FPGA Upload the random number FPGA Test the asymmetric cryptographic algorithm Task Split Milestone Summary Project Summary Inactive Task	Upload the benchmark random number gen algorithm to a Development Board Verilog Programming Create benchmark for the asymmetric crypticalgorithm verilog file Create benchmark for the random number galgorithm verilog file Generate bitstream for the asymmetric cryptographic algorithm Generate bitstream for the random number generator algorithm Upload the asymmetric cryptographic algorithe FPGA Upload the random number generator algorithe FPGA Test the asymmetric cryptographic algorithm FPGA Test the random number generator algorithm FPGA Task Split Milestone Summary Project Summary Inactive Task	Upload the benchmark asymmetric cryptographic algorithm to the Development Board Upload the benchmark random number generator algorithm to a Development Board Verilog Programming Create benchmark for the asymmetric cryptographic algorithm verilog file Create benchmark for the random number generator algorithm verilog file Generate bitstream for the asymmetric cyrptographic algorithm Generate bitstream for the random number generator algorithm Upload the asymmetric cryptographic algorithm to the FPGA Upload the random number generator algorithm to the FPGA Test the asymmetric cryptographic algorithm on the FPGA Test the random number generator algorithm on the FPGA Test the random number generator algorithm on the FPGA Task Split Manual Task Split Millestone Summary Project Summary Inactive Task Inactive Milestone Finish-onl	Upload the benchmark asymmetric cryptographic algorithm to the Development Board Upload the benchmark random number generator algorithm to a Development Board Verilog Programming Create benchmark for the asymmetric cryptographic algorithm verilog file Create benchmark for the random number generator algorithm verilog file Generate bitstream for the asymmetric cryptographic algorithm Generate bitstream for the random number generator algorithm Upload the asymmetric cryptographic algorithm to the FPGA Upload the random number generator algorithm to the FPGA Test the asymmetric cryptographic algorithm on the FPGA Test the random number generator algorithm on the FPGA Test the random number generator algorithm on the FPGA Task Inactive Summary Manual Summary Project Summary Inactive Task Start-only	Upload the benchmark asymmetric cryptographic algorithm to the Development Board Upload the benchmark random number generator algorithm to a Development Board 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