ID	Task Mode	Task Name	Duration	Start	Finish
1		**Initial Research**	**33 days**	**Mon 1/8/18**	**Wed 2/21/18**
2		Arduino Research	33 days	Mon 1/8/18	Wed 2/21/18
3		**FPGA Research**	**21 days**	**Wed 1/24/18**	**Wed 2/21/18**
4		Research Xilinx FPGAs	19 days	Wed 1/24/18	Sun 2/18/18
5		Research Microsemiconductor FPGAs	19 days	Wed 1/24/18	Sun 2/18/18
6		Research Lattice FPGAs	19 days	Wed 1/24/18	Sun 2/18/18
7		Research Intel FPGAs	19 days	Wed 1/24/18	Sun 2/18/18
8		Compare and choose FPGA for project (dependent on success of prototype)	3 days	Mon 2/19/18	Wed 2/21/18
9		Resreach possible development boards	4 days	Mon 1/22/18	Thu 1/25/18
10		Initial software research	19 days	Fri 1/26/18	Wed 2/21/18
11		Initial popular AES algorithm research	14 days	Fri 2/2/18	Wed 2/21/18
12		**Detailed Research**	**36 days**	**Fri 2/9/18**	**Fri 3/30/18**
13		**Development Board Research**	**27 days**	**Fri 2/9/18**	**Mon 3/19/18**
14		Research documentation on the Mojo v3	11 days	Fri 2/9/18	Fri 2/23/18
15		Research documentation on the Papilio One 250k	11 days	Fri 2/9/18	Fri 2/23/18
16		Research documentation on the PulseRain M10	11 days	Fri 2/23/18	Fri 3/9/18
17		Choose a development board for prototyping	2 days	Fri 3/16/18	Mon 3/19/18
18		**Specific Software and Crypto Resreach**	**28 days**	**Wed 2/21/18**	**Fri 3/30/18**
19		Cryptol software SAW software research	13 days	Wed 2/21/18	Fri 3/9/18
20		Read Cryptol documentation	28 days	Wed 2/21/18	Fri 3/30/18
21		**Develop First Two Algorithms**	**53 days**	**Wed 2/21/18**	**Fri 5/4/18**

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Progress
Manual Progress

ID	Task Mode	Task Name	Duration	Start	Finish
22		Resreach AES algorithm (1st Choosen Cryptographic Algorithm)	13 days	Wed 2/21/18	Fri 3/9/18
23		Resreach SHA algorithm (2nd Choosen Cryptographic Algorithm)	13 days	Wed 2/21/18	Fri 3/9/18
24		Run functions provided in AES-128 cryptographic file	12 days	Fri 3/9/18	Sun 3/25/18
25		Run functions provided in SHA-1 cryptographic file	12 days	Fri 3/9/18	Sun 3/25/18
26		**Testing & Prototype**	**31 days**	**Fri 3/23/18**	**Fri 5/4/18**
27		**AES-128 Testing & Prototype**	**16 days**	**Fri 3/23/18**	**Sun 4/15/18**
28		Create benchmark for the AES-128 c file	6 days	Fri 3/23/18	Fri 3/30/18
29		Test AES-128 benchmark	6 days	Sat 3/31/18	Fri 4/6/18
30		Upload the benchmark AES-128 to the Arduino	2 days	Fri 4/6/18	Sun 4/8/18
31		Upload the benchmark AES-128 to a Development Board	5 days	Mon 4/9/18	Fri 4/13/18
32		Create benchmark for the AES-128 verilog file	5 days	Mon 4/2/18	Fri 4/6/18
33		Generate bitstream for the AES-128	4 days	Fri 4/6/18	Wed 4/11/18
34		Upload AES-128 bitstream to a FPGA board	3 days	Thu 4/12/18	Sun 4/15/18
35		Test the AES-128 algorithm on the FPGA board			
36		**SHA-1 Testing & Prototype**	**10 days**	**Mon 4/16/18**	**Sun 4/29/18**
37		Create benchmark for the SHA-1 c file	3 days	Mon 4/16/18	Wed 4/18/18
38		Test SHA-1 benchmark	3 days	Wed 4/18/18	Fri 4/20/18
39		Upload the benchmark SHA-1 to the Arduino	2 days	Fri 4/20/18	Sun 4/22/18

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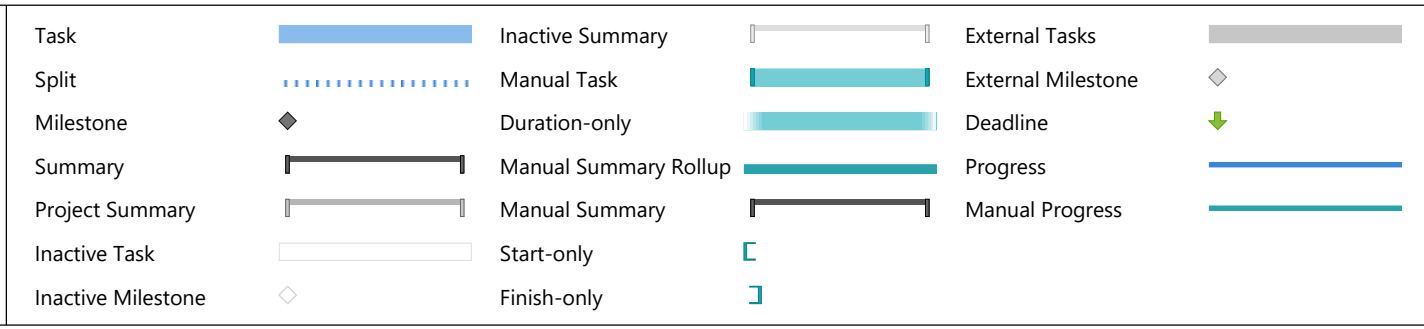
40		Upload the benchmark SHA-1 to a Development Board	4 days	Sun 4/22/18	Wed 4/25/18
41		Create benchmark for the SHA-1 verilog file	3 days	Fri 4/20/18	Tue 4/24/18
42		Generate bitstream for the SHA-1	2 days	Wed 4/25/18	Thu 4/26/18
43		Upload SHA-1 bitstream to a FPGA board	2 days	Thu 4/26/18	Fri 4/27/18
44		Test the SHA-1 algorithm on the FPGA board	2 days	Fri 4/27/18	Sun 4/29/18
45		Check benchmarks with sponser	5 days	Mon 4/30/18	Fri 5/4/18
46		**Develop Next Two Algorithms**	**1 day**	**Fri 2/9/18**	**Fri 2/9/18**
47		Resreach choosen asymmetic cryptographic algorithm			
48		Resreach random number generator algorithm			
49		Run asymmetric algoritm provided or choosen from NaCl (Salt)			
50		Run random number generator algorithm provided or choosen from NaCl			
51		**Benchmark & Test Next Two Algorithms**	**1 day**	**Fri 2/9/18**	**Fri 2/9/18**
52		**C Programming**	**1 day**	**Fri 2/9/18**	**Fri 2/9/18**
53		Create benchmark for the asymmetric cryptographic algorithm			
54		Create benchmark for the random number generator algorithm			
55		Test the benchmark asymmetric cryptographic algorithm			
56		Test the benchmark random generator algorithm			



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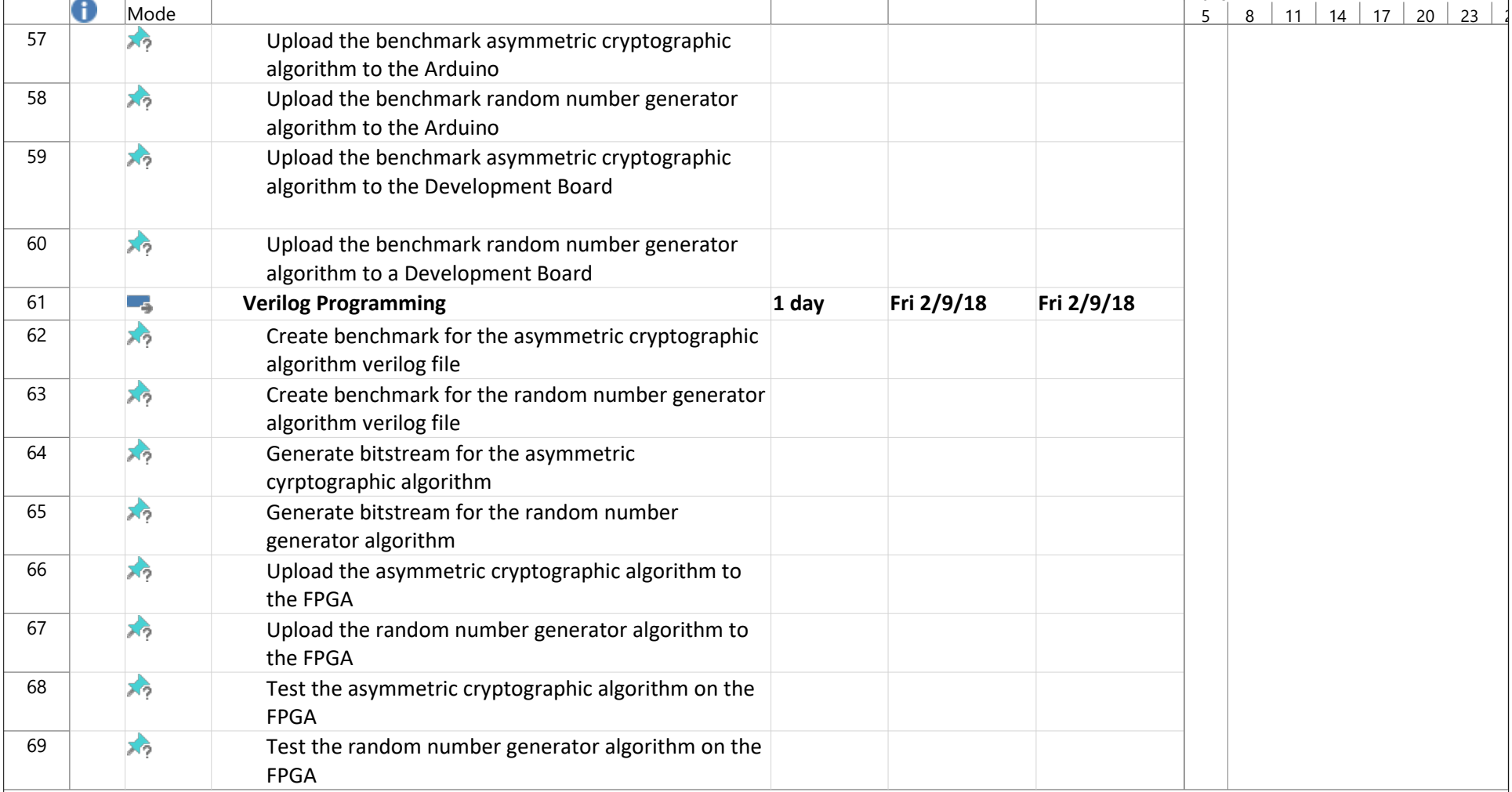
57		Upload the benchmark asymmetric cryptographic algorithm to the Arduino			
58		Upload the benchmark random number generator algorithm to the Arduino			
59		Upload the benchmark asymmetric cryptographic algorithm to the Development Board			
60		Upload the benchmark random number generator algorithm to a Development Board			
61		**Verilog Programming**	**1 day**	**Fri 2/9/18**	**Fri 2/9/18**
62		Create benchmark for the asymmetric cryptographic algorithm verilog file			
63		Create benchmark for the random number generator algorithm verilog file			
64		Generate bitstream for the asymmetric cyrptographic algorithm			
65		Generate bitstream for the random number generator algorithm			
66		Upload the asymmetric cryptographic algorithm to the FPGA			
67		Upload the random number generator algorithm to the FPGA			
68		Test the asymmetric cryptographic algorithm on the FPGA			
69		Test the random number generator algorithm on the FPGA			



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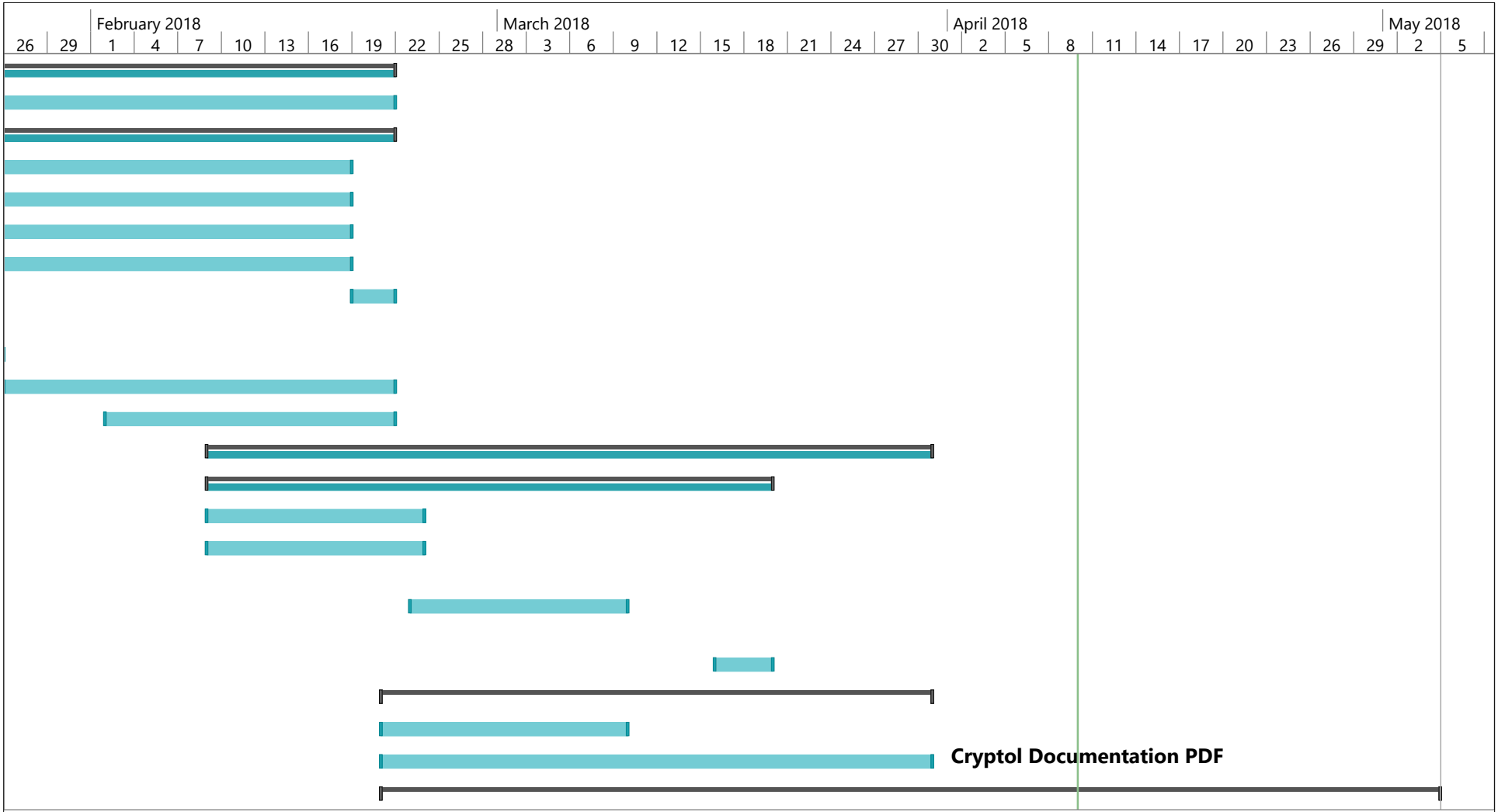

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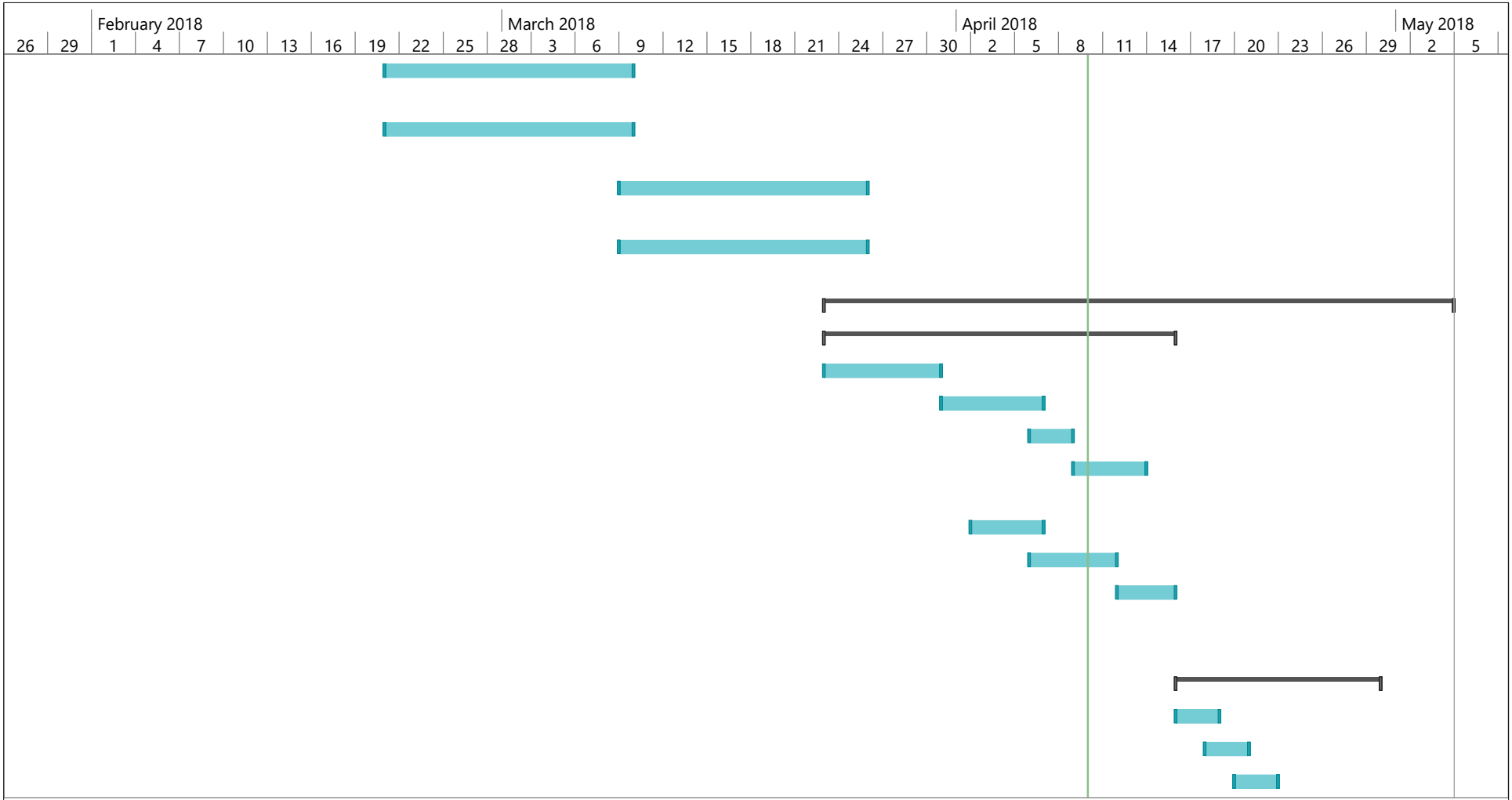

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