

EECS151/251A

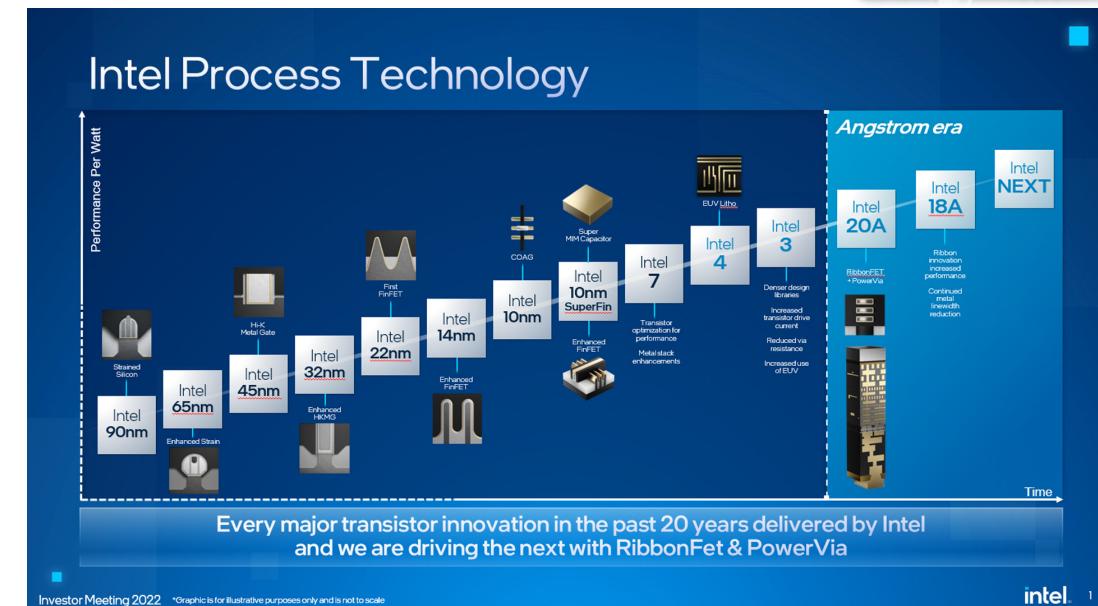
Introduction to Digital Design and ICs

Lecture 13: CMOS Transistors and Gates Sophia Shao



Intel's Process Roadmap to 2025: with 4nm, 3nm, 20A and 18A?!

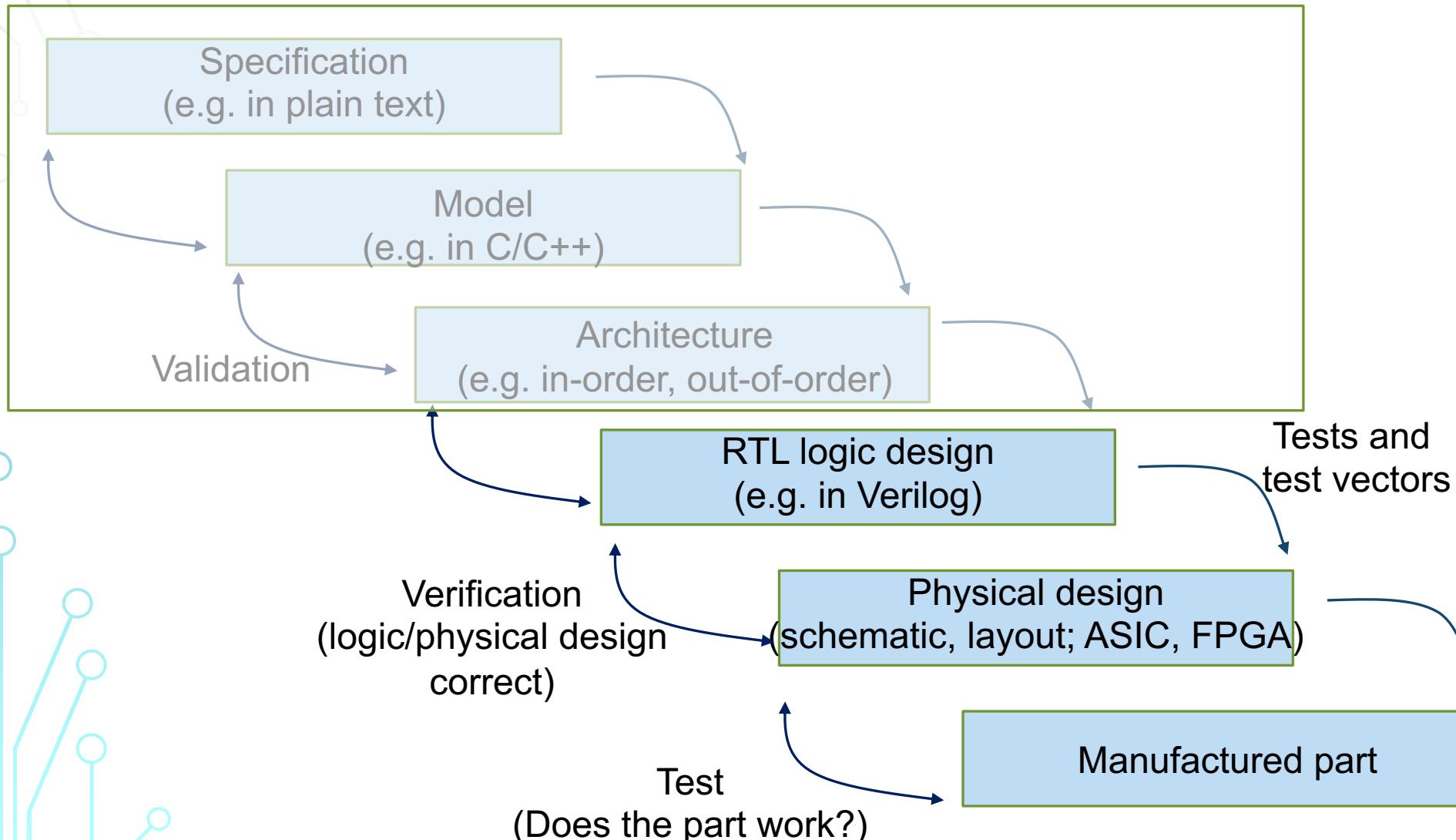
CEO Pat Gelsinger earlier this year stated that Intel would be returning to product leadership in 2025, but hasn't yet explained how this is coming about – that is until today, where Intel has disclosed its roadmap for its next five generations of process node technology leading to 2025. Intel believes it can follow an aggressive strategy to match and pass its foundry rivals, while at the same time developing new packaging offerings and starting a foundry business for external customers. On top of all this, Intel has renamed its process nodes.



<https://www.anandtech.com/show/16823/intel-accelerated-offensive-process-roadmap-updates-to-10nm-7nm-4nm-3nm-20a-18a-packaging-foundry-emib-foveros>

Design Process

- Design through layers of abstractions



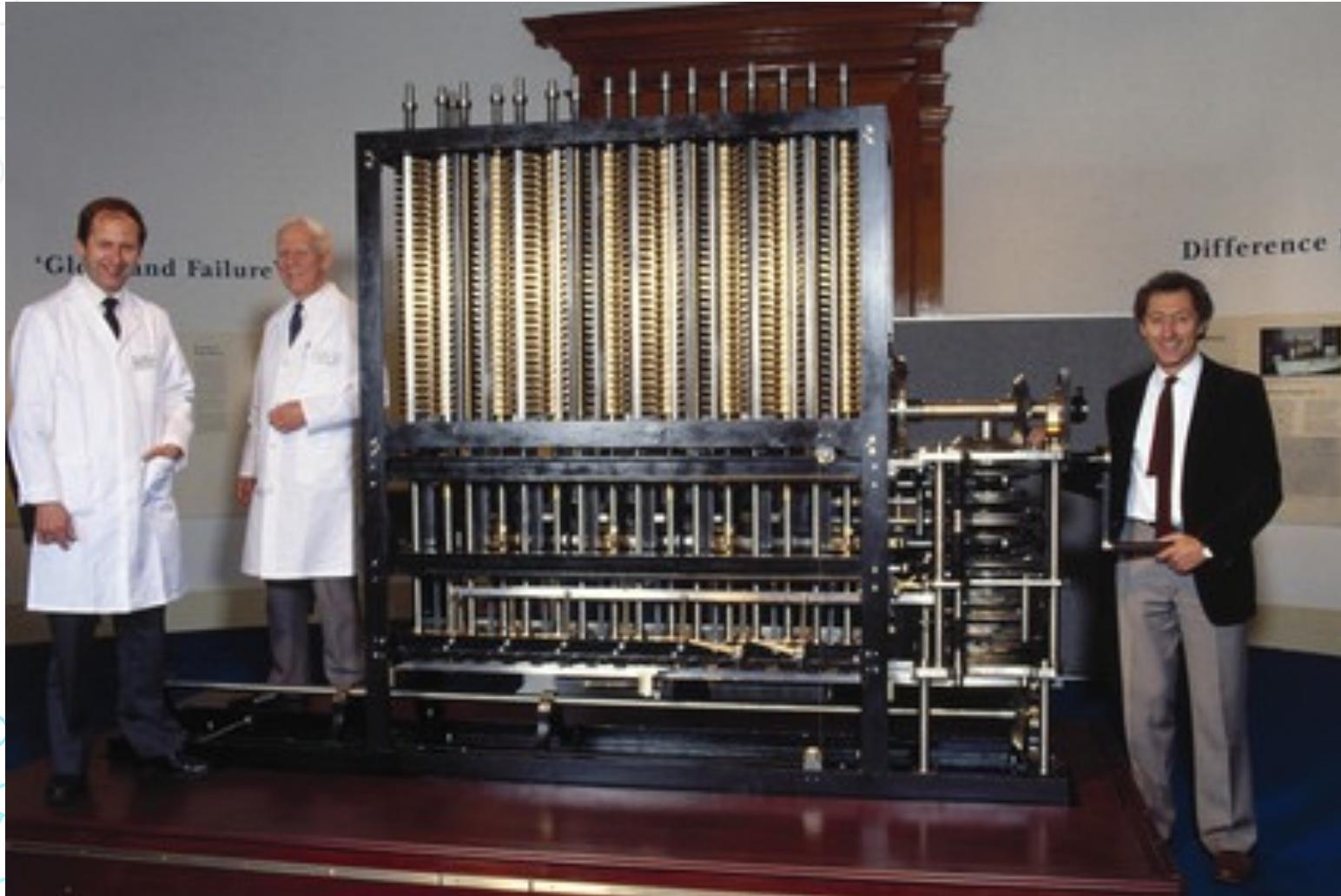
Review

- FPGAs are widely used for hardware prototyping and accelerating key applications.
- Core FPGA building blocks:
 - Configurable Logic Blocks (CLBs)
 - Slices
 - Look-Up Tables
 - FlipFlops
 - Carry chain
 - Configurable Interconnect
 - Switch boxes
- Modern FPGA Designs:
 - BRAMs, DSPs, and AI Engines



- Overview
- CMOS Transistors
 - MOS Transistor as a Switch
 - NMOS & PMOS
- CMOS Gates
 - Inverter
 - Pull-Up and Pull-Down Networks
 - Complex Gates

First Computing Machines Were Mechanical

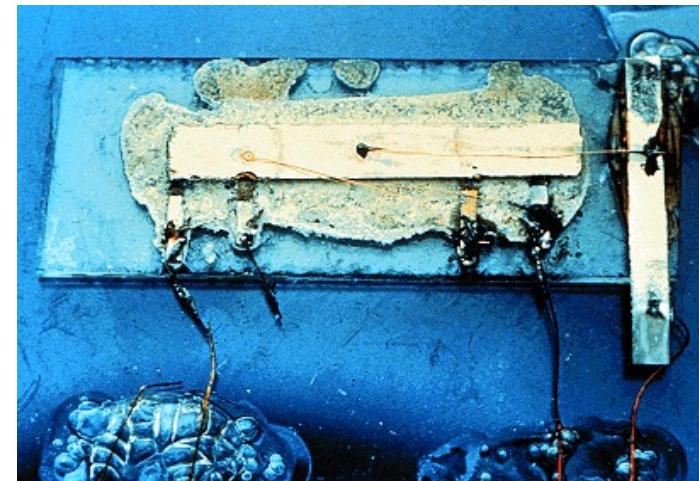


- Babbage Engine (Difference Engine No. 2), built faithfully at the Science Museum in London.
- The Engine consists of 8,000 parts, weighs 5 tons and measures eleven feet long and seven feet high.

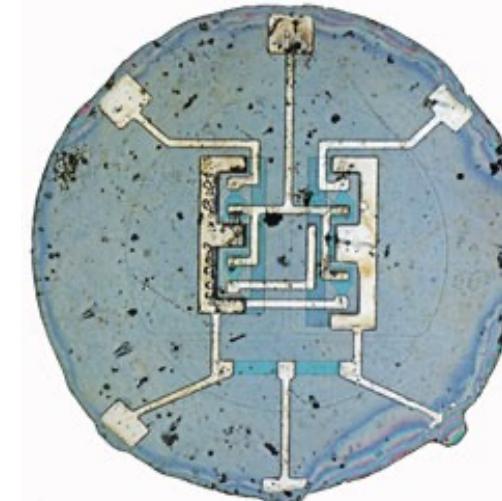
<https://www.computerhistory.org/babbage/>

Instead of Moving Metals, Moving Electrons!

- 1st Transistor: Bell Labs, Dec 1947
- 1st Integrated Circuits (1958-59)



Jack Kilby,
Texas
Instruments



Bob Noyce,
Fairchild

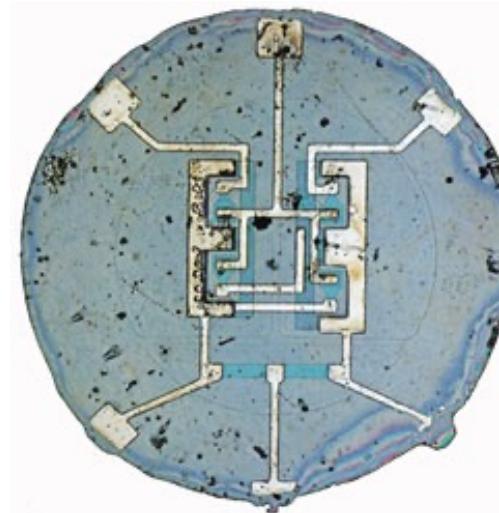
How far we have achieved!

From This



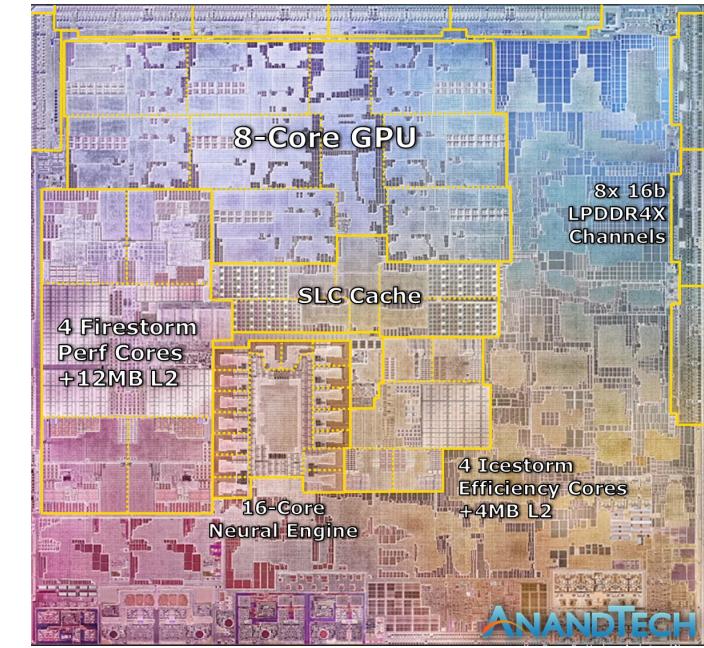
1st Transistor

To This



1st Integrated Circuit

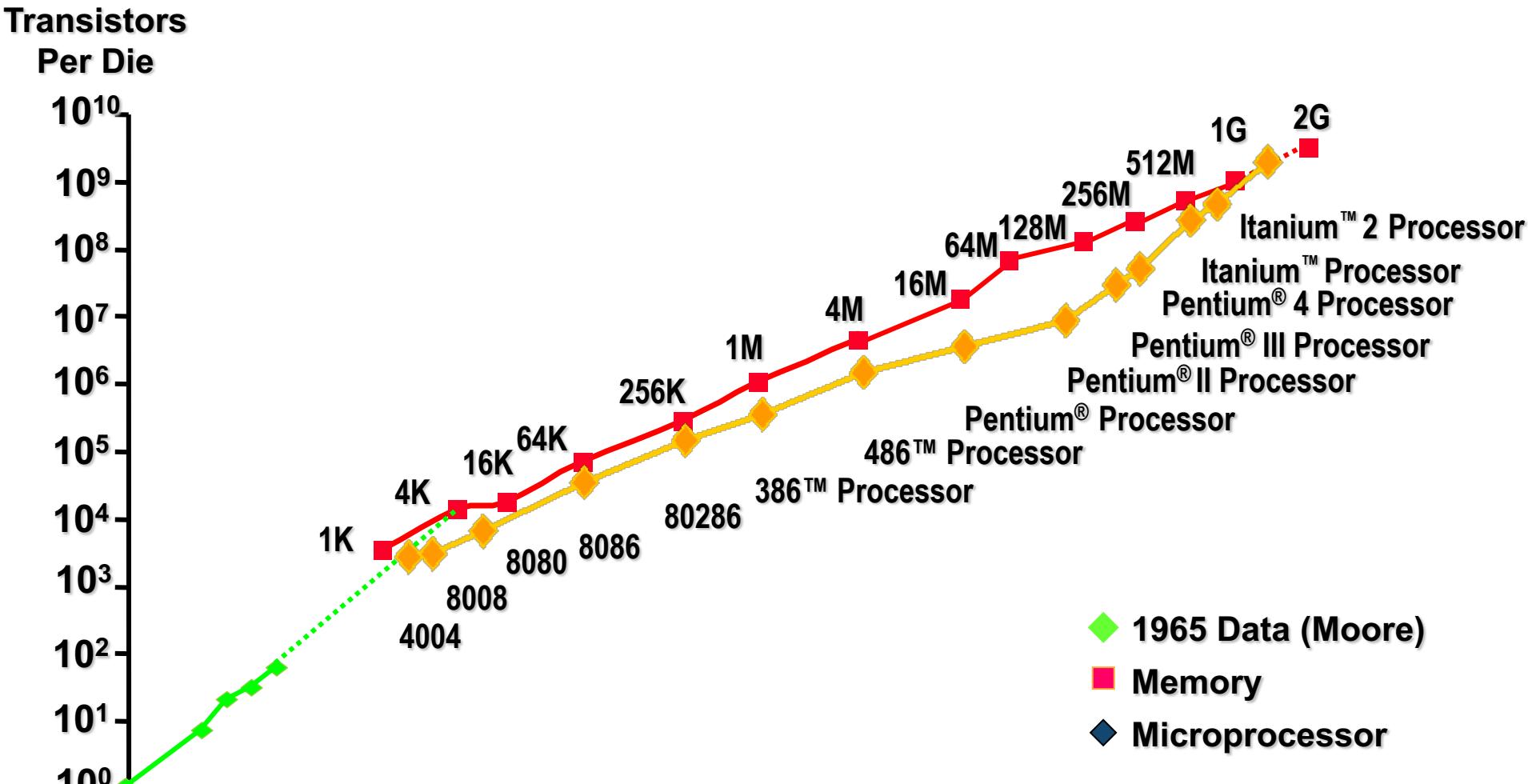
To This



Modern SoC

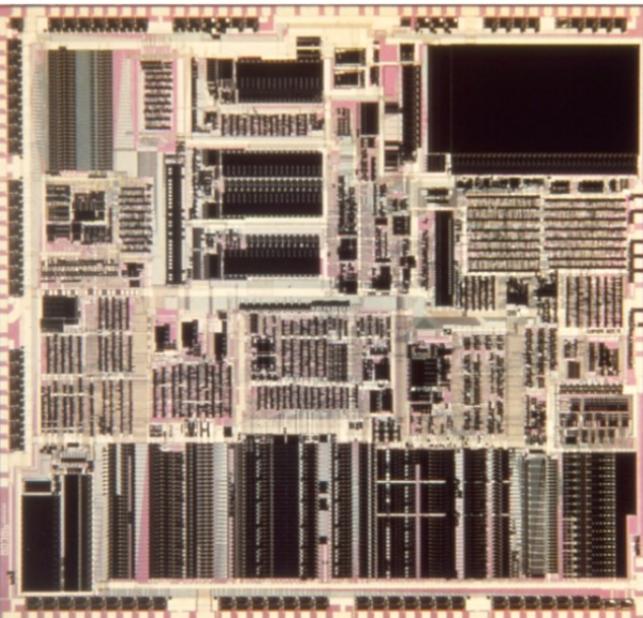
- Modern process can fabricate more than 100 million Transistors / mm²!

Moore's Law



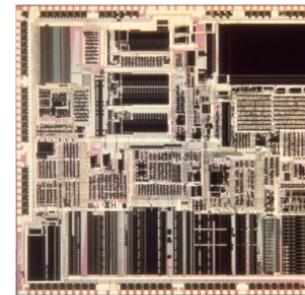
Graph from S.Chou, ISSCC'2005

What this means



1985 (Intel 80386)
275,000 transistors
 104 mm^2 ; 2640 Tr/mm^2

80386 chip area
shrinks to 17 mm^2



80386 die size
shrinks to 0.05 mm^2

Chip edge is only twice the
diameter of a human hair!

1989 (Intel 80486)
1,180,235 transistors
 $16,170 \text{ Tr/mm}^2$

Intel 10 nm CMOS*
circa 2019
 $100,000,000 \text{ Tr/mm}^2$

- ... or the original chip area could contain > 10 billion transistors!

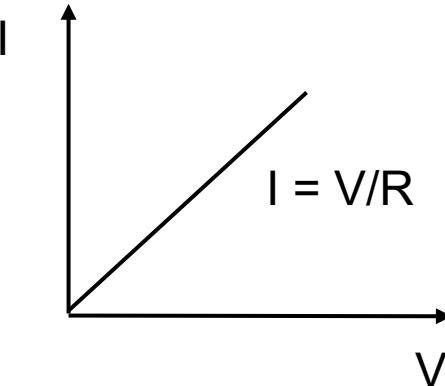
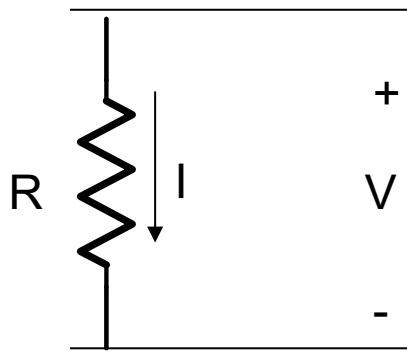


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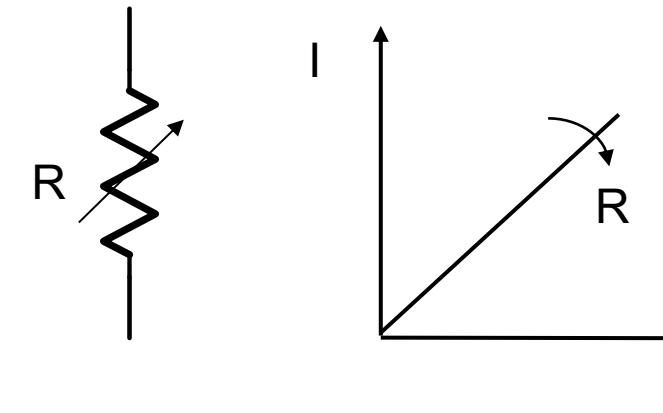
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 - MOS Transistor as a Switch
 - NMOS & PMOS
- CMOS Gates
 - Inverter
 - Pull-Up and Pull-Down Networks
 - Complex Gates

Ohm's Law

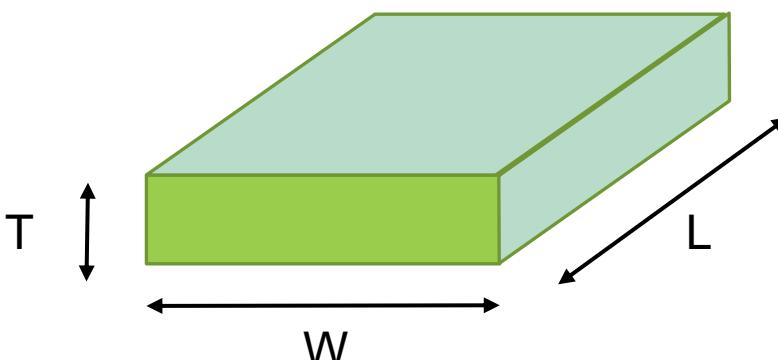
- Resistors



- Variable resistors



- Physical resistors

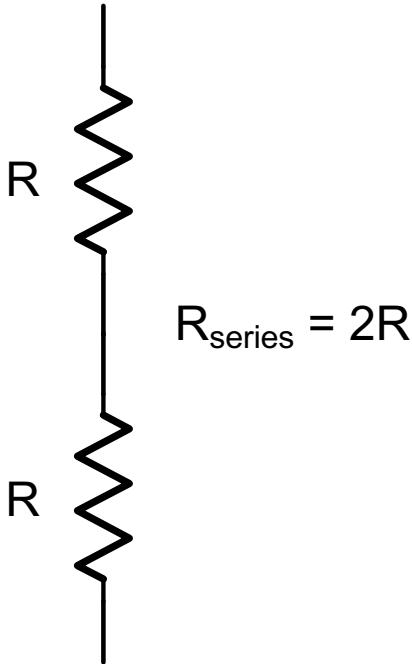


$$R = \rho \frac{L}{TW}$$

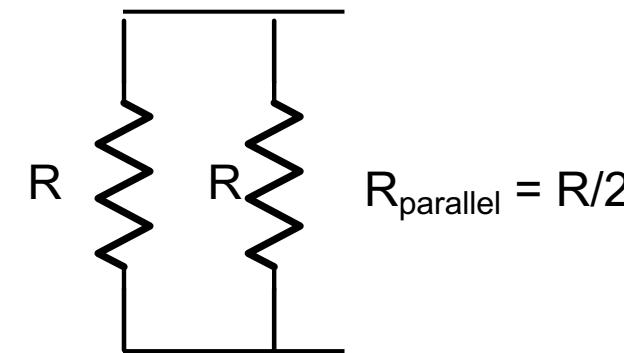
- In a planar process, designer controls W and L

Series and Parallel

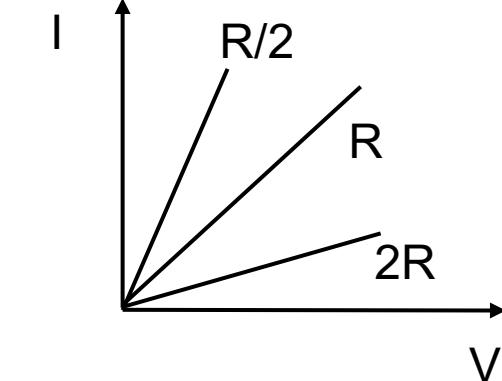
- With two identical resistors, R



Equivalent to doubling length

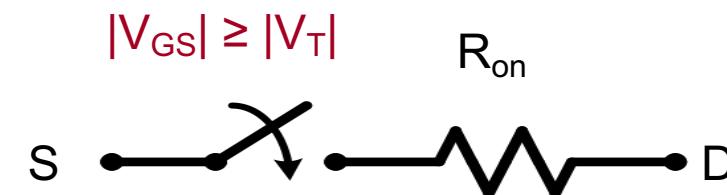
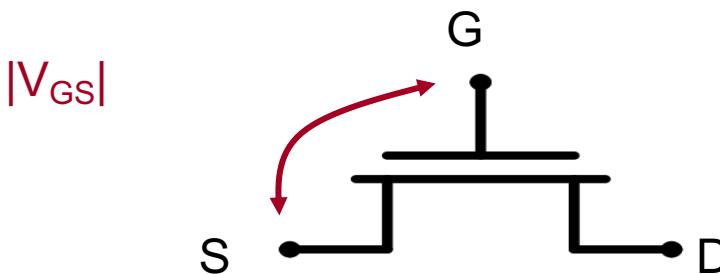


Equivalent to doubling width



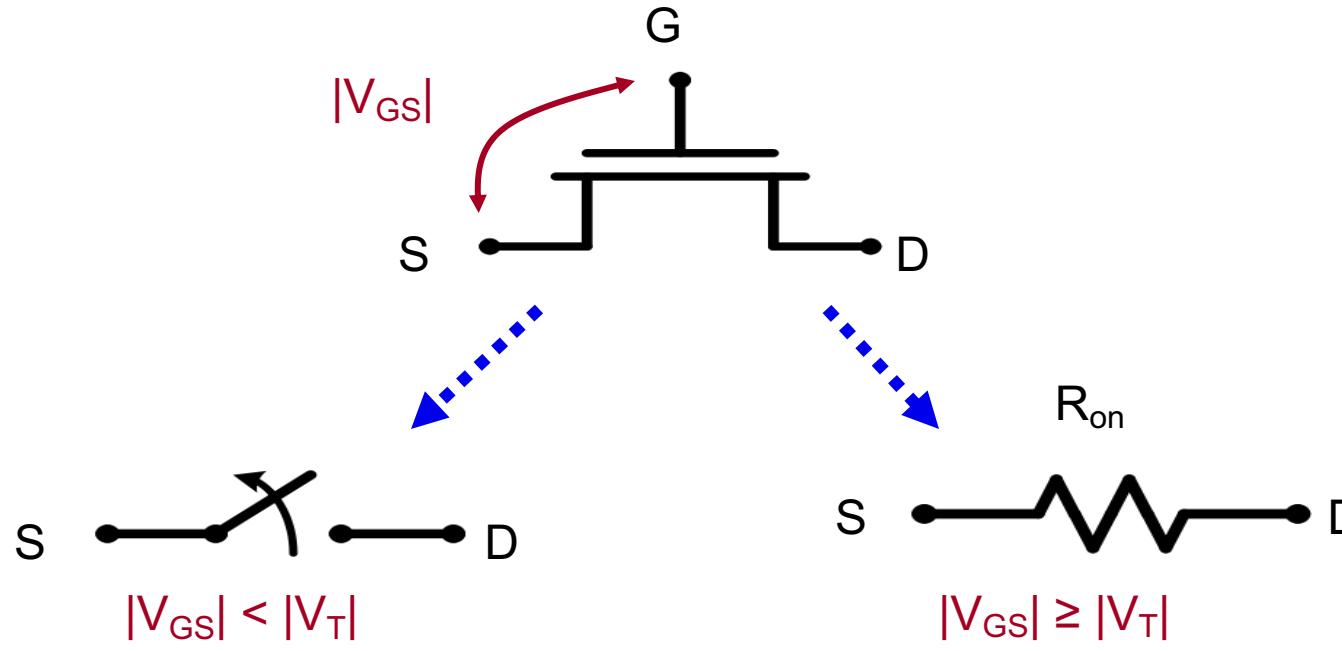
MOS Transistor as a Resistive Switch

MOS Transistor \longleftrightarrow A Switch!



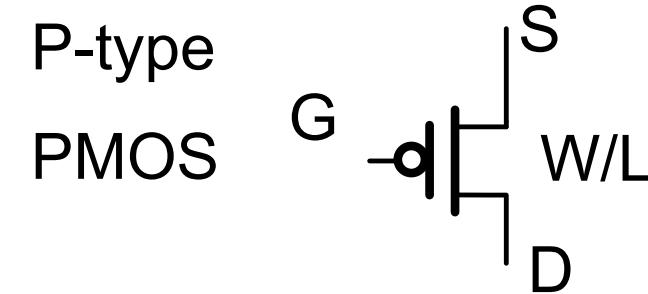
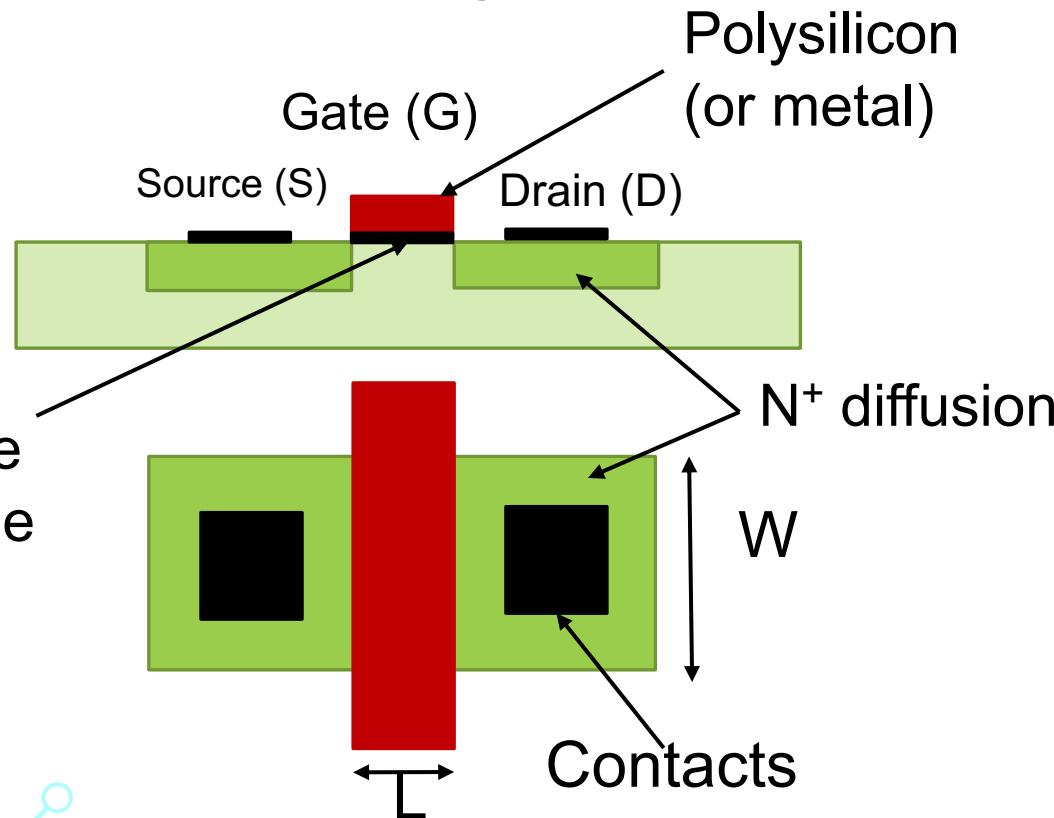
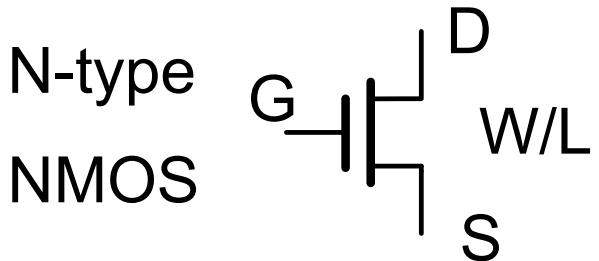
- V_{GS} controls the switch
 - (it also charges the channel capacitor)

ON/OFF Switch Model of MOS Transistor

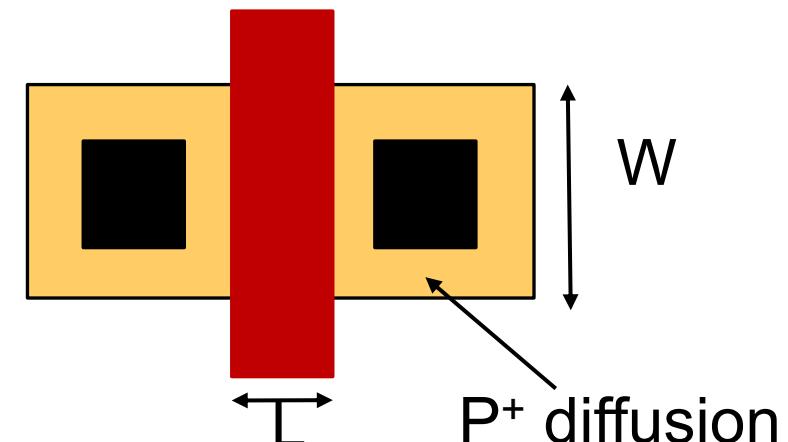


“Metal”-Oxide-Semiconductor (MOS) Transistors

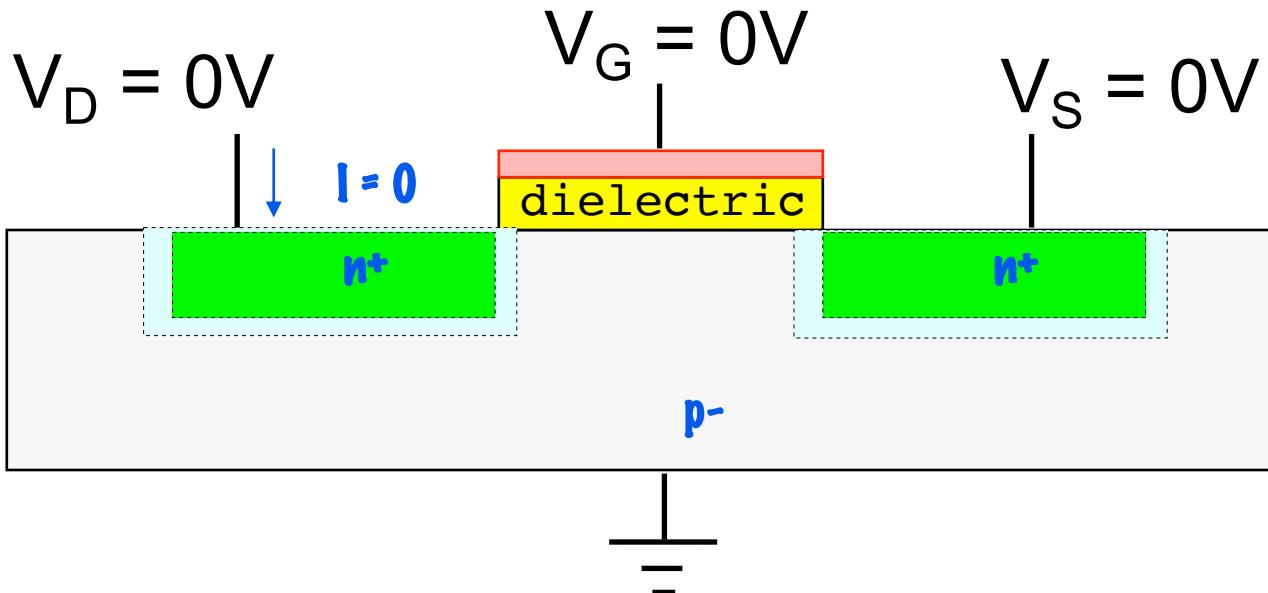
- Symbol



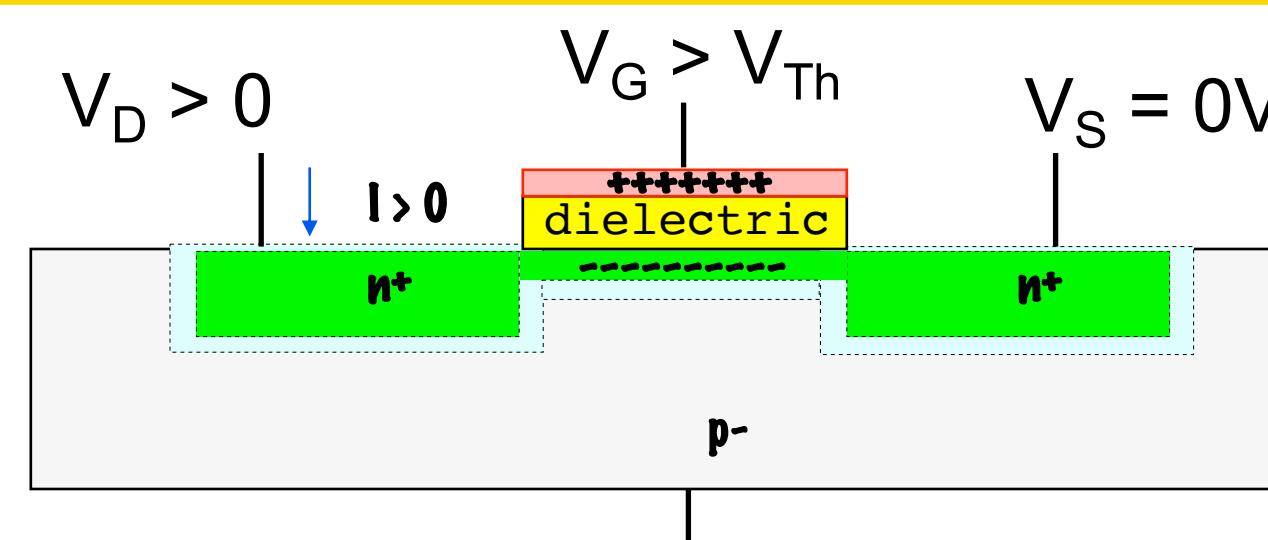
- Devices are symmetrical
 - NMOS: Drain is at higher voltage
 - PMOS: Source is at higher voltage



How does NMOS transistor actually work?



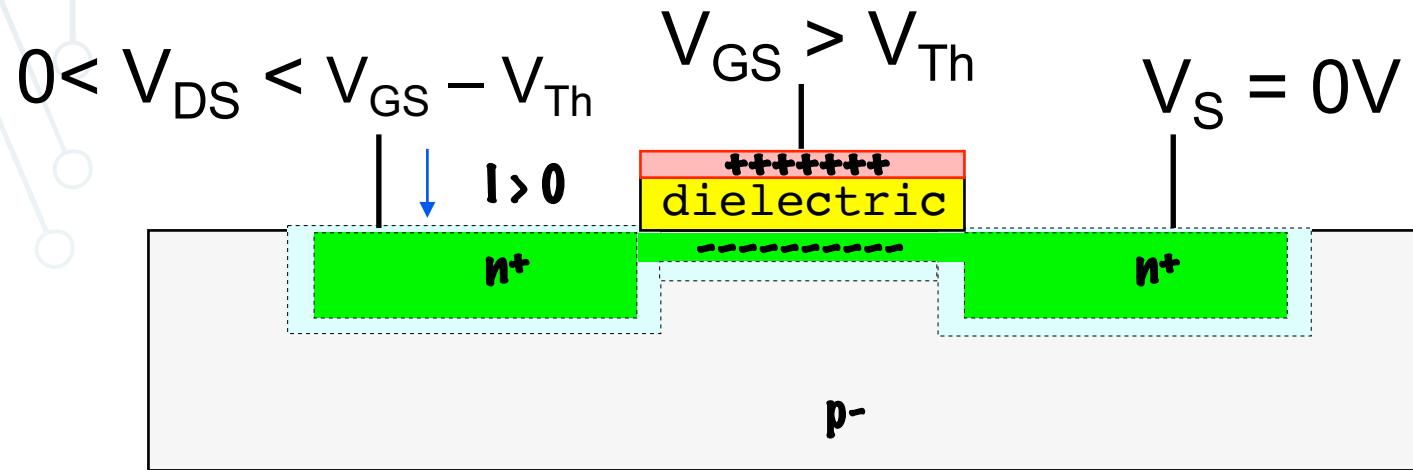
When $V_{GS} < V_{Th}$ transistor is off



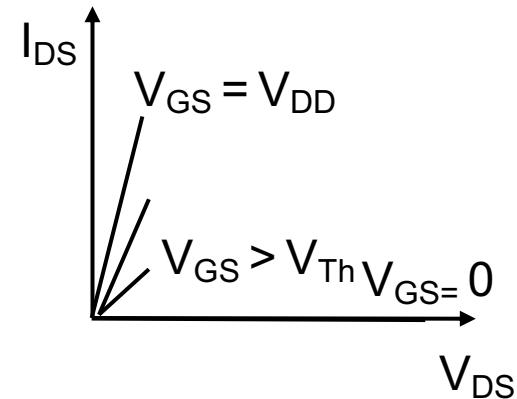
$V_G > V_{Th}$, small region near the surface turns from p-type to n-type.

NMOS is on.
Current is proportional to V_{DS}

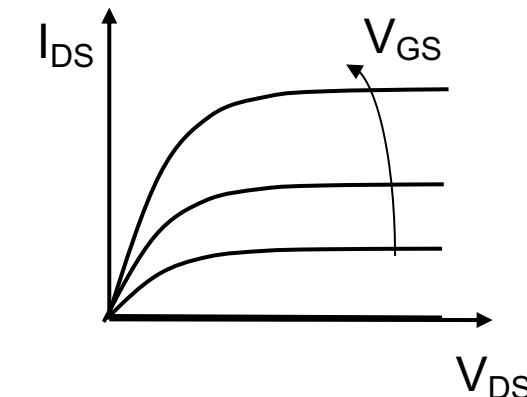
How does NMOS transistor actually work?



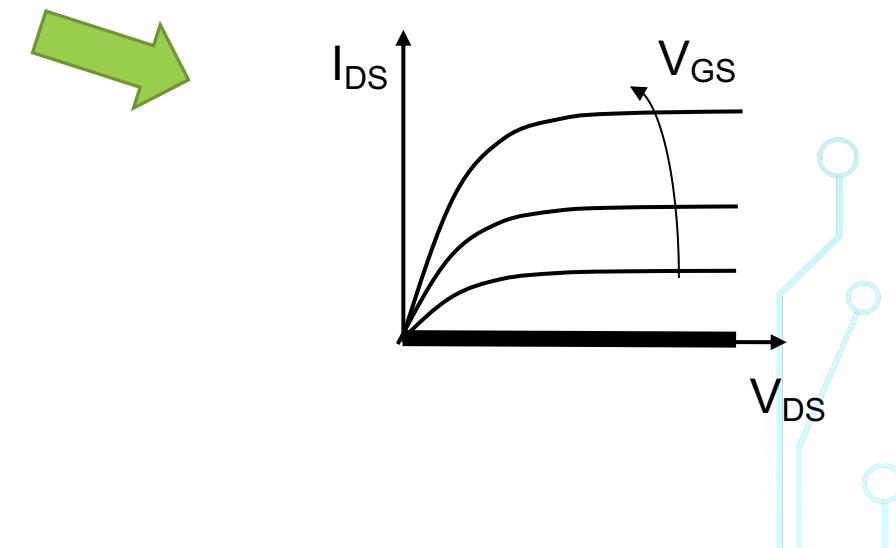
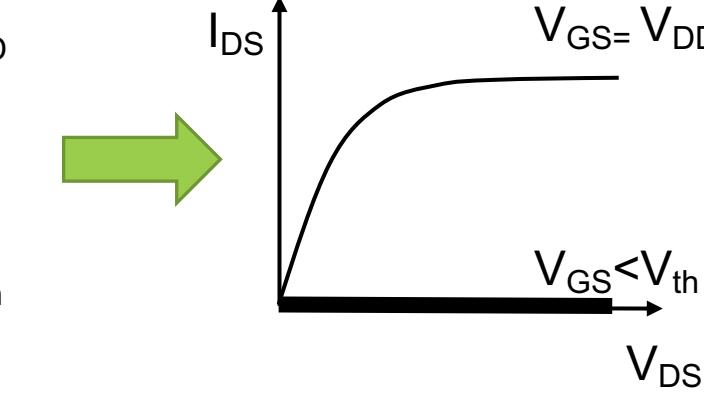
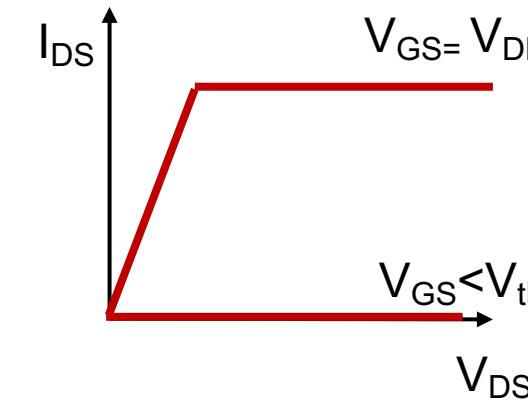
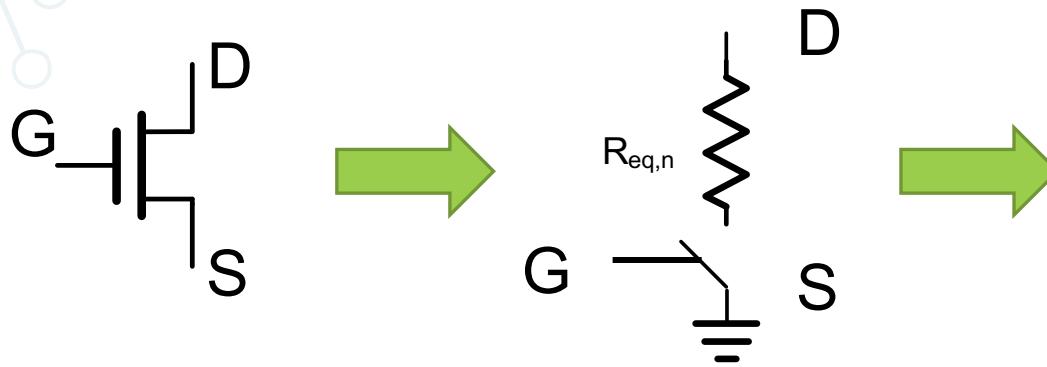
V_{DS} and V_{GS} change I_{DS}



$V_{GD} < V_{Th}$ transistor saturates
($V_{DS} > V_{GS} - V_{Th}$)

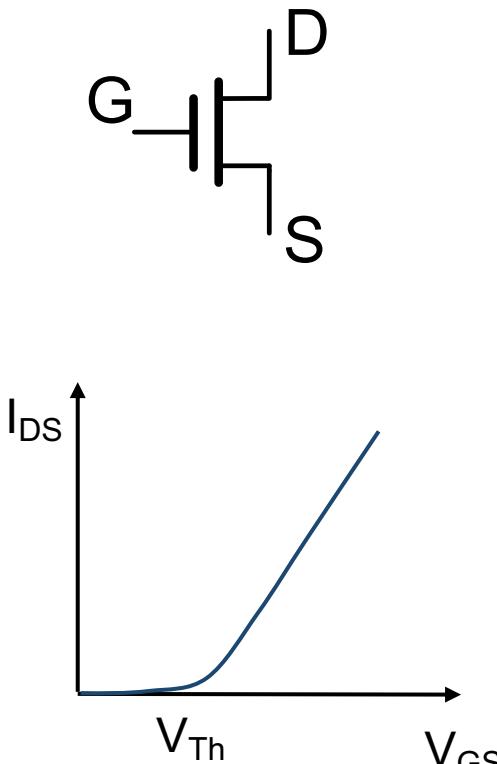


MOS Transistors



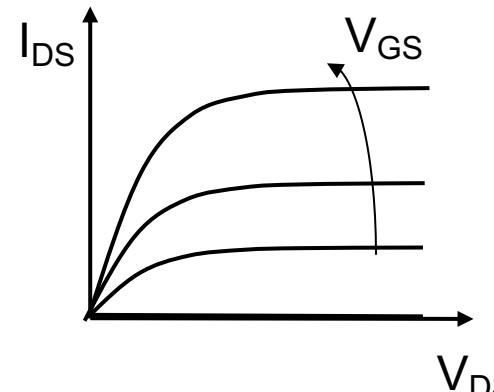
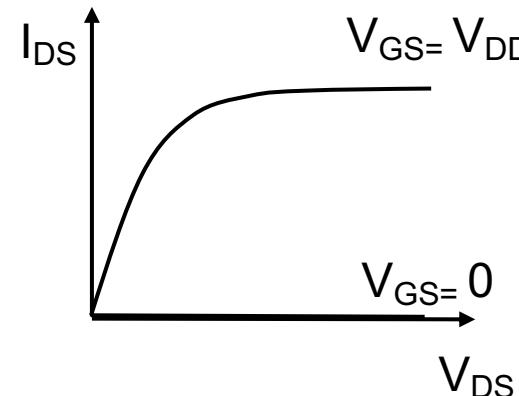
MOS Transistors

- NMOS Transistor I-V characteristics

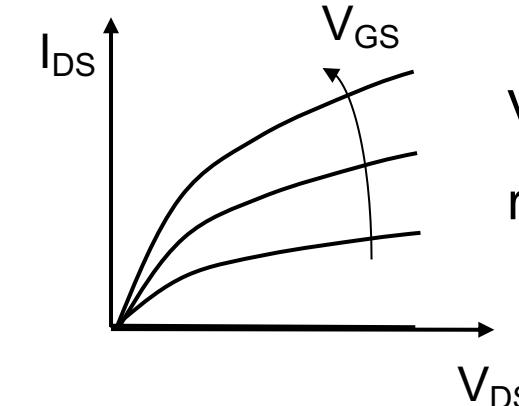
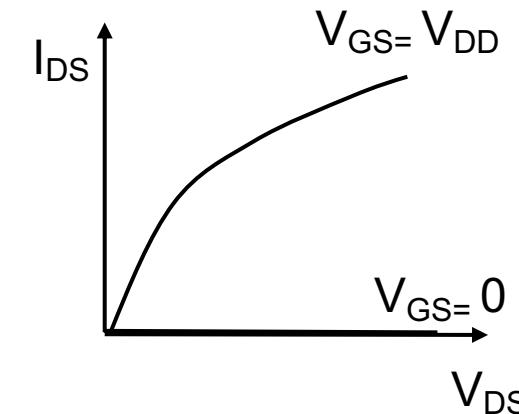


Nearly linear
 $I_{DS} \sim K(V_{GS}-V_{Th})$

Ideal transistor



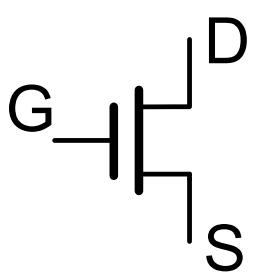
~7nm transistor



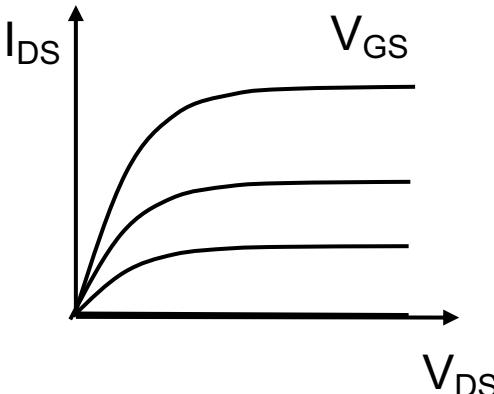
Variable
resistor!

MOS Transistors

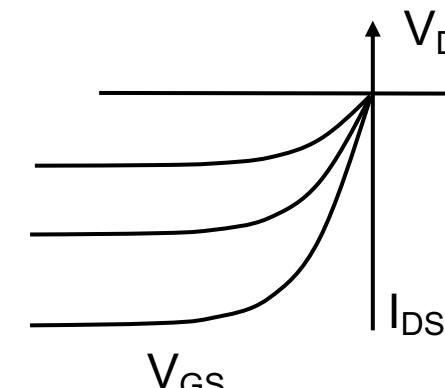
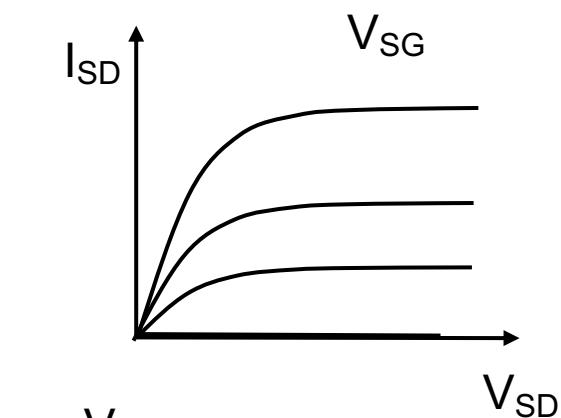
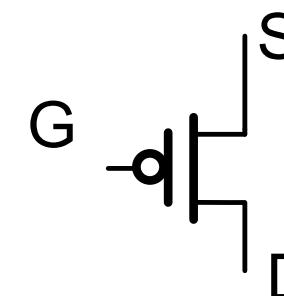
- PMOS Transistor I-V characteristics



NMOS

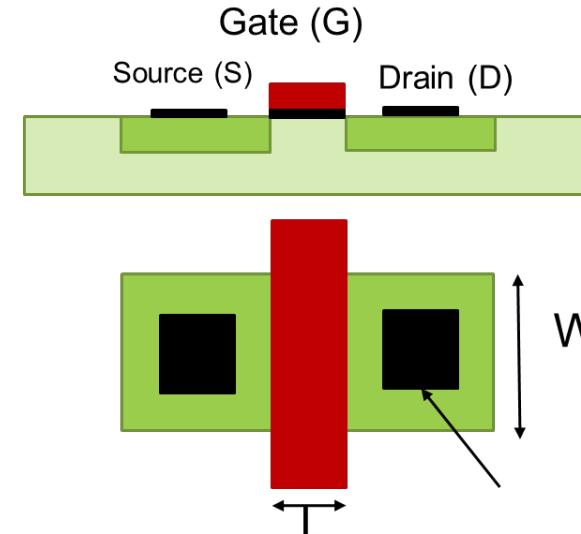
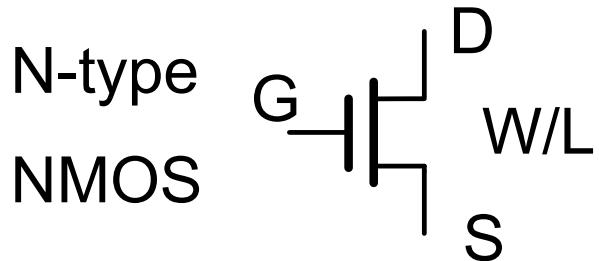


PMOS



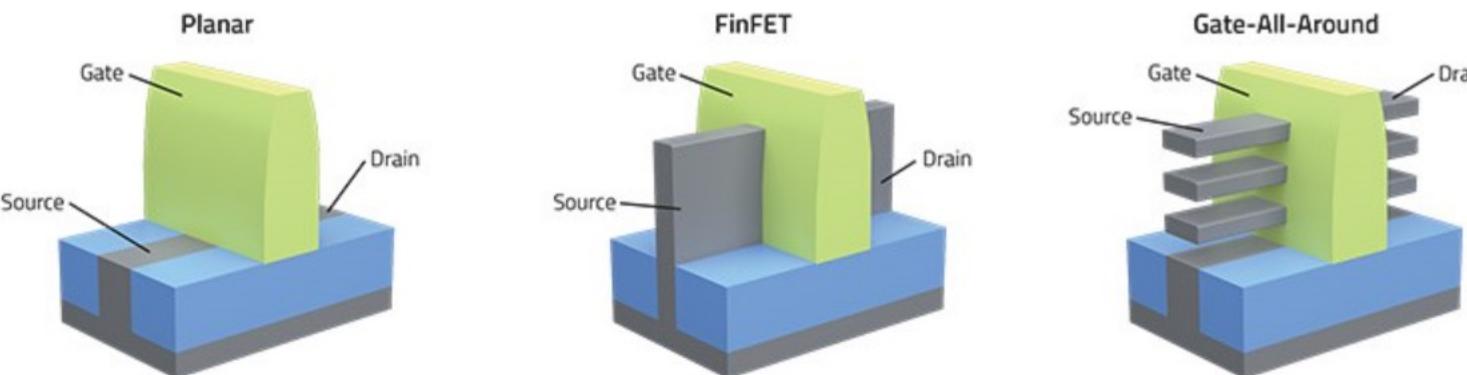
Different Kinds of MOS Transistors

- Planar bulk CMOS



(12) United States Patent
Hu et al.

(10) Patent No.: US 6,413,802 B1
(45) Date of Patent: Jul. 2, 2002



(54) FINFET TRANSISTOR STRUCTURES HAVING A DOUBLE GATE CHANNEL EXTENDING VERTICALLY FROM A SUBSTRATE AND METHODS OF MANUFACTURE

(75) Inventor: Cheeming Hu, Alvin, You-Jae King, Hisamatsu, Masaaki, Venk Subramanian, Richard City, Lihua Chang, Berkeley; Xuejue Huang, Yang-Kyu Choi, both of Albany; Jakab Tadeusz Ketzler, Jeffrey J. Bokor, Nira Liderit, Bothmar, Jeffrey Bokor, Oakland, all of CA (US); Wen-Chun Lee, Beaverton, OR (US)

signee: The Regents of the University of California, Oakland, CA (US)

title: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

pl. No.: 09/695,532
ad. Oct. 23, 2000

cl. 7 H01L 21/00, H01L 21/84

5 cl. 438/151, 438/283

id. of search 438/151, 157, 438/201, 223, 241, 258, 279, 283, 437, 588, 594, 256, 270, 303, 305, 592, 592

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1,331 A * 6/1/98 Solomon et al. 438/164
1,049 A * 8/1/99 Taur et al. 253/348
1,710 A * 5/1/99 Mukai 438/156
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Hsiang et al., "Sub-50-nm FinFET: PMOS," 1999 IEEE International Electron Devices Meeting Technical Digest, pp. 67-70 (1999).

Auth et al., "Vertical Fully-Depleted, Surrounding-Gate MOSFETs on sub-0.1-μm Thick Silicon Pillars," 1996 54th Annual Device Research Conference Digest, pp. 108-109 (1996).

Hiyama et al., "A Fully Depleted Ion-Channel Transistor (IDETA)—A Novel Vertical Ultrathin SOI MOSFET," IEEE Electron Device Letters, v. 11(1), pp. 36-38 (1990).

(Last continued on next page.)

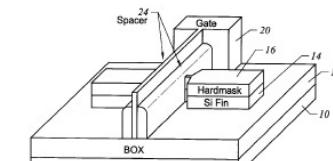
Primary Examiner—David N. Barnes
Attorney, Agent, or Firm—Townsend and Townsend and Clegg LLP, Henry K. Woodward, Jr.

Patent Drawing—None
(74) Attorney, Agent, or Firm—Townsend and Townsend and Clegg LLP, Henry K. Woodward, Jr.

ABSTRACT

A FinFET device is fabricated using conventional planar MOSFET technology. The device is fabricated in a silicon layer overlying an insulating layer (e.g., SiMOX) with the device extending from the insulating layer as a fin. Double-gate structures are formed on the top surface of the fin to enhance drive current and effectively suppress short channel effects. A plurality of channels can be provided between a source and a drain for increased current capacity. In one embodiment two transistors can be stacked in a fin to provide a CMOS transistor pair having a shared gate.

28 Claims, 4 Drawing Sheets



Administrivia

- Relax after Midterm ☺
 - No new lab this week.
 - Wrap up Lab 5 soon.
 - No new HW this week.
- Discussion: go through midterm problems.
- Midterm grades will be released early next week.

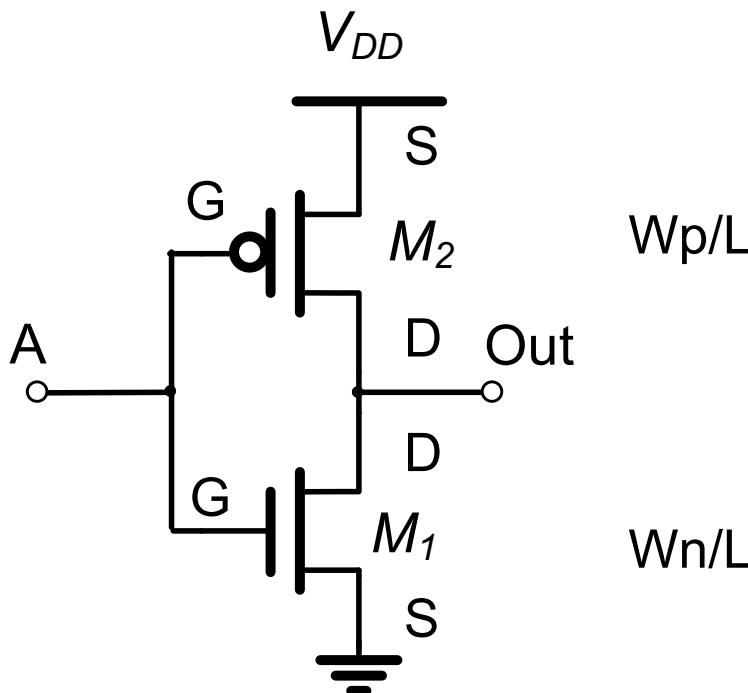


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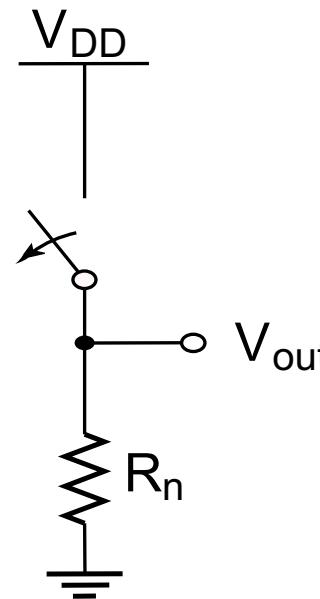
CMOS Inverter

- Simple DC behavior

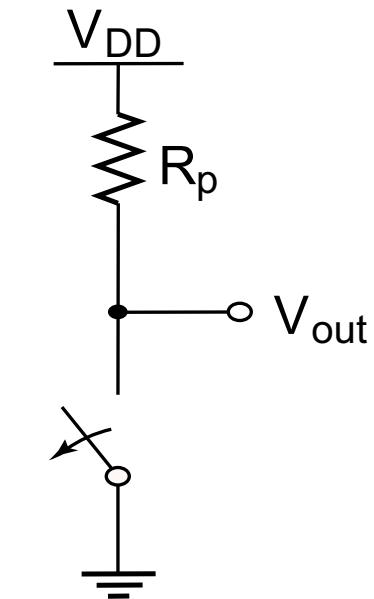
- Schematic



- Switch model



$$V_{in} = V_{DD}$$



$$V_{in} = 0$$

$$\begin{aligned}V_{OL} &= 0 \\V_{OH} &= V_{DD}\end{aligned}$$

Digital Circuits

- One logic representation
- Multiple libraries
- Layouts

$$\text{Out} = \overline{A}$$

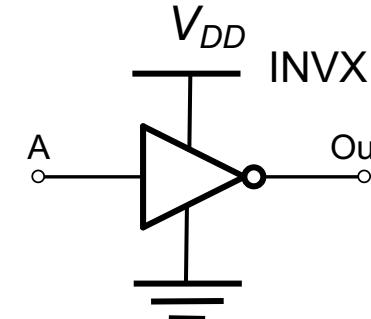
Truth table

A	Out
0	1
1	0

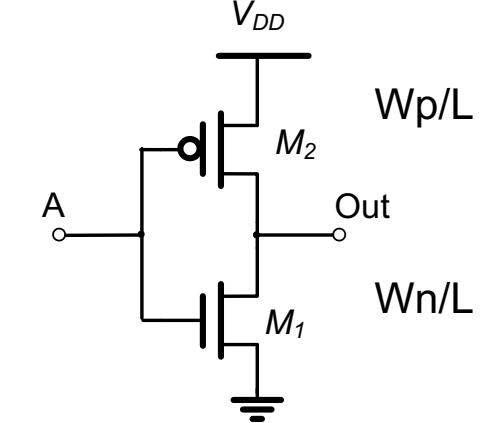
- Transistor thresholds (V_{Th}) (for each track height):
 - Regular (RVT)
 - Low (LVT)
 - Faster, higher power
 - Slower, lower power
 - High (HVT)
- Transistor sizes

- Multiple gate sizes within a library

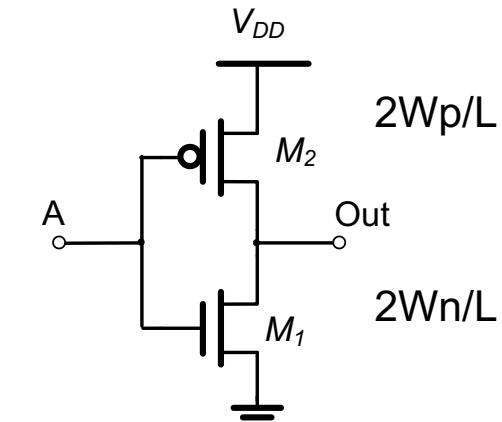
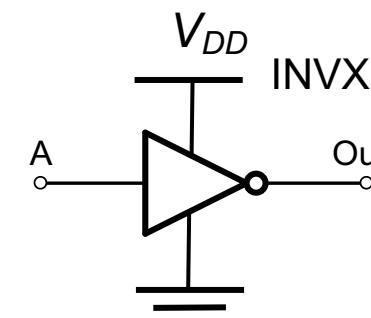
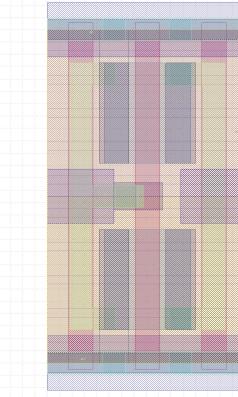
- Symbol



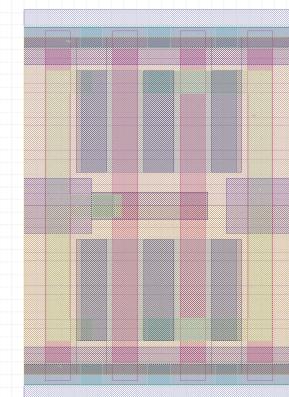
- Schematic



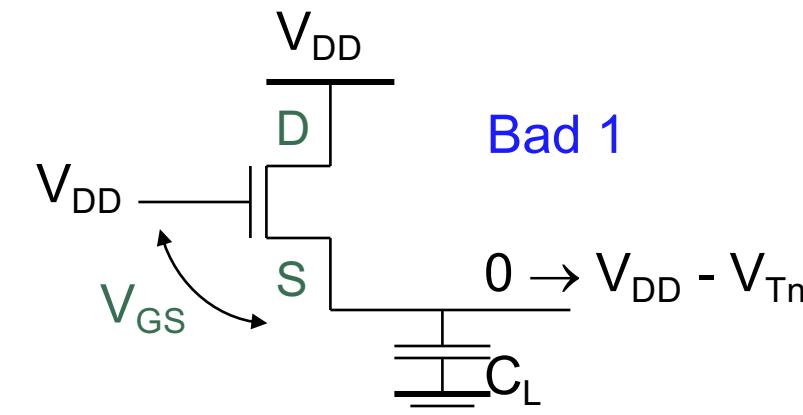
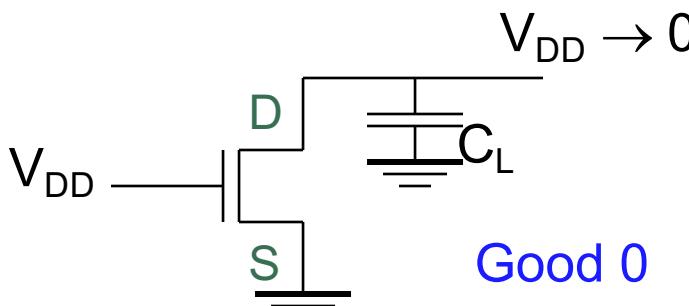
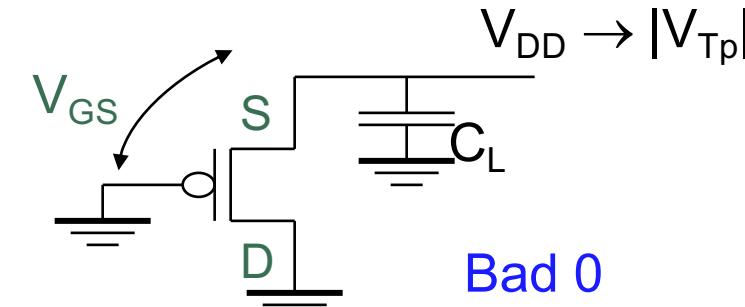
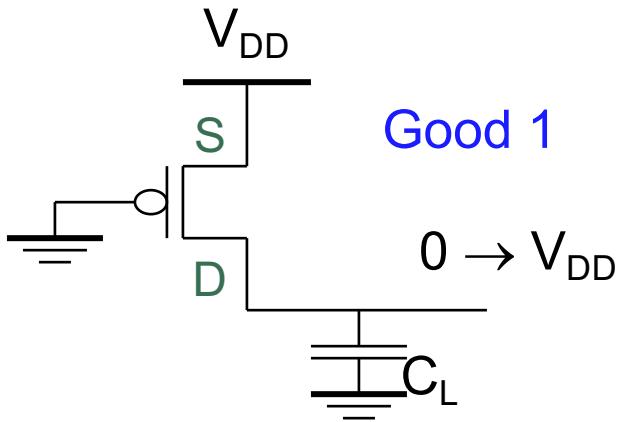
- Layout



INVX3,
INVX4,...



Switch Limitations

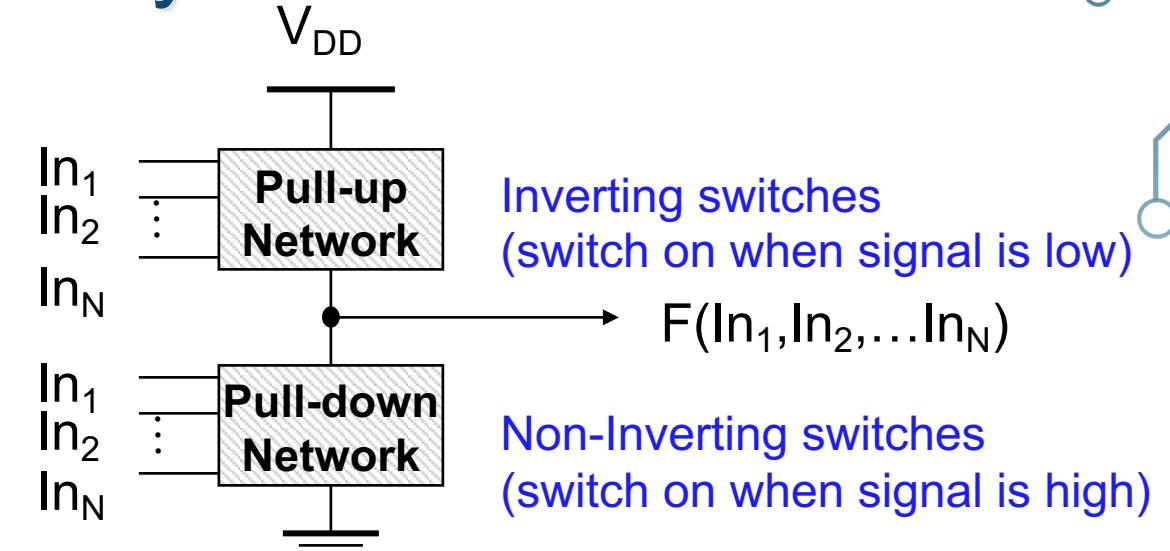


Complementary CMOS Logic Style

- PUN is the **dual** to PDN
(can be shown using DeMorgan's Theorems)

$$\overline{A + B} = \overline{A}\overline{B}$$

$$\overline{AB} = \overline{A} + \overline{B}$$



- Static CMOS gates are always inverting
- PUN in PMOS and PDN in CMOS



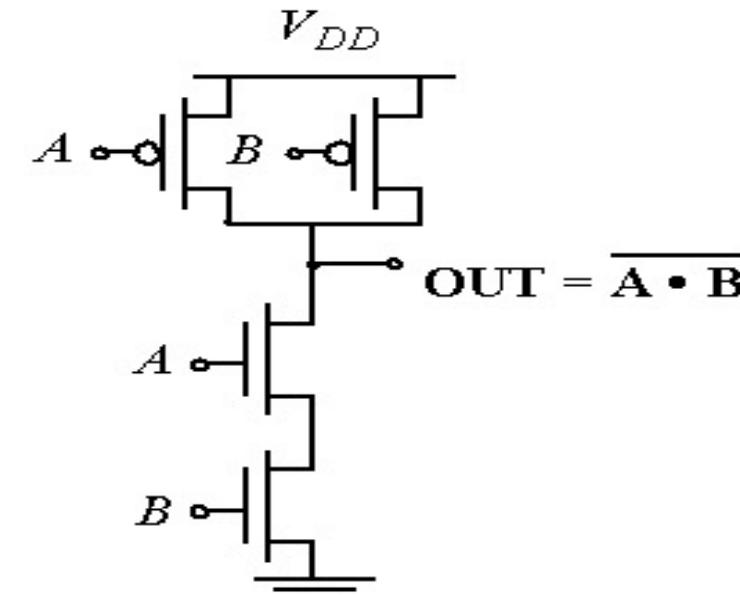
AND = NAND + INV



Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate

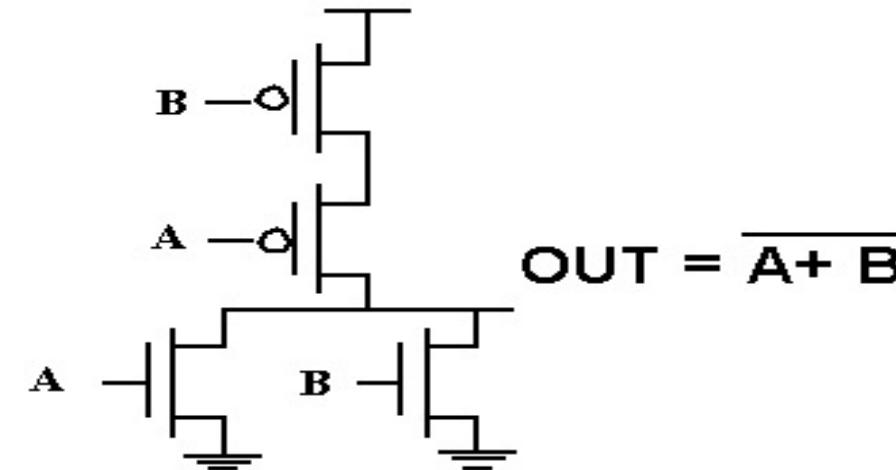


- PDN: $G = \overline{AB} \Rightarrow$ Conduction to GND
- PUN: $F = \overline{A} + \overline{B} = \overline{AB} \Rightarrow$ Conduction to V_{DD}
- $\overline{G(\ln_1, \ln_2, \ln_3, \dots)} \equiv F(\overline{\ln_1}, \overline{\ln_2}, \overline{\ln_3}, \dots)$

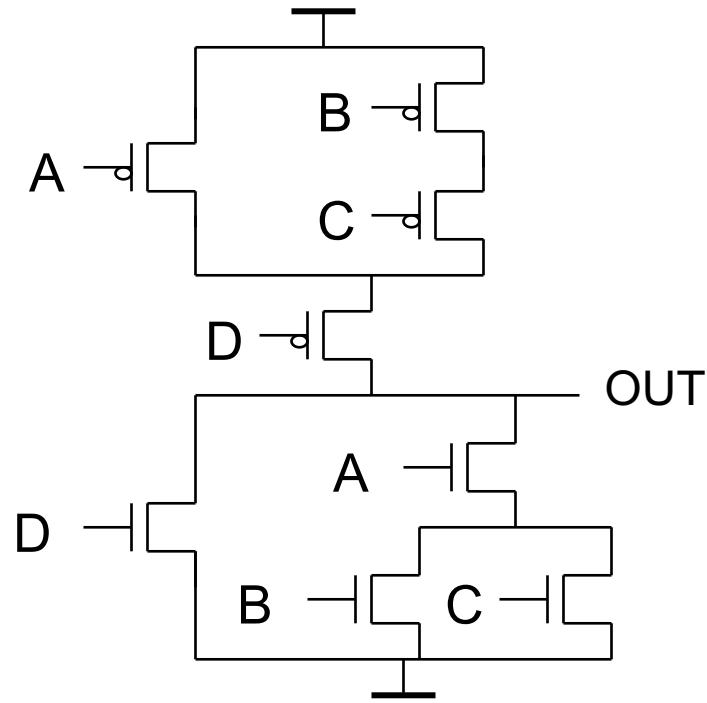
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate

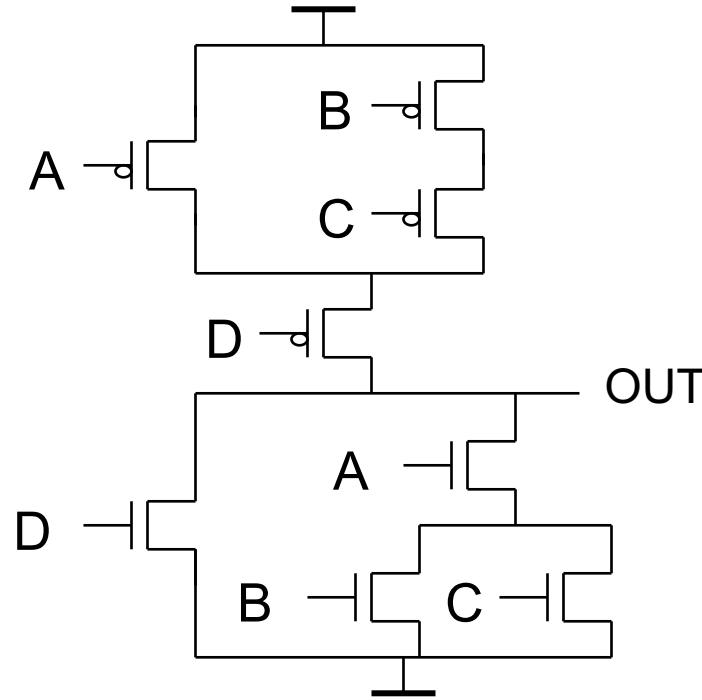


Complex CMOS Gate

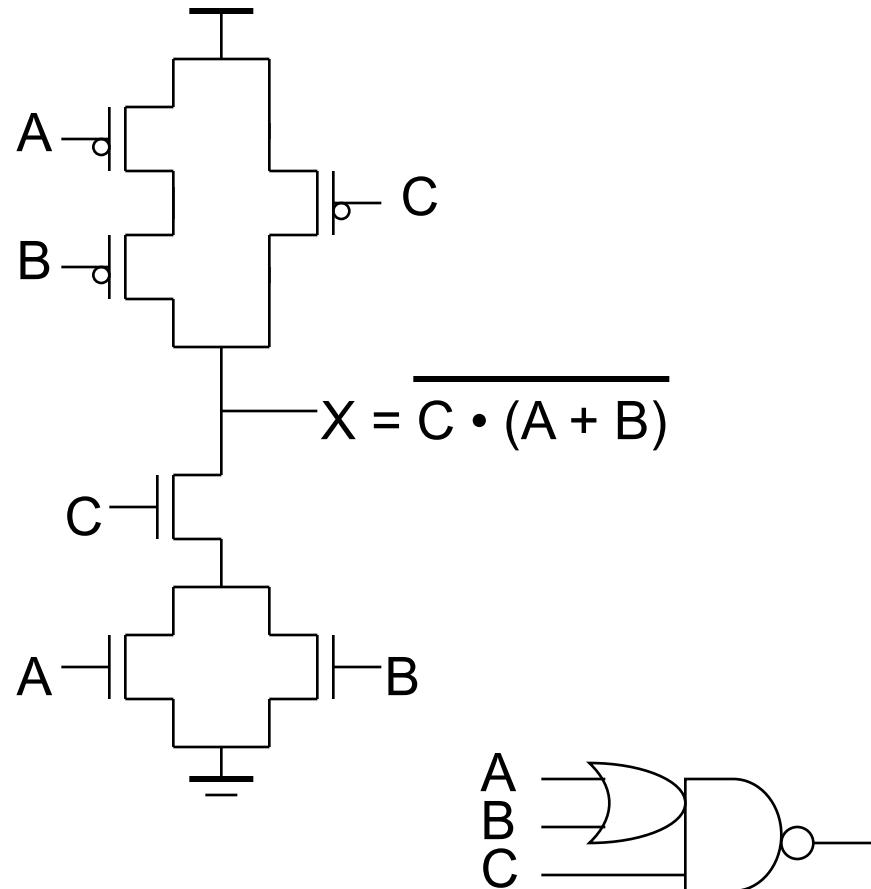


Complex CMOS Gate

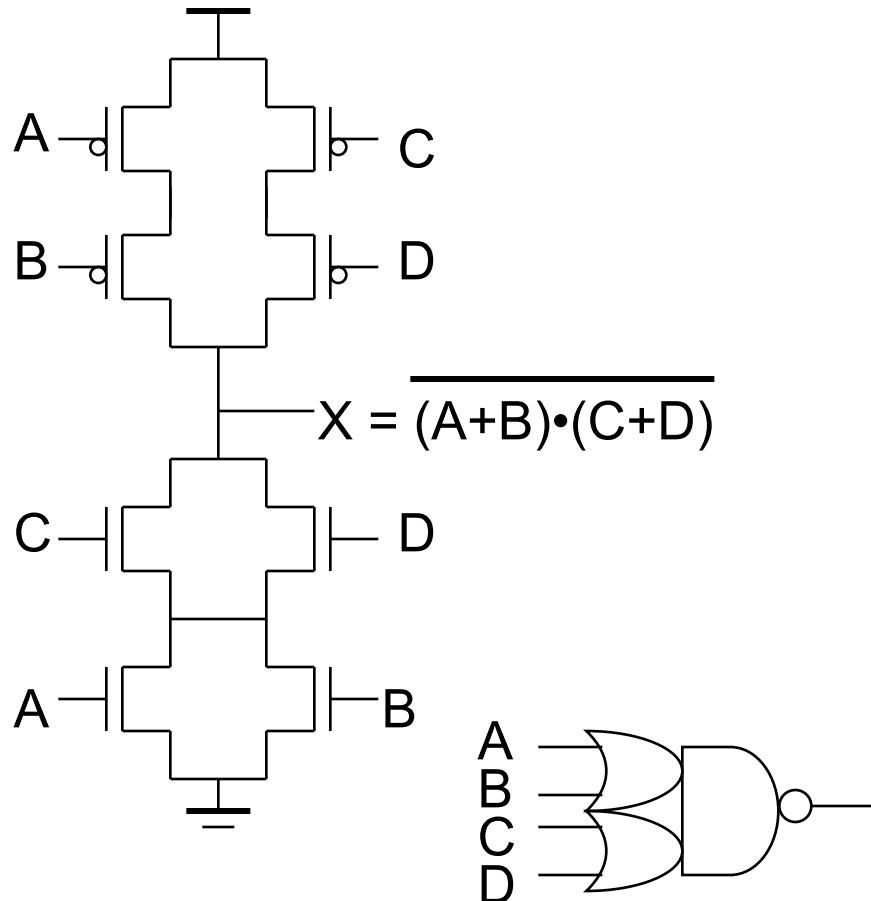
$$OUT = \overline{D + A \cdot (B + C)}$$



Complex CMOS Gate



Complex CMOS Gate



Summary

- CMOS Transistors and Gates
 - CMOS Transistors
 - MOS Transistor as a Switch
 - NMOS & PMOS
 - CMOS Gates
 - Inverter
 - Pull-Up and Pull-Down Networks
 - Complex Gates