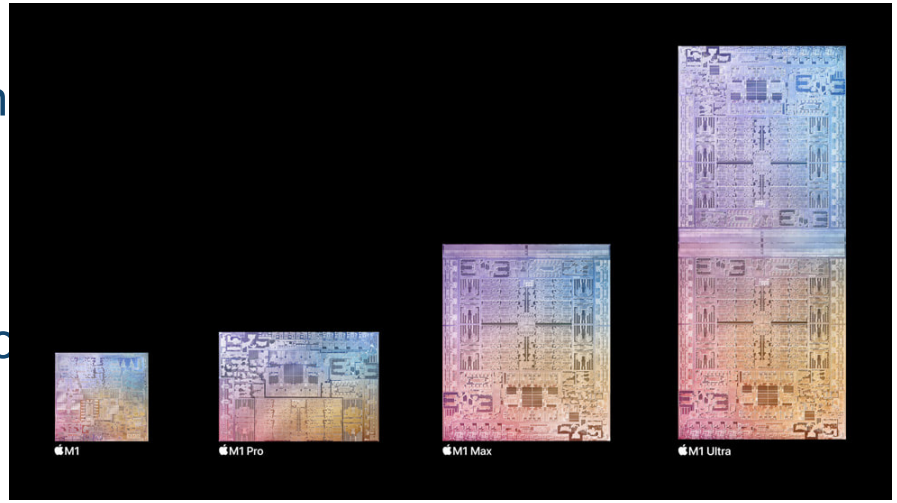
EECS151/251A
Introduction to Digital Design and ICs

Lecture 14: Inverter Delay

Sophia Shao

Apple unveils M1 Ultra, the world's most powerful chip for a personal computer

Apple today announced M1 Ultra, the next giant leap for Apple silicon and the Mac. Featuring UltraFusion — Apple's innovative packaging architecture that interconnects the die of two M1 Max chips to create a system on a chip (SoC) with unprecedented levels of performance and capabilities — M1 Ultra delivers breathtaking computing power to the new Mac Studio while maintaining industry-leading performance per watt. The new SoC consists of 114 billion transistors, the most ever in a personal computer chip.



https://www.apple.com/newsroom/2022/03/apple-unveils-m1-ultra-the-worlds-most-powerful-chip-for-a-personal-computer/

Review

- CMOS Transistors and Gates
  - CMOS Transistors
    - MOS Transistor as a Switch
    - NMOS & PMOS
  - CMOS Gates
    - Inverter

- CMOS Transistors
  - Review
  - Gates
- Inverter Delay
  - Overview
  - Inverter RC Delay
  - Inverter Size

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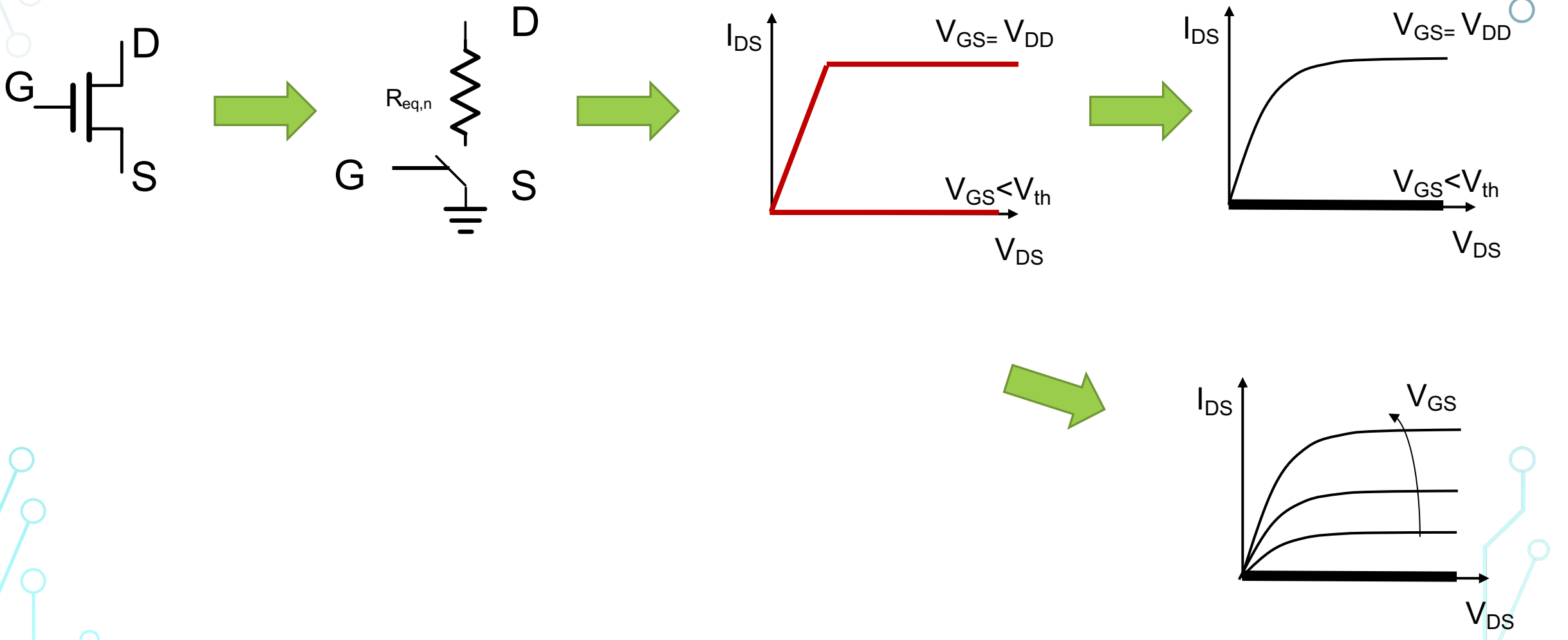
MOS Transistors



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- CMOS Transistors
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- **Inverter Delay**
  - **Overview**
  - **Inverter RC Delay**
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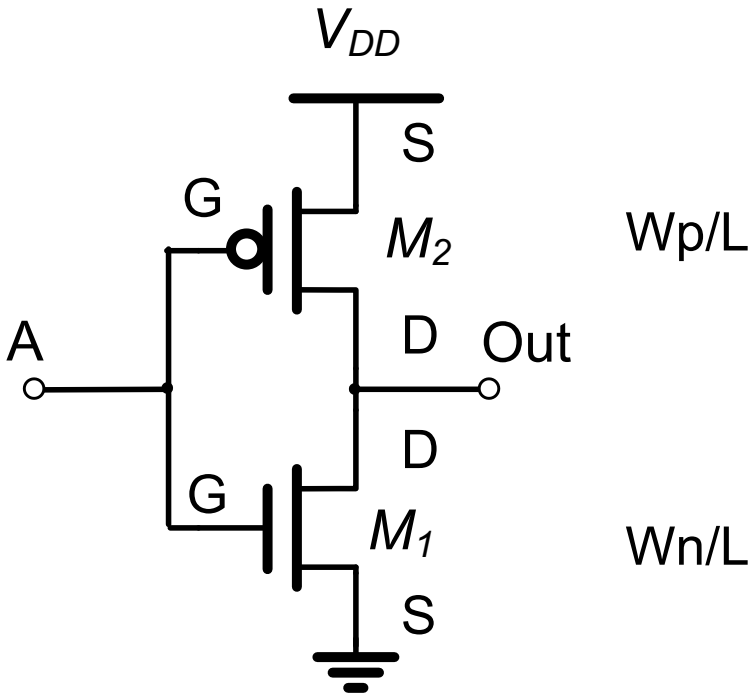
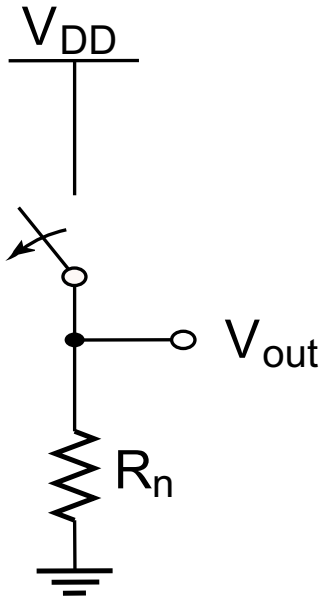
CMOS Inverter

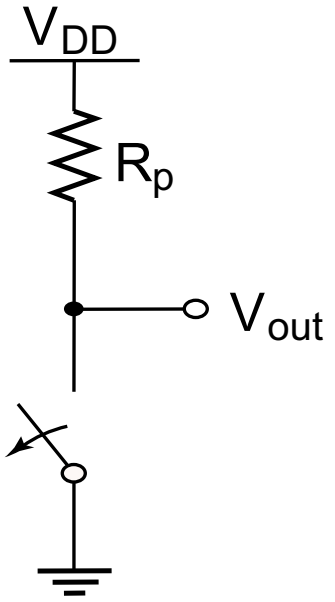
- Simple DC behavior
  - Schematic



- Switch model



$V_{in} = V_{DD}$



$V_{in} = 0$

$V_{OL} = 0$
$V_{OH} = V_{DD}$

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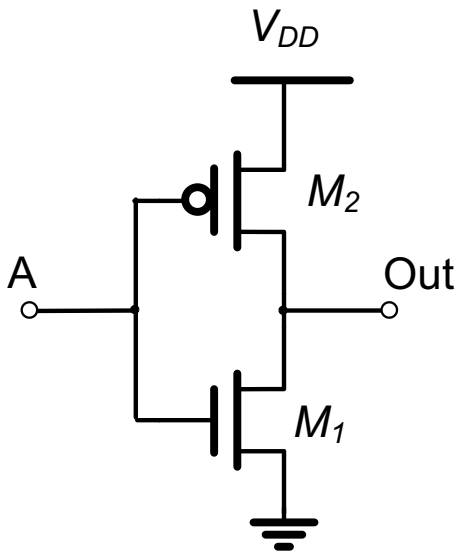
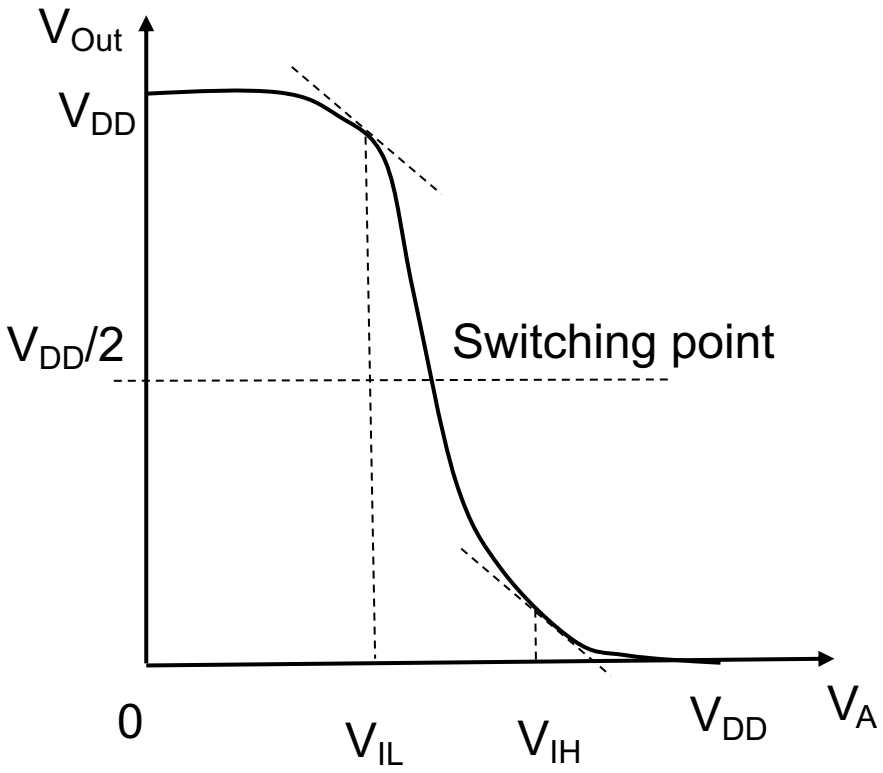
Voltage Transfer Characteristic (VTC)





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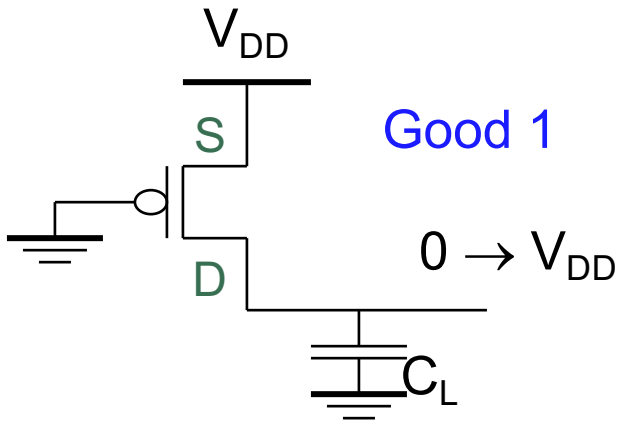
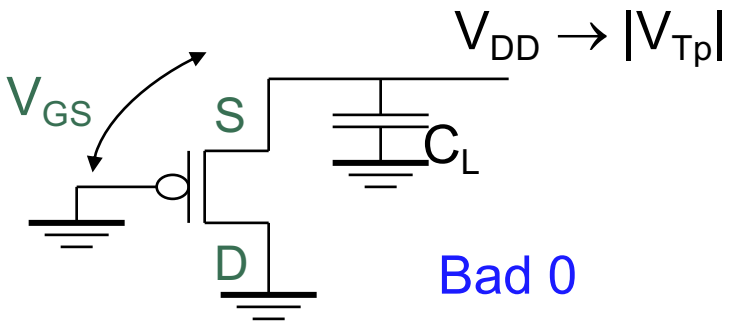
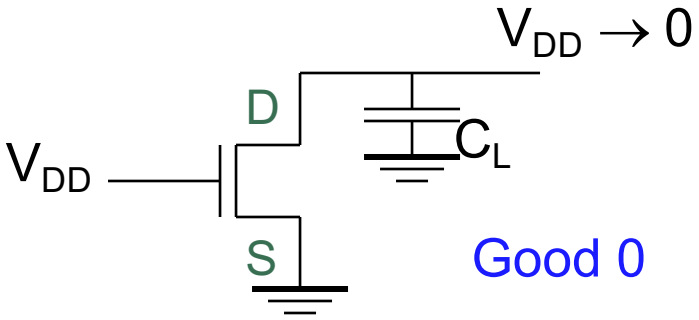
Good/Bad “0” and “1”



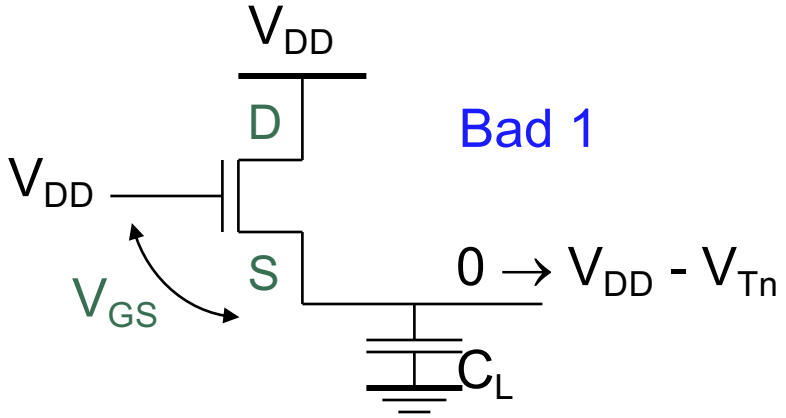
Good 1



Bad 0



Good 0



Bad 1

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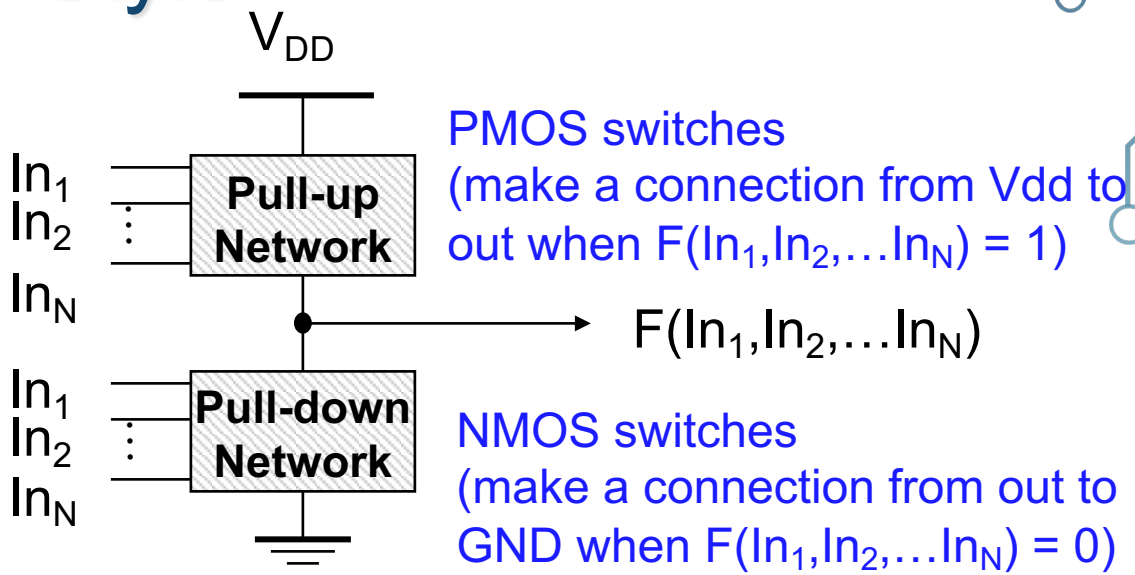
Complementary CMOS Logic Style

- PUN is the **dual** to PDN (can be shown using DeMorgan's Theorems)

$$\overline{A + B} = \overline{A}\,\overline{B}$$

$$\overline{AB} = \overline{A} + \overline{B}$$



- PUN in PMOS and PDN in NMOS
  - Using NMOS to produce 0 -> Pull Down
  - Using PMOS to produce 1 -> Pull Up

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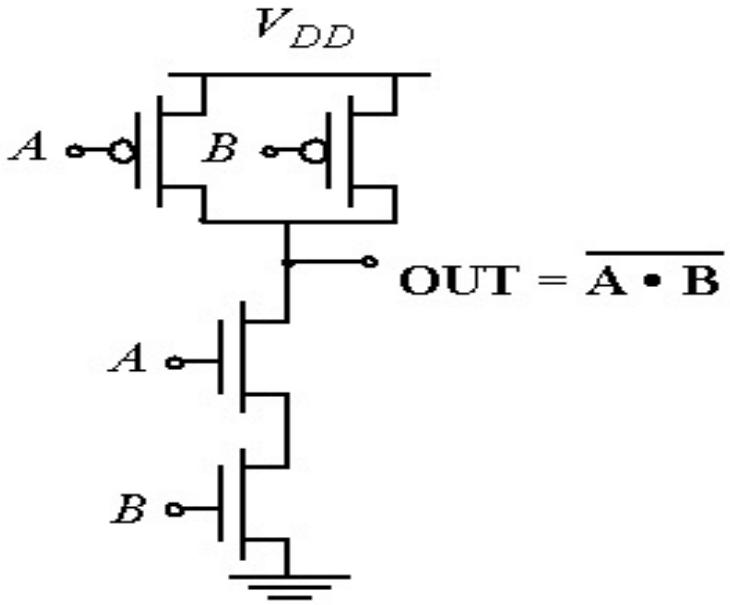
Example Gate: NAND

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

Truth Table of a 2 input NAND gate



- PDN: G = AB $\Rightarrow$ Conduction to GND
- PUN: F = $\overline{A}$ + $\overline{B}$ = $\overline{AB}$ $\Rightarrow$ Conduction to V_{DD}
- $\overline{G(In_1,In_2,In_3,\ldots)} \equiv F(\overline{In_1}, \overline{In_2}, \overline{In_3},\ldots)$

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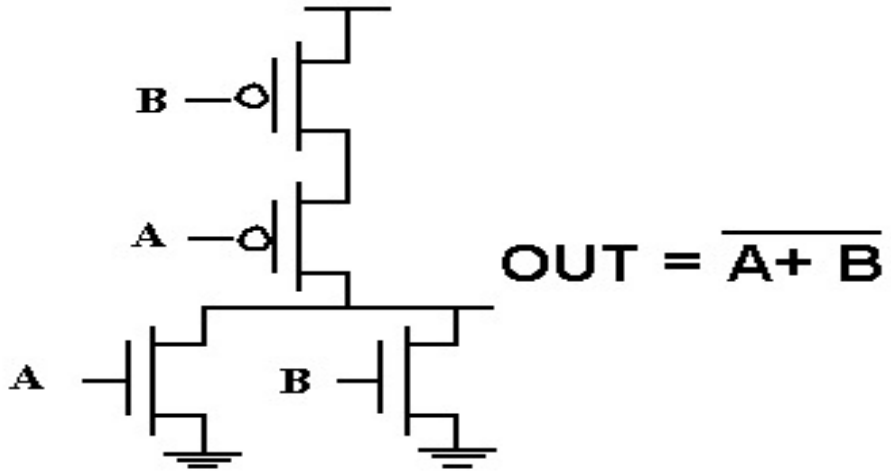
Example Gate: NOR

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

Truth Table of a 2 input NOR gate



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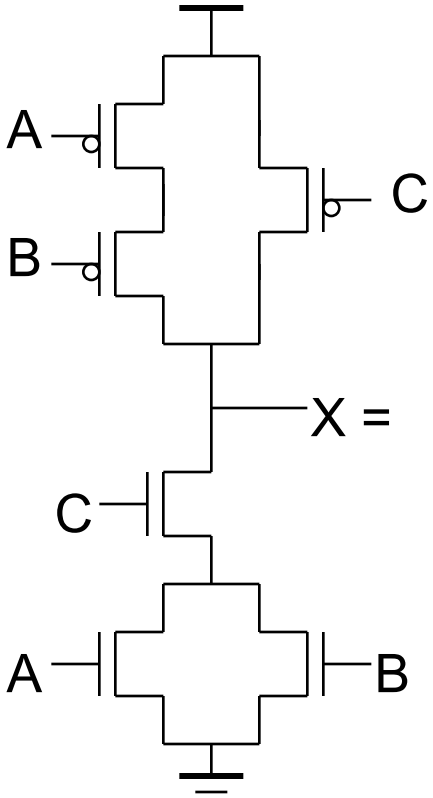
Complex CMOS Gate



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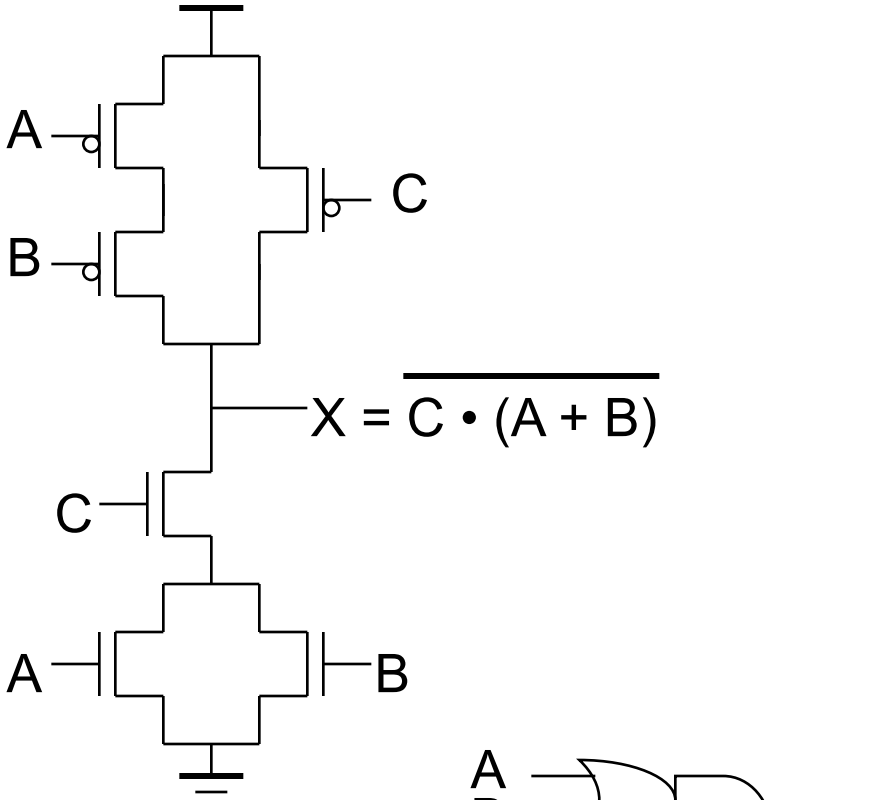
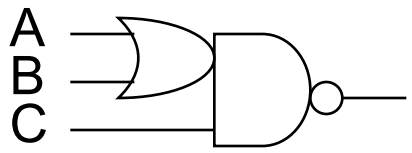
Complex CMOS Gate





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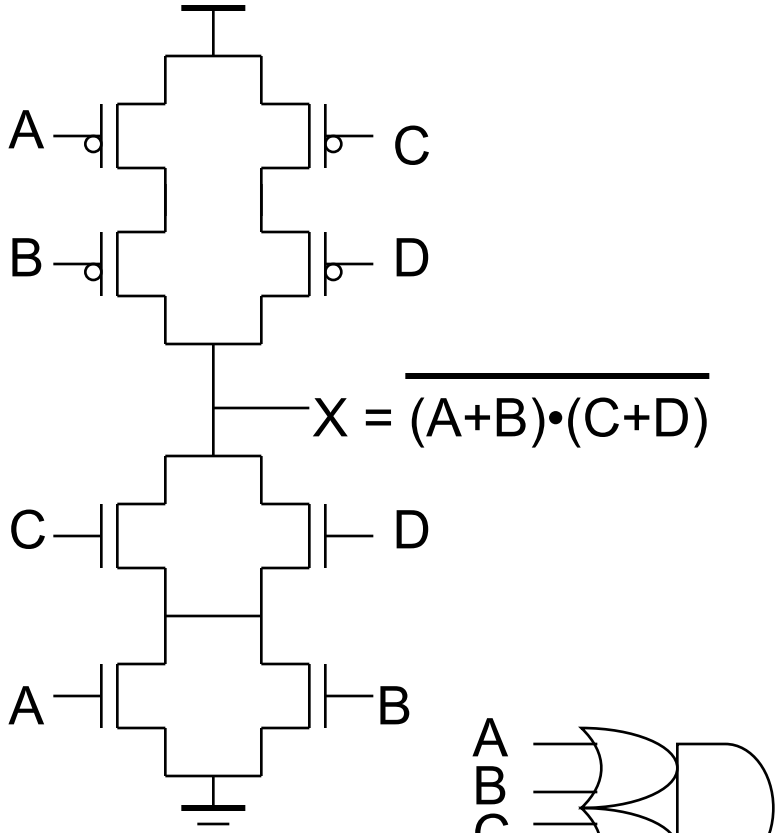
Complex CMOS Gate



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- CMOS Transistors
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- **Inverter Delay**
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  - **Inverter RC Delay**
  - **Inverter Size**

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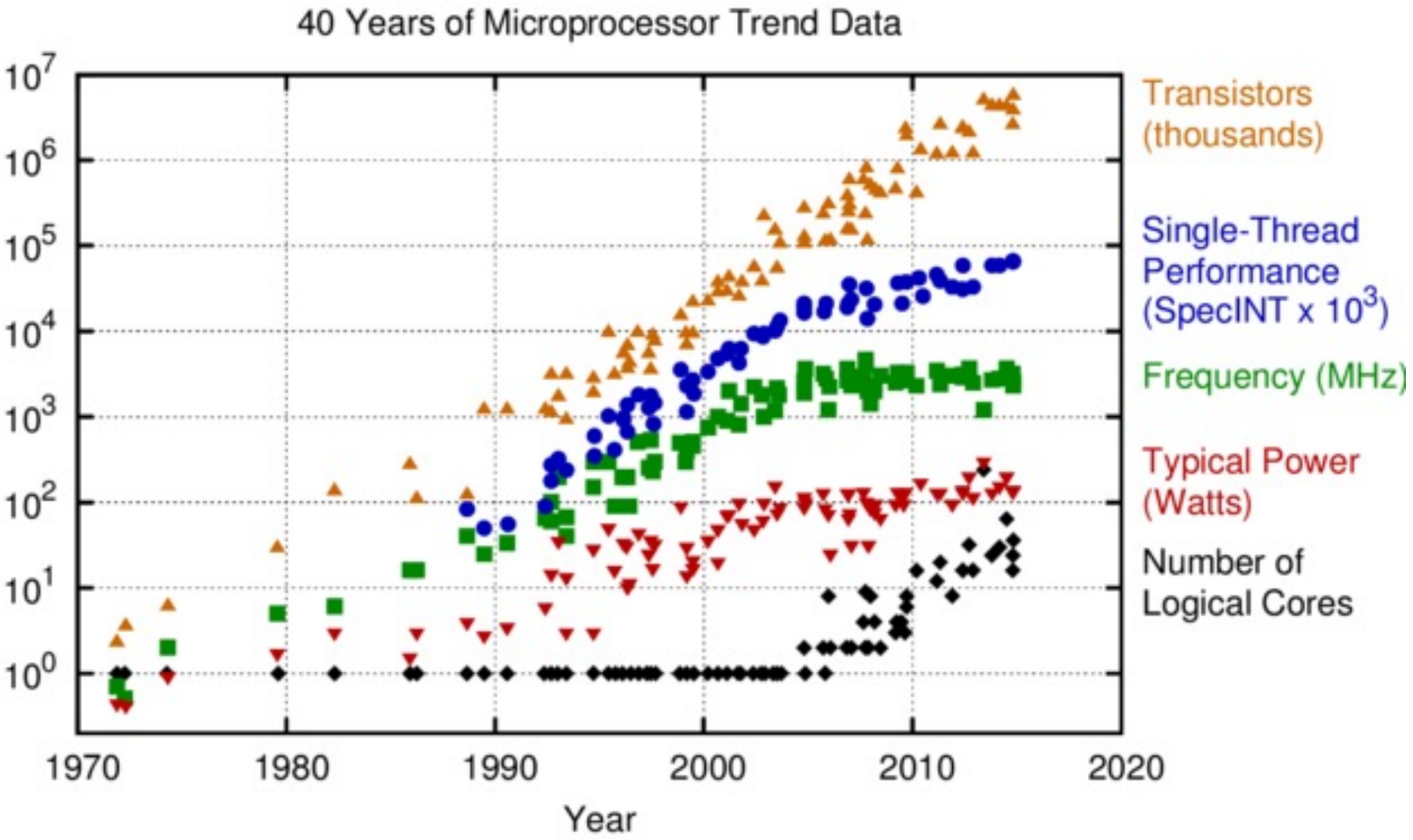
Processor Frequency Scaling



Original data up to the year 2010 collected and plotted by M. Horowitz, F. Labonte, O. Shacham, K. Olukotun, L. Hammond, and C. Batten
New plot and data collected for 2010-2015 by K. Rupp

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Delay Optimization

- Critical paths limit the operating speed of the system.
- Four main levels:
  - Architectural/Microarchitectural Level, e.g., # of pipeline stages
  - Logic Level, e.g., types of functional blocks
  - Circuit Level, e.g., transistor sizings
  - Layout Level, e.g., floorplanning
- This lecture: using simple models that offer designers intuitions on logic and circuit optimizations.
  - Invertor RC delay model: transistor -> resistor + capacitor
  - Transistor Sizing & Logical effort (next lecture)
- Generalize to other gates (next lecture)

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Administrivia

- Midterm done!
  - Great job everyone!
- New Lab this week.
  - Last lab.
  - Will start project next week.
- Homework 5 out this week.

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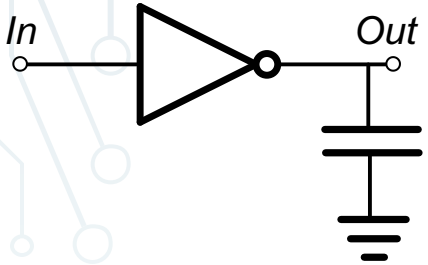
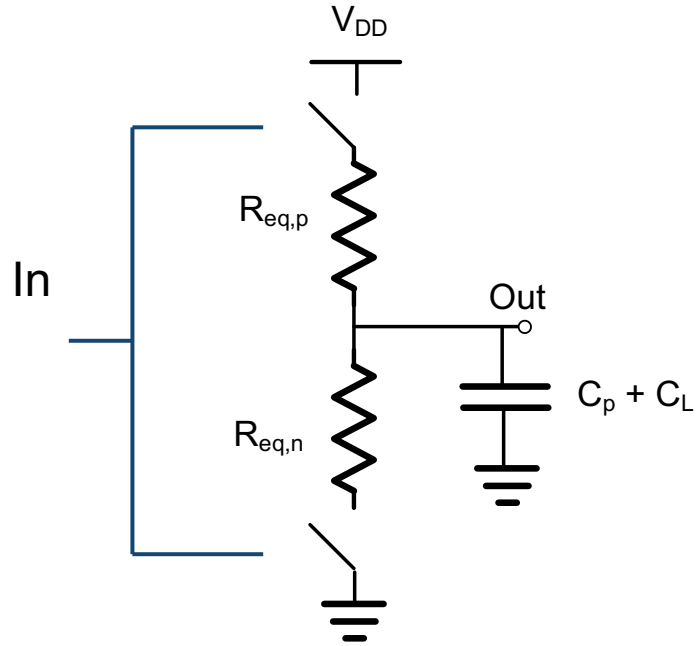
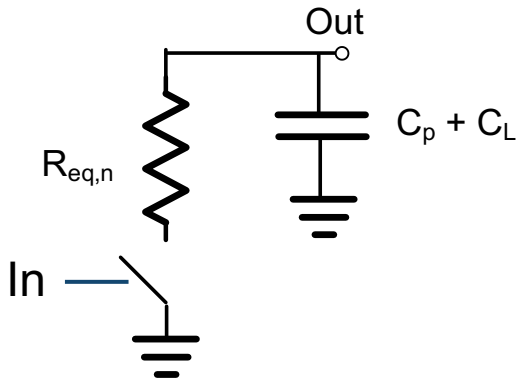
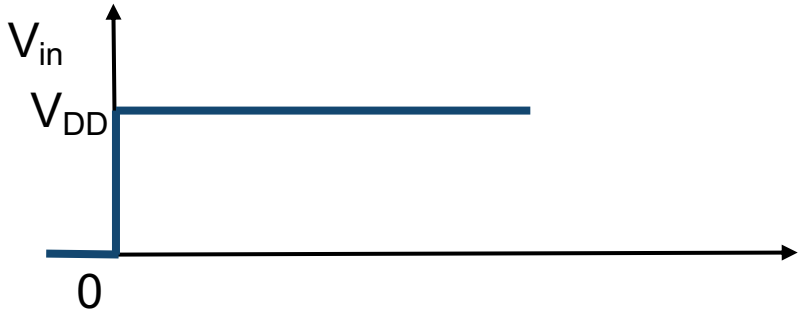
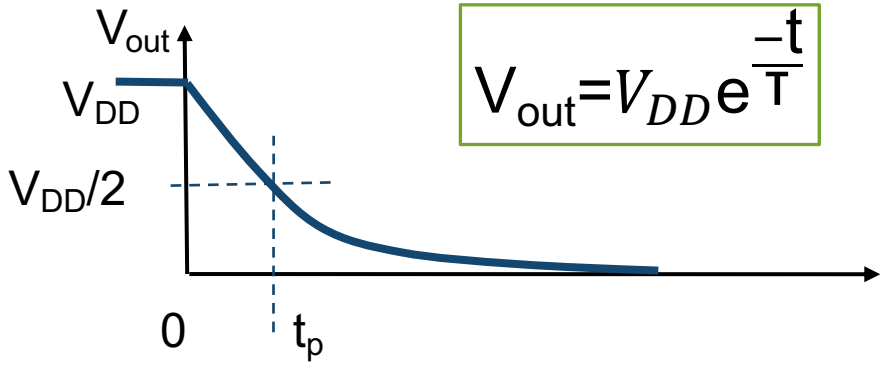
Inverter Delay: High-to-low











$$V_{out} = V_{DD} e^{\frac{-t}{\tau}}$$

$$\tau = Req_{,n}(C_p + C_L)$$

$$t_{p,HL} = (\ln 2)\tau = 0.7\, Req_{,n}(C_p + C_L)$$

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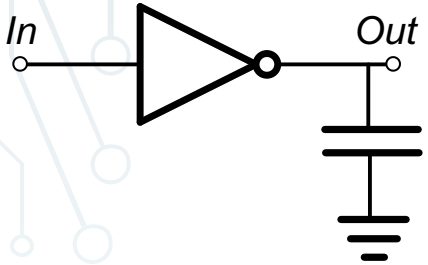
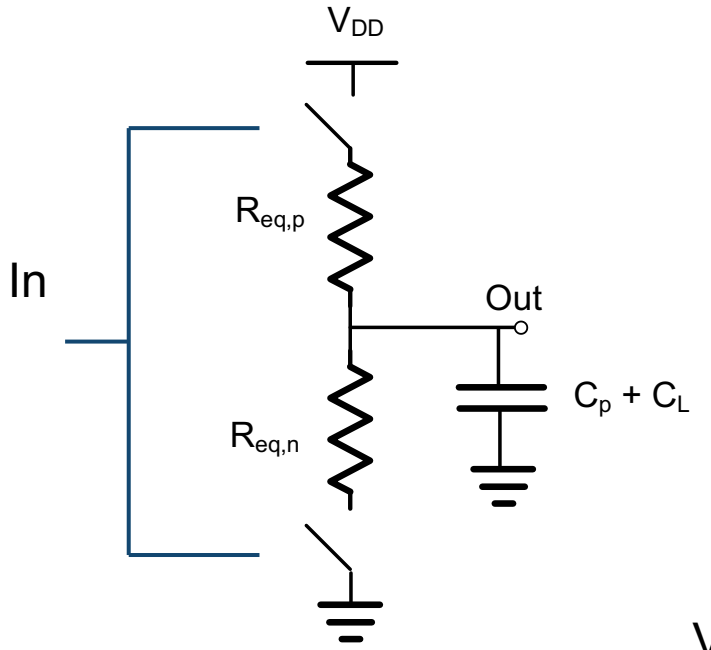
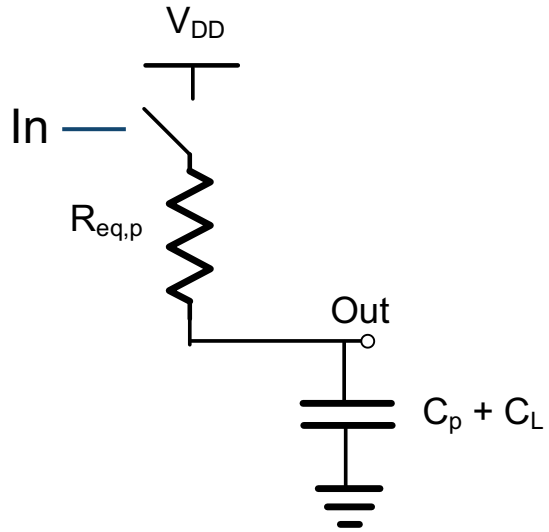
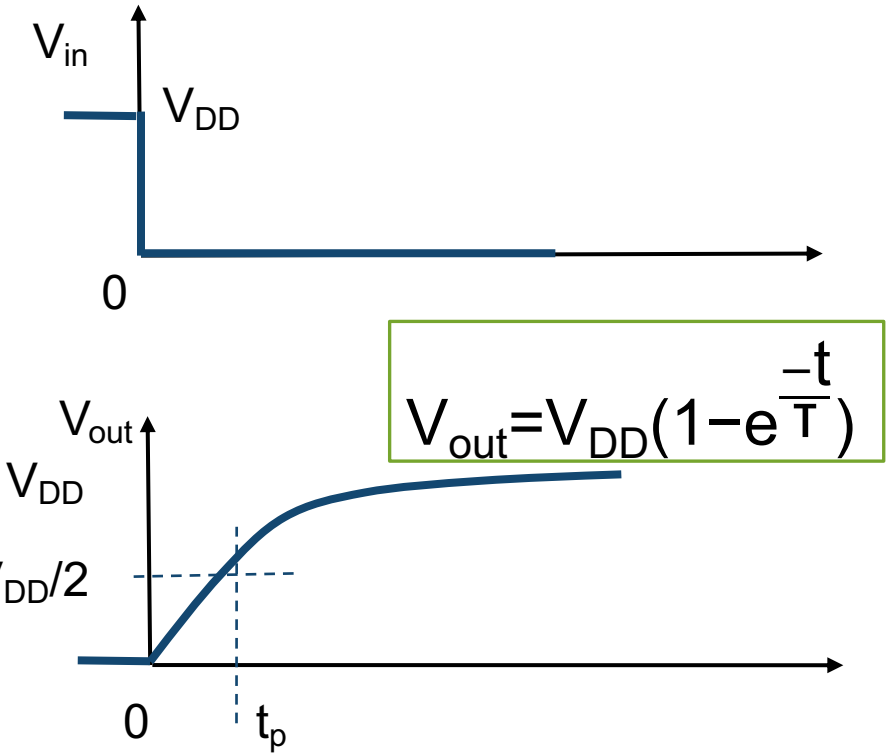
Inverter Delay: Low-to-high









$$t_{p,LH} = (\ln 2)\tau = 0.7\, Req_{,p}(C_p + C_L)$$

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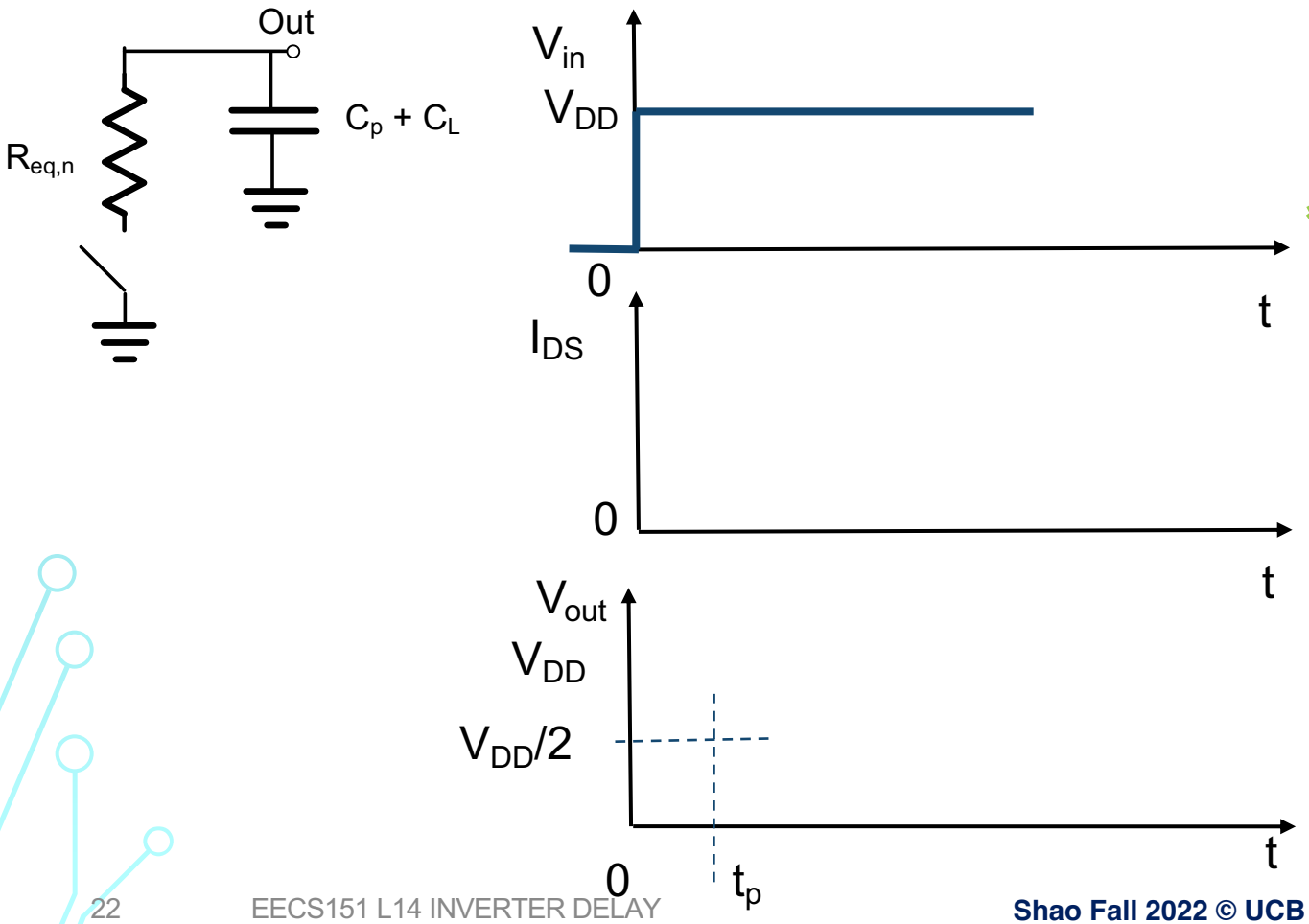
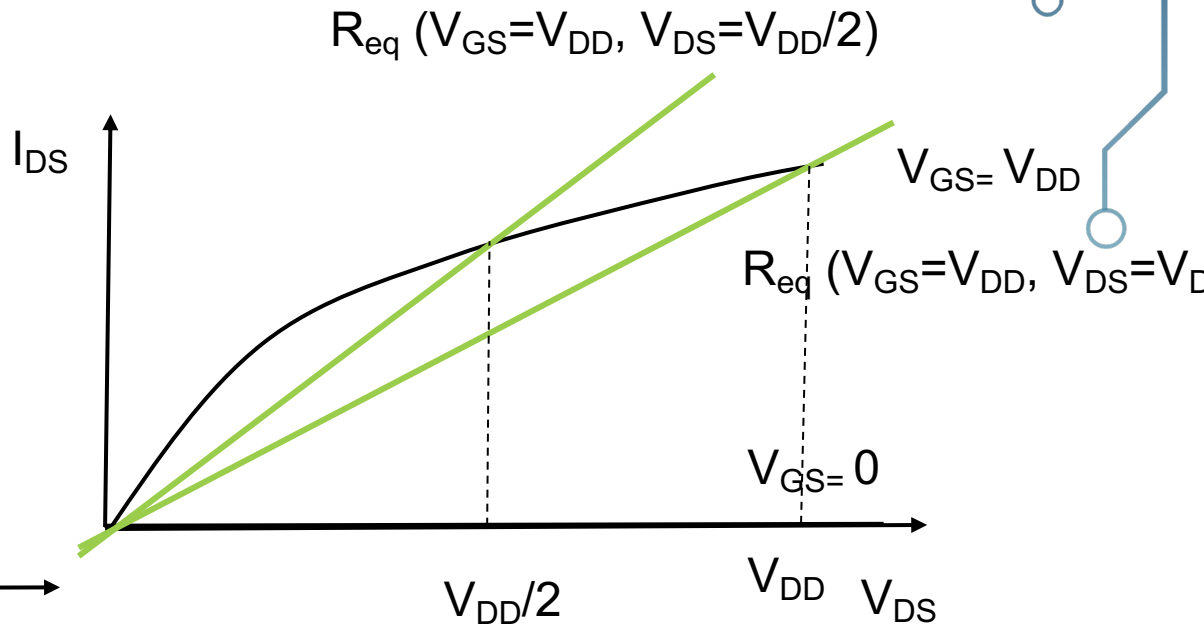
Equivalent Resistances

- Transistor I_{DS}-V_{DS} trajectory
- Averaging produces R_{eq}





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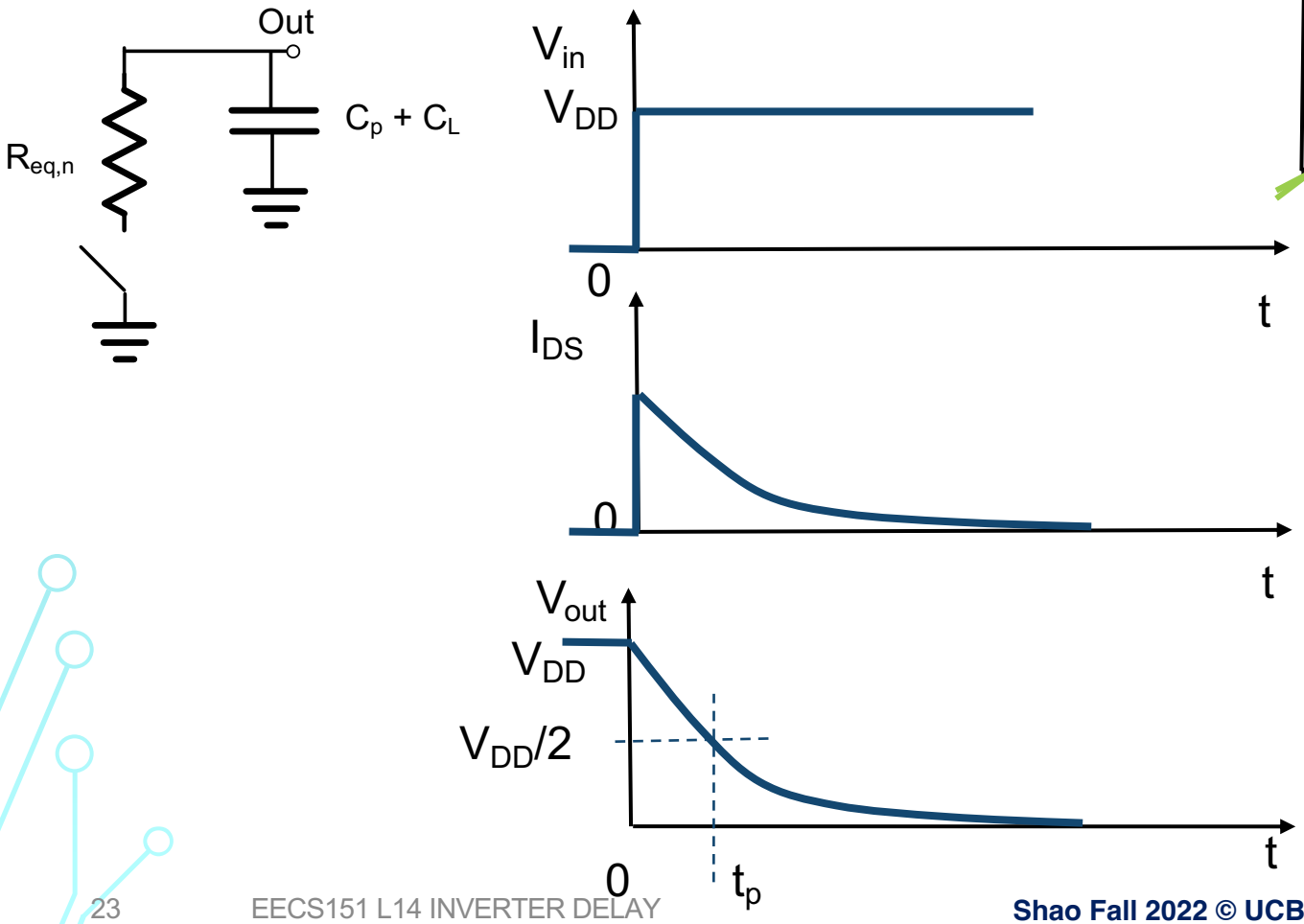
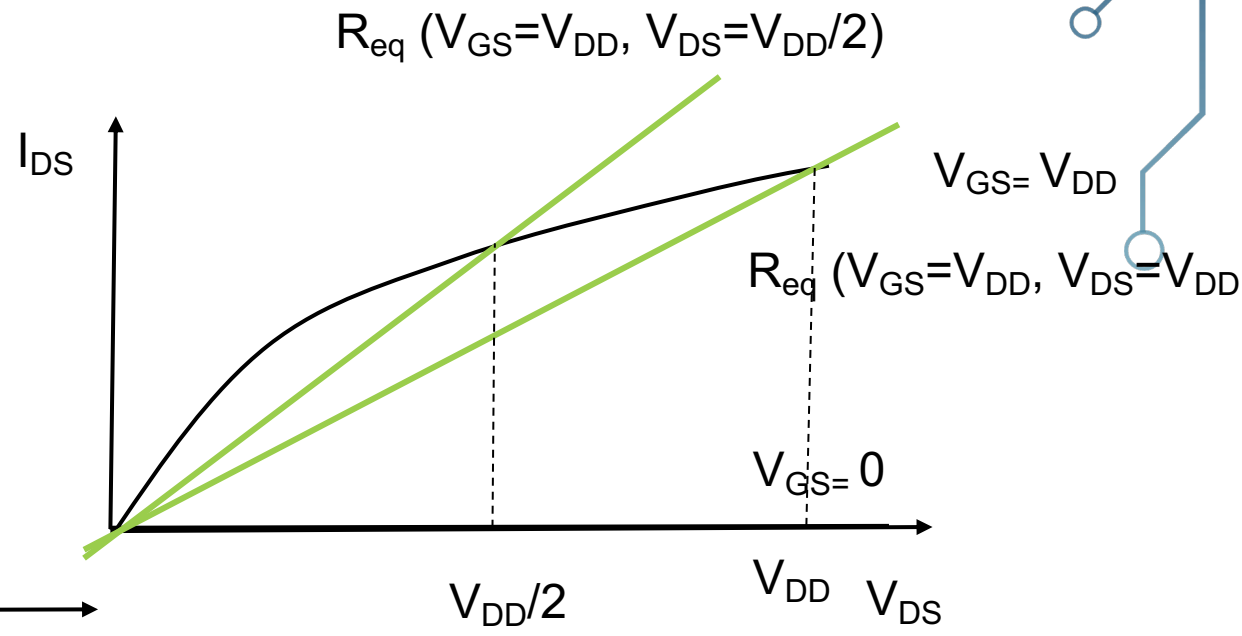
Equivalent Resistances

- Transistor I_{DS}-V_{DS} trajectory
- Averaging produces R_{eq}





$$R_{eq} = (R_{eq,start} + R_{eq,mid})/2$$

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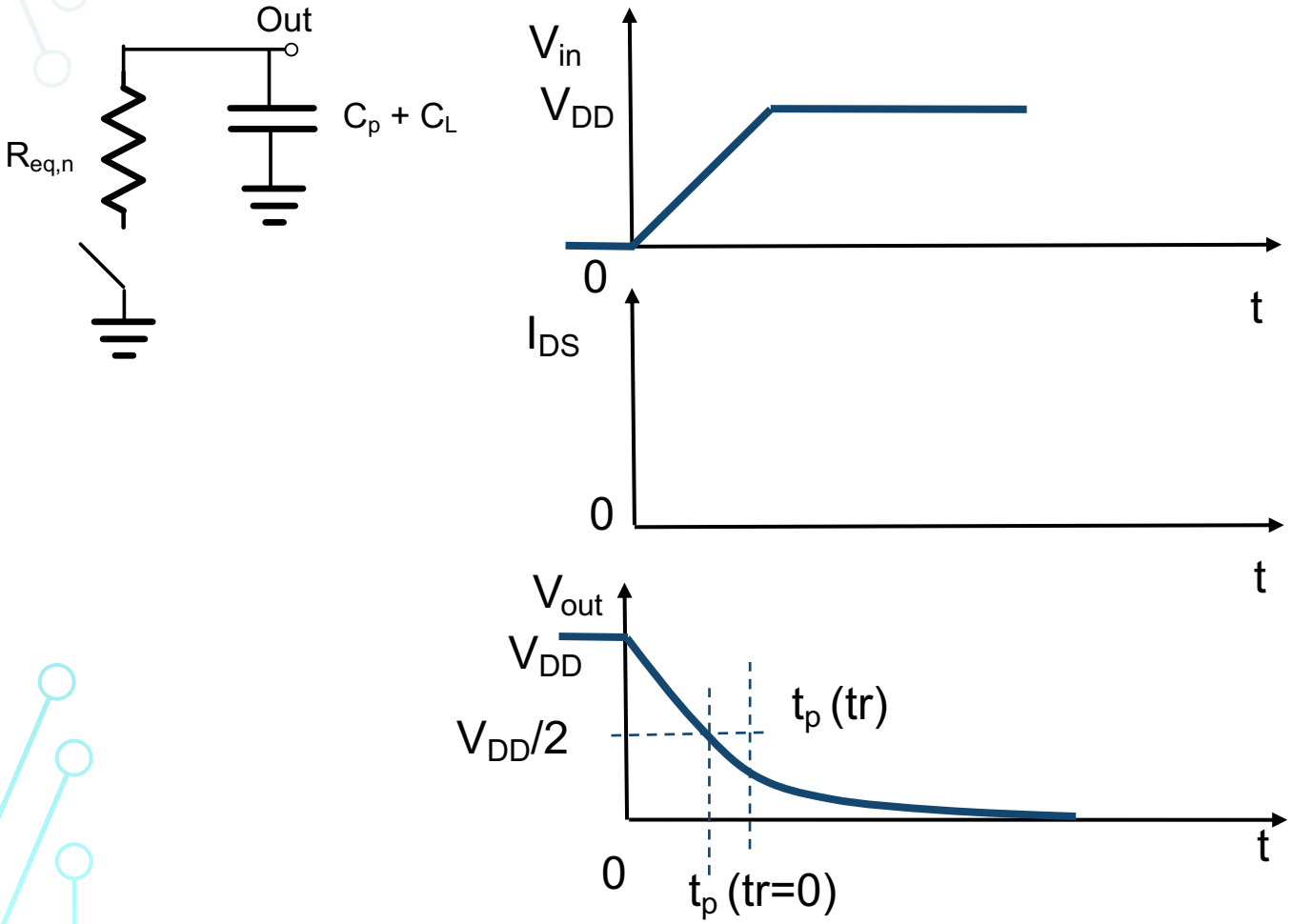
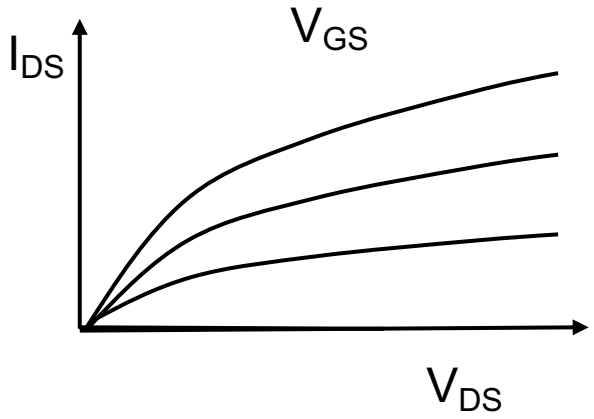
Impact of Rise/Fall times

- Impacts the I_{DS}-V_{DS} trajectory





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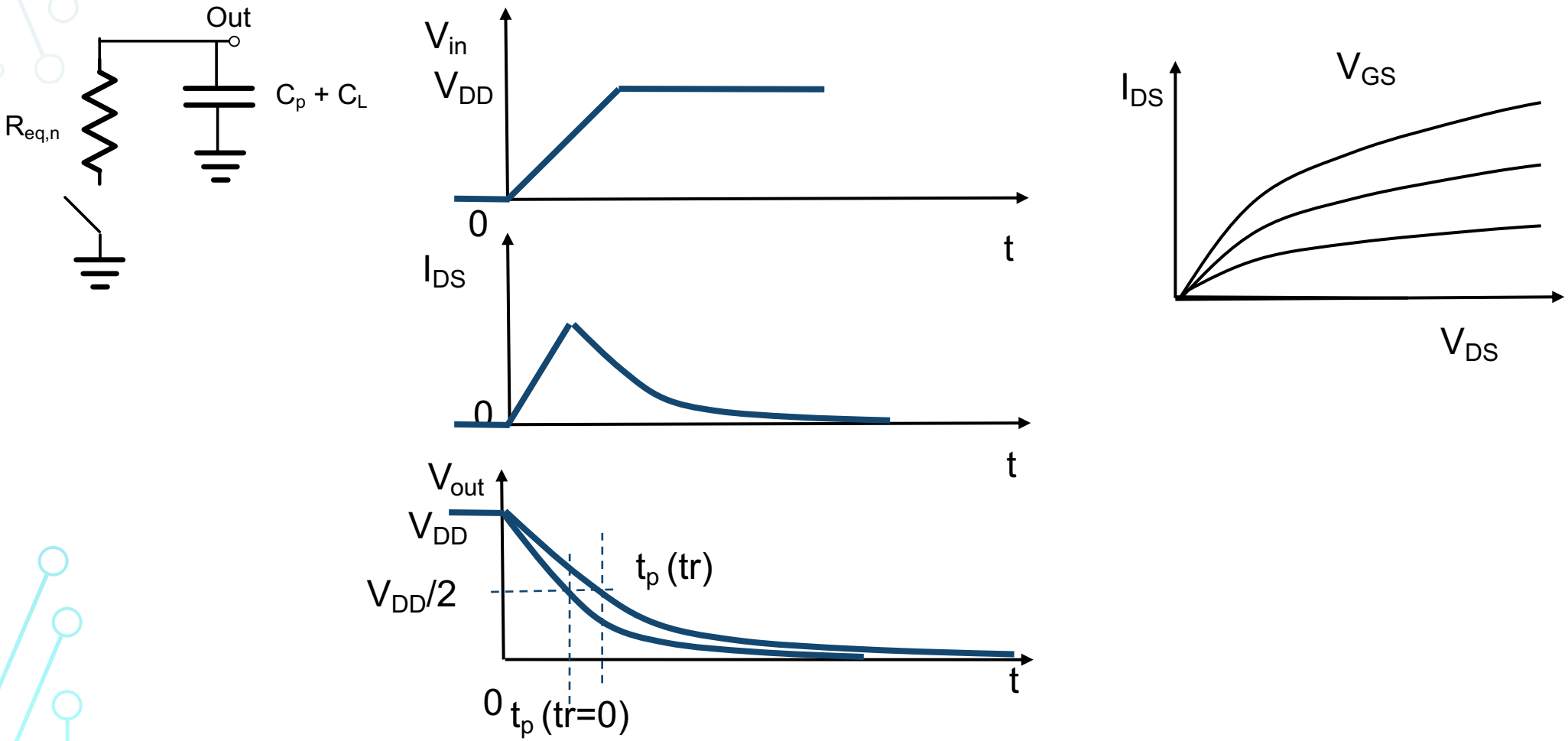
Impact of Rise/Fall times

- Impacts the I_{DS}-V_{DS} trajectory



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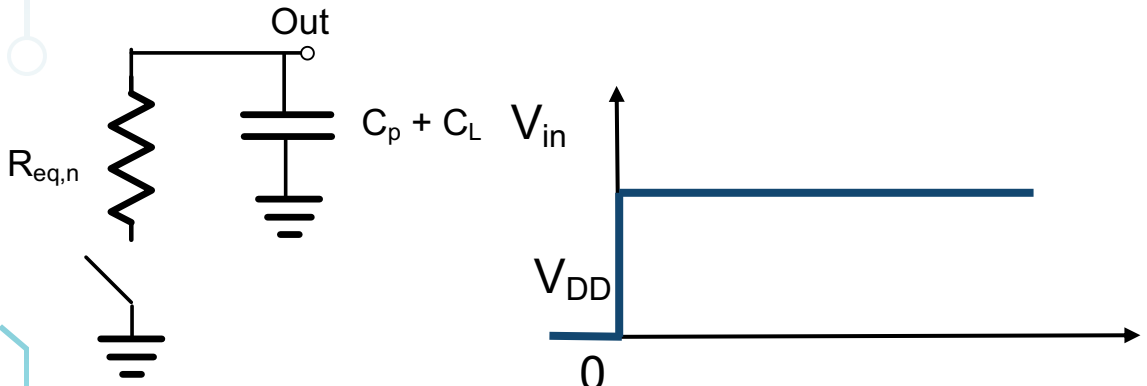
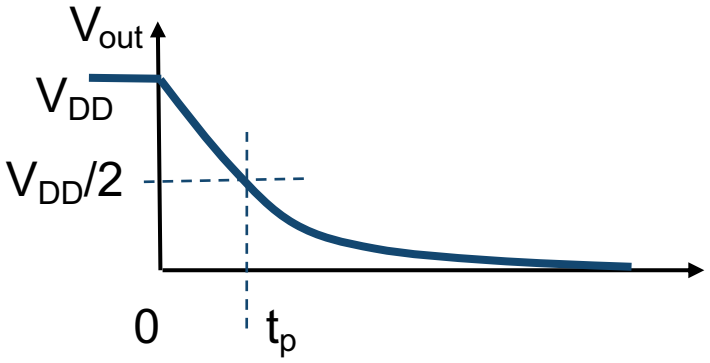
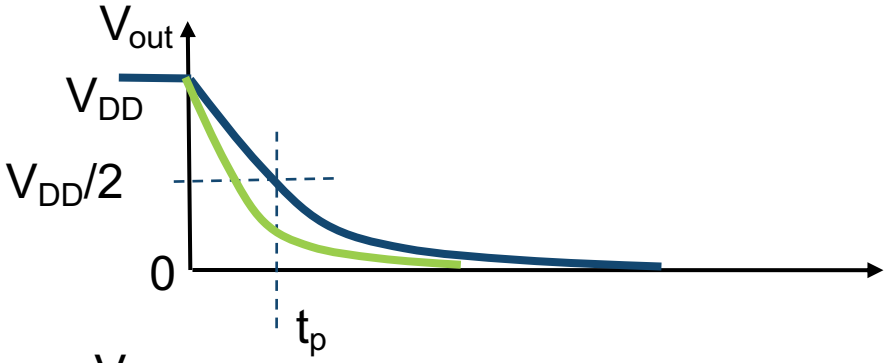
Quiz: Inverter RC Delay

- If we double the load capacitance, assuming the default Vout shown in blue, which of the following waveforms shows the new Vout?

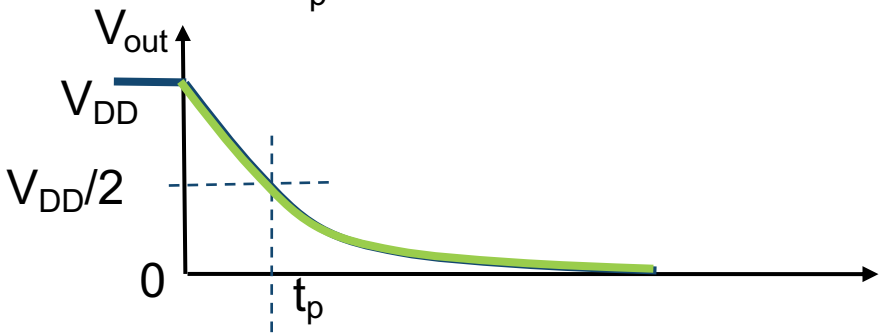




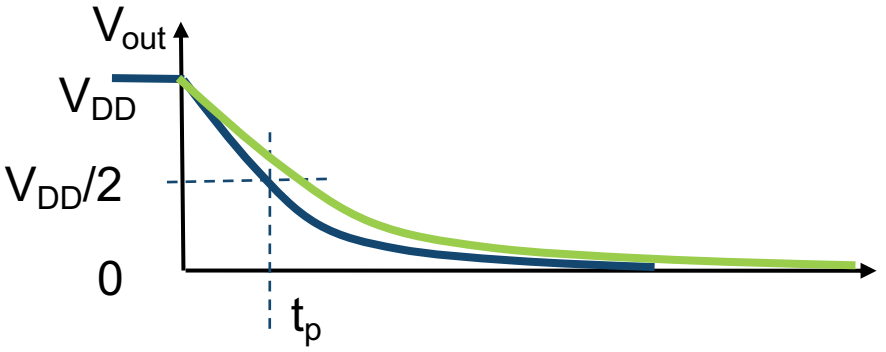
A



B



C



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Review

- CMOS Transistors and Gates
  - MOS transistor as a switch
  - Pull-up and Pull-down for CMOS design
  - CMOS Gates
- Inverter Delay
  - Delay affects achievable frequency.
  - Propagation delay from input to output
  - RC Delay model

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