EECS151/251A
Introduction to Digital Design and ICs

Lecture 22: SRAM

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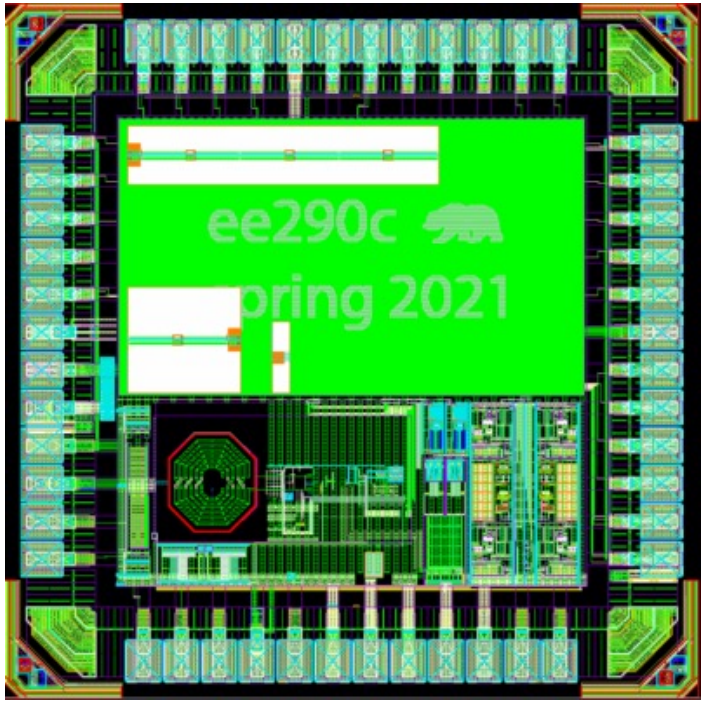
Berkeley engineering students pull off novel chip design in a single semester

In what could have important implications for engineering education as well as the field of chip design, a class of Berkeley Engineering students has successfully completed the design process — or “tape-out” — for a novel chip that will be manufactured this summer. As part of this spring’s Advanced Topics in Circuit Design course, 19 students with no prior experience in chip design went from basic introductions to tape-out by the end of a four-month period.

https://engineering.berkeley.edu/news/2021/06/berkeley-engineering-students-design-novel-chip-in-semester-long-course/



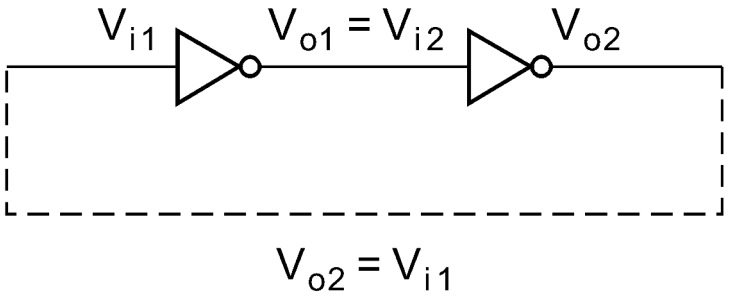
Review

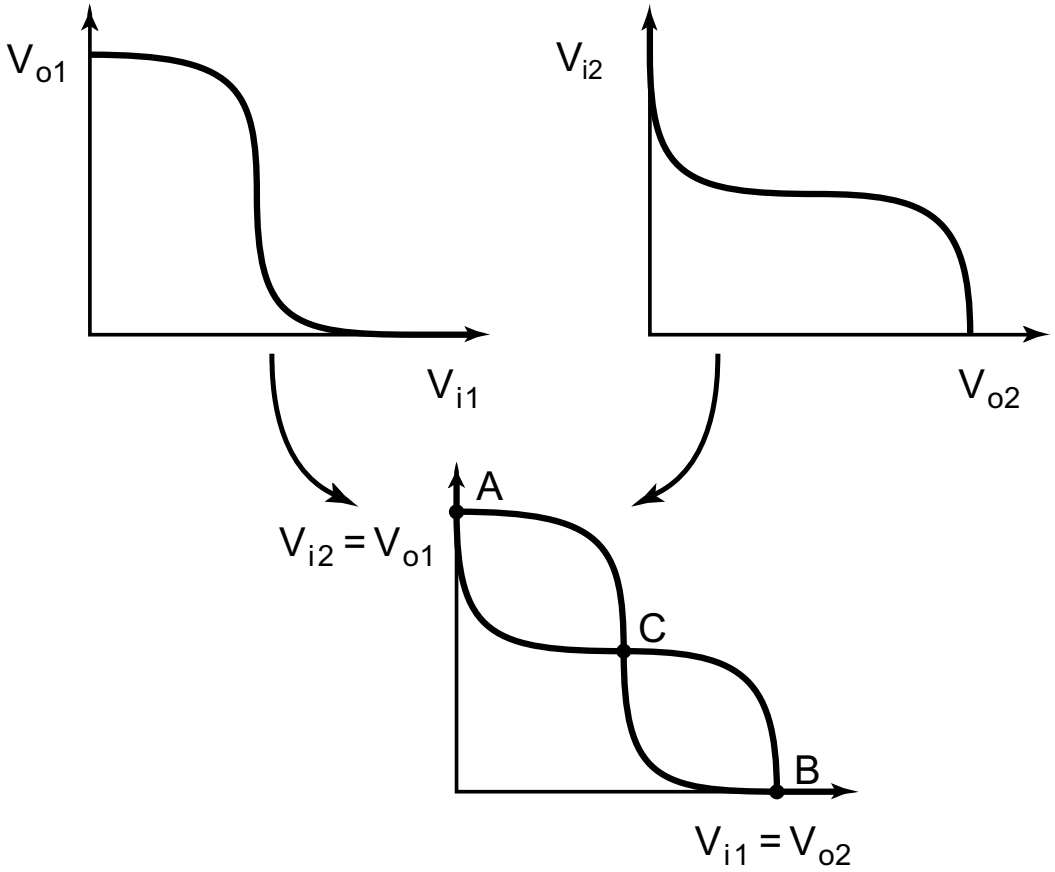
- Timing analysis for early and late signal arrivals
- Flip-flop-based pipelines are a lot easier to analyze than latch-based ones
  - Setup time
  - Hold time
  - Clk-q delay
- Flip-flop is typically a latch pair

- **FlipFlops**
  - Timing
  - **Latches**
  - **FlipFlops**

Cross-Coupled Inverter

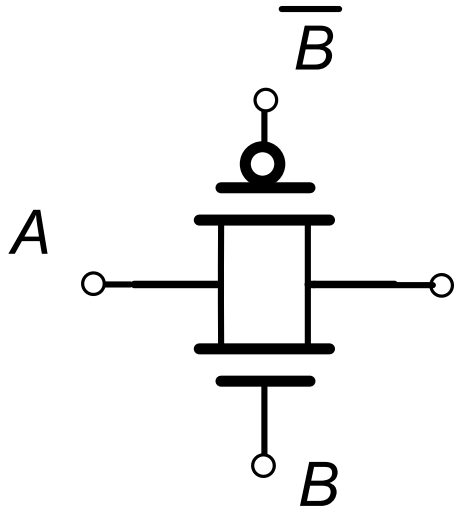
- Positive feedback stores the data





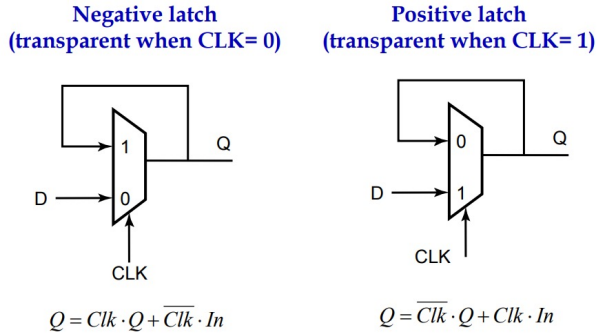
Transmission Gate

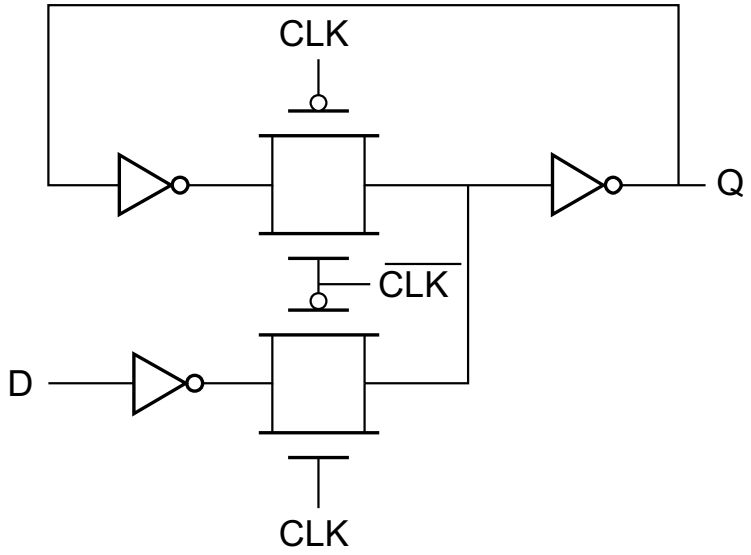
- Transmission gates are the way to build “switches” in CMOS.
- In general, both transistor types are needed:
  - ❑ nFET to pass zeros.
  - ❑ pFET to pass ones.



Writing into a Latch

Use the clock as a control signal (to break the positive feedback), that distinguishes between the transparent and opaque states

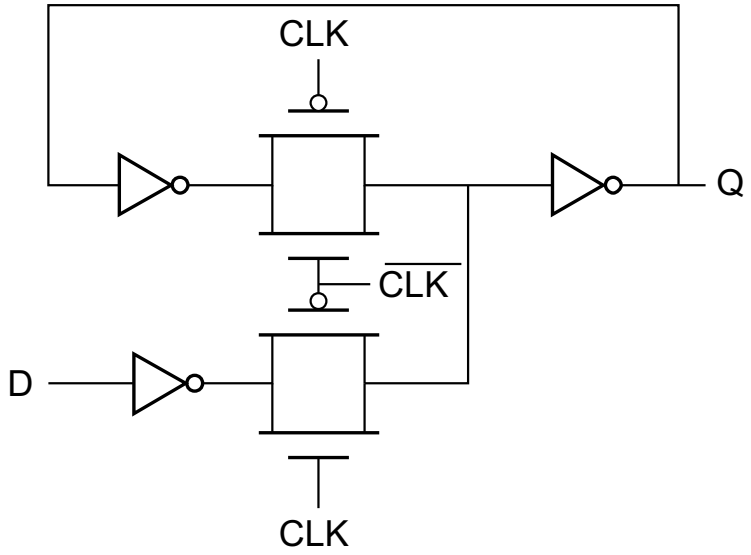




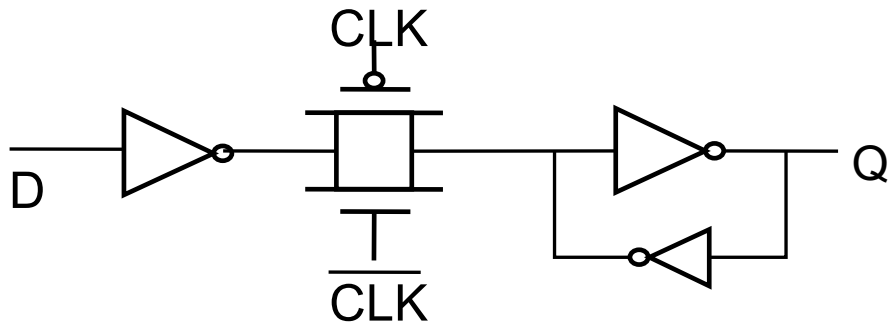
Converting into a MUX

Writing into a Latch

Use the clock as a control signal (to break the positive feedback), that distinguishes between the transparent and opaque states



Converting into a MUX

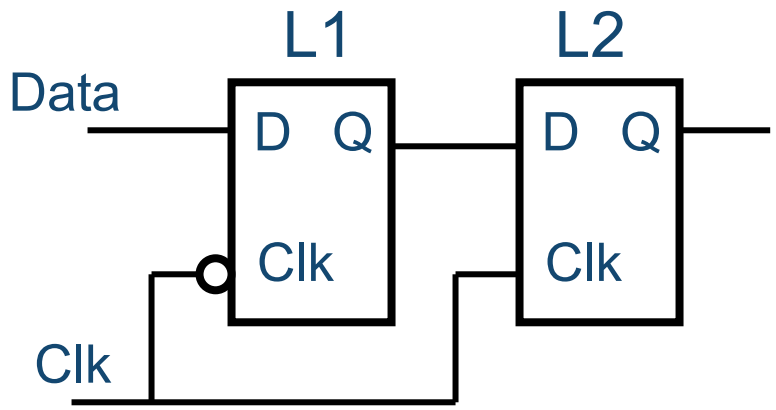


Forcing the state (depends on sizing)

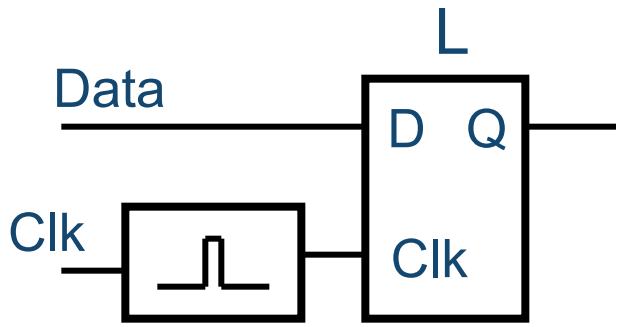
- **FlipFlops**
  - Timing
  - Latches
  - **FlipFlops**

Flip-Flops

Latch Pair

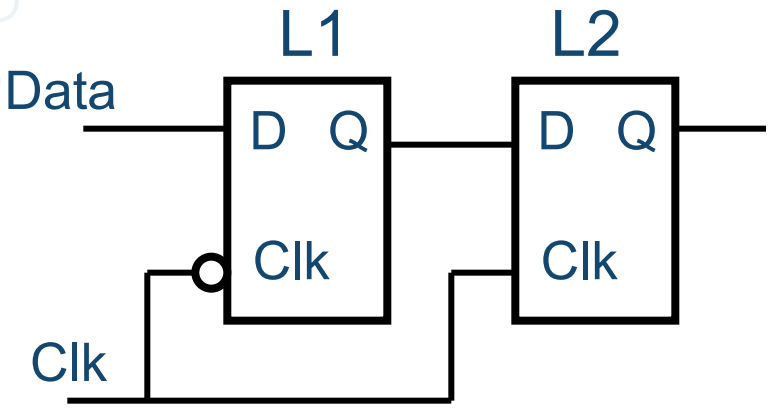


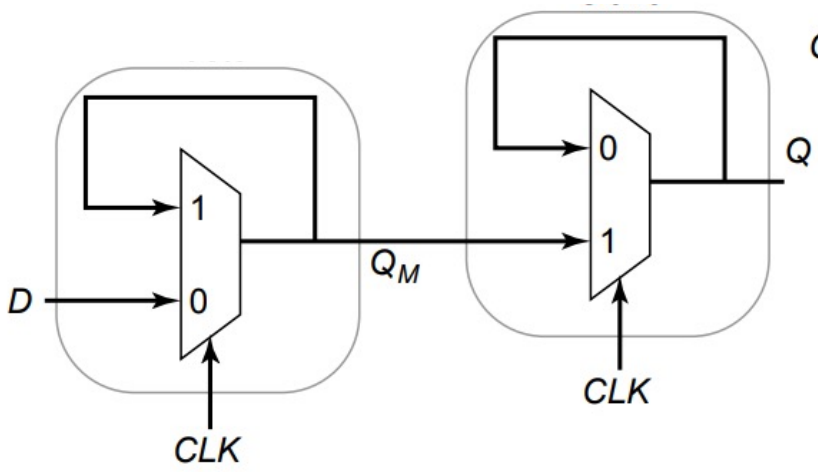
Pulse-Triggered Latch

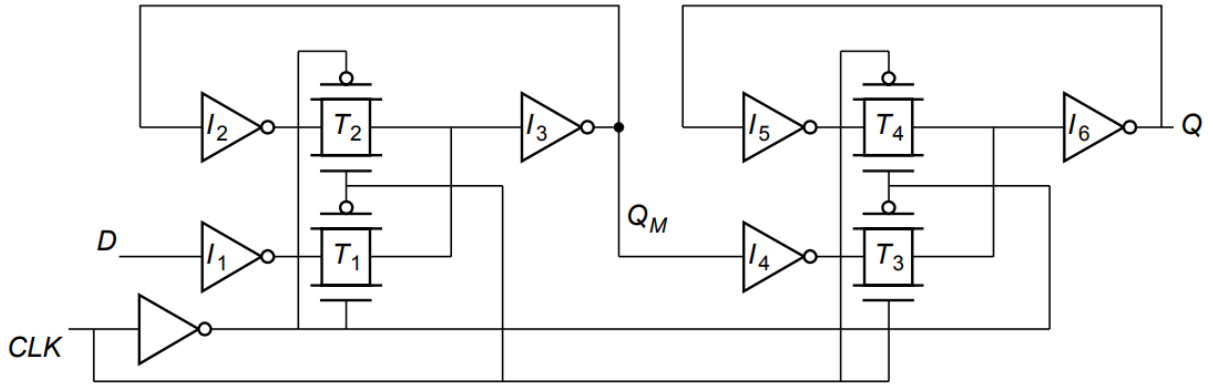


Flip-Flops

Latch Pair







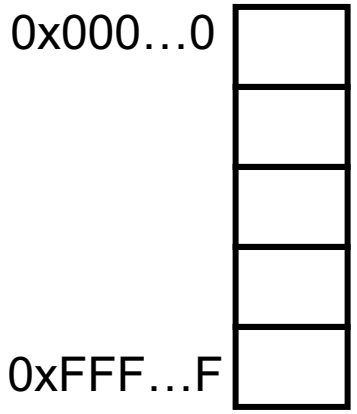
Announcement

- Project checkpoint 2 this week.
  - Reserve a slot to talk to a GSI.
- Adder/Multiplier HW will a 2-week HW.
- SystemVerilog guest lecture on Tuesday, 4/26.

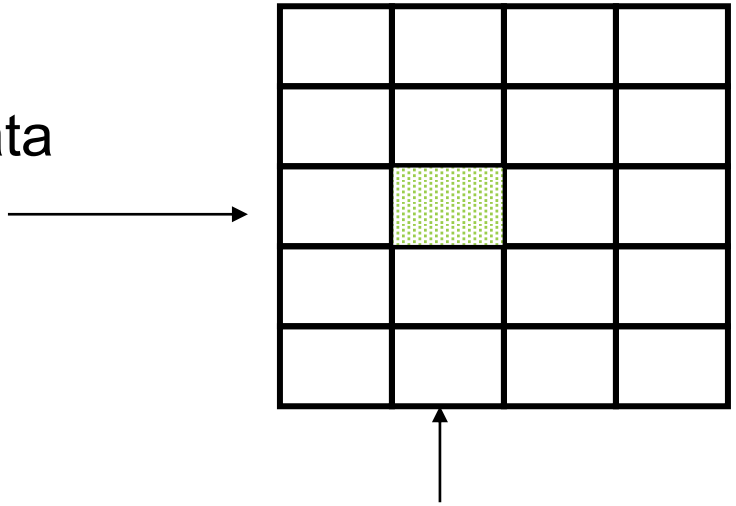
- SRAM
  - Overview
  - 6-T SRAM Cell
  - Sizing SRAM Cell

Random Access Memory Architecture

- Conceptual: Linear array of addresses
  - Each box holds some data
  - Not practical to physically realize
    – millions of 32b/64b words

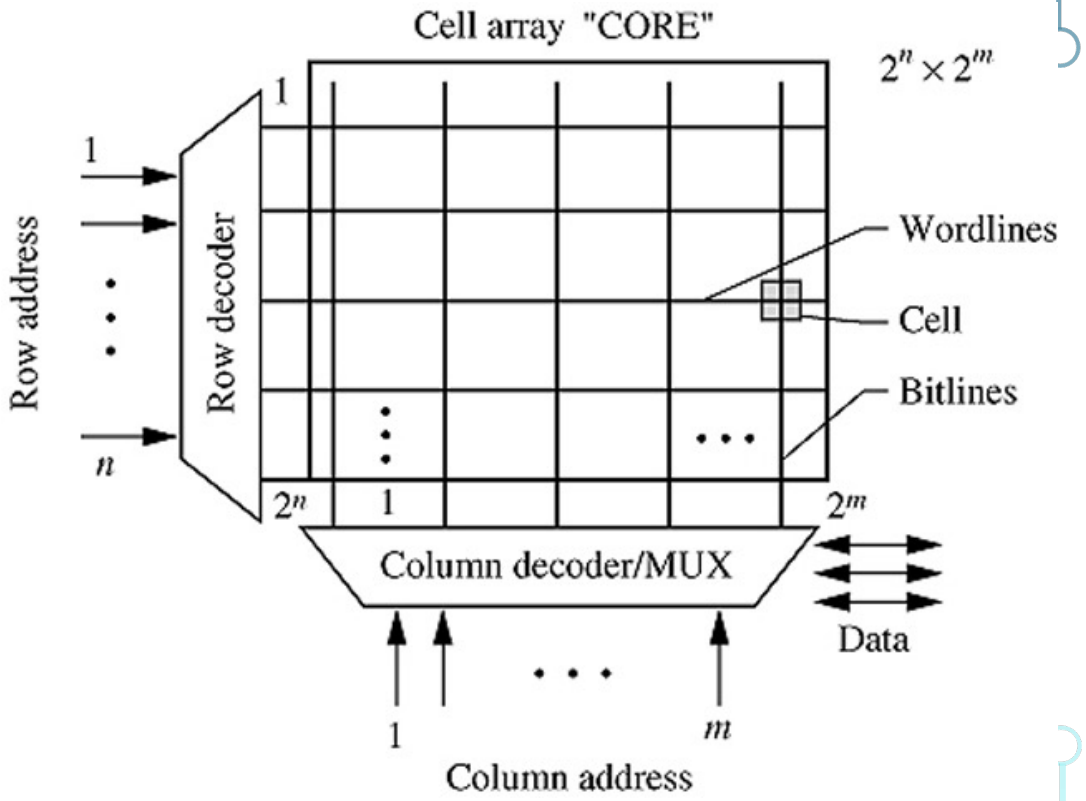


- Create a 2-D array
  - Decode Row and Column address to get data

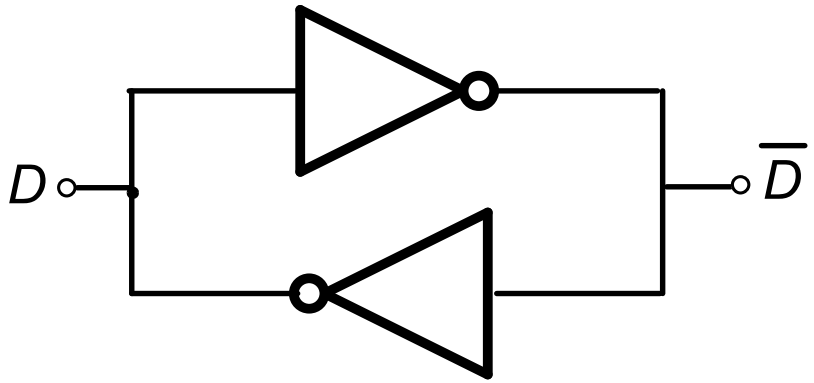


Basic Memory Array

- CORE
  - Wordlines to access rows
  - Bitlines to access columns
  - Data multiplexed onto columns
- Decoders
  - Addresses are binary
  - Row/column MUXes are ‘one-hot’ - only one is active at a time



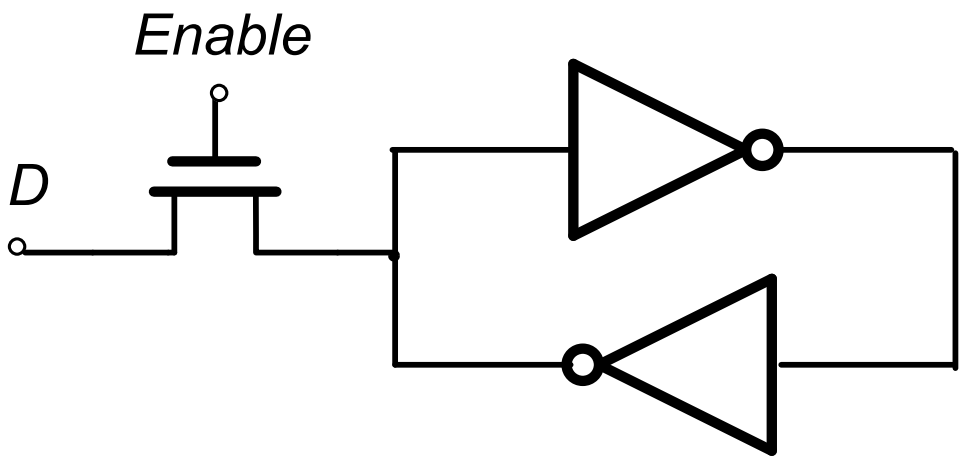
Basic Static Memory Element



- If D is high, $\overline{D}$ will be driven low
  - Which makes D stay high

- Positive feedback
- Same principle as in latches

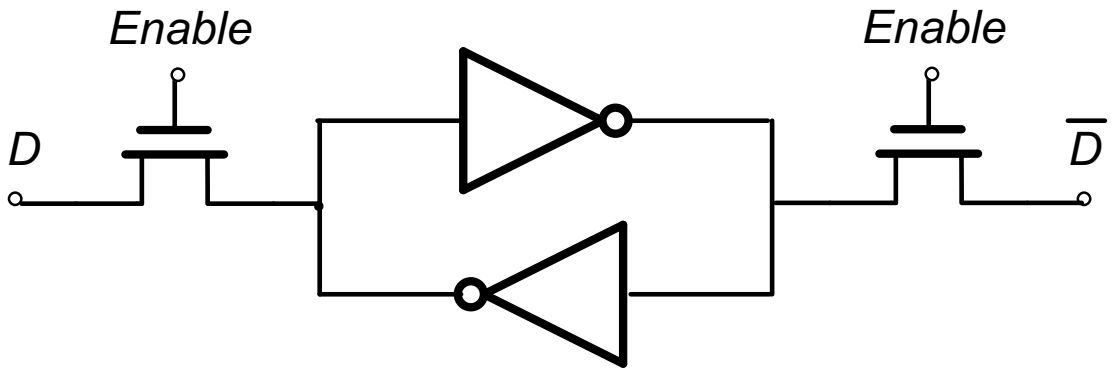
Writing into a Cross-Coupled Pair



- This is a 5T SRAM cell
  - Access transistor must be able to overpower the feedback; therefore must be large
  - Easier to write a 0, harder to write 1 (Vdd-Vth)
- Can implement as a transmission gate as well; single-ended 6T cell

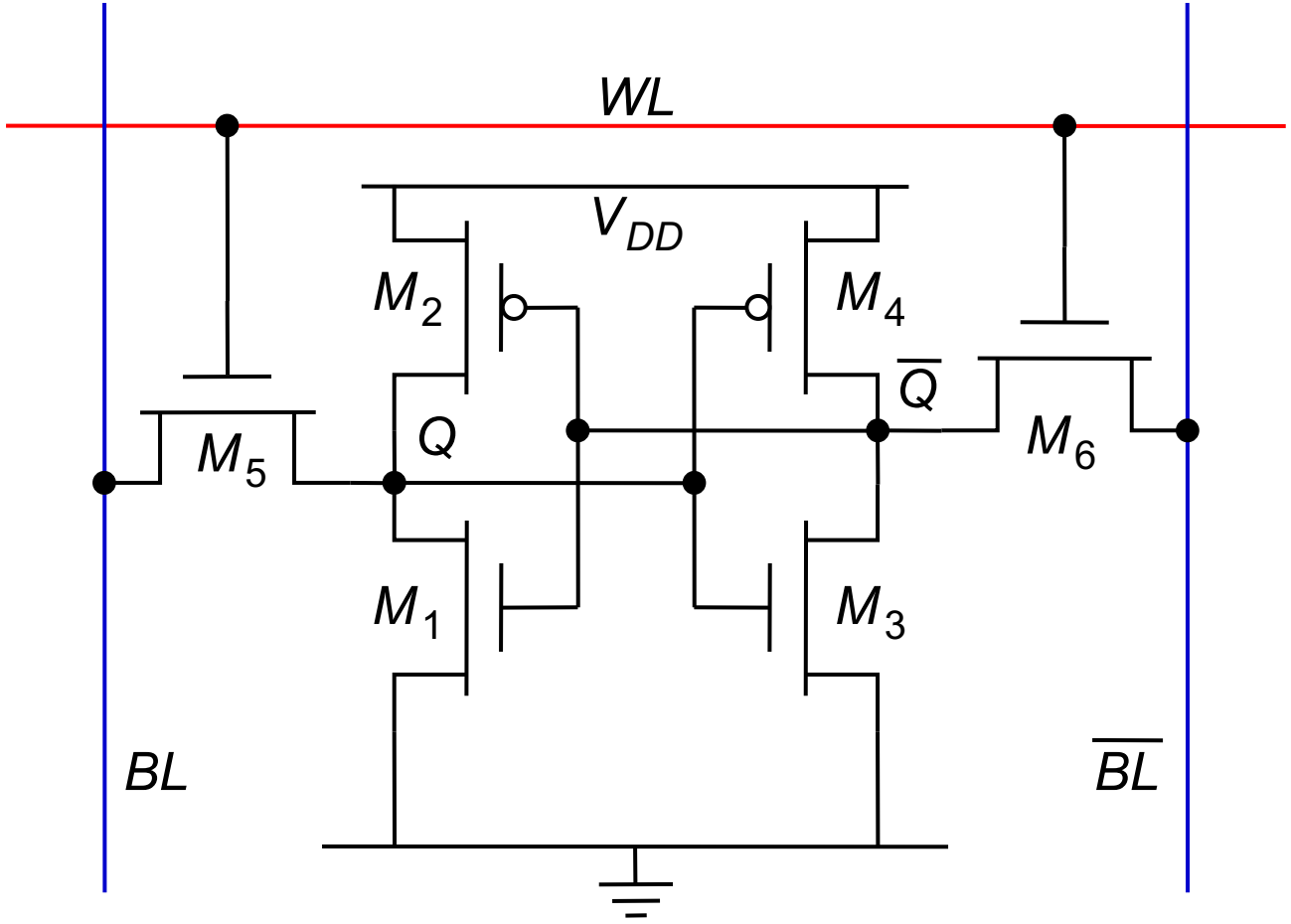
- There is a better solution…

SRAM Cell



Since it is easier to write a 0 through NMOS, write only 0s, but on opposite sides!

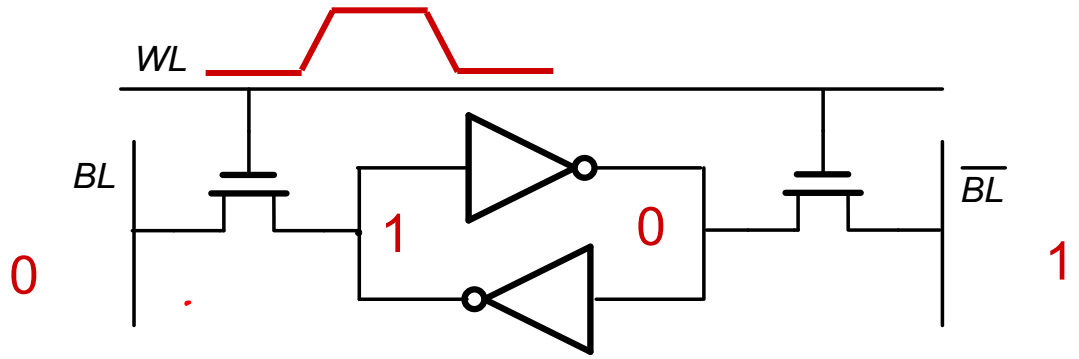
6-transistor CMOS SRAM Cell



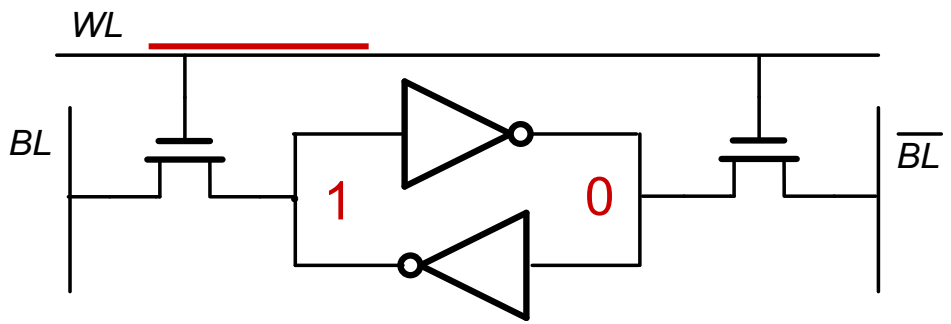
- Wordline (WL) enables read/write access for a row
- Data is written/read differentially through shared BL, $\overline{BL}$

SRAM Operation

Write

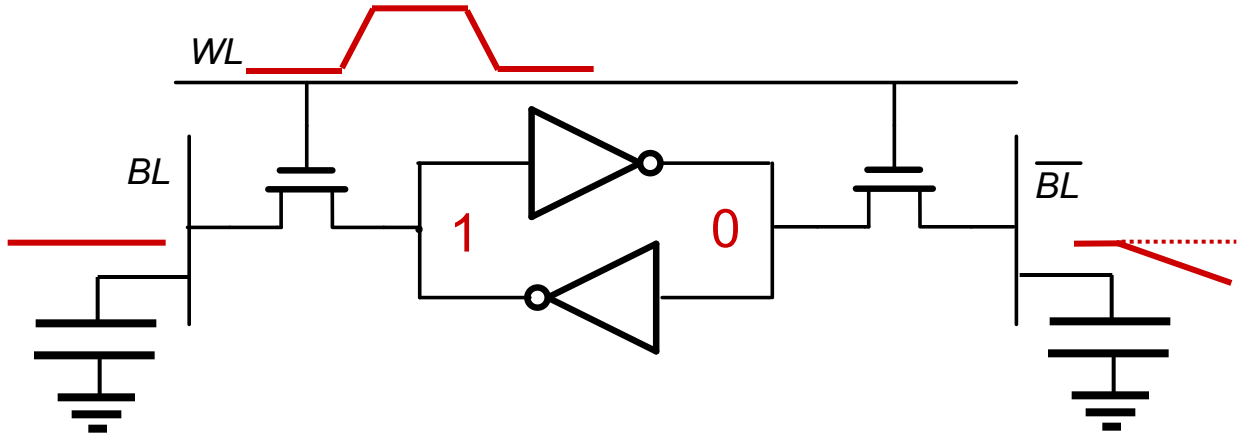


Hold



SRAM Operation

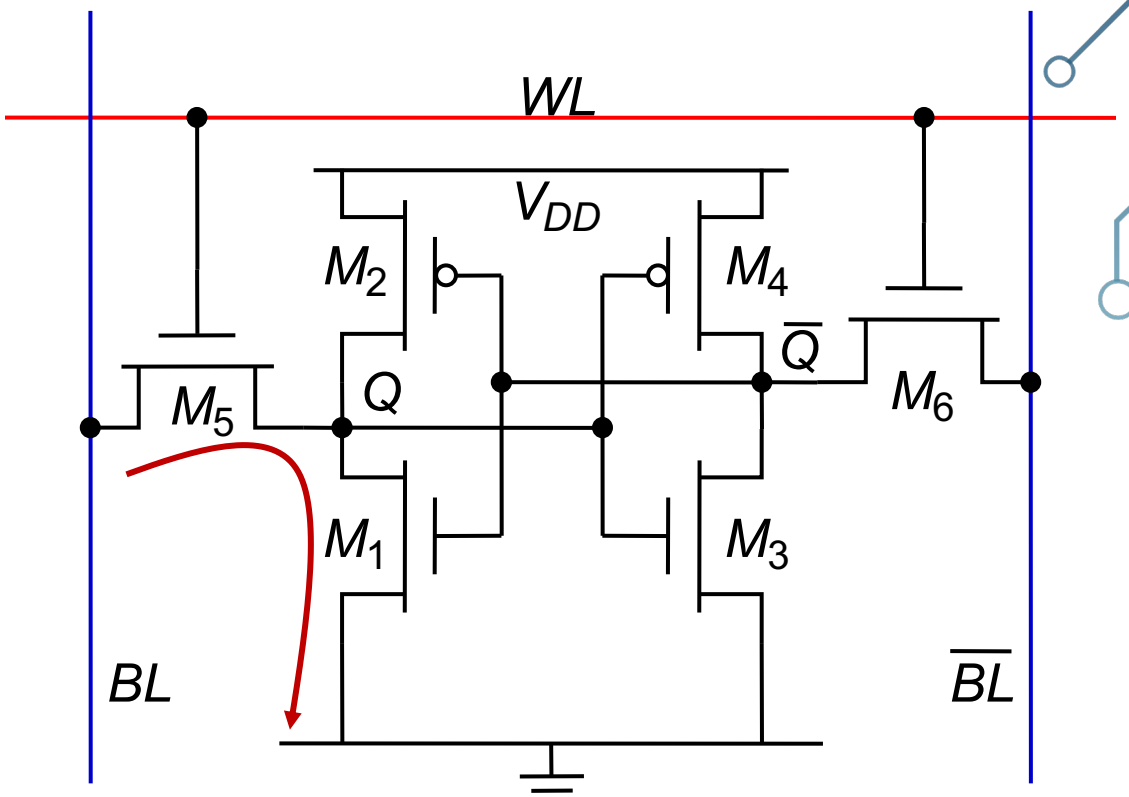
Read



Pre-charge both BLs to Vdd.
SRAM read in non-destructive
- Reading the cell should not destroy the stored value

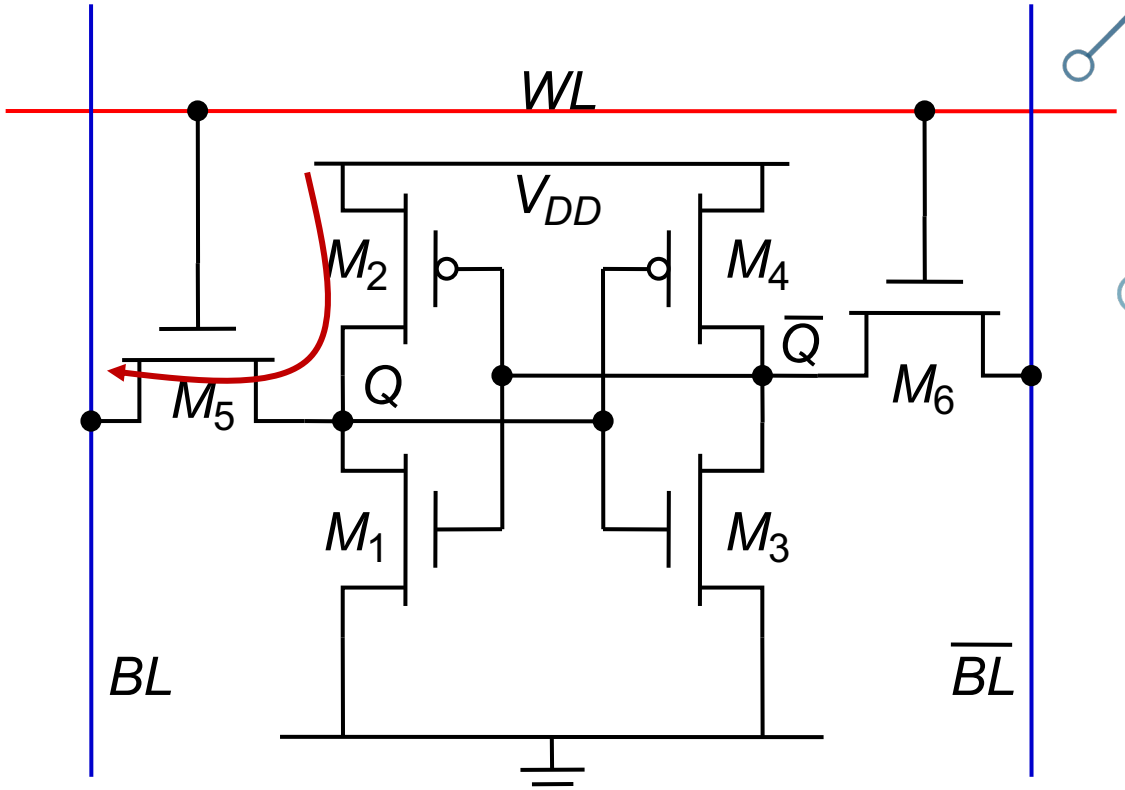
Sizing SRAM Cell

- Read stability: Cell should not change value during read
  - Q = 0: M_5, M_1 both on
  - Voltage divider between M_5, M_1
  - V_Q should stay low, not to flip M_4-M_3 inverter
  - R1 < R5 => $(W/L)_1 > (W/L)_5$
- Typically $(W/L)_1 = 1.5\ (W/L)_5$
  - In FinFETs: $(W/L)_1 = 2(W/L)_5$
- Read speed: Both M_5 and M_1



Sizing SRAM Cell

- Writeability: Cell should be writeable by pulling BL low
  - Q = 1, M_5, M_2 both on
  - Voltage divider between M_5, M_2
  - V_Q should pull below the switching point of M_4-M_3 inverter
  - R5 < R2 => $(W/L)_5 > (W/L)_2$
- Typically $(W/L)_5 = (W/L)_2$ in planar
  - In FinFETs: $(W/L)_5 = 2(W/L)_2$
  - Pull Up: Access: Pull Down:
    - 1:2:2 and 1:2:3 sizing



True or False

1. Transistor leakage doesn’t affect SRAM read speed.
2. One should write into an SRAM cell by pulling BL high.
3. One can write into a part of a selected WL.

Review

- Flip-flop is typically a latch pair
- Setup and hold times are defined at constant percentage increases over clk-q delay
- SRAM has unique combination of density, speed, power
- SRAM cells sized for stability and writeability