EECS151/251A
Introduction to Digital Design and ICs

Lecture 21: FlipFlops

Sophia Shao

1 Tera Floating-point Operations/second (TFLOPS)

ASCI Red, with over 6,000 200MHz Pentium Pros and a cost of $46 million ($67 million today), was the first supercomputer to break the 1 teraflop barrier. Later upgraded to 9,298 Pentium II Xeons, ASCI Red reached 3.1 teraflops. It was the fastest supercomputer in the world for four years, and also the first supercomputer installation to use more than 1 megawatt of power. It was only decommissioned in 2006, after 10 years of use by the Sandia National Laboratories.

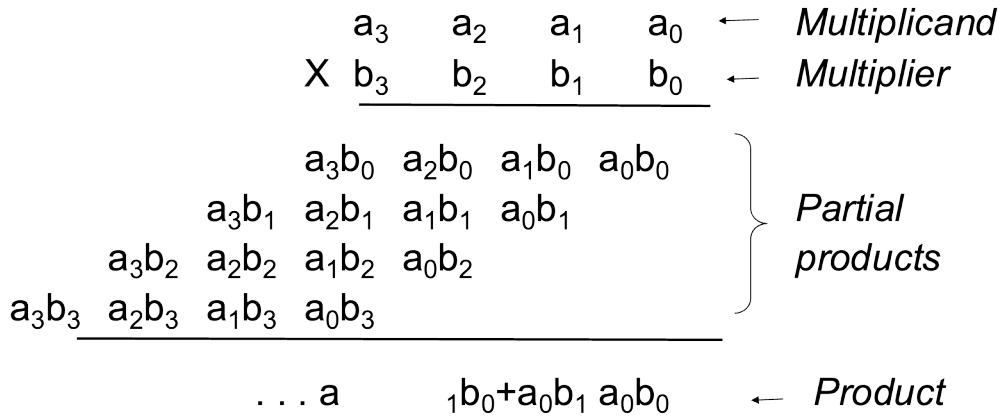
https://www.extremetech.com/extreme/125271-the-history-of-supercomputers/6

1996

2019

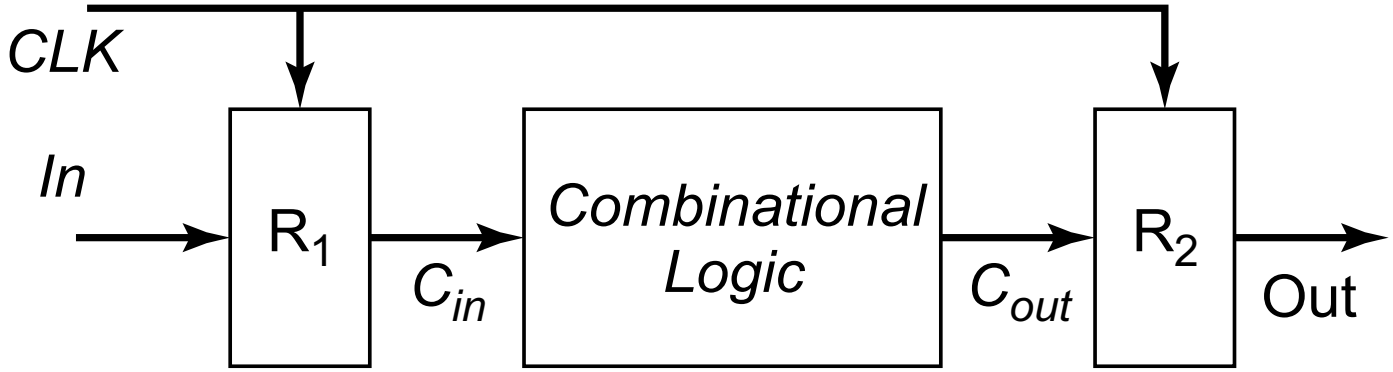
Review

- Binary multipliers have three blocks:
  - Partial-product generation
  - Partial-product accumulation
- Partial-Product accumulation
  - Carry-save adder
  - Wallace Tree multiplier
- Partial-Product Generation
  - Booth Encoding



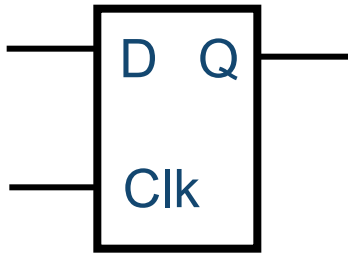
- FlipFlops
  - Timing
  - Latches
  - FlipFlops

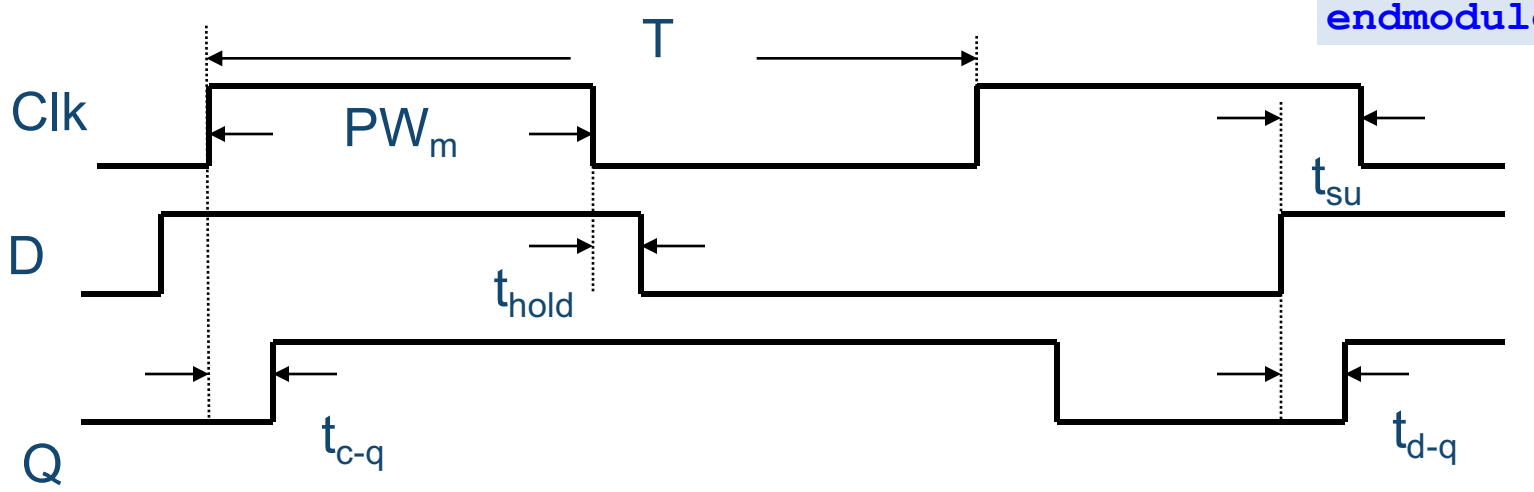
Sequential Logic



Latch

- Latch is transparent high or low



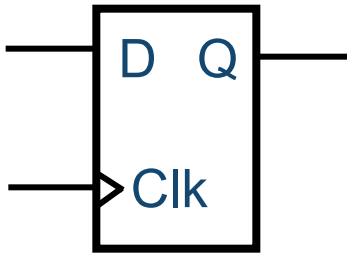



```
module latch
(
    input clk,
    input d,
    output reg q
);

  always @(clk or d)
  begin
    if ( clk )
      q <= d;
  end

endmodule
```

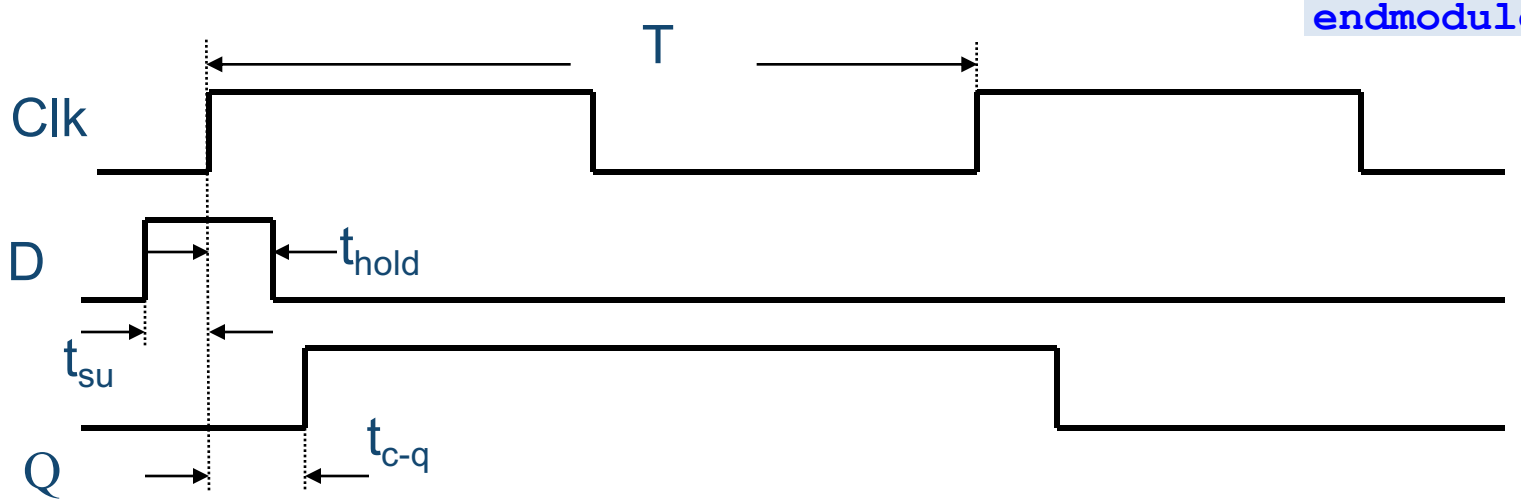
Delays can be different for rising and falling data transitions

Flip-Flop

- Flip-flop is edge-triggered



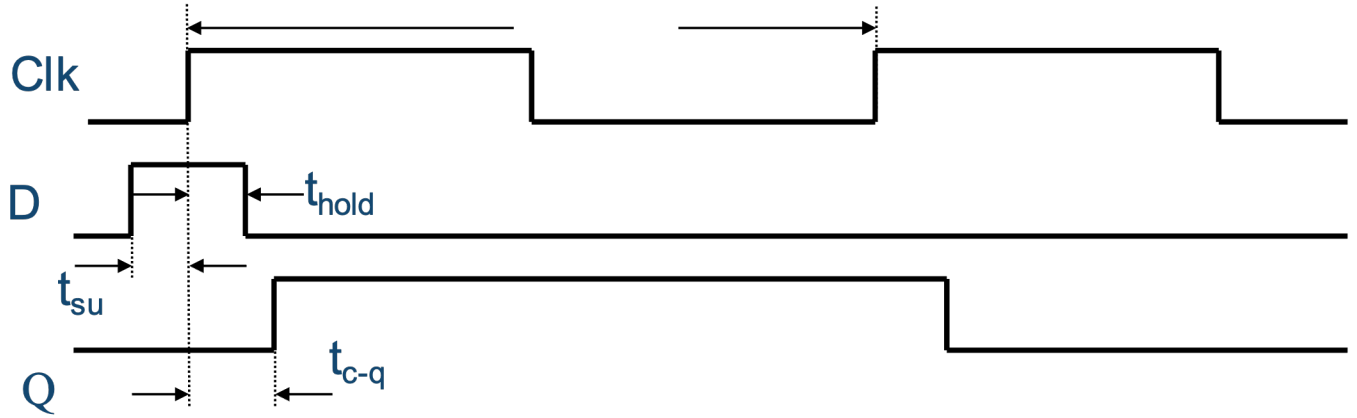

```
module flipflop
(
    input clk,
    input d,
    output reg q
);

  always @(posedge clk)
  begin
    q <= d;
  end

endmodule
```



Delays can be different for rising and falling data transitions

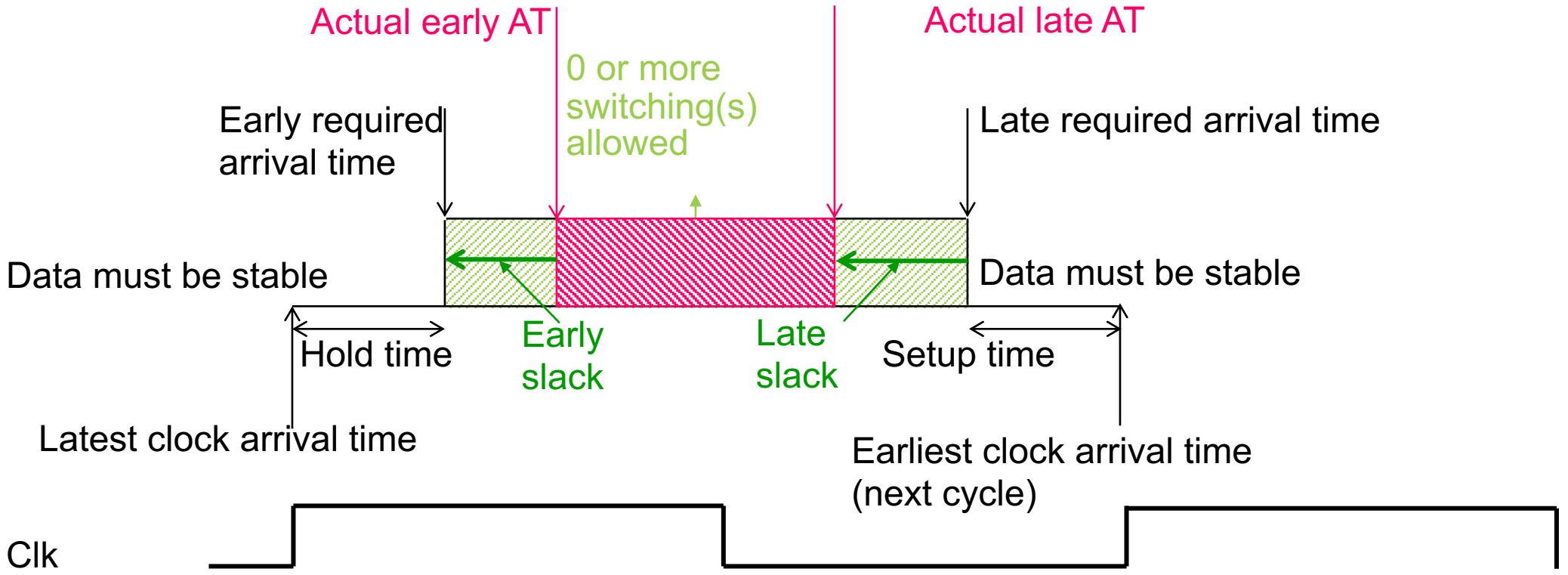
Flip-Flop Timing Characterization

- Combinational logic delay is a function of output load and input slope
- Sequential timing (flip-flop):
  - **Setup** time = the amount of time ***before*** a clock edge that the data input needs to be stable to be properly latched internally
  - **Hold** time = the amount of time ***after*** a clock edge that the data input needs to be stable for
  - **Clk-q** time = delay from a clock edge to data output q being updated with the new value written



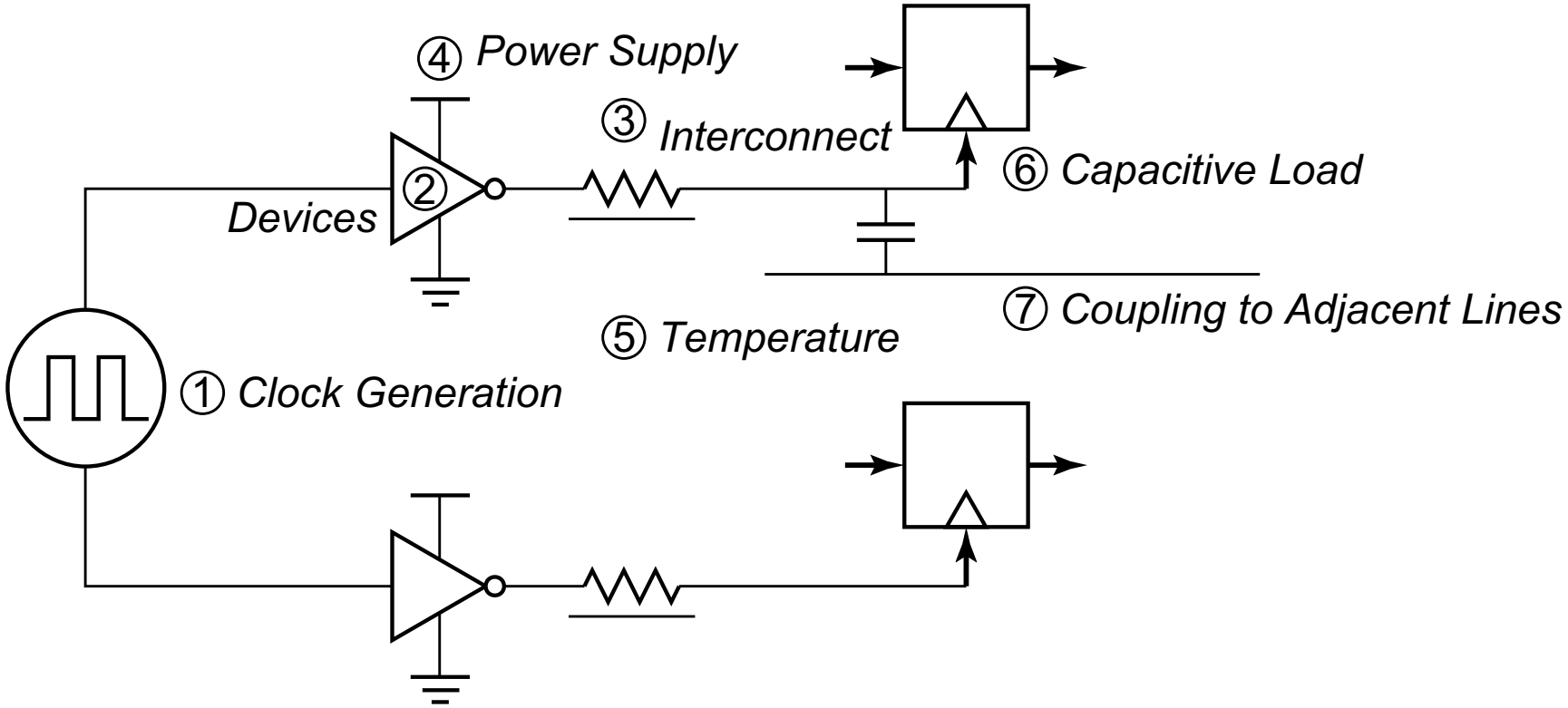
Slack

- Visualizing arrival times



Clock Uncertainties

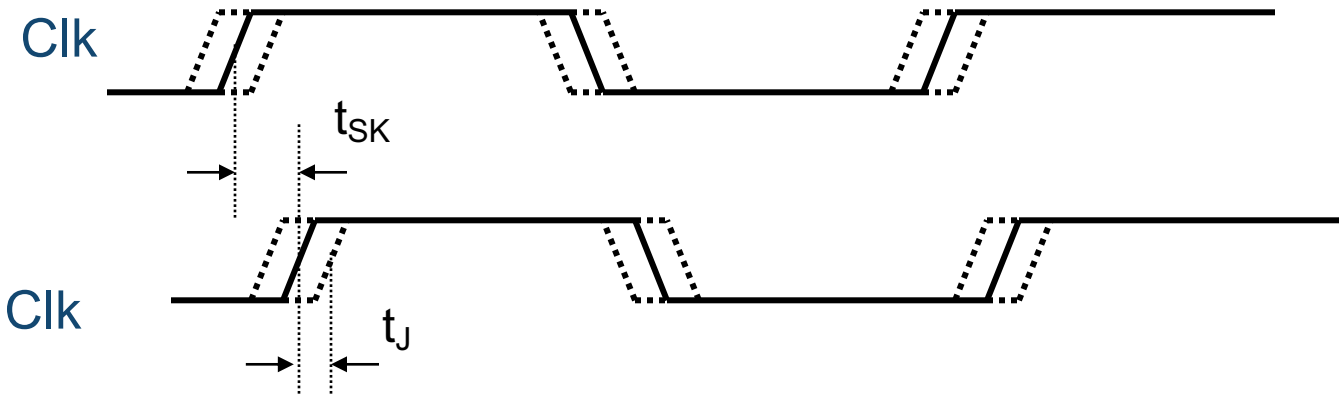
- Clock arrival time varies in space and time



Sources of clock uncertainty

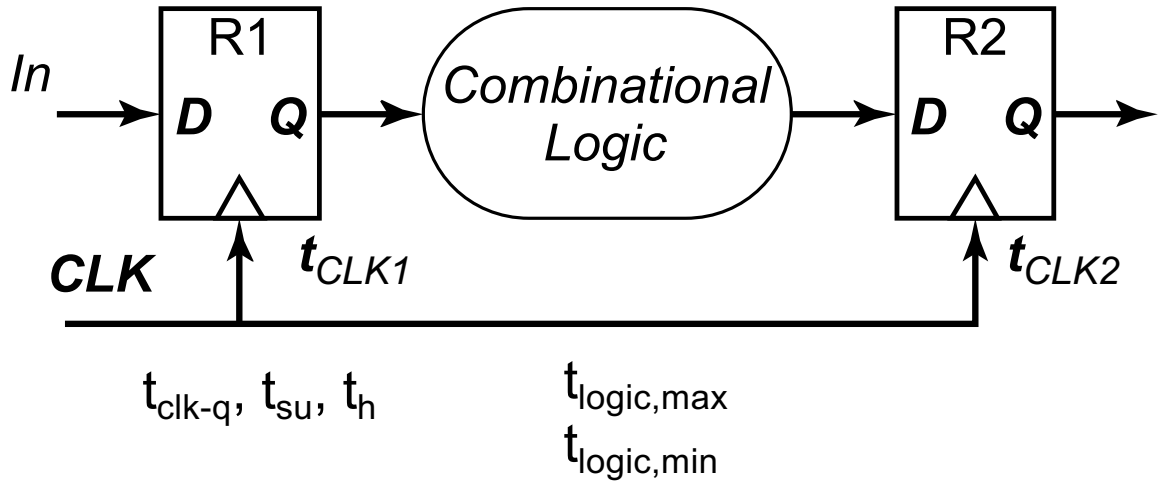
Clock Nonidealities

- Clock skew
  - Spatial variation in temporally equivalent clock edges; deterministic + random, t_{SK}
- Clock jitter
  - Temporal variations in consecutive edges of the clock signal; modulation + random noise
    - Cycle-to-cycle (short-term) t_{JS}
    - (there also exists long term jitter t_{JL})
- Variation of the pulse width
  - Important for level sensitive clocking with latches



Timing Constraints

- First flip-flop launches data on the first clock edge, the second one captures on the second clock edge



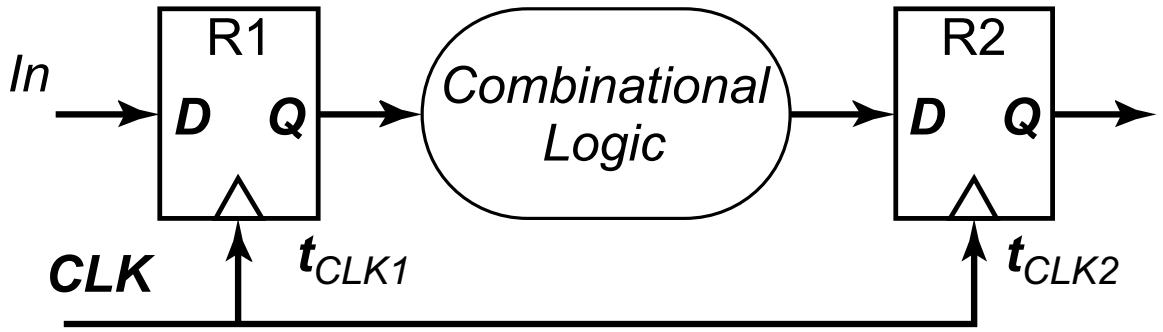
Minimum cycle time is set by the longest logic path:

$$T > t_{c\text{-}q} + t_{logic,max} + t_{su} + t_{sk} + t_j$$

Worst case is when receiving edge arrives early

Timing Constraints

- Launching flip-flop shoudn't contaminate its own data



$t_{clk\text{-}q}$, t_{su}, t_h $t_{logic,max}$ $t_{logic,min}$

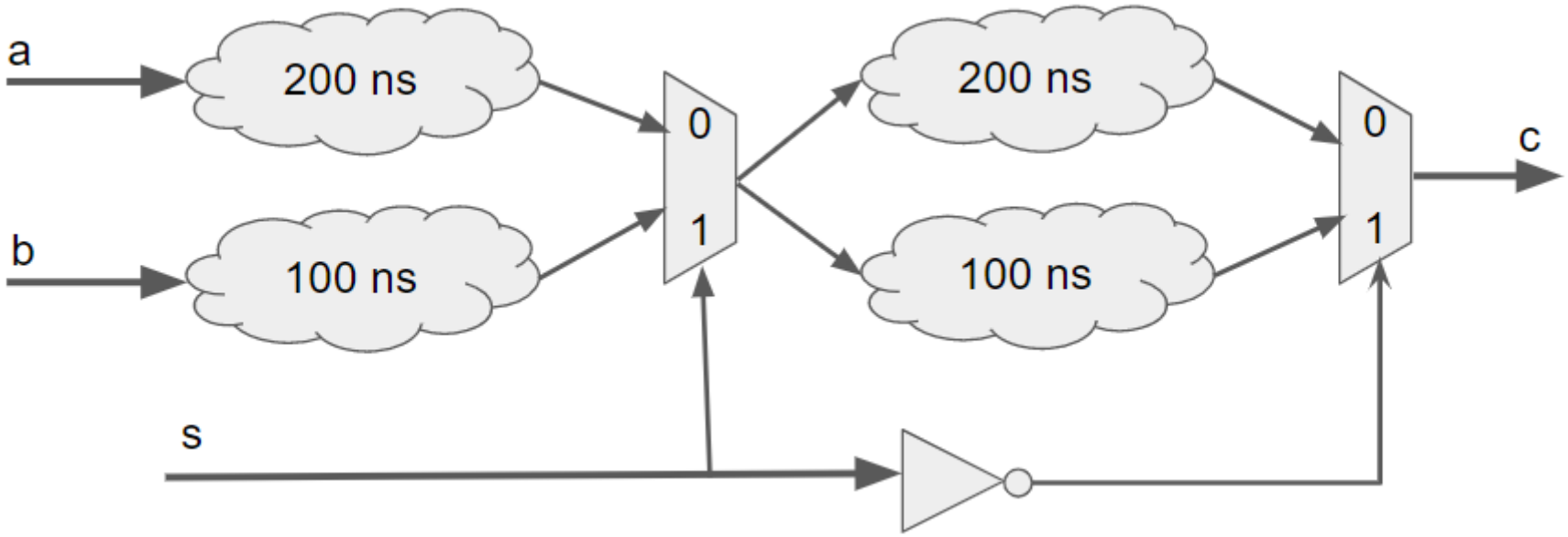
Hold time constraint:

$$t_{c\text{-}q} + t_{logic,\,min} > t_{hold} + t_{sk} + t_j$$

Worst case is when receiving edge arrives late
Race between data and clock

Critical Path

- Find the critical path of the following logic:

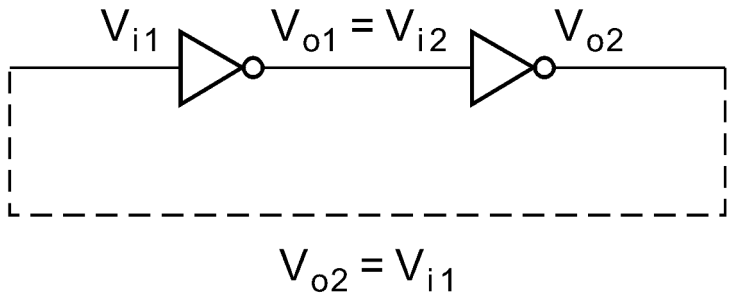


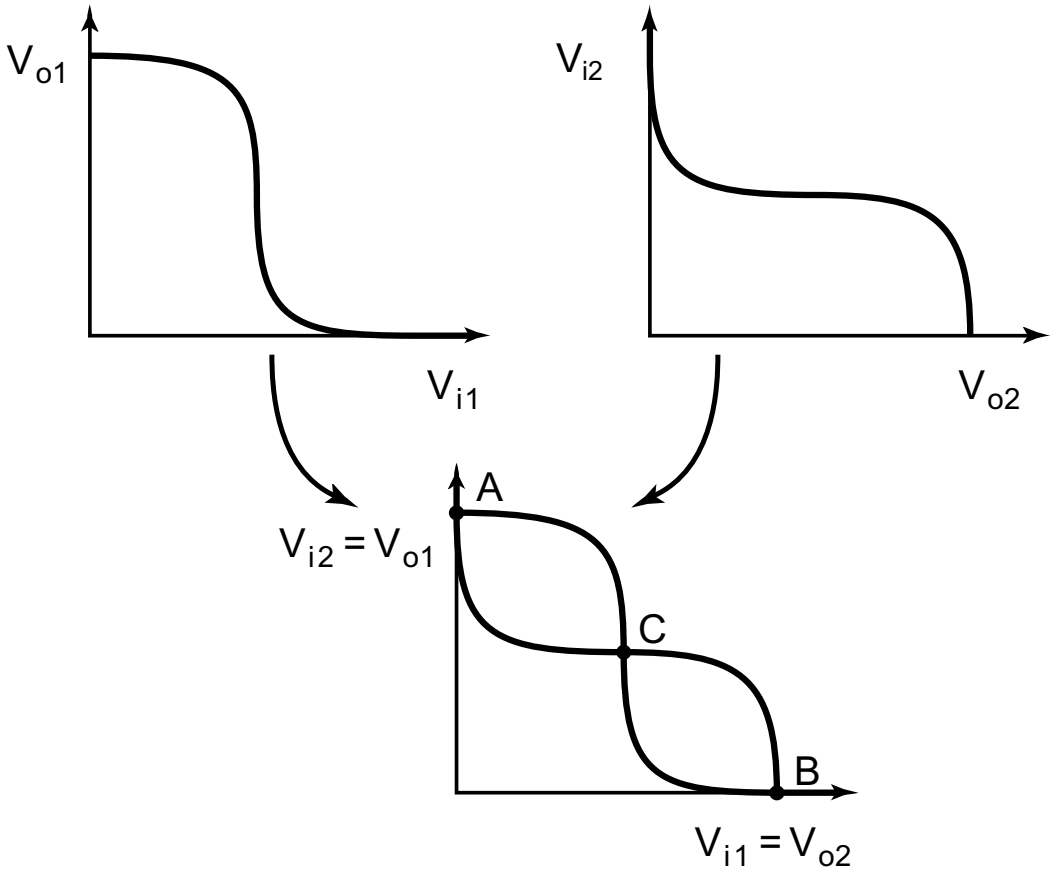
A: 200 ns
B: 300 ns
C: 400 ns

- FlipFlops
  - Timing
  - Latches
  - FlipFlops

Cross-Coupled Inverter

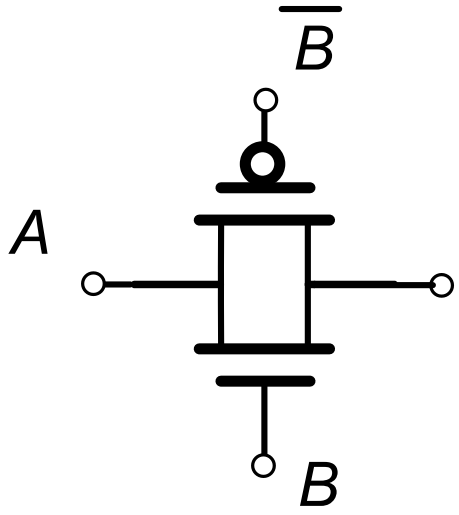
- Positive feedback stores the data





Transmission Gate

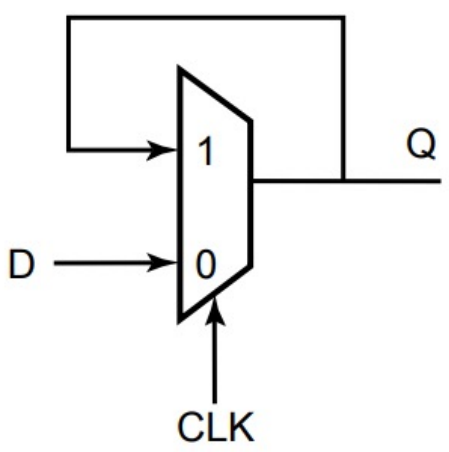
- Transmission gates are the way to build “switches” in CMOS.
- In general, both transistor types are needed:
  - ❑ nFET to pass zeros.
  - ❑ pFET to pass ones.



Writing into a Latch

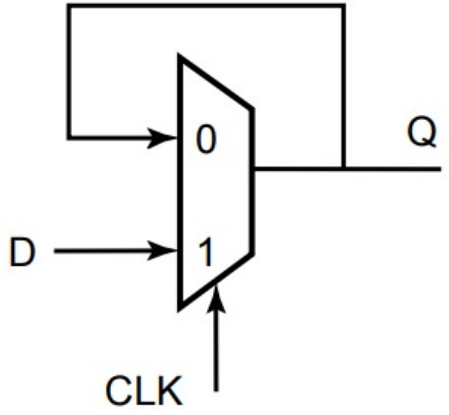
Use the clock as a control signal (to break the positive feedback), that distinguishes between the transparent and opaque states

Negative latch (transparent when CLK= 0)



$$Q = Clk \cdot Q + \overline{Clk} \cdot In$$

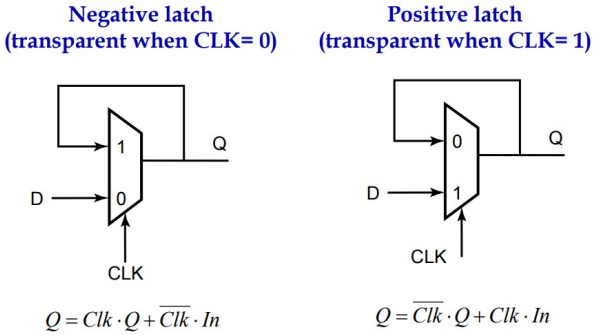
Positive latch (transparent when CLK= 1)

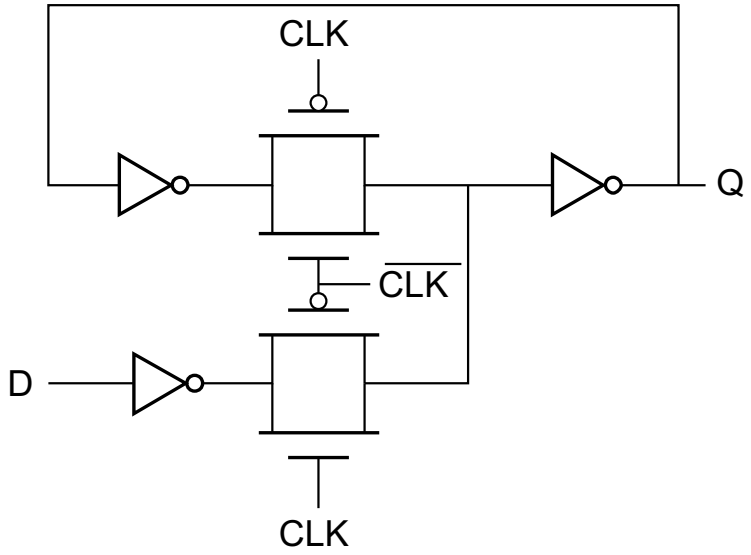


$$Q = \overline{Clk} \cdot Q + Clk \cdot In$$

Writing into a Latch

Use the clock as a control signal (to break the positive feedback), that distinguishes between the transparent and opaque states

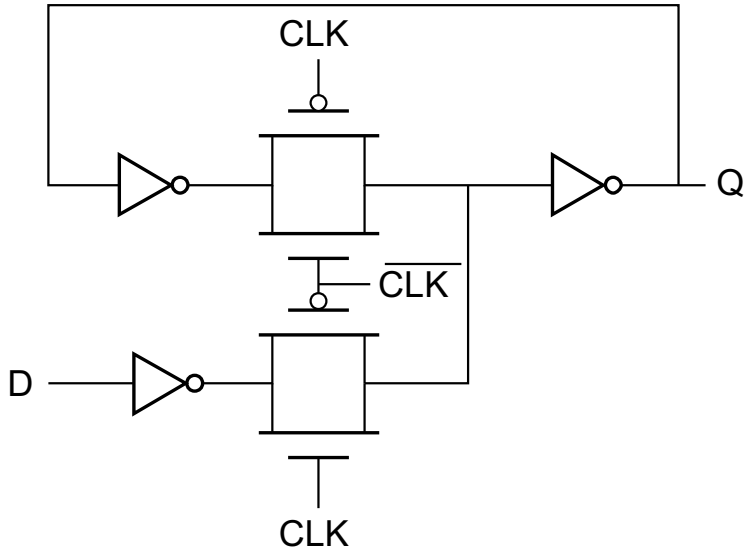




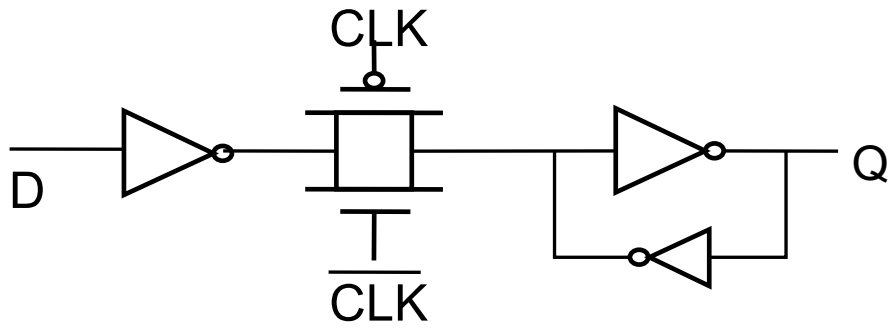
Converting into a MUX

Writing into a Latch

Use the clock as a control signal (to break the positive feedback), that distinguishes between the transparent and opaque states



Converting into a MUX

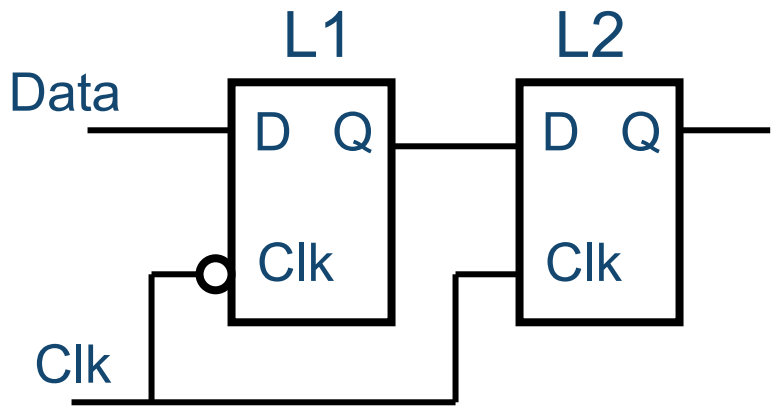


Forcing the state (depends on sizing)

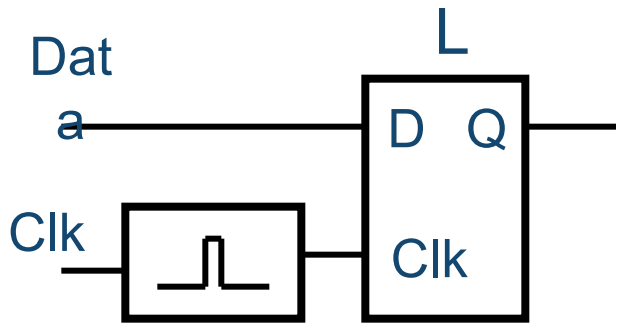
- FlipFlops
  - Timing
  - Latches
  - FlipFlops

Flip-Flops

Latch Pair

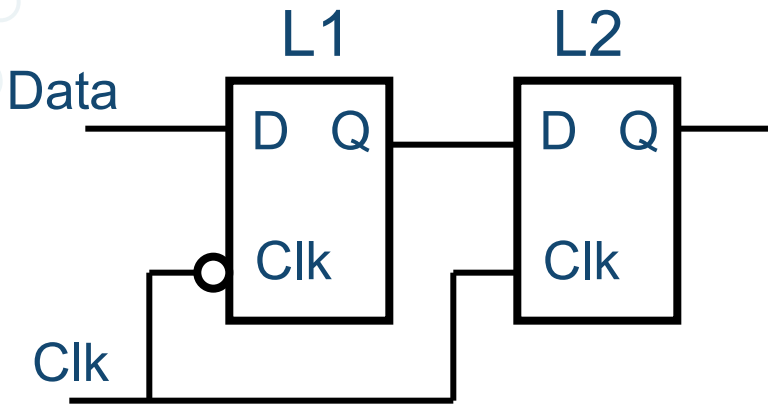


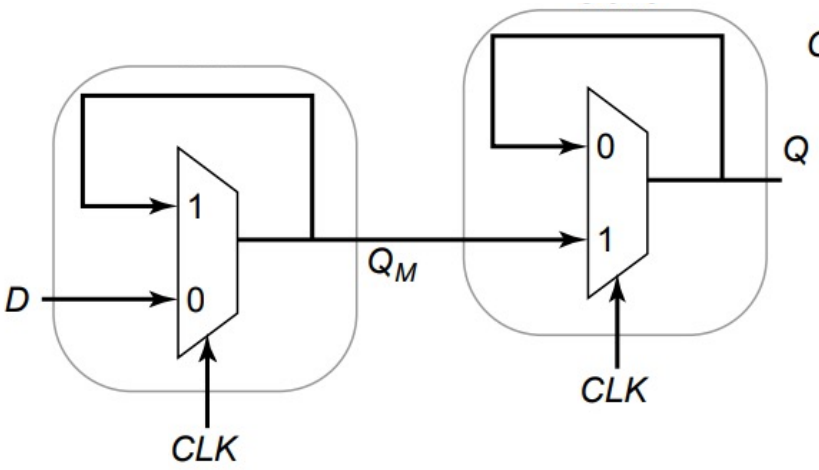
Pulse-Triggered Latch

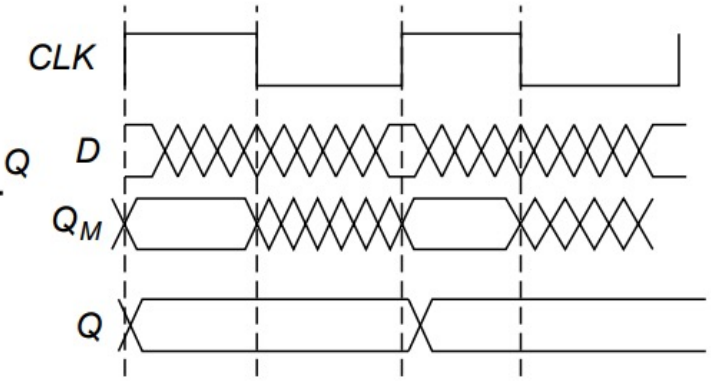


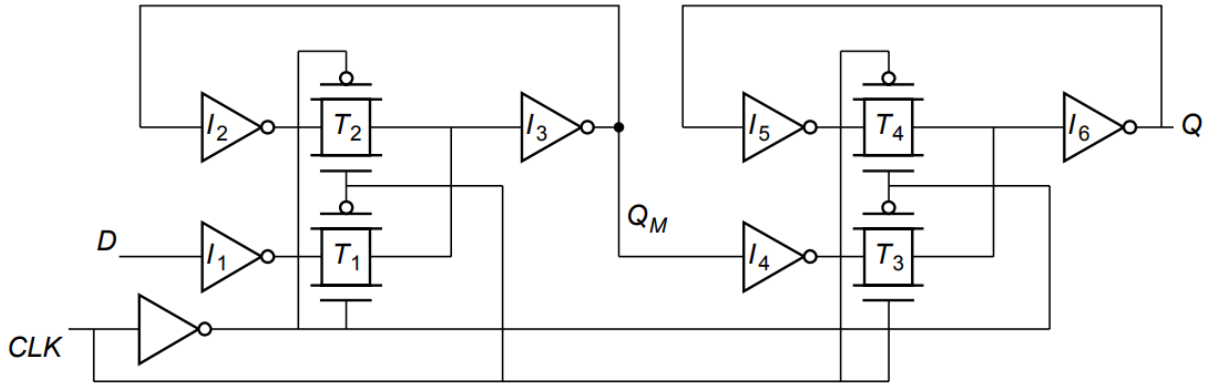
Flip-Flops

Latch Pair



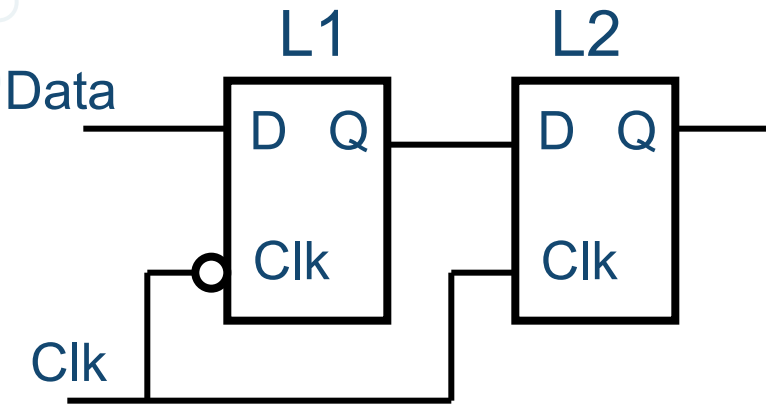


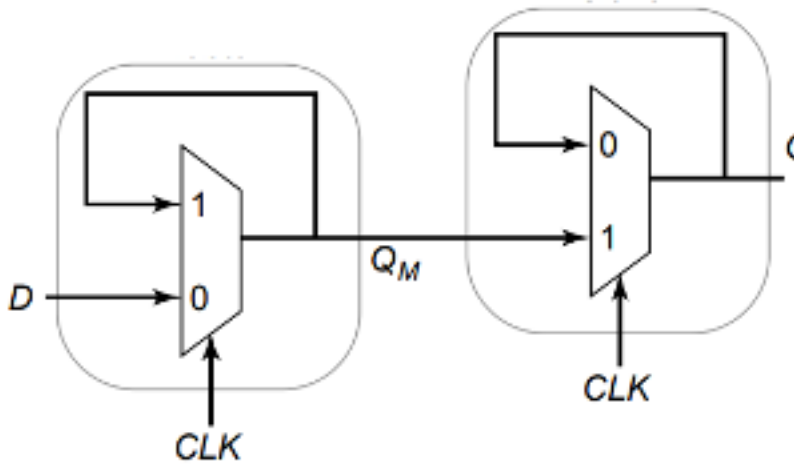


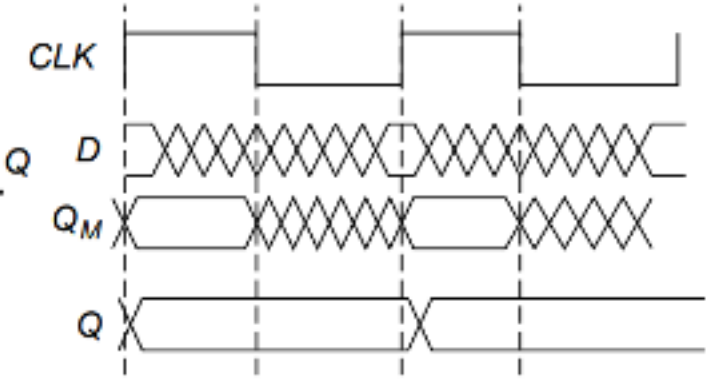


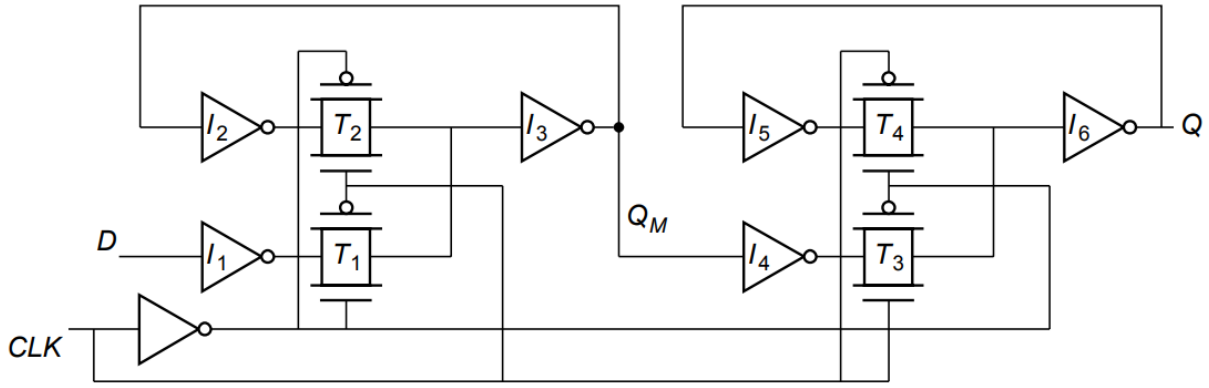
Flip-Flops

Latch Pair









Review

- Timing analysis for early and late signal arrivals
- Flip-flop-based pipelines are a lot easier to analyze than latch-based ones
- Latches are based on positive feedback
- Clk-Q delay calculated similarly to combinational logic
- Setup, hold defined as D-Clk times that correspond to CLk-Q delay increases
- Flip-flop is typically a latch pair