

EECS151/251A Introduction to Digital Design and ICs

Lecture 11: FPGA

Intel's Altera Acquisition

On June 1, 2015, Altera and Intel announced that Intel would acquire Altera in an all-cash transaction valued at approximately \$16.7 billion. As of December 28, 2015, the acquisition has been completed.

Sophia Shao



Intel acquired Altera at \$16.7 billion in 2015.

<https://newsroom.intel.com/news-releases/intel-completes-acquisition-of-altera/#gs.i5jkp3>

Review

- RISC-V Instruction Formats
 - R/I/S/B/U/J-Type
- RISC-V Single-cycle Datapath
 - Simple but has a long critical path
- RISC-V Control Logic
 - Use instructions + BrEq/BrLT to set control signals of the datapath.
- RISC-V Pipelining
 - Improve the overall system throughput
- RISC-V Pipeline Hazards
 - Prevent fully pipelined execution

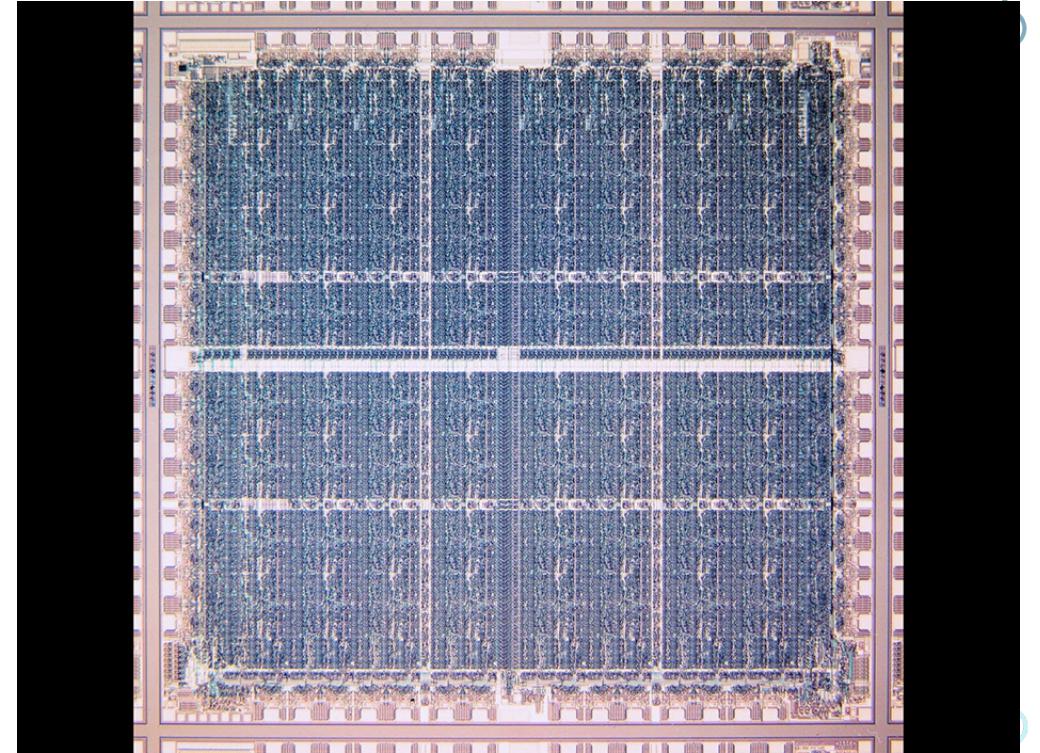


- **FPGA**

- Overview
- Key Configurable Resources
 - Configurable Logic Blocks (CLBs)
 - Look-Up Tables
 - Slices
 - Configurable Interconnect
 - BRAM, DSP, and AI Engine

Chip Hall of Fame: Xilinx XC2064 FPGA

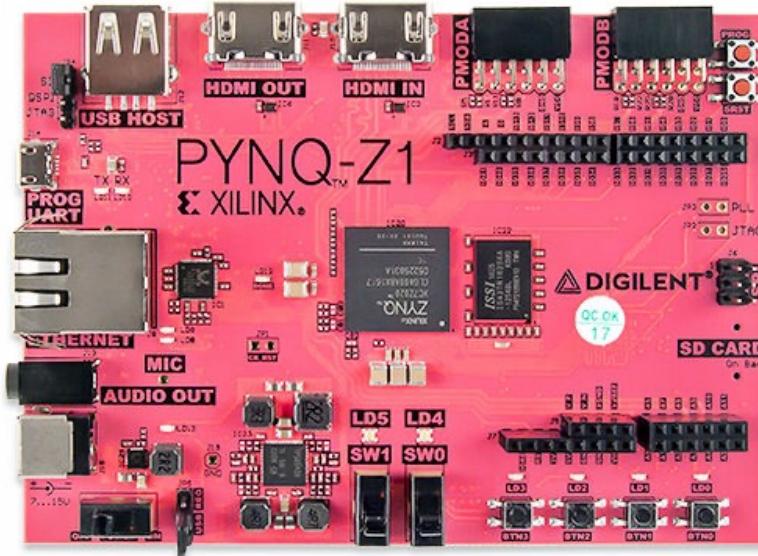
- Back in the early 1980s, chip designers tried to get the most out of each transistor on their circuits.
- Ross Freeman came up with a chip packed with transistors that formed loosely organized logic blocks with connections that could be configured and reconfigured with software.
- As a result, sometimes a bunch of transistors wouldn't be used, but Freeman was betting that Moore's Law would eventually make transistors so cheap that no one would care.



<https://spectrum.ieee.org/tech-history/silicon-revolution/chip-hall-of-fame-xilinx-xc2064-fpga>

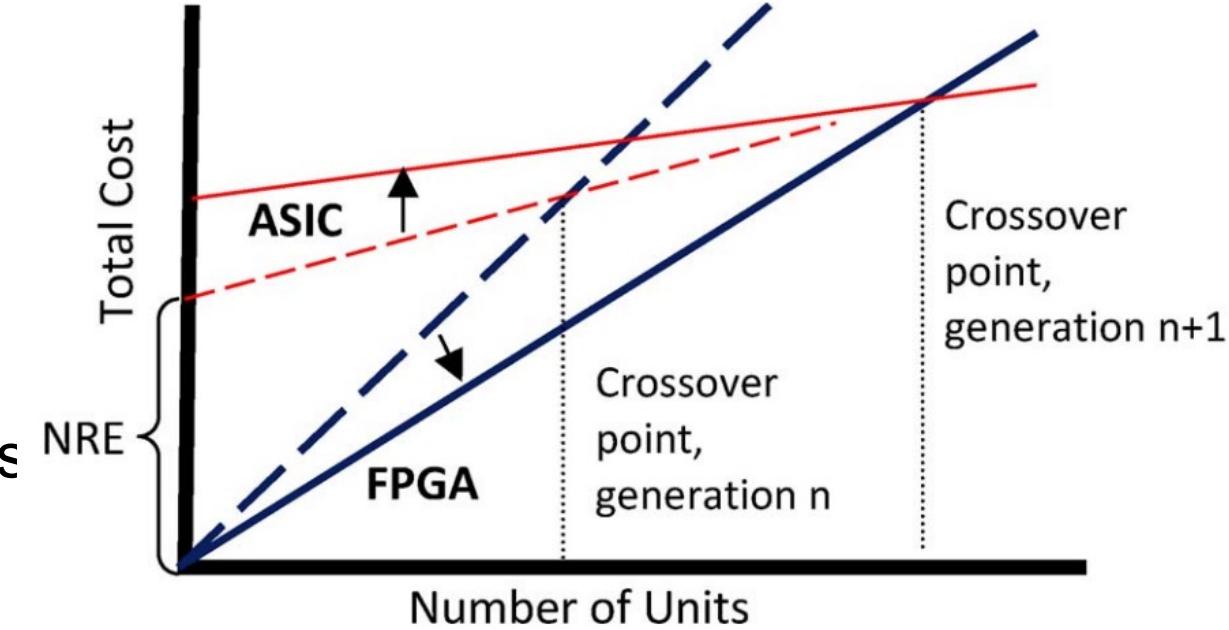
Why are FPGAs Interesting?

- Technical viewpoint:
 - For hardware/system designers, FPGAs are quite similar to ASICs but can be designed faster:
 - “Tape-out” new design every few minutes/hours
 - “reconfigurability” or “reprogrammability” may offer other advantages over fixed logic
 - On the other hand, the relative flexibility comes at the expense of larger die area, slower circuits, and more energy per operation.
 - Modern FPGAs are “reconfigurable systems on a chip”



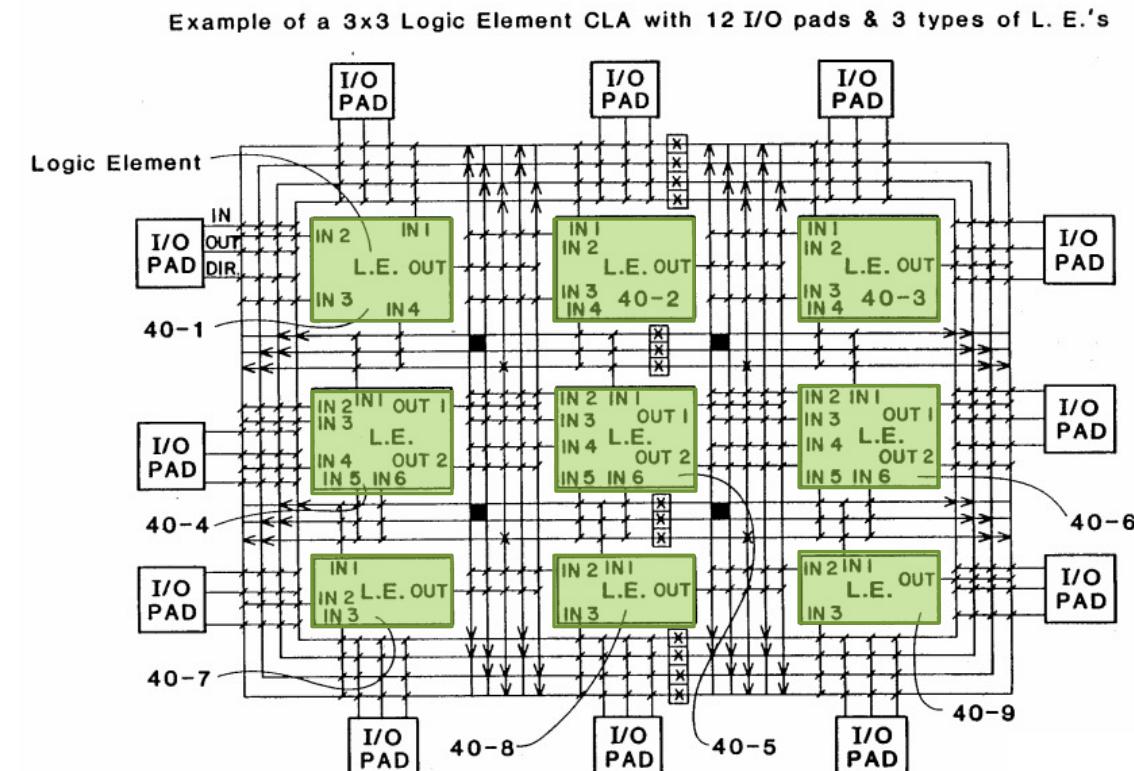
Field Programmable Gate Arrays (FPGAs)

- An integrated circuit designed to be configured by a customer or a designer after manufacturing, i.e., field programmable.
 - Low NRE cost compared to ASIC
- The FPGA configuration is generally specified using a hardware description language, similar to that used for ASICs
- Two dominant FPGA makers:
 - Xilinx (now AMD)
 - Altera (now Intel)



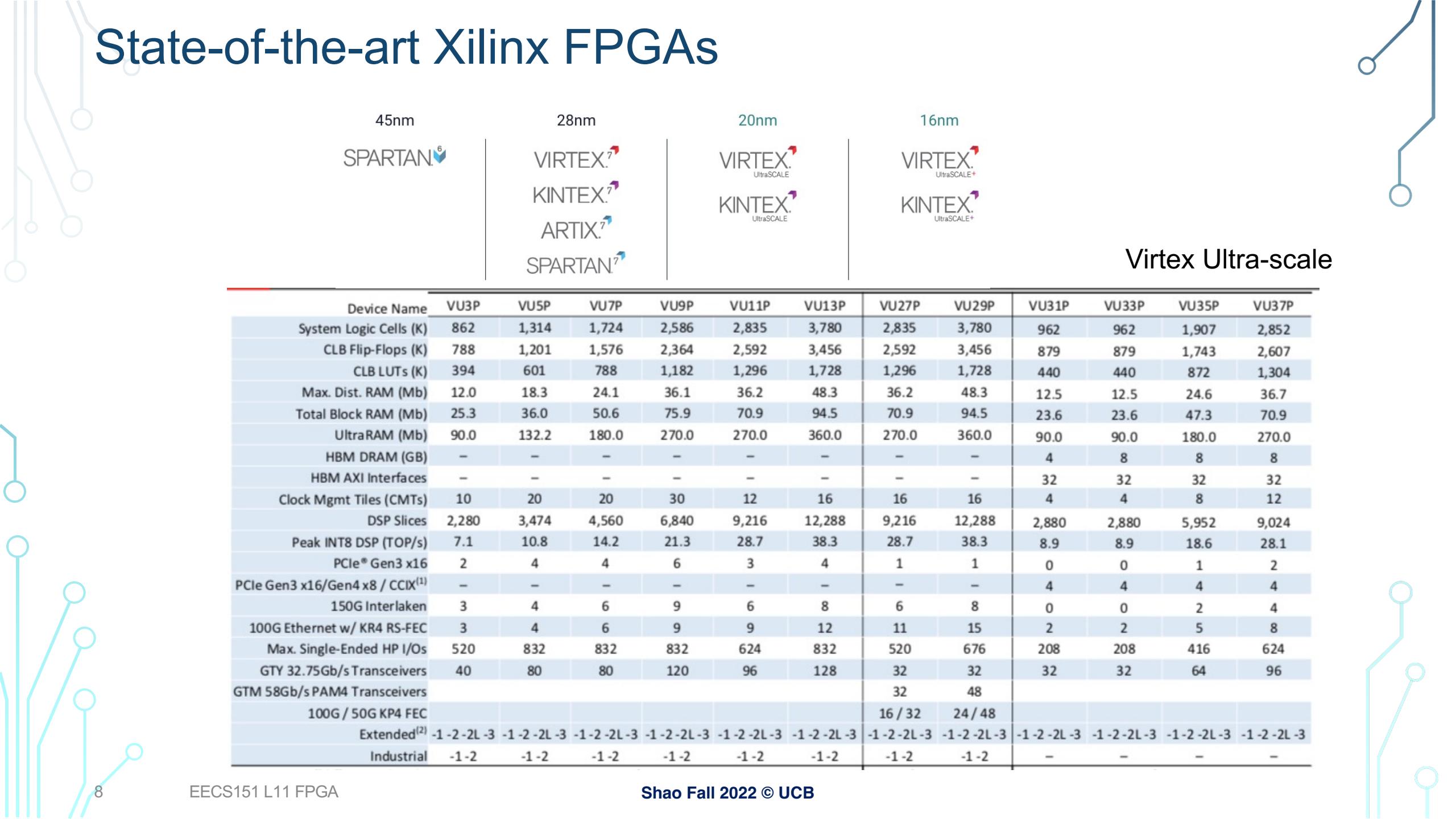
FPGA Overview

- Basic idea:
 - Two-dimensional array of logic blocks and flip-flops with means for the user to configure:
 - The function of each block
 - The interconnection between blocks
- Configurable Logic Blocks (CLBs)
 - FPGA's Functional Units
- Configurable Interconnect
 - Connecting CLBs together



Xilinx FPGA Patent

State-of-the-art Xilinx FPGAs



The table compares the performance metrics of various Xilinx FPGA families across four technology nodes: 45nm, 28nm, 20nm, and 16nm. The Virtex Ultra-scale family is shown separately at the bottom.

Device Name	VU3P	VU5P	VU7P	VU9P	VU11P	VU13P	VU27P	VU29P	VU31P	VU33P	VU35P	VU37P
System Logic Cells (K)	862	1,314	1,724	2,586	2,835	3,780	2,835	3,780	962	962	1,907	2,852
CLB Flip-Flops (K)	788	1,201	1,576	2,364	2,592	3,456	2,592	3,456	879	879	1,743	2,607
CLB LUTs (K)	394	601	788	1,182	1,296	1,728	1,296	1,728	440	440	872	1,304
Max. Dist. RAM (Mb)	12.0	18.3	24.1	36.1	36.2	48.3	36.2	48.3	12.5	12.5	24.6	36.7
Total Block RAM (Mb)	25.3	36.0	50.6	75.9	70.9	94.5	70.9	94.5	23.6	23.6	47.3	70.9
UltraRAM (Mb)	90.0	132.2	180.0	270.0	270.0	360.0	270.0	360.0	90.0	90.0	180.0	270.0
HBM DRAM (GB)	-	-	-	-	-	-	-	-	4	8	8	8
HBM AXI Interfaces	-	-	-	-	-	-	-	-	32	32	32	32
Clock Mgmt Tiles (CMTs)	10	20	20	30	12	16	16	16	4	4	8	12
DSP Slices	2,280	3,474	4,560	6,840	9,216	12,288	9,216	12,288	2,880	2,880	5,952	9,024
Peak INT8 DSP (TOP/s)	7.1	10.8	14.2	21.3	28.7	38.3	28.7	38.3	8.9	8.9	18.6	28.1
PCIe® Gen3 x16	2	4	4	6	3	4	1	1	0	0	1	2
PCIe Gen3 x16/Gen4 x8 / CCIX ⁽¹⁾	-	-	-	-	-	-	-	-	4	4	4	4
150G Interlaken	3	4	6	9	6	8	6	8	0	0	2	4
100G Ethernet w/ KR4 RS-FEC	3	4	6	9	9	12	11	15	2	2	5	8
Max. Single-Ended HP I/Os	520	832	832	832	624	832	520	676	208	208	416	624
GTy 32.75Gb/s Transceivers	40	80	80	120	96	128	32	32	32	32	64	96
GTM 58Gb/s PAM4 Transceivers							32	48				
100G / 50G KP4 FEC							16 / 32	24 / 48				
Extended ⁽²⁾	-1-2-2L-3											
Industrial	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-1-2	-	-	-	-

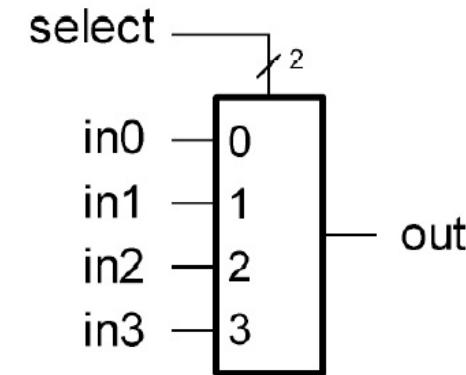


- **FPGA**

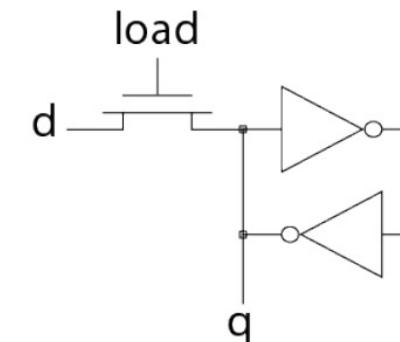
- Overview
- Key Configurable Resources
 - Configurable Logic Blocks (CLBs)
 - Look-Up Tables
 - Slices
 - Configurable Interconnect
 - BRAM, DSP, and AI Engine

Background

- A MUX or multiplexor is a combinational logic circuit that chooses between 2^N inputs under the control of N control signals.

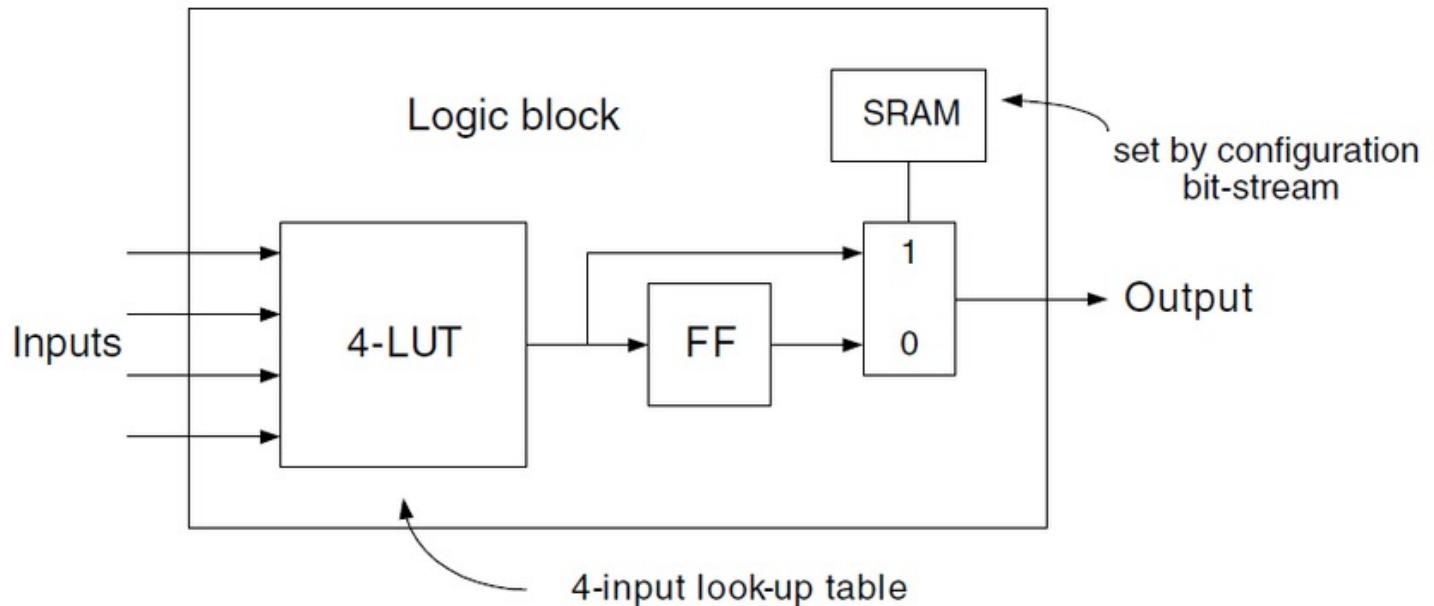


- A latch is a 1-bit memory (similar to a flip-flop).



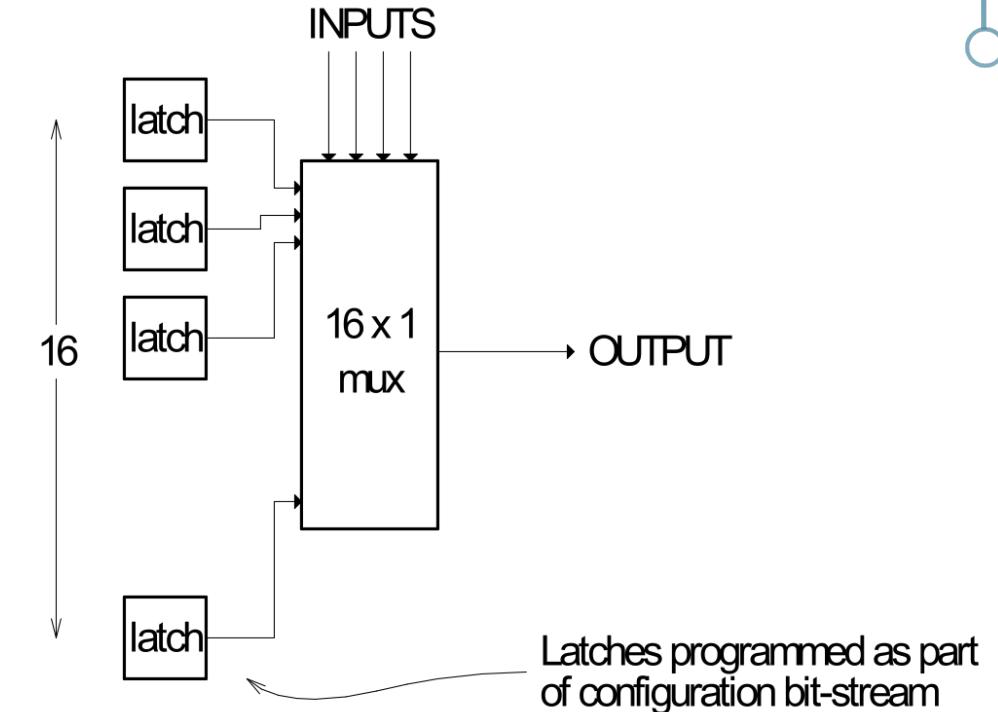
Configurable Logic Blocks (CLBs)

- Basic FPGA functional unit
- Implements both combinational and sequential logic
- Includes:
 - Look-up table
 - Register (Flip-Flop)
 - Multiplexers



Look-Up Table Implementation

- Implement truth table in small memories
 - Latches/SRAM
- n-bit LUT is implemented as a $2^n * 1b$ memory:
 - inputs choose one of 2^n memory locations.
 - memory locations (latches) are normally loaded with values from user's configuration bit stream.
 - Inputs to mux control are the CLB inputs.
- Result is a general purpose “logic gate”.
 - n-LUT can implement any function of n inputs!



Look-Up Table Implementation

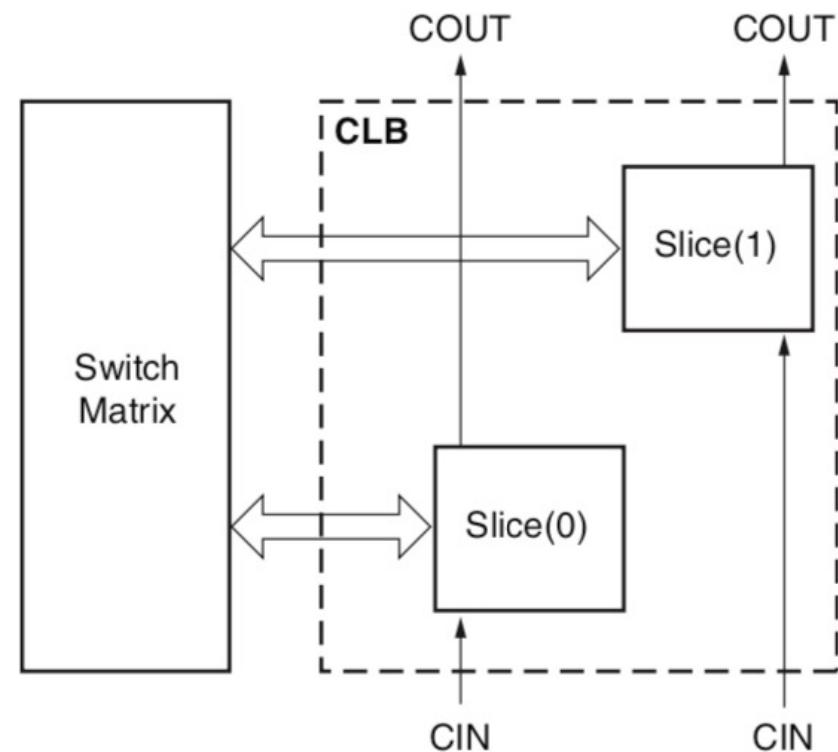
- An n-LUT is a direct implementation of a function truth-table.
- Each location holds the value of the function corresponding to one input combination.
- LUT size grows exponentially with # of inputs.
 - 64 input LUT requires $2^{64} = 1.84 * 10^{19}$ bits storage.
 - 4-input ~ 8-input LUT

Example: 4-LUT

INPUTS	
0000	F(0,0,0,0) ← store in 1st latch
0001	F(0,0,0,1) ← store in 2nd latch
0010	F(0,0,1,0) ←
0011	F(0,0,1,1) ←
0011	
0100	•
0101	•
0110	•
0111	
1000	
1001	
1010	
1011	
1100	
1101	
1110	
1111	

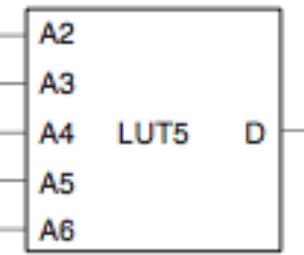
Slices

- Each CLB contains two slices in 7 series.
- LUTs and registers are split across slices.
 - 4 LUTS and 8 FFs in 7-series.
- Two types of slices:
 - SLICEM: Full slice
 - LUT can be used for logic **and** memory/shift registers.
 - Has wide multiplexers and carry chain
 - SLICEL: logic and arithmetic only
 - LUT can only be used for logic (no memory)
 - Has wide multiplexers and carry chain

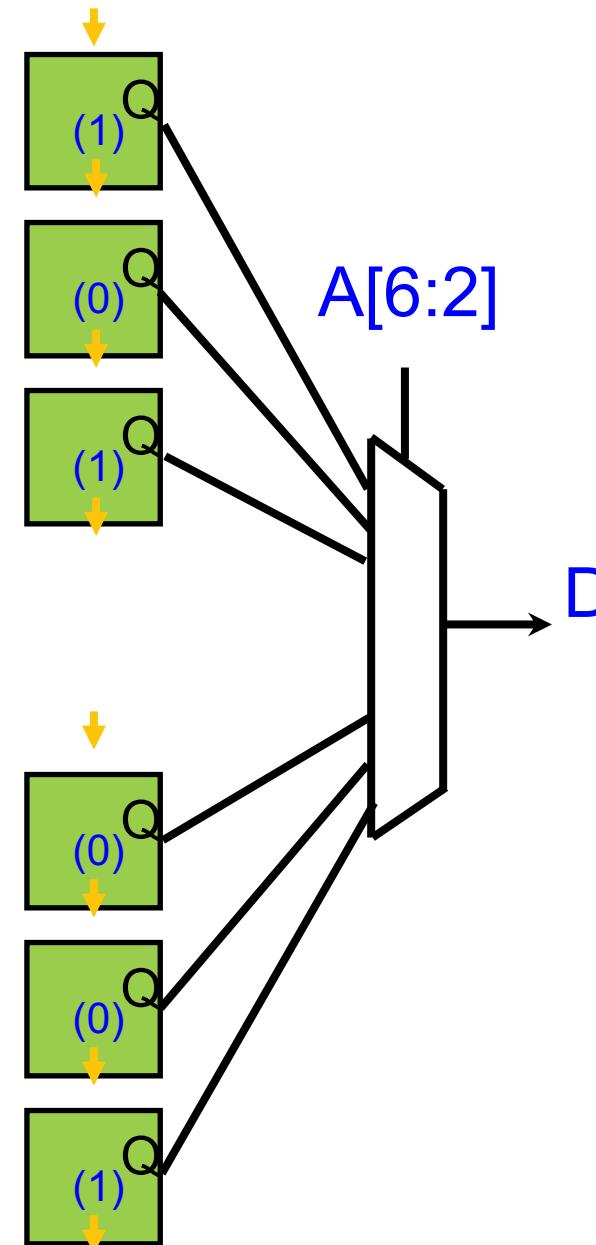


Constructing a SLICE

- 5-Input Look-Up Table



A[6:2]	D
00000	1
00001	0
00010	1
11101	0
11110	0
11111	1



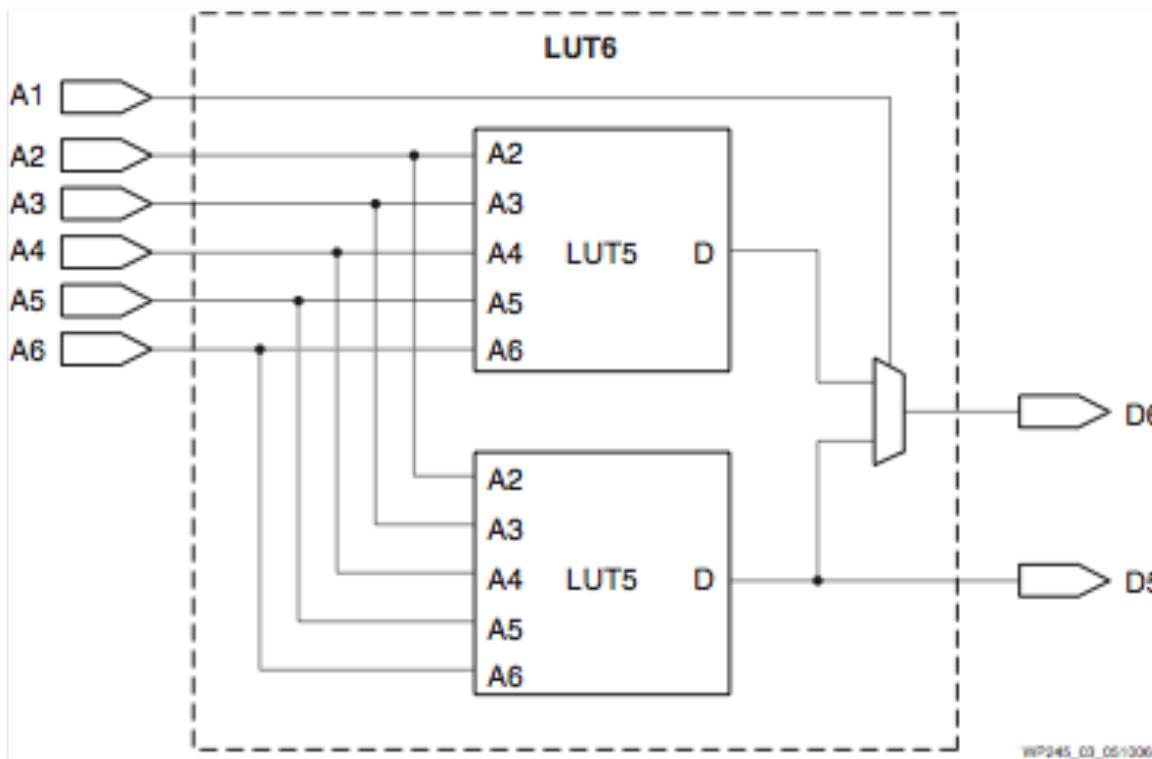
Computes any 5-input logic function.

Timing is independent of function.

Latches set during configuration.

Constructing a SLICE

- 6-input LUT



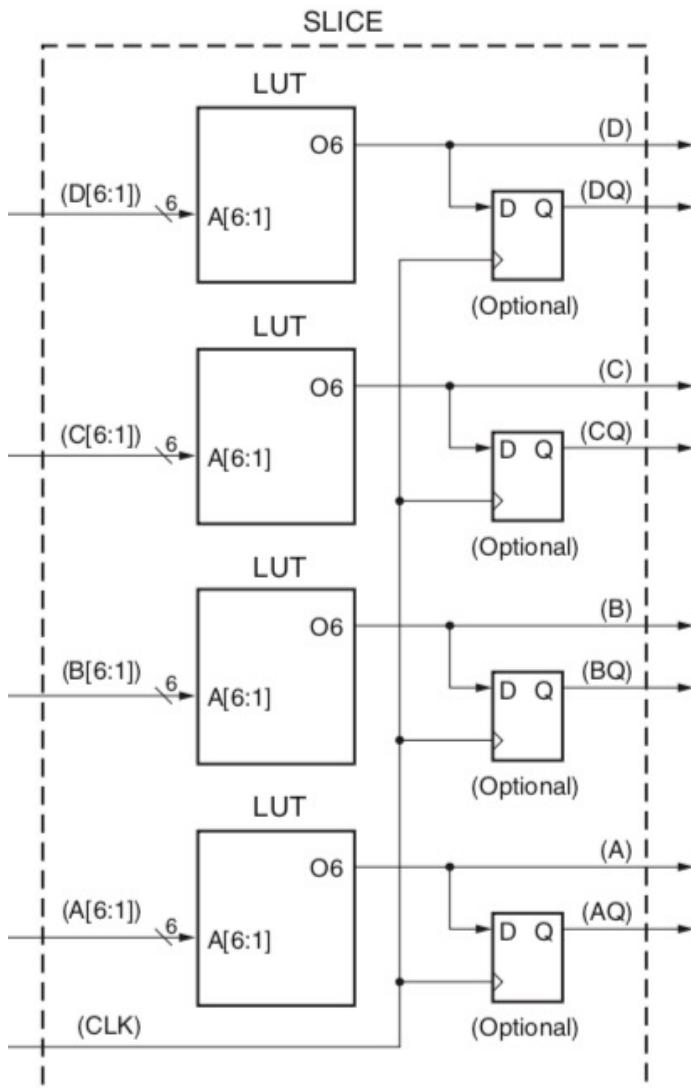
May be used
as one 6-input LUT
(D6 out)

...

... or as two
5-input LUTS
(D6 and D5)

Combinational
logic
(post configuration)

The Simplest View of A Slice



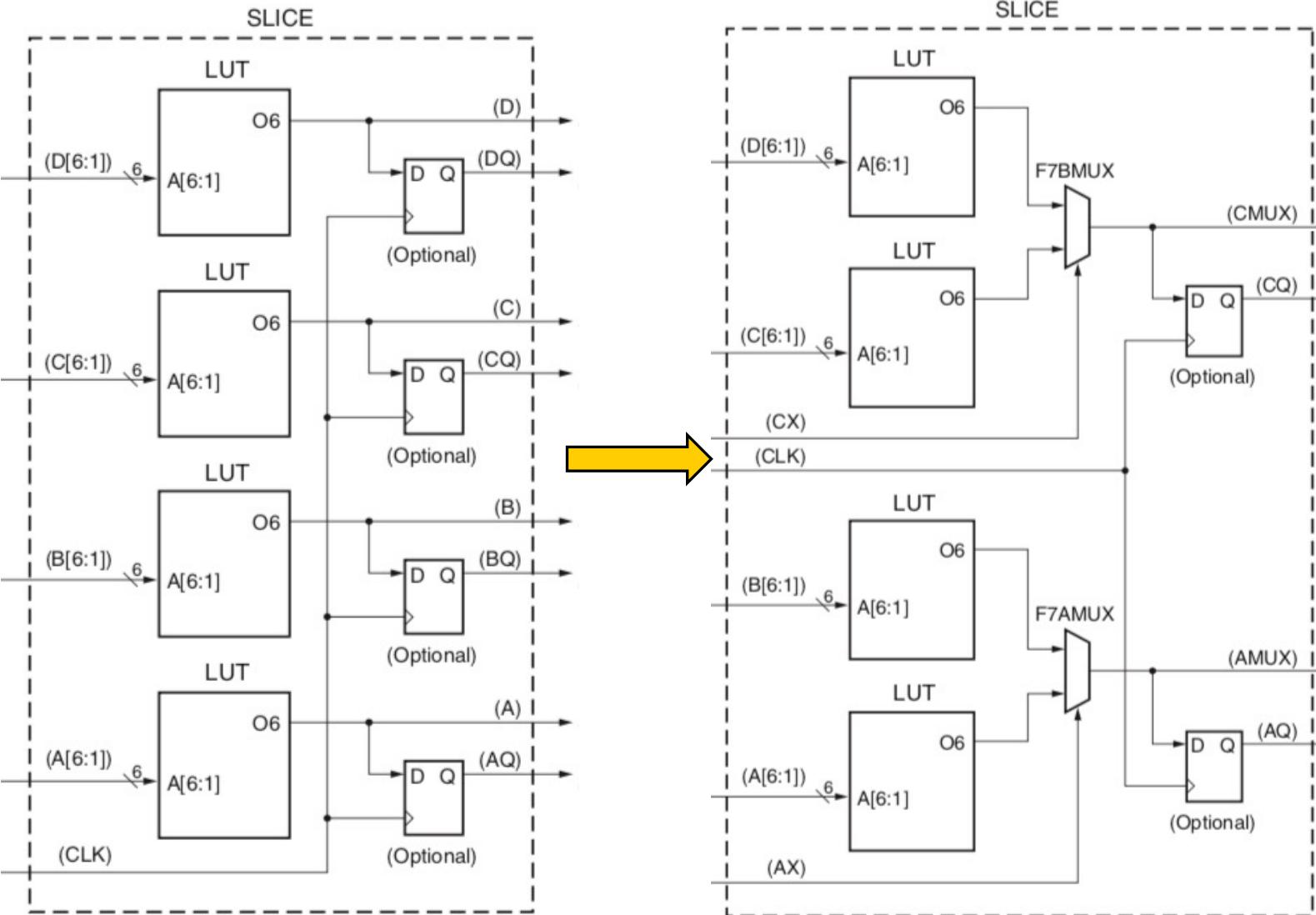
Four 6-LUTs

Four Flip-Flops

Switching fabric may see
combinational and registered
outputs.

An actual Virtex slice adds many
small features to this simplified
diagram.
We show them one by one ...

How about 7-input LUT in a slice?

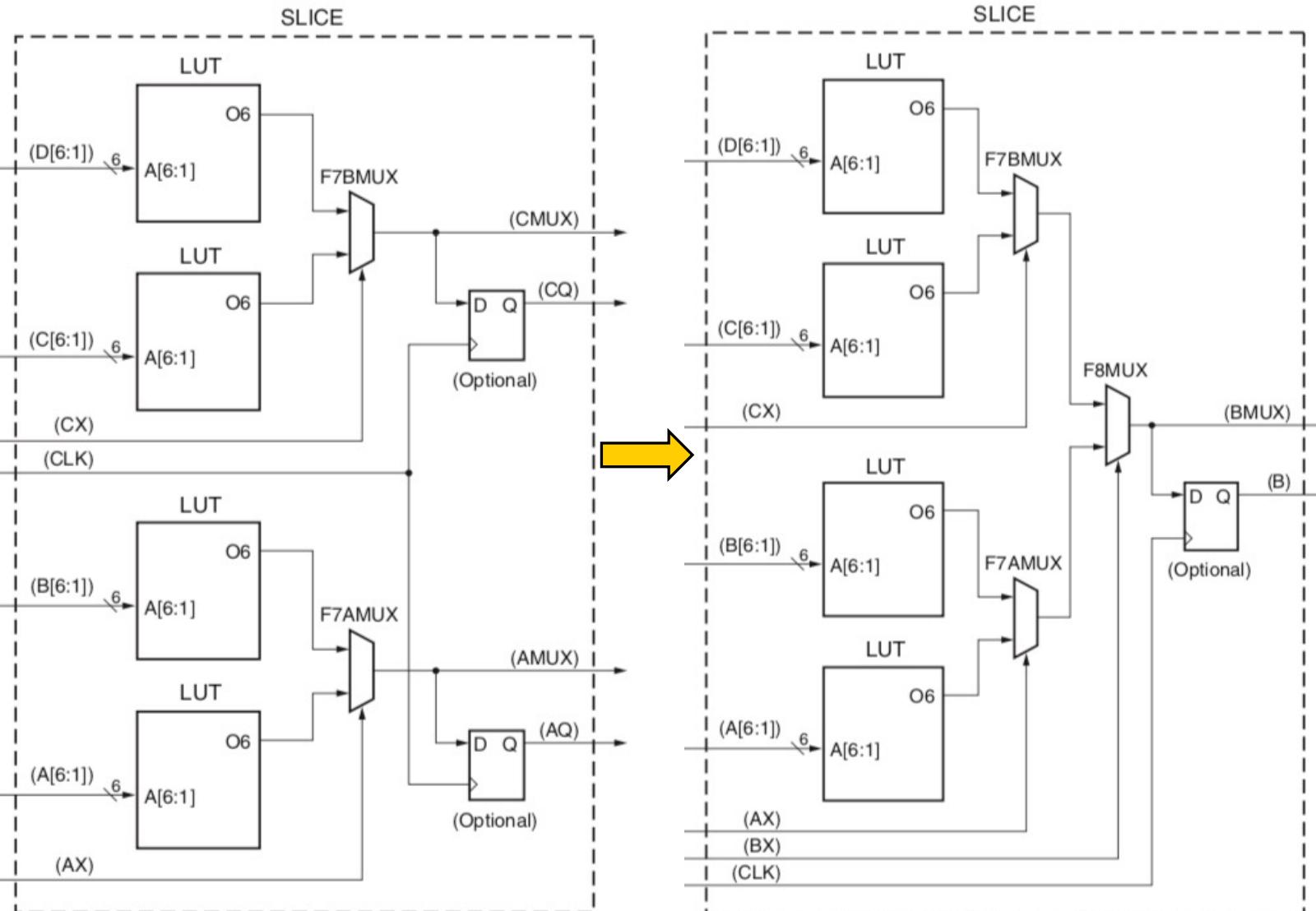


Two 7-LUTs

Extra MUX
(F7AMUX, F7BMUX)

Extra inputs
(AX and CX)

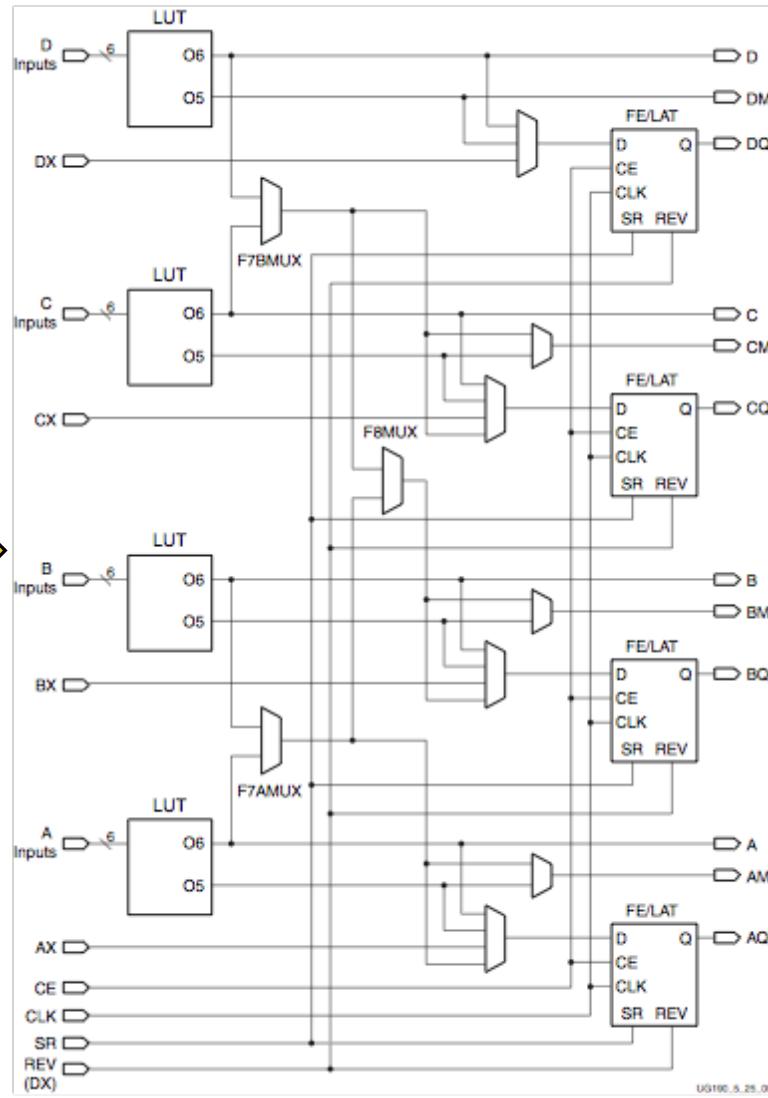
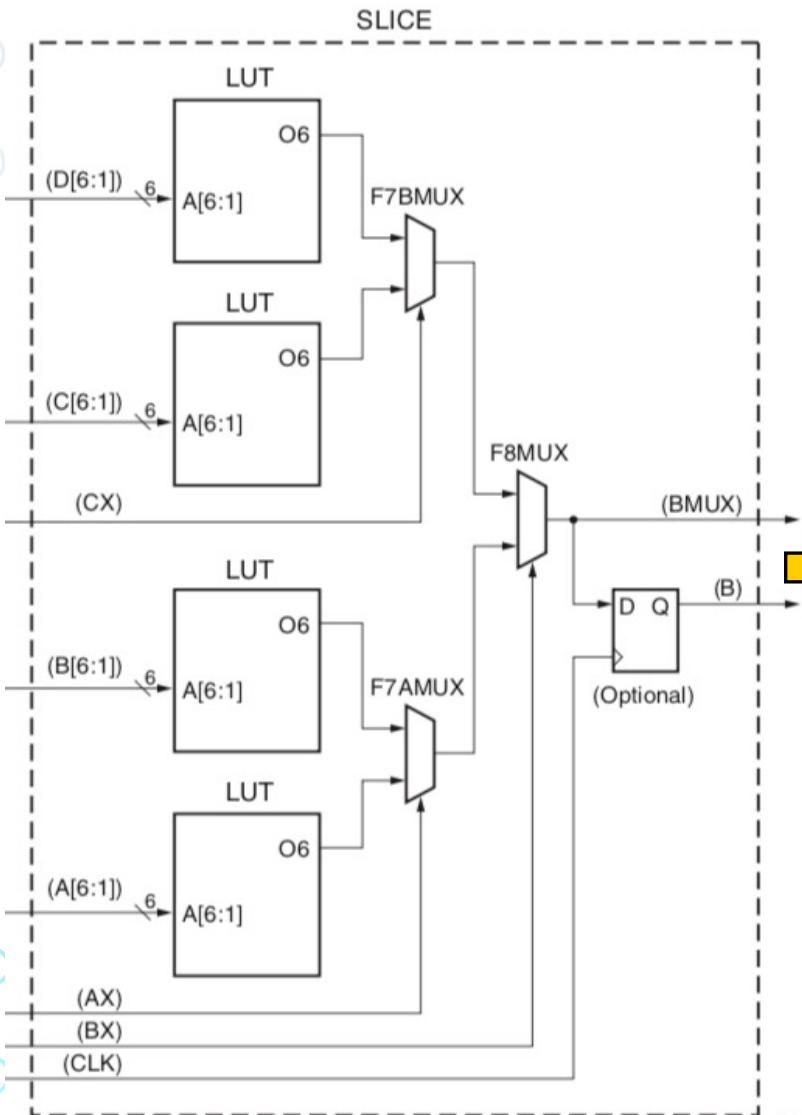
How about 8-input LUT in a slice?



Third MUX
(F8MUX)

Third input
(BX)

Extra MUXes to choose LUT outputs

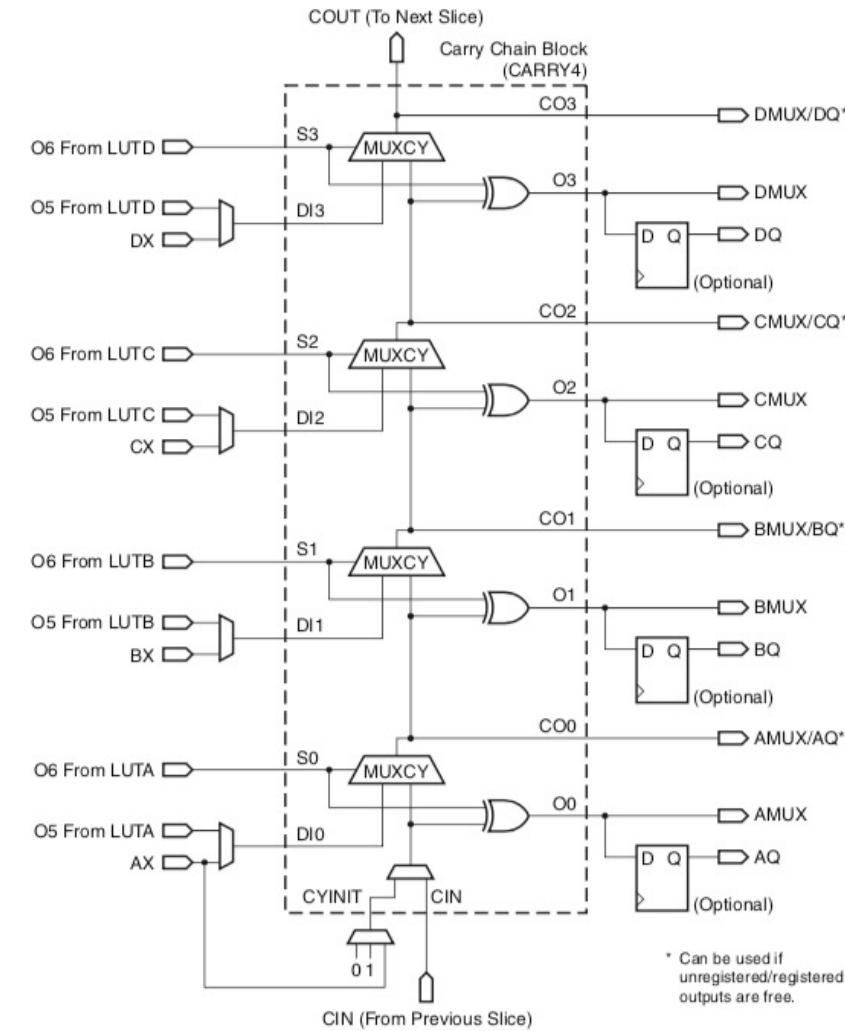
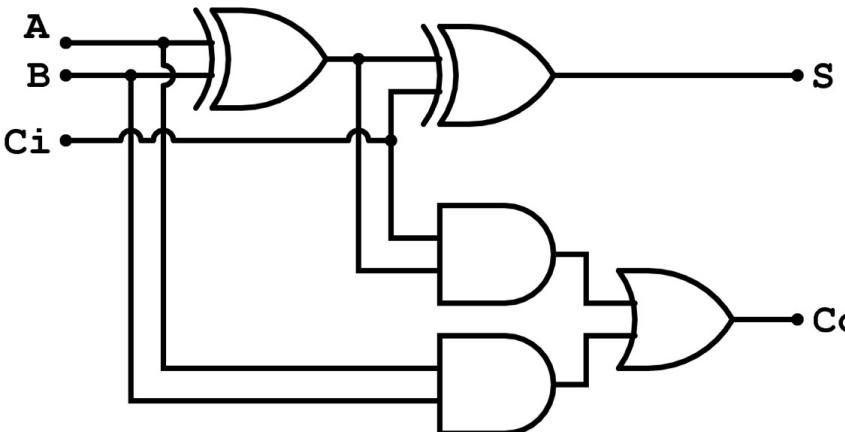


From eight 5-LUTs
... to one 8-LUT.

Combinational
or registered outs.

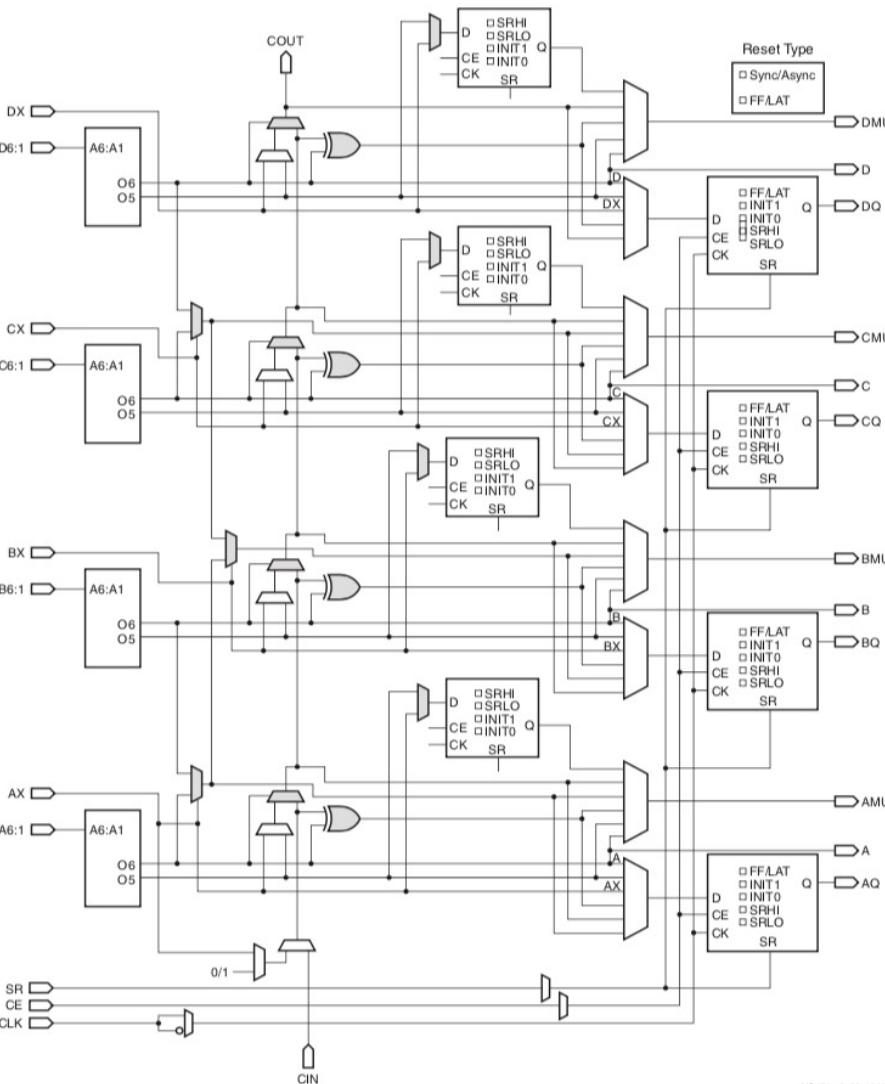
Extra Carry Chain

We can map
ripple-carry addition onto
carry-chain block.



* Can be used if
unregistered/registered
outputs are free.

Putting it all together ... a SLICEL.



The previous slides explain all SLICEL features.

About 50% of the are SLICELs.

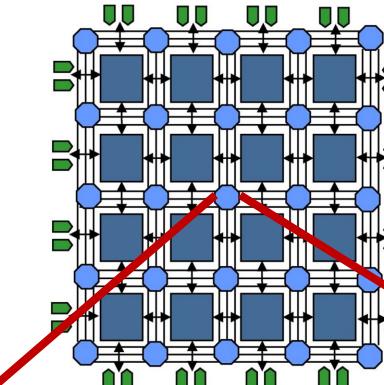
The other slices are SLICEMs, and have extra features.

Administrivia

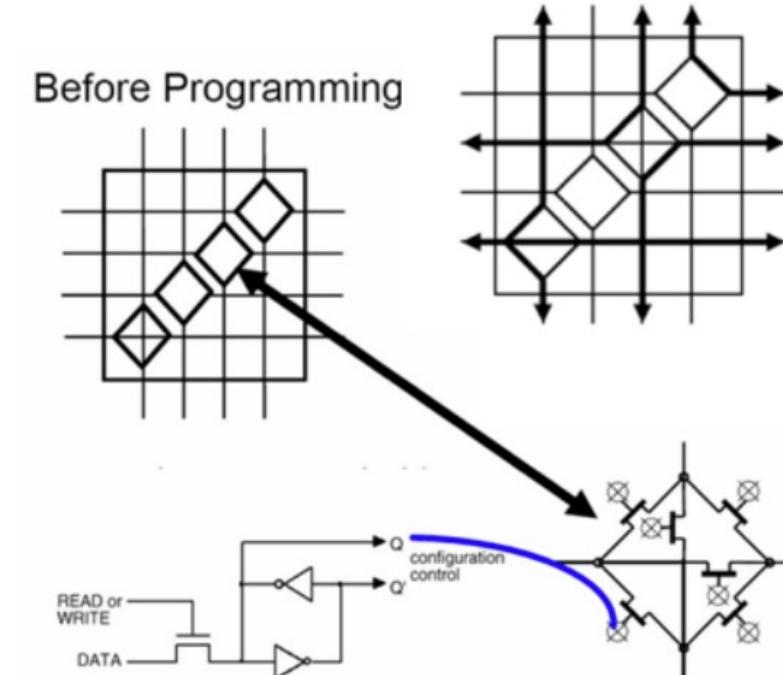
- Lab 5 starts this week.
- No new homework this week.
 - Homework 4 due this week.
- Midterm next Tuesday.
 - Review session today 5-7pm in Cory 540.

Configurable Interconnect

- Between rows and columns of CLBs are wiring channels.
- These are programmable. Each wire can be connected in many ways.
- Switch Box:
 - Each interconnection has a transistor switch.
 - Each switch is controlled by 1-bit configuration register.



After Programming





25

EECS151 L11 FPGA

- **FPGA**

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Diverse Resources on FPGA

Colors represent different types of resources:

Logic

Block RAM

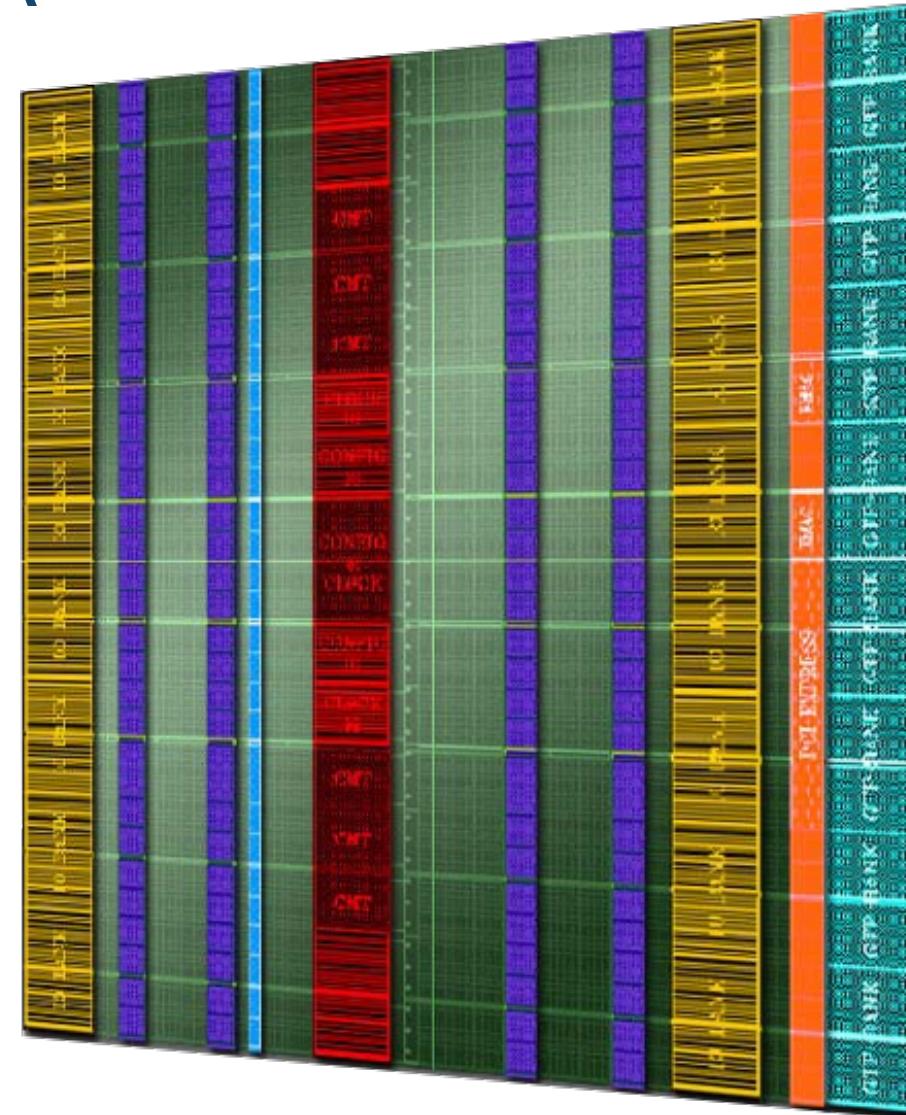
DSPs

Clocking

I/O

Serial I/O + PCI

A routing fabric runs throughout the chip to wire everything together.



Virtex-5 Die
Photo

Block RAM

- Block Random Access Memory
- Used for storing large amounts of data:
 - 18Kb or 36Kb
 - Configurable bitwidth
 - 2 read and write ports
- More recently
 - UltraRAM in UltraScale+ devices
 - 288Kb

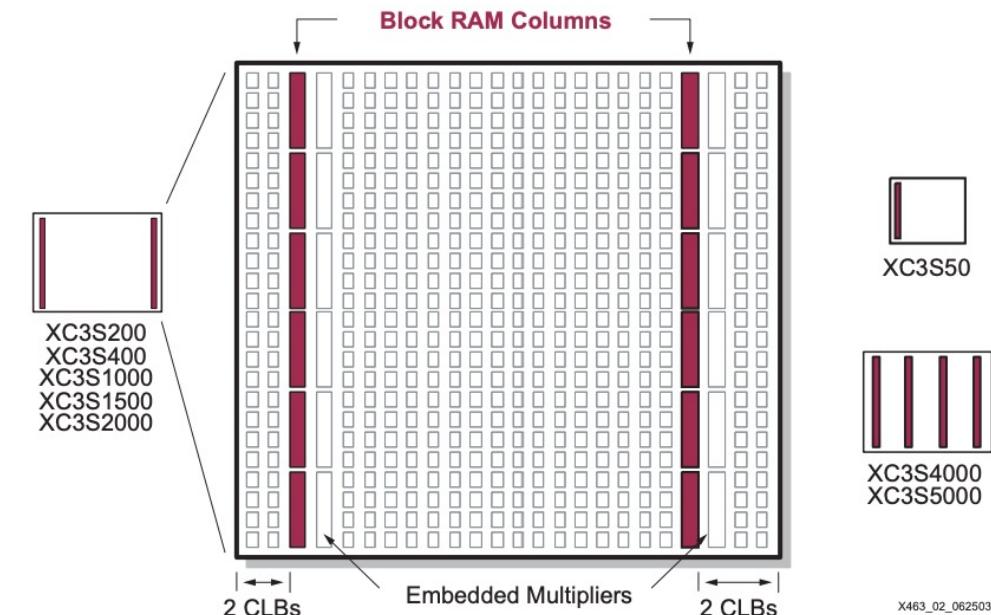
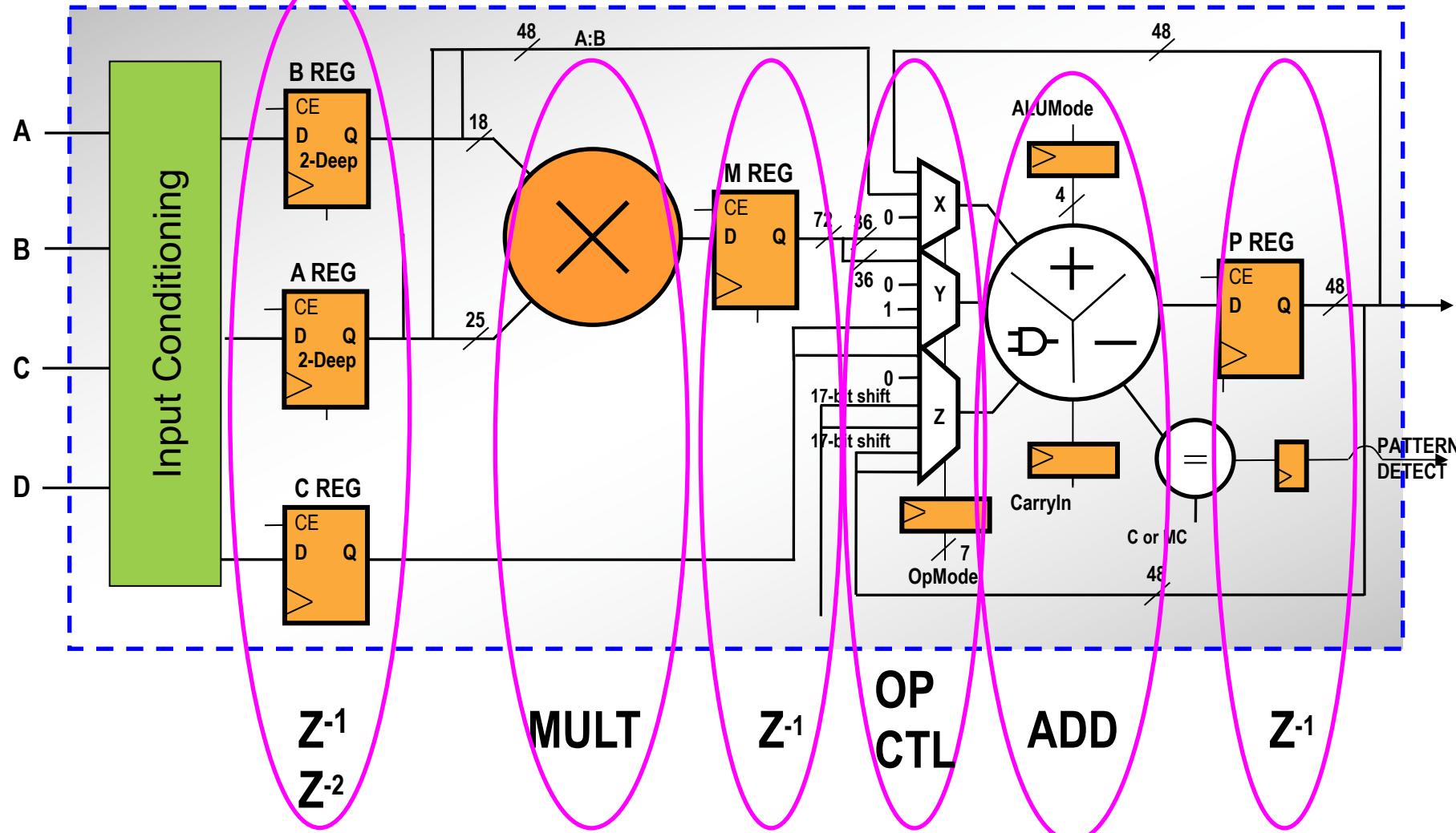


Figure 2: Block RAMs Arranged in Columns with Detailed Floorplan of XC3S200

Xilinx Datasheet

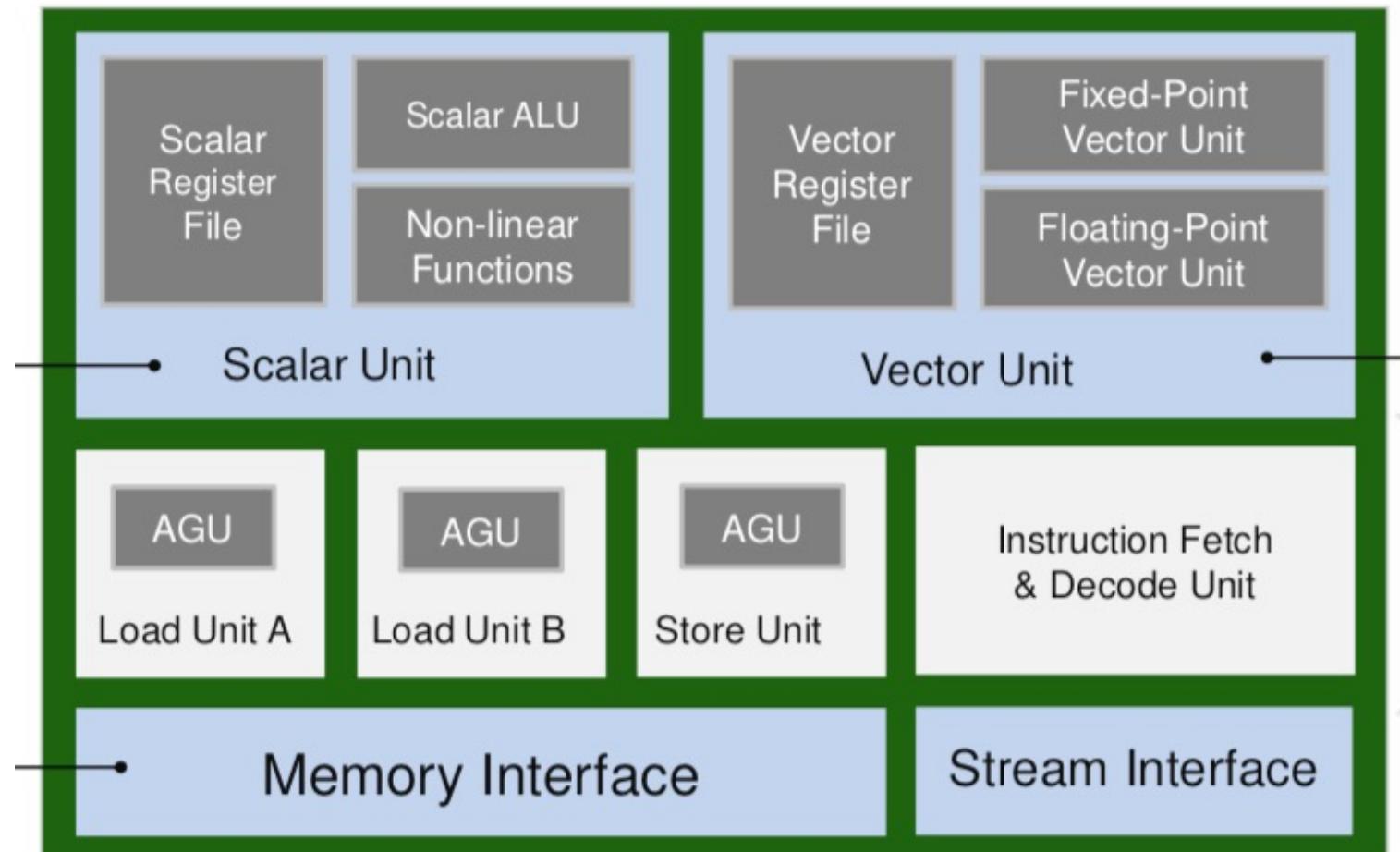
DSP Slice



Efficient implementation of multiply, add, bit-wise logical. Xilinx Resource

AI Engine

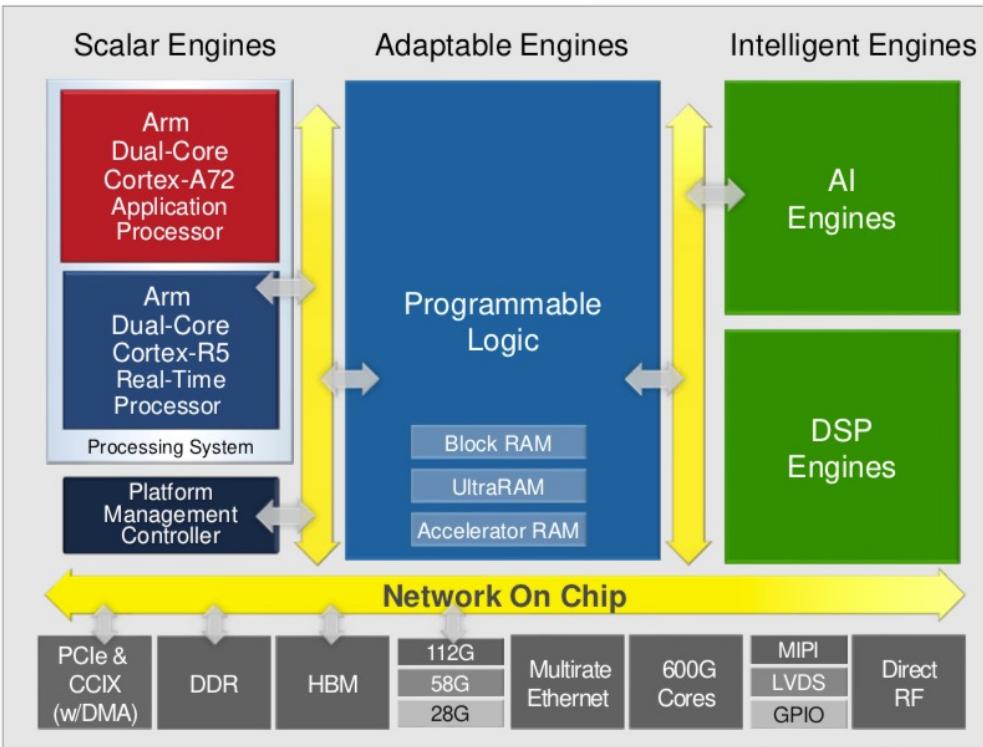
- Versal AI Core



Xilinx
HotChips'2019

State-of-the-art Xilinx FPGA Platform

- Versal (ACAP: Adaptive Compute Acceleration Platform)

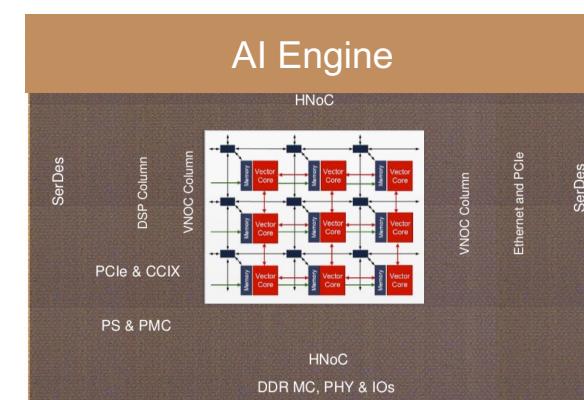
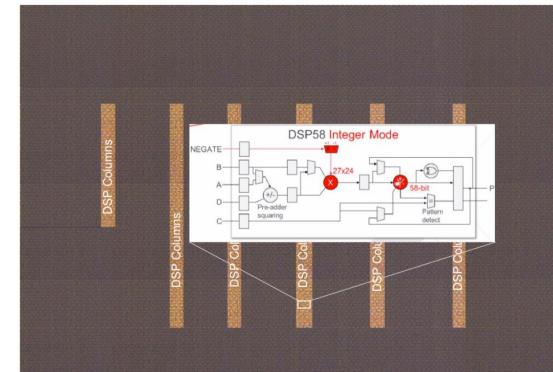
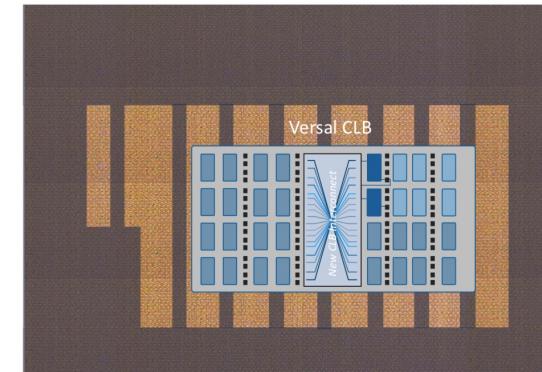


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30

EECS151 L11 FPGA

Shao Fall 2022 © UCB



Summary

- FPGAs are widely used for hardware prototyping and accelerating key applications.
- Core FPGA building blocks:
 - Configurable Logic Blocks (CLBs)
 - Slices
 - Look-Up Tables
 - FlipFlops
 - Carry chain
 - Configurable Interconnect
 - Switch boxes
- Modern FPGA Designs:
 - BRAMs, DSPs, and AI Engines