[pp4fpga] Matrix Multiplication

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HLS C-sim/Synthesis/Cosim (Screenshot + brief intro) :

矩陣乘法是一種根據兩個矩陣得到第三個矩陣的二元運算，第三個矩陣即前兩者的乘積，矩陣可以用來表示線性映射，矩陣積則可以用來表示線性映射的複合。因此，矩陣乘法是線性代數的基礎工具，不僅在數學中有大量應用，在應用數學、物理學、工程學等領域也有廣泛使用。

這次的實驗是用 HLS 實做一個簡單的矩陣乘法，source 如下

```
#include "matrixmultiplication.h"



void matrixmul(int A[N][M], int B[M][P], int AB[N][P]) {
  //#pragma HLS ARRAY_RESHAPE variable=A complete dim=2
  //#pragma HLS ARRAY_RESHAPE variable=B complete dim=1
  /* for each row and column of AB */
  row: for(int i = 0; i < N; ++i) {
    col: for(int j = 0; j < P; ++j) {
      //#pragma HLS PIPELINE II=1
      /* compute (AB)i,j */
      int ABij = 0;
    product: for(int k = 0; k < M; ++k) {
        ABij += A[i][k] * B[k][j];
      }
      AB[i][j] = ABij;
    }
  }
}
```

C-sim :

```
INFO: [SIM 2] *************** CSIM start ***************
INFO: [SIM 4] CSIM will launch GCC as the compiler.
   Compiling ../../../matrixmultiplication-top.cpp in debug mode
   Compiling ../../../matrixmultiplication.cpp in debug mode
   Generating csim.exe
INPUTS
Output:
   0     10416 10912 11408 11904 12400 12896 13392 13888 14384 14880 15376 15872 16368 16864 17360 17856 18352 18848 19344 19840 20336 20832 21328 21824 22320 22816 23312 23808 24304 24800 25296 25792
   1     10912 11440 11968 12496 13024 13552 14080 14608 15136 15664 16192 16720 17248 17776 18304 18832 19360 19888 20416 20944 21472 22000 22528 23056 23584 24112 24640 25168 25696 26224 26752 27280
   2     11408 11968 12528 13088 13648 14208 14768 15328 15888 16448 17008 17568 18128 18688 19248 19808 20368 20928 21488 22048 22608 23168 23728 24288 24848 25408 25968 26528 27088 27648 28208 28768
   3     11904 12496 13088 13680 14272 14864 15456 16048 16640 17232 17824 18416 19008 19600 20192 20784 21376 21968 22560 23152 23744 24336 24928 25520 26112 26704 27296 27888 28480 29072 29664 30256
   4     12400 13024 13648 14272 14896 15520 16144 16768 17392 18016 18640 19264 19888 20512 21136 21760 22384 23008 23632 24256 24880 25504 26128 26752 27376 28000 28624 29248 29872 30496 31120 31744
   5     12896 13552 14208 14864 15520 16176 16832 17488 18144 18800 19456 20112 20768 21424 22080 22736 23392 24048 24704 25360 26016 26672 27328 27984 28640 29296 29952 30608 31264 31920 32576 33232
   6     13392 14080 14768 15456 16144 16832 17520 18208 18896 19584 20272 20960 21648 22336 23024 23712 24400 25088 25776 26464 27152 27840 28528 29216 29904 30592 31280 31968 32656 33344 34032 34720
   7     13888 14608 15328 16048 16768 17488 18208 18928 19648 20368 21088 21808 22528 23248 23968 24688 25408 26128 26848 27568 28288 29008 29728 30448 31168 31888 32608 33328 34048 34768 35488 36208
   8     14384 15136 15888 16640 17392 18144 18896 19648 20400 21152 21904 22656 23408 24160 24912 25664 26416 27168 27920 28672 29424 30176 30928 31680 32432 33184 33936 34688 35440 36192 36944 37696
   9     14880 15664 16448 17232 18016 18800 19584 20368 21152 21936 22720 23504 24288 25072 25856 26640 27424 28208 28992 29776 30560 31344 32128 32912 33696 34480 35264 36048 36832 37616 38400 39184
  10     15376 16192 17008 17824 18640 19456 20272 21088 21904 22720 23536 24352 25168 25984 26800 27616 28432 29248 30064 30880 31696 32512 33328 34144 34960 35776 36592 37408 38224 39040 39856 40672
  11     15872 16720 17568 18416 19264 20112 20960 21808 22656 23504 24352 25200 26048 26896 27744 28592 29440 30288 31136 31984 32832 33680 34528 35376 36224 37072 37920 38768 39616 40464 41312 42160
  12     16368 17248 18128 19008 19888 20768 21648 22528 23408 24288 25168 26048 26928 27808 28688 29568 30448 31328 32208 33088 33968 34848 35728 36608 37488 38368 39248 40128 41008 41888 42768 43648
  13     16864 17776 18688 19600 20512 21424 22336 23248 24160 25072 25984 26896 27808 28720 29632 30544 31456 32368 33280 34192 35104 36016 36928 37840 38752 39664 40576 41488 42400 43312 44224 45136
  14     17360 18304 19248 20192 21136 22080 23024 23968 24912 25856 26800 27744 28688 29632 30576 31520 32464 33408 34352 35296 36240 37184 38128 39072 40016 40960 41904 42848 43792 44736 45680 46624
  15     17856 18832 19808 20784 21760 22736 23712 24688 25664 26640 27616 28592 29568 30544 31520 32496 33472 34448 35424 36400 37376 38352 39328 40304 41280 42256 43232 44208 45184 46160 47136 48112
  16     18352 19360 20368 21376 22384 23392 24400 25408 26416 27424 28432 29440 30448 31456 32464 33472 34480 35488 36496 37504 38512 39520 40528 41536 42544 43552 44560 45568 46576 47584 48592 49600
  17     18848 19888 20928 21968 23008 24048 25088 26128 27168 28208 29248 30288 31328 32368 33408 34448 35488 36528 37568 38608 39648 40688 41728 42768 43808 44848 45888 46928 47968 49008 50048 51088
  18     19344 20416 21488 22560 23632 24704 25776 26848 27920 28992 30064 31136 32208 33280 34352 35424 36496 37568 38640 39712 40784 41856 42928 44000 45072 46144 47216 48288 49360 50432 51504 52576
  19     19840 20944 22048 23152 24256 25360 26464 27568 28672 29776 30880 31984 33088 34192 35296 36400 37504 38608 39712 40816 41920 43024 44128 45232 46336 47440 48544 49648 50752 51856 52960 54064
  20     20336 21472 22608 23744 24880 26016 27152 28288 29424 30560 31696 32832 33968 35104 36240 37376 38512 39648 40784 41920 43056 44192 45328 46464 47600 48736 49872 51008 52144 53280 54416 55552
  21     20832 22000 23168 24336 25504 26672 27840 29008 30176 31344 32512 33680 34848 36016 37184 38352 39520 40688 41856 43024 44192 45360 46528 47696 48864 50032 51200 52368 53536 54704 55872 57040
  22     21328 22528 23728 24928 26128 27328 28528 29728 30928 32128 33328 34528 35728 36928 38128 39328 40528 41728 42928 44128 45328 46528 47728 48928 50128 51328 52528 53728 54928 56128 57328 58528
  23     21824 23056 24288 25520 26752 27984 29216 30448 31680 32912 34144 35376 36608 37840 39072 40304 41536 42768 44000 45232 46464 47696 48928 50160 51392 52624 53856 55088 56320 57552 58784 60016
  24     22320 23584 24848 26112 27376 28640 29904 31168 32432 33696 34960 36224 37488 38752 40016 41280 42544 43808 45072 46336 47600 48864 50128 51392 52656 53920 55184 56448 57712 58976 60240 61504
  25     22816 24112 25408 26704 28000 29296 30592 31888 33184 34480 35776 37072 38368 39664 40960 42256 43552 44848 46144 47440 48736 50032 51328 52624 53920 55216 56512 57808 59104 60400 61696 62992
  26     23312 24640 25968 27296 28624 29952 31280 32608 33936 35264 36592 37920 39248 40576 41904 43232 44560 45888 47216 48544 49872 51200 52528 53856 55184 56512 57840 59168 60496 61824 63152 64480
  27     23808 25168 26528 27888 29248 30608 31968 33328 34688 36048 37408 38768 40128 41488 42848 44208 45568 46928 48288 49648 51008 52368 53728 55088 56448 57808 59168 60528 61888 63248 64608 65968
  28     24304 25696 27088 28480 29872 31264 32656 34048 35440 36832 38224 39616 41008 42400 43792 45184 46576 47968 49360 50752 52144 53536 54928 56320 57712 59104 60496 61888 63280 64672 66064 67456
  29     24800 26224 27648 29072 30496 31920 33344 34768 36192 37616 39040 40464 41888 43312 44736 46160 47584 49008 50432 51856 53280 54704 56128 57552 58976 60400 61824 63248 64672 66096 67520 68944
  30     25296 26752 28208 29664 31120 32576 34032 35488 36944 38400 39856 41312 42768 44224 45680 47136 48592 50048 51504 52960 54416 55872 57328 58784 60240 61696 63152 64608 66064 67520 68976 70432
  31     25792 27280 28768 30256 31744 33232 34720 36208 37696 39184 40672 42160 43648 45136 46624 48112 49600 51088 52576 54064 55552 57040 58528 60016 61504 62992 64480 65968 67456 68944 70432 71920
Comparing against output data
*********************************************
PASS: The output matches the golden output!
*********************************************
INFO: [SIM 1] CSim done with 0 errors.
INFO: [SIM 3] *************** CSIM finish ***************
```

Synthesis :

Performance Estimates

Timing

Summary

Clock	Target	Estimated	Uncertainty
ap_clk	5.00 ns	4.108 ns	0.63 ns

Latency

Summary

Latency (cycles)		Latency (absolute)		Interval (cycles)		
min	max	min	max	min	max	Type
198721	198721	0.994 ms	0.994 ms	198721	198721	none

Detail

Instance

Loop

Utilization Estimates

Summary

Name	BRAM_18K	DSP48E	FF	LUT	URAM
DSP	-	-	-	-	-
Expression	-	-	0	174	-
FIFO	-	-	-	-	-
Instance	6	3	442	299	-
Memory	-	-	-	-	-
Multiplexer	-	-	-	83	-
Register	-	-	195	-	-
Total	6	3	637	556	0
Available	1590	1260	728400	364200	0
Utilization (%)	~0	~0	~0	~0	0

Cosim :

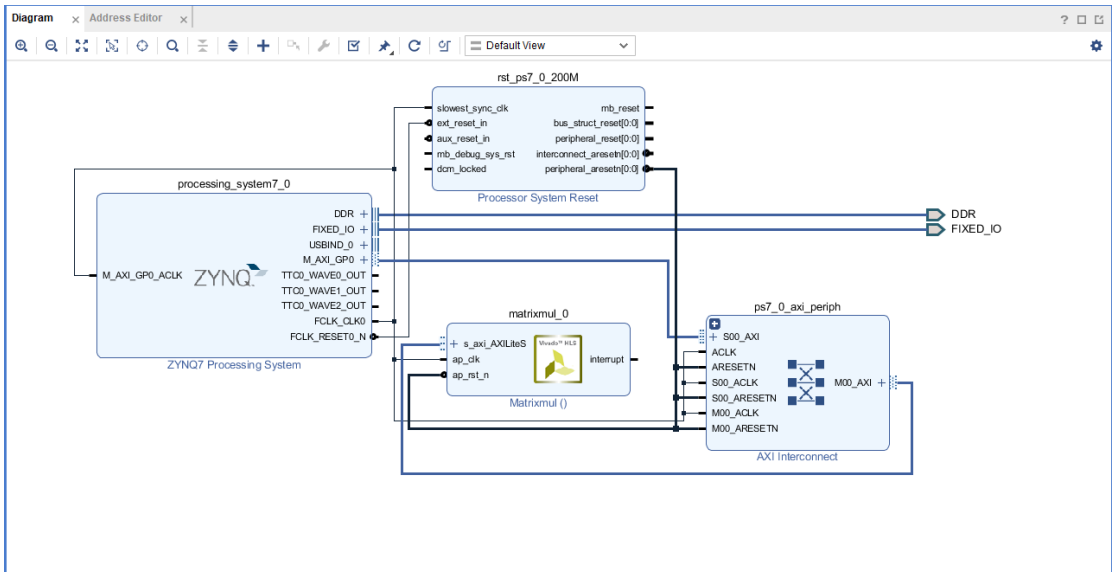
Cosimulation Report for 'matrixmul'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	233549	233549	233549	NA	NA	NA

Export the report(.html) using the Export Wizard

System level bring-up (Pynq or U50)



Improvement - throughput, area

對輸入的兩個矩陣做 array partition，並且加上 pipeline II = 1，由 synthesis 比較的結果(如下圖)可以發現 latency 下降了非常多，但也因為有做 array partition，所以 reosurce 用的也多了不少

Synthesis comparisom :

Performance Estimates

Timing

Clock		solution	improve
ap_clk	Target	5.00 ns	5.00 ns
	Estimated	4.108 ns	4.108 ns

Latency

		solution	improve
Latency (cycles)	min	198721	1033
	max	198721	1033
Latency (absolute)	min	0.994 ms	5.165 us
	max	0.994 ms	5.165 us
Interval (cycles)	min	198721	1033
	max	198721	1033

Utilization Estimates

	solution	improve
BRAM_18K	6	116
DSP48E	3	96
FF	637	9508
LUT	556	3165
URAM	0	0

Cosim :

Cosimulation Report for 'matrixmul'

Result

		Latency			Interval		
RTL	Status	min	avg	max	min	avg	max
VHDL	NA	NA	NA	NA	NA	NA	NA
Verilog	Pass	24952	24952	24952	NA	NA	NA

Export the report(.html) using the Export Wizard

Github : https://github.com/schuang23/MSOC.git