

SESSION 2

MEMORY HIERARCHY



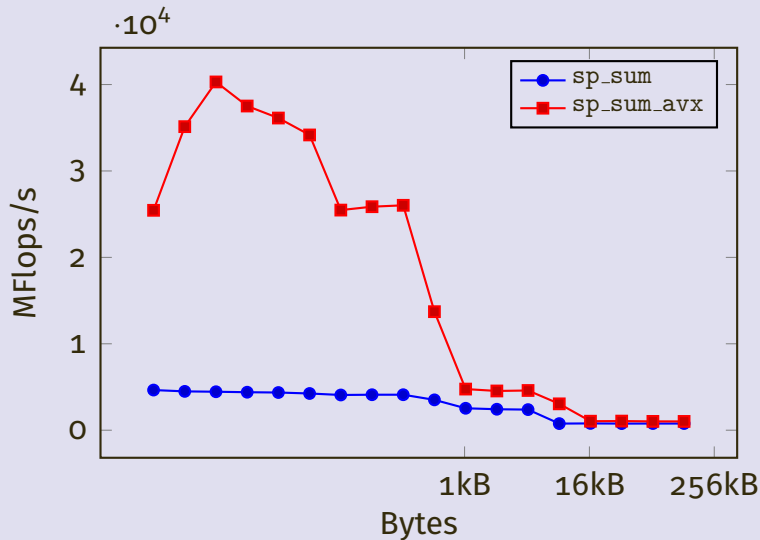
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Sum reduction benchmark (Exercise 1)

- ▶ SIMD: 4 plateaus
- ▶ scalar: 3 plateaus



Performance peak

Variability

This is due to CPU Boosting.

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Hardware bottlenecks

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Hardware bottlenecks

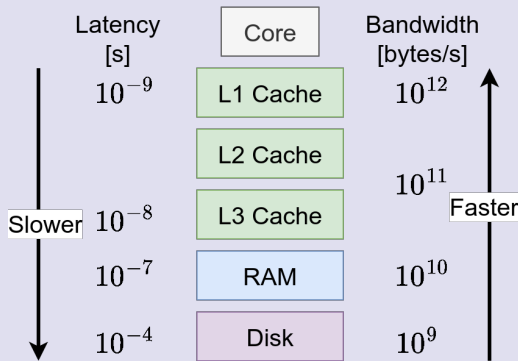
- ▶ Cannot be instruction throughput.
- ▶ Memory bandwidth decreases with vector size

Memory hierarchy

Two types of memory:

- ▶ *small and fast*
- ▶ *large and slow*

Large and fast is impossible:
⇒ physics gets in the way.



Optimisation: refactor algorithms to keep data in fast memory.

Check Colin Scott's page for more detail on latencies.

Cache memory: overview

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Issues

- ▶ Frequently accessed data not known *a priori*
- ▶ Only heuristics are possible \Rightarrow *principle of locality*

Principle of locality

- ▶ Frequently accessed data often unknown before execution
- ▶ In practice, most programs exhibit *locality* of data access.
- ▶ Optimised algorithms attempt to *exploit* this locality.

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Temporal locality

If I access data at some memory address, it is likely that I will do so again “soon”.

Spatial locality

If I access data at some memory address, it is likely that I will access neighbouring addresses.

Temporal locality

On **first access** to a new address, the data is:

- ▶ loaded from main memory to registers
- ▶ stored in cache

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On **first access** to a new address, the data is:

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Trade-off solution:

- ▶ Small performance penalty for first access (storing is not free)
- ▶ Subsequent accesses use cached copy and are much faster.

Spatial locality

On **first access** to a new address, the data is:

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- ▶ neighbouring addresses are also stored in cache

Spatial locality

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- ▶ loaded from main memory to registers
- ▶ stored in cache
- ▶ neighbouring addresses are also stored in cache

Trade-off solution:

- ▶ Large performance penalty for first access
- ▶ Subsequent accesses to neighbouring data will be fast

Example: sum reduction

```
float s[16] = 0  
for (i = 0; i < N; i++)  
    s[i%16] += a[i];
```

- ▶ Temporal locality
 - ▶ 16 entries of `s` are accessed repeatedly
 - ▶ Makes to keep all of `s` in cache
- ▶ Spatial locality
 - ▶ Contiguous entries of `a` are accessed
 - ▶ When loading `a[i]` it makes sense to load `a[i+1]` too.

Designing a cache

Important questions

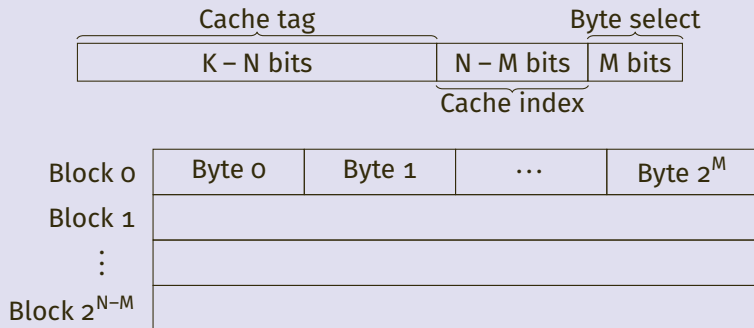
1. When we load data into the cache, where do we put it?
 2. If we have an address, how do determine if it is in the cache?
 3. What do we do when the cache becomes full?
- ▶ Each datum uniquely referenced by its K-bit *address*
 - ▶ Need to turn this large memory address into a cache location
 - ▶ K is typically large ($2^{32} / 2^{64}$ addresses)

Direct mapped cache

- ▶ Cache can store 2^N bytes.
- ▶ Divided into *blocks* (or *cache lines*) each of 2^M bytes.
- ▶ Each address references one byte.
- ▶ Use N bits of the address to select which slot in the cache to use.

Simple solution:

Direct mapped caches: indexing



- **Byte select:** Use lowest M bits to select correct byte in block.
- **Cache index:** Use next $N - M$ bits to select correct block.
- **Cache tag:** Use remaining $K - N$ bits as a key.

Choice of cache line size

- ▶ Data is loaded one *cache line* at a time
- ▶ Immediately exploits *spatial locality*
- ▶ Larger cache lines are not always better
- ▶ Almost all modern CPUs use 64-byte size

Rule of thumb

Cache-friendly algorithms work on cache line-sized chunks of data.

Direct mapped caches: eviction

- ▶ **Conflict:** two addresses have the same low bit pattern
- ▶ **Resolution:** newest loaded address wins.
- ▶ This is a *least recently used* (LRU) eviction policy.

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What can go wrong?

```
int a[64], b[64], r = 0;
for (int i = 0; i < 100; i++)
    for (int j = 0; j < 64; j++)
        r += a[j] + b[j];
```

- ▶ 1KB cache
- ▶ 32-byte block size
- ▶ So $N = 10, M = 5$
- ▶ 32 blocks in the cache

Conflicts reduce *effective* cache size

```
for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```


```
&a[00] = ... 00000 00000 => block 0, byte offset 0  
&a[01] = ... 00000 00100 => block 0, byte offset 4  
&a[02] = ... 00000 01000 => block 0, byte offset 8  
&a[03] = ... 00000 01100 => block 0, byte offset 12  
&a[04] = ... 00000 10000 => block 0, byte offset 16  
&a[05] = ... 00000 10100 => block 0, byte offset 20  
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...
```

Conflicts reduce *effective* cache size

```
for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```

a _{0:7}	a _{8:15}	a _{16:23}	a _{24:31}
b _{0:7}	b _{8:15}	b _{16:23}	b _{24:31}

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Conflicts reduce *effective* cache size

```
for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```

$b_{32:39}$	$a_{8:15}$	$a_{16:23}$	$a_{24:31}$
$a_{32:39}$			
$b_{0:7}$	$b_{8:15}$	$b_{16:23}$	$b_{24:31}$

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Conflicts reduce *effective* cache size

```
for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```

$b_{32:39}$	$b_{40:47}$	$a_{16:23}$	$a_{24:31}$
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```

Conflicts reduce *effective* cache size

```
for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```

$b_{32:39}$	$b_{40:47}$	$b_{48:55}$	$a_{24:31}$
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for (int j = 0; j < 64; j++)  
    r += a[j] + b[j];
```

$b_{32:39}$	$b_{40:47}$	$b_{48:55}$	$b_{56:63}$
$a_{32:39}$	$a_{40:47}$	$a_{48:55}$	$a_{56:63}$
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Cache thrashing

What can go wrong?

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for (int i = 0; i < 100; i++)
    for (int j = 0; j < 64; j++)
        r += A[j] + B[j];
```

- ▶ 1KB cache
- ▶ 32 byte block size
- ▶ So $N = 10$, $M = 5$.
32 blocks in the cache.

- ▶ We need $2 \cdot 64 \cdot 4 = 512$ bytes to store A and B in cache.
- ▶ This only requires 16 blocks, so our cache is large enough.
- ▶ If low bits of addresses match, same cache lines are mapped.
- ▶ In the worst case, every load of $B[j]$ evicts $A[j]$, and vice versa.

Cache associativity

- ▶ Direct mapped
 - ▶ Each RAM *block* maps to exactly one cache line.
 - ▶ LRU eviction policy (new data overwrite old)

Cache associativity

- ▶ Direct mapped
 - ▶ Each RAM *block* maps to exactly one cache line.
 - ▶ LRU eviction policy (new data overwrite old)
- ▶ Fully associative
 - ▶ Each RAM *byte* can map to any cache line
 - ▶ Data is stored in first unused cache line
 - ▶ If all lines are used, overall LRU one is replaced
 - ▶ Most flexible, but also most expensive

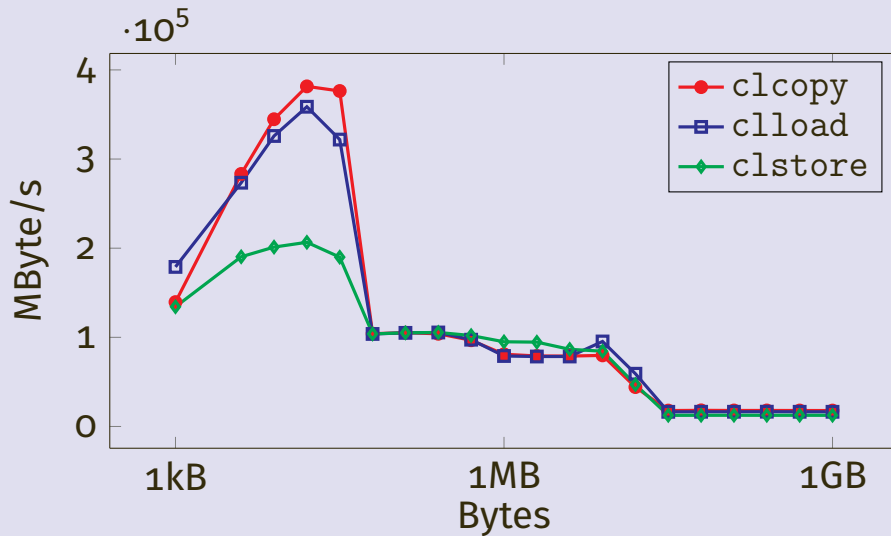
k-way set associative cache

- ▶ k “copies” of a direct mapped cache. Each block from main memory maps to one of k cache lines, called *sets*.
- ▶ Typically use LRU eviction.
- ▶ Usual choice: $N \in \{2, 4, 8, 16\}$.
- ▶ Skylake has $N = 8$ for L1, $N = 16$ for L2, $N = 11$ for L3.

Exercise: cache and memory bandwidth

1. Split into small groups
2. Make sure one person per group has access to Hamilton
3. Benchmark memory bandwidth as a function of vector size
4. You can use the bash script from last week.
5. Ask questions!

Results



Results

