ECE 411

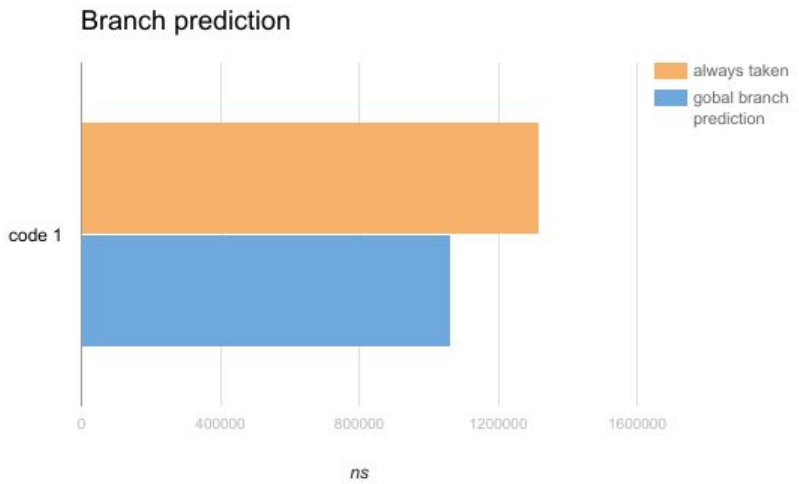
Group 1

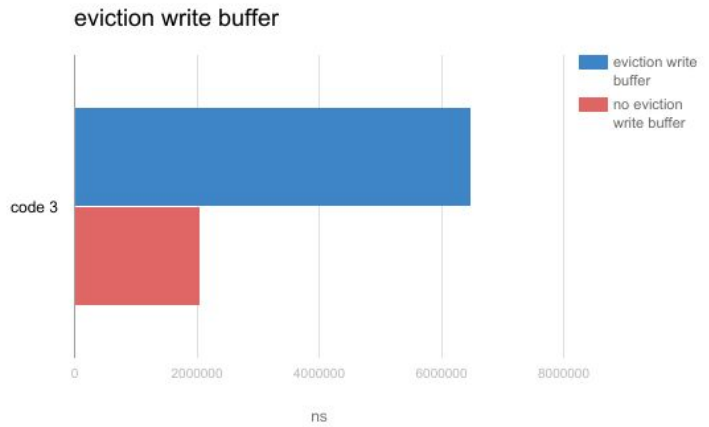
What's so cool about our design?

- We have a 4-way L2 cache with true LRU.
- 2-level branch history table.
- 4 cycle L2 accesses.

How our feature affect performance

Original Fmax 50 Mhz Final 111 Mhz after advanced features implementations.





If we had a time machine

- Start early
- Getting everything working before adding features.