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MP3.1 Progress Report

This first checkpoint we implemented the basic structure of a pipelined processor. We needed to implement the five main stages, fetch, decode, execute, memory, and write-back. We based each of these stages off of our earlier MPs of a regular LC-3b processor datapath. One big change with the pipeline design is the addition of stage registers. We determined what data needed to be pasted to the next stage of the processor through the stage registers and what data needed to be passed back to previous stages. Jay implemented fetch and decode, Steven implemented execute, and Sean implemented memory and write-back stages. Once everything was created we tested our design with the LDR, STR, ADD, AND, NOT, and BR instructions with NOPs in between instructions to stall the pipeline.