A Normally-Off GaN MIS-HEMT Fabricated Using Atomic Layer Etching to Improve Device Performance Uniformity for High Power Applications

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***Abstract*— Normally-off ferroelectric charge trap gate stack GaN high electron mobility transistor (FEG-HEMT) was fabricated with atomic layer etching (ALE) to precisely control the device parameters including V_{th} of the device. The ALE process consists of cyclic Cl_2 adsorption modification steps and the Ar ion removal steps. The ALE process achieved etch-per-cycle (EPC) of 0.347 nm/cycle and superior etching morphology with RMS = 0.281 nm. The fabricated GaN HEMT using the ALE process exhibited a high threshold voltage (V_{th}) of 5.06 V, high maximum drain current ($I_{D,MAX}$) of 772 mA/mm with low on-resistance (R_{on}) of 8.57 Ω · mm and high breakdown voltage (BV) of 888 V, the device also showed good V_{th} uniformity. Finally, the contact resistance (R_c) was reduced from 0.46 Ω · mm to 0.15 Ω · mm by the ALE process, and the dynamic on-resistance (dyn-R_{on}) was improved at the same time.**

***Index Terms*— Atomic layer etching, AlGaN/GaN, enhancement-mode, charge trap gate stack, threshold voltage uniformity.**

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I. Introduction

ALGAN/GAN high-electron-mobility transistors (HEMTs) are promising for high power applications due to the superior electrical properties [1], [2]. For power applications, normally off or enhancement-mode (E-mode) device operation mode is preferred to simplify the design of the circuits and to diminish the power loss during switching and for safety reasons. To date, the E-mode GaN HEMT has been achieved by p-GaN [3], [4], [5], gate-recessed process [6], [7], and cascode approaches [8], [9]. Recently, gate recessed with hybrid ferroelectric charge trap gate stack has been demonstrated with high threshold voltage and high current due to the polarization effect of the ferroelectric layer [10], [11], [12]. In this study, the atomic layer etching process was implemented on the FEG-HEMT process to further increase the V_{th} value of the E-mode device and the uniformity of the V_{th} value across the wafer.

In the GaN device fabrication, GaN and AlGaN materials etching process was performed by inductively coupled plasma (ICP) etching system for both gate recess and ohmic recess processes [13], [14]. The drawback of the plasma etching techniques is that the radicals, ions, and UV light included due to plasma discharges can cause lattice damages of the etched surface [15].

ALE is a self-limiting chemical etching process consisting of cyclic surface modification and removal steps, these steps have extremely low etching damage during the process. Thus, the ALE method is a good candidate for device process due to the excellent quality of the interface after etching [16], [17], [18], [19], [20], [21], [22]. In the past research, most of the ALE studies on GaN focused on the etching mechanisms of the materials, studies of ALE etching with different processing conditions for GaN HEMT power devices are still lacking in the literature [23], [24].

In this work, we fabricated the GaN HEMT with the ALE process and made a systematic comparison between ALE and traditional Cl_2 plasma etching (Cl_2 etch) for the GaN device. The ALE process precisely controlled the etch depth and resulted in better surface morphology with RMS = 0.281 nm. The fabricated GaN HEMT by ALE process exhibited a high threshold voltage (V_{th}) of 5.06 V, high maximum drain current ($I_{D,MAX}$) of 772 mA/mm with low on-resistance (R_{on}) of 8.57 Ω·mm, high breakdown voltage (BV) of 888 V, and the

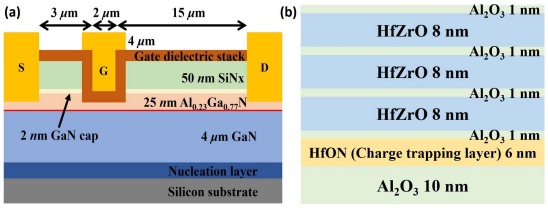

Fig. 1. (a) Cross section schematic of the GaN FEG-HEMTs grown on (111) Si substrate. (b) Ferroelectric gate stack structure.

uniformity of V_{th} across the whole sample was also improved. Finally, the contact resistance was reduced from 0.46 $\Omega \cdot$ mm to 0.15 $\Omega \cdot$ mm, and the dynamic on-resistance (dyn-R_{on}) of the devices was also improved by the ALE process.

II. Device Fabrication

Fig. 1(a) shows the cross-section of the AlGaN/GaN FEG-HEMT. The epitaxial structure includes 4 μm GaN buffer layer/25nm buffer layer with aluminum concentration of 23%/2 nm GaN cap layer. The devices process started with mesa isolation using Cl_2-based dry etching by ICP to define the active area. Ohmic recess was etched by the ALE process and Ti/Al/Ni/Au was deposited as source/drain metals, followed by annealing at 800 ° for 60 seconds. A 50 nm SiN_x film was deposited as the passivation layer by plasma-enhanced chemical vapor deposition (PECVD), a pre-treatment with *in-situ* nitrogen plasma was carried out before the passivation layer was deposited [25].

Gate recess process was performed by etching the passivation layer with CF_4 plasma and then etching the AlGaN with the ALE process. Ferroelectric charge trap gate stack was deposited by atomic layer deposition (ALD) system. The gate stacks were deposited with 10 nm Al_2O_3 tunnel oxide layer, 6 nm HfON charge trapping layer, where the ratio of O to N is 1:1, and 28 nm Al_2O_3/HfZrO/Al_2O_3 blocking oxide layer, the gate stack structure is as shown in Fig. 1(b). After the deposition of the gate stacks, post-deposition annealing at 400 °C in N_2 atmosphere was performed. Ni/Au was deposited as the gate metal. The gate length, gate-source spacing, and gate-drain spacing of the fabricated GaN HEMT were 3 μm, 2 μm, and 15 μm, respectively.

III. Result and Discussion

The ALE process in this study was performed using ICP tool. Fig. 2 shows the steps of the ALE process. A full ALE cycle consists of two half-reactions. The first half-reaction is the modification step, in which the binding energy of the surface atoms is modified by the chlorination reaction. In this step, chlorine is introduced into the chamber and the top ICP power of 300W and down RF power of 0 W was turned on to react with the surface atoms, where the reaction time is 10 seconds. Followed by argon purge and evacuation to ensure that no residual chlorine remains in the chamber to affect the next half-reaction. The second half-reaction is the removal step, which removes the chlorinated surface in the modification step by bombarding the surface of the sample with top ICP power of 100W and down RF power of 15W low-energy argon ions for 10 seconds.

Fig. 3(a) shows the etch depth of ALE at different etch cycles, the EPC equals to 0.347 nm/cycle. Fig. 3(b) shows

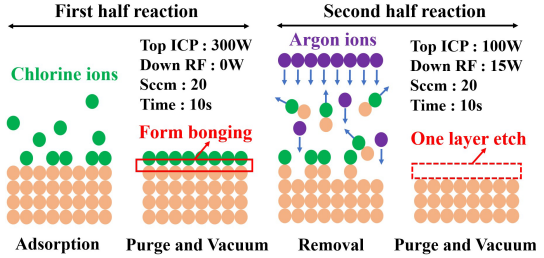

Fig. 2. AlGaN/GaN one atomic layer etching cycle process. Modification Step and Removal Step are included.

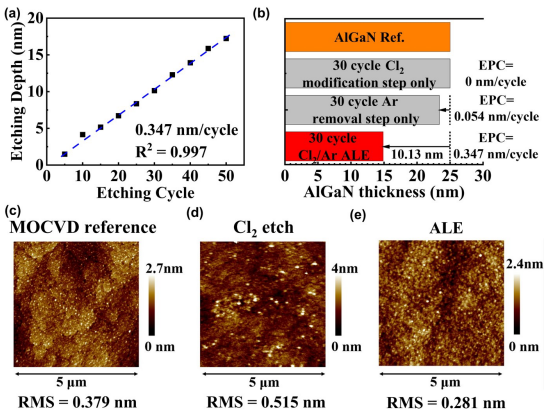

Fig. 3. (a) Etching depth of the ALE process. (b) Etching level for each step and ALE process. (c) Roughness image of MOCVD reference, (d) Cl_2 plasma etching, and (e) ALE.

the etch depth if two steps were performed individually for 30 cycle. For the modification step, the chlorine reacts chemically with the atoms in contact with the surface to form compounds with lower binding energy, and the EPC for this step was 0 nm/cycle. In contrast, the EPC of Ar removal step was 0.054 nm/cycle, causing physical etching about 1.62 nm. Based on the comparison of Cl_2 modification step and Ar removal step, the results indicated AlGaN could not be etched by any single reaction step. However, the EPC for ALE process was 0.347 nm/cycle. It is clarifying that AlGaN could be only etched by sequential modification step and removal step, attributed to the self-limiting reactions of ALE process.

The surface roughness obtained by MOCVD before etching shows the RMS of 0.379 nm as shown in Fig. 3(c). However, the surface RMS of 0.515 nm was obtained after the ICP Cl_2 plasma etching with a significant increase in roughness. Fig. 3(e) shows the surface RMS of 0.281 nm after the ALE process, which is better than the ICP Cl_2 plasma etching and the pristine condition after MOCVD growth. The surface was examined by the AFM. This demonstrates, the ALE process used in this study is a promising way to achieve a smooth surface.

In this work, the gate region of the device was etched by the ALE process with a residual AlGaN thickness of 5 nm after etching, and then a ferroelectric gate dielectric layer was deposited on top to achieve a normally-off GaN HEMT. Before testing the devices, an initialization process ($V_G = 16$ V, $V_D = 0$ V for 1 ms) for the FEG-HEMT is required. The I_D-V_G characteristics are shown in Fig. 4(a). The V_{th} shifted from -1.65 V to 5.06 V due to the application of ferroelectric gate stack. In Fig. 4(b), we also measured the threshold voltages of the devices with the ALE process and

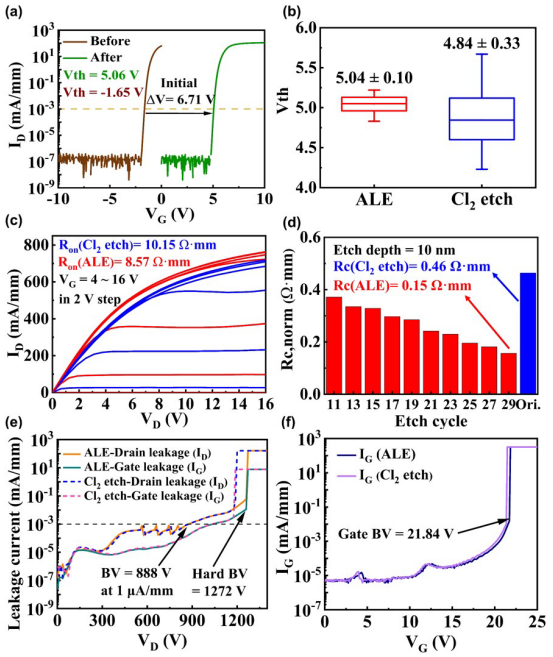

Fig. 4. (a) I_D-V_G before and after the initialization process. (b) V_{th} error bar for both processes. (c) I_D-V_D characteristics between two processes. (d) Compare the contact resistance of the two processes at the same etch depth. (e) Off-state leakage and breakdown voltage. (f) Gate breakdown voltage.

the devices with the ICP Cl_2 plasma etch process separately with a sample size of 25 devices, the results show that the devices processed with ALE have good control of etch depth and etch uniformity and average etch depths are smaller than the ICP Cl_2 plasma etch process.

Fig. 4(c) shows the I_D-V_D output characteristics of two devices, etched with the ALE process and Cl_2 plasma etching process respectively. The device using ALE shows a $I_{D,\,MAX}$ of 772 mA/mm at $V_G = 16$ V, and an excellent R_{on} of 8.57 $\Omega \cdot$ mm. The device using Cl_2 plasma etching shows a $I_{D,MAX}$ of 714 mA/mm at $V_G = 16$ V, and a high R_{on} of 10.15 $\Omega \cdot$ mm.

To further evaluate the effect of the ALE process on the contact resistance, Fig. 4(d) shows the contact resistance versus the etch cycle. The contact resistance was reduced when the ohmic metal is close to the 2DEG interface, due to the reduction of barrier height [26], [27]. The red column represents the data obtained using the ALE process, the contact resistance gradually decreased from 0.37 Ω·mm for the sample etched with 11 cycles to 0.15 Ω·mm for the sample etched with 29 cycles. For the devices with 29 etch cycles, the etch depth was about 10 nm. We also etched the device with the same depth using ICP Cl_2 plasma etching and obtained a contact resistance of 0.46 $\Omega \cdot$mm, which is shown in the blue column.

The off-state leakage current of the two devices is shown in Fig. 4(e). The ALE device exhibits a high breakdown voltage of 888 V at drain current of 1 μA/mm, while the Cl_2 plasma etching device also exhibits a breakdown voltage of 876 V. And the hard breakdown of the two devices are 1272 V and 1188V. The gate breakdown voltage of the two devices are 21.84 V and 21.48 V shown in Fig. 4(f).

However, the positive bias stress (PBS) conditions and negative bias stress (NBS) were performed using $V_D = 0$ V and $V_G = +16$ V for PBS tests and $V_G = -16$ V for NBS tests at room temperature (RT) for 0 s to 1,000 s. The V_{th} shifts after PBS and NBS were +1.18 V and −2.85 V (Not shown here). Therefore, the issue of reliability should be further improved in the future work.

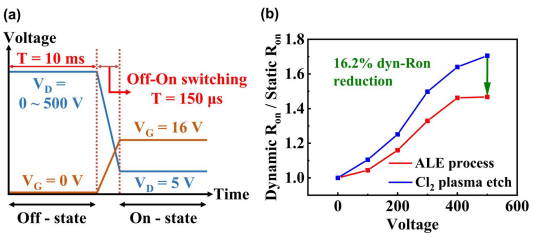

Fig. 5. (a) Dynamic R_{on} measurement setting condition. (b) Dynamic R_{on} ratio comparison of two processes.

TABLE I
THE MEASUREMENT RESULTS OF EACH DATA OF THE CL_2 PLASMA ETCH AND THE ALE PROCESS

Etching method	*Cl_2 plasma etch*	*ALE*
Etching rate	1 nm/second	0.347 nm/cycle
RMS (nm)	0.515	0.281
V_{th} uniformity (V)	4.84 ± 0.33	5.04 ± 0.10
$I_{D,\,MAX}$ (mA/mm)	714	772
R_{on} (Ω·mm)	10.15	8.57
R_c (Ω·mm)	0.46	0.15
Dyn-R_{on}/Static R_{on}	1.705	1.467
BV (V)	876	888
Gate BV (V)	21.48	21.84

The other important feature for the GaN HEMTs is the dynamic on-resistance (dyn-R_{on}) [28], [29]. The dyn-R_{on} can be attributed to the decrease in 2DEG concentration due to the trapping of electrons in the different areas of the device, such as the interface or in the buffer layer [30], [31]. To investigate the device quality improvement by using the ALE process, a stress test was performed to evaluate the switching loss. The test conditions are shown in Fig. 5(a), the gate voltage was switched from OFF-state ($V_G = 0$ V) to ON-state ($V_G = 16$ V) and the drain voltage from 0 V to 500 V.

Fig. 5(b) shows the dyn-R_{on} results of the two devices. Compared to the ICP Cl_2 plasma etch process, the ALE process demonstrates a 16.2% reduction in dynamic R_{on} when stressed $V_D = 500$ V at OFF-state, indicating that the ALE process can effectively reduce the trapping states at the interface. The device performance of the GaN HEMT using ALE process is summarized in Table I.

IV. CONCLUSION

A normally-off hybrid FEG-HEMT was fabricated using the ALE process for ohmic and gate recess. The ALE process consists of cyclic Cl_2 adsorption modification steps and Ar ion removal steps which results in an etch rate of 0.347 nm/cycle, and with a superior etching morphology of RMS = 0.281 nm. The GaN HEMT fabricated with the ALE process exhibited a high V_{th} of 5.06 V, $I_{D,\,MAX}$ of 772 mA/mm with low R_{on} of 8.57 $\Omega \cdot$ mm and high BV of 888 V. Finally, the contact resistance was reduced from 0.46 $\Omega \cdot$mm to 0.15 $\Omega \cdot$mm, and the dynamic R_{on} of the device was also improved by the ALE process. Thus, this work demonstrates that the ALE process can be applied to the FEG-HEMT fabrication with improved device parameter uniformity and overall device performance.

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