

SANYO LC7883

SEGA ENTERPRISES, LTD.

Sega Ozisoft

SANYO LC7883

Dual 16 bit D/A Converter with Digital Filter for Audio System

TENTATIVE

1. Summary

LC7883 is 16 bit D/A converter with eight-times over sampling digital filter.

2. Features

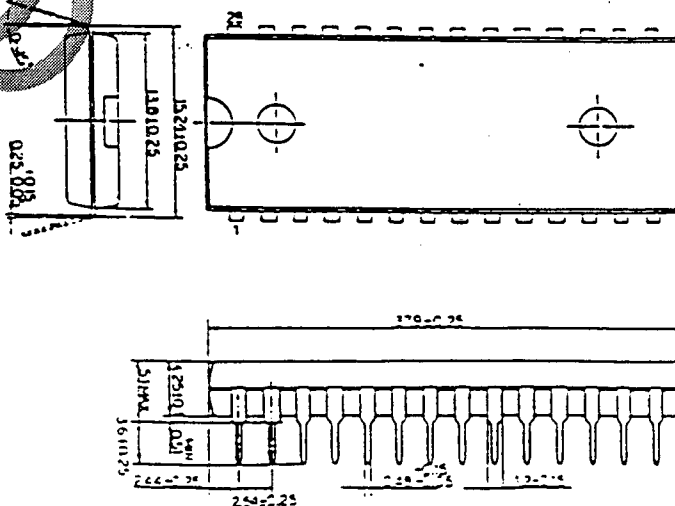
- ★ Eight-times over sampling digital filter
- ★ Digital de-emphasis
- ★ Digital attenuation
- ★ Double speed operation
- ★ 48CLK-384Fs, 49CLK-392Fs, 56CLK-448Fs, 64CLK-512Fs operations
- ★ Dynamic level shift conversion method
- ★ Independent dual channel D/A converter (in-phase output)
- ★ Single 5v power supply

3. Absolute Maximum Rating/ $T_a=25^{\circ}\text{C}$ ($V_{SS}=0\text{V}$)

item	symbol	rating	unit
max. power supply voltage	V_{DD}	$-0.3 \sim +7.0$	V
input voltage	V_{IN}	$-0.3 \sim V_{DD} + 0.3$	V
output voltage	V_{OUT}	$-0.3 \sim V_{DD} + 0.3$	V
operating temp.	T_{OPG}	$-30 \sim +75$	$^{\circ}\text{C}$
storage temp.	T_{STG}	$-40 \sim +125$	$^{\circ}\text{C}$

4. Physical Configuration Diagrams

DIP-28
(600mil)



5. Recommended Operating Conditions

item	symbol	min.	typ.	max.	unit
power supply voltage	V_{DD}	4.5	5.0	5.5	V
reference voltage "H"	V_{refH}	$V_{DD}-0.5$		V_{DD}	V
reference voltage "L"	V_{refL}	0		0.5	V
input voltage "H"	V_{IH}	2.2		$V_{DD}+0.3$	V
input voltage "L"	V_{IL}	-0.3		0.8	V
operating ambient temp.	T_a	-30		75	°C

6. Pin Layout

CH1OUT	1	28	CH2OUT
V_{refH}	2	27	V_{refL}
AVDD	3	26	AGND
DVDD	4	25	XOUT
BCLK	5	24	XIN
DATA	6	23	CLKOUT
LCK	7	22	DGND
TEST	8	21	TEST
ATT	9	20	TEST
SHIFT	10	19	MODE
LATCH	11	18	SOC1
INITB	12	17	SOC2
TEST	13	16	D/X
EMPH2	14	15	EMPH1

PIN No	PIN name	I/O	FUNCTION
1	CH1OUT	O	DAC CH-1 output pin
2	VrefH	R	reference voltage "H" input pin
3	AVDD	P	analog system power supply pin
4	DVDD	P	digital system power supply pin
5	BCLK	I	bit CLK pin
6	DATA	I	digital audio data input pin input in bit serial from MSB
7	LRCK	I	LR CLK input pin LRCK= "H" CH1 LRCK= "L" CH2
8	TEST	I	test pin (normally "L")
9	ATT	I	attenuation data input pin input in bit serial from LSB
10	SHIFT	I	attenuation data shift CLK input pin
11	LATCH	I	attenuation data latch CLK input pin
12	INITB	I	initializing signal input pin(normally "H")

PIN No	PIN name	I/O	FUNCTION
13	TEST	I	test pin (normally "L")
14	EMPH2	I	de-emphasis set pin
15	EMPH1	I	
16	D/N	I	normal/double speed switch pin
17	SOC2	I	input source select pin (PULL DOWN)
18	SOC1	I	
19	MODE	I	operation mode set pin (PULL DOWN)
20	TEST	I	test pin (normally "L") (PULL DOWN)
21	TEST	I	
22	DGND	P	digital system GND pin
23	CLKOUT	O	CLK output pin At 392Fs : 1/2 XOUT At 384Fs, 448Fs, 512Fs : 1/4 XOUT
24	XIN	I	crystal oscillation input pin
25	XOUT	O	crystal oscillation output pin
26	AGND	P	analog system GND pin
27	VrefL	R	reference voltage "L" input pin
28	CH2OUT	O	D A C C H - 2 output pin

I : INPUT PIN
 O : OUTPUT PIN
 P : POWER PIN
 R : REFERENCE VOLTAGE PIN

8. Electric Characteristics

($T_a=25^{\circ}\text{C}$, $V_{DD}=5.0\text{V}$, $V_{refH}=5.0\text{V}$, $V_{refL}=0.0\text{V}$ unless it is specified)

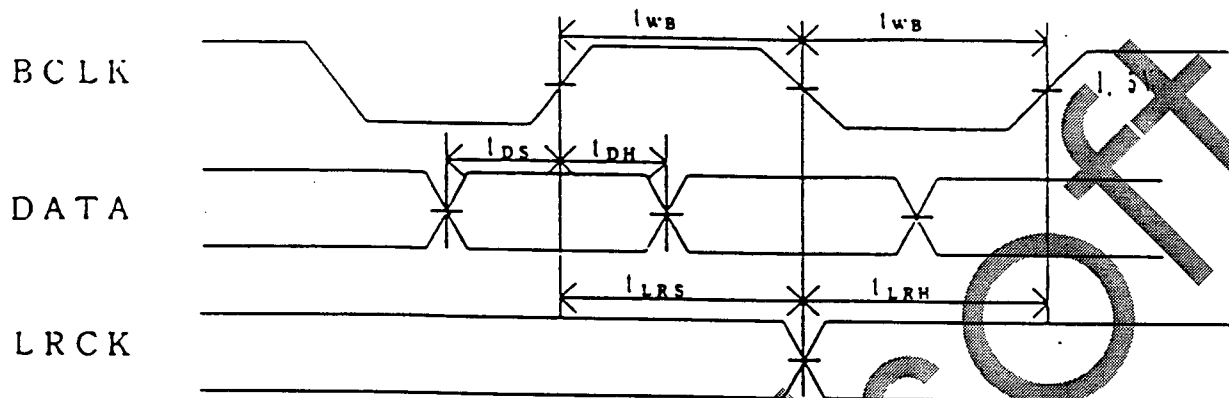
item	symbol	condition	MIN.	TYP.	MAX.	unit
D A C resolution	RES			16		bit
total harmonic distortion	THD1	1KHz, 0dB			0.08	%
cross talk	C·I	1KHz, 0dB		-85	-79	dB
signal/noise ratio	S/N	1KHz, 0dB	85	92		dB
power consumption	Pd	※1		250	300	mW
oscillating frequency	fx			16.9344	25	MHz
amplitude of clkout(pin23)	A _{CLK}	※2	1			V _{PP}
PULL DOWN resistance (PIN 17,18,19,20,21)	R _{DOWN}		10		80	KΩ
input BCLK frequency	f _{BCK}				3.1	MHz
input BCLK pulse width	t _{WB}		100			nS
input DATA setup time	t _{DS}		20			
input DATA hold time	t _{DH}		20			
input LRCK setup time	t _{LRs}		50			
input LRCK hold time	t _{LRH}		50			
program input basic time	t _{PR}	fx=	250			
latch input pulse width	t _{WLT}	16.9344MHz	50			
SHIFT.LATCH.rise time	t _r				200	
SHIFT.LATCH.fall time	t _f				200	
A T T setup time	t _{SET}		500			
A T T hold time	t _{HOLD}		500			
interval	t _{INT}		1000			

※1 X1N amp. 1.5~3.5V, $f_x = 16.9344\text{MHz}$

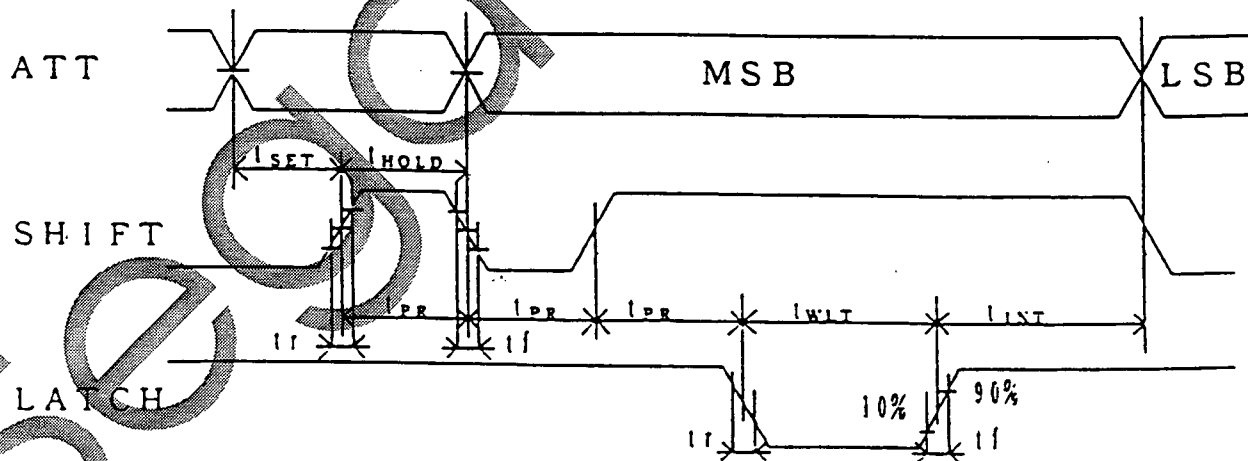
※2 $f_x = 16.9344\text{MHz}$ $C_L = 20\text{pF}$

Measuring circuits accord with application circuit examples.

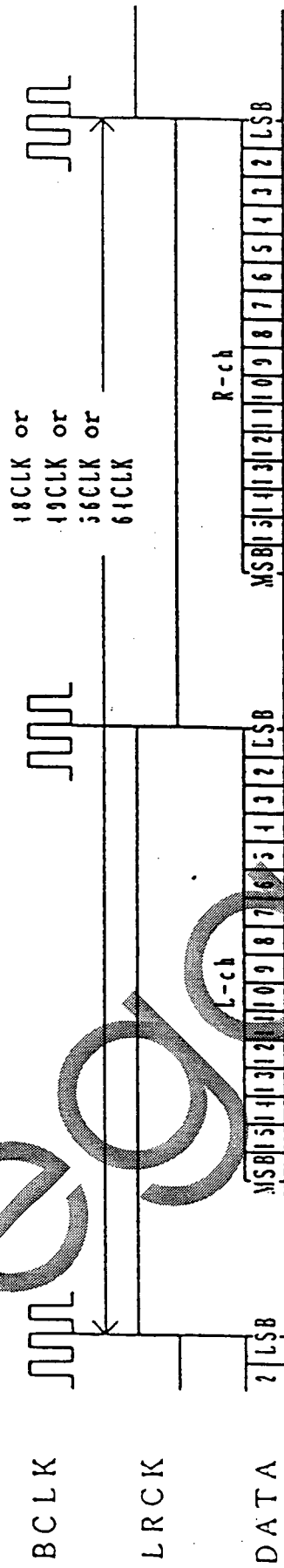
[Audio Input]



[Program Input]



9. Input Data Format



10. Filter Characteristics (Theoretical value)

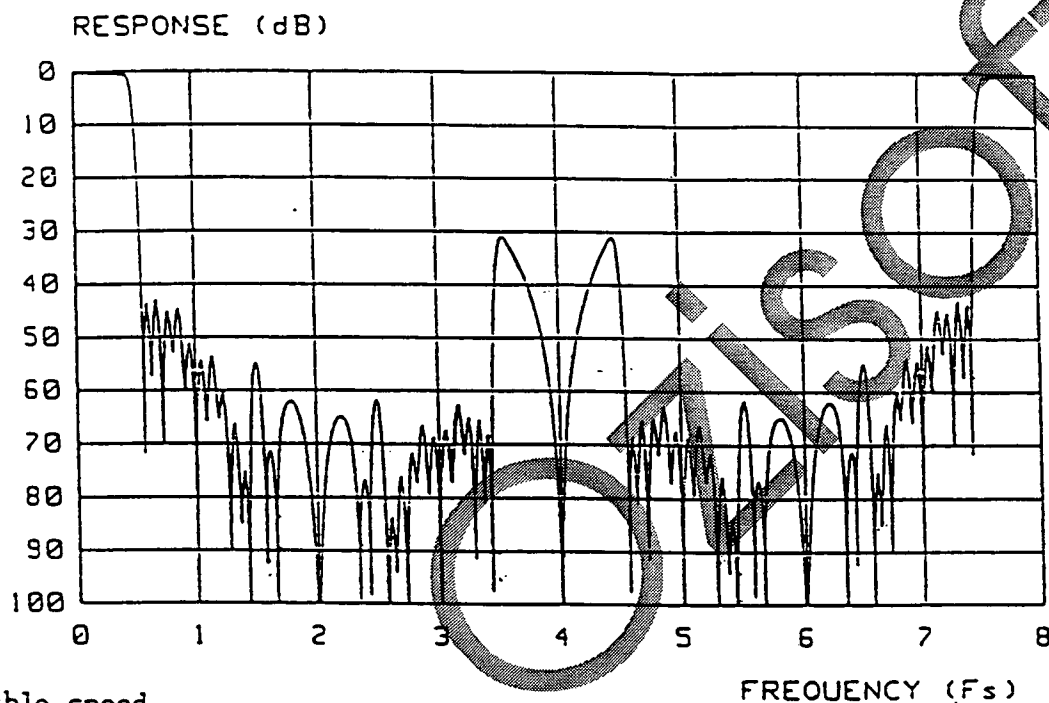
At normal speed: 8 times over sampling

At double speed: 4 times over sampling

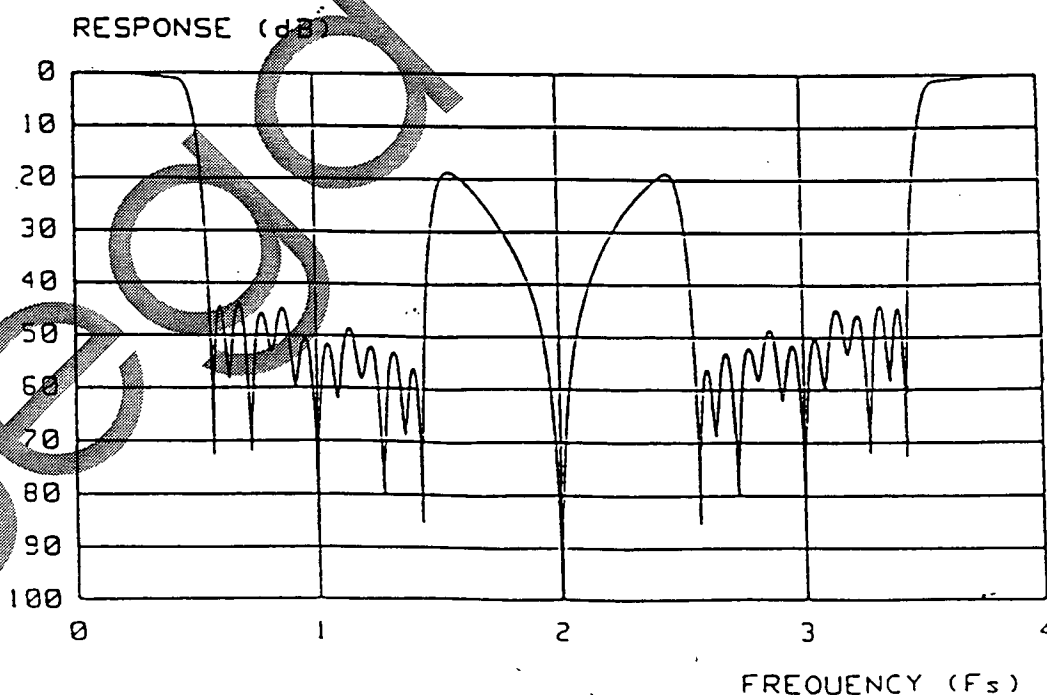
Ripple: within $\pm 0.05\text{dB}$

Stop-band attenuation: under -40dB

Normal speed



Double speed



11. Operation Description

LC7883M consists of 8-times over sampling digital filter and 16bit D/A converter.

·8-times over sampling digital filter

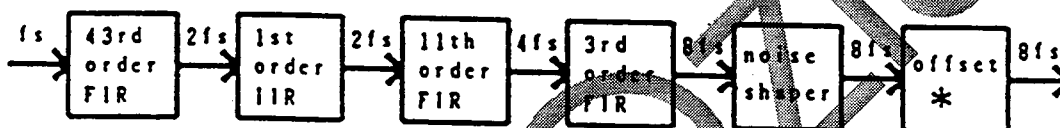
The digital filter process functions are shown in block diagram below. During the process, 18-bit data transfer are performed and 16-bit data are output to DAC after noise shaping of lower 6 bit of 22 bit data.

The digital filter has normal and double speed modes.

The normal speed mode does 2-times over sampling at each stage 43rd order FIR, 11th order FIR and 3rd order FIR, finally composes 8-times over sampling digital filter. 1st order IIR does de-emphasis.

The double speed mode is way to copy CD to cassette tape at double the speed. On this mode, BCLK, DATA and LRCK are input at double the speed, but XIN is input at the normal speed. This mode does 2-times over sampling at each stage 43rd order FIR and 3rd order FIR, finally composes 4-times over sampling digital filter.

·Normal speed



·Double speed



*offset : "02AAH"

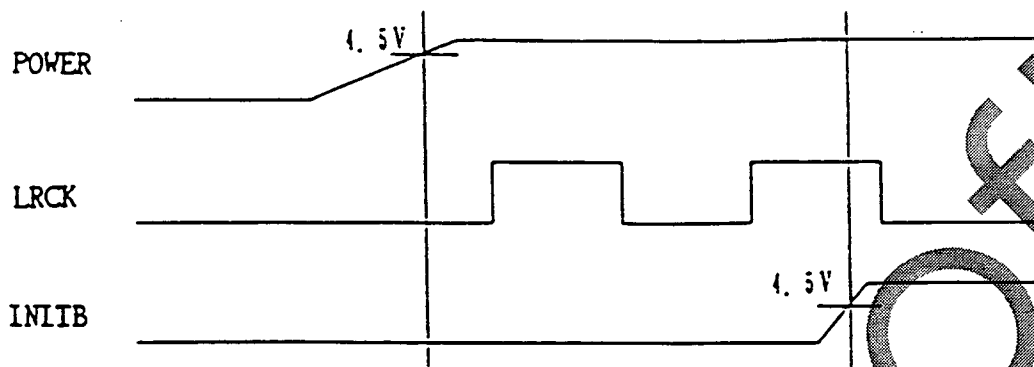
fs* : double speed input

·16bit D/A Converter

DAC is same as Sanyo LC7881 basically and has dynamic level shift conversion method using CH1, CH2, independent D/A converters. D/A conversion by resistance string (R-string DAC). D/A conversion by pulse width modulation (PWMDAC) and D/A conversion by level shift (Level Shift DAC).

12. Initiation

The IC needs to be initialized when power supply is on and when input source is changed. "L" level is longer than on period of LRCK shown below should be input to INITB when XIN, BCKL and LRCK are supplied and when power supply is stable for the initialization.



13. Input Source Setting

SOC1 and SOC2 pins are set according to frequency of oscillator as shown below.

frequency	SOC1	SOC2
384Fs	L	L
392Fs	L	H
448Fs	H	L
512Fs	H	H

14. Mode Setting

When MODE pin is high level, de-emphasis ON/OFF and normal/double speed are set by EMPH1, EMPH2 and D/N pins.

When MODE pin is low level, the mode is serial data transfer mode using ATT, SHIFT and LATCH pins.

At MODE pin "H" (PINs setting mode)

EMPH1	EMPH2	de-emphasis
L	L	OFF
L	H	Fs=32KHz
H	L	Fs=44.1KHz
H	H	Fs=48KHz

D/N pin "H" double speed mode.
"L" normal speed mode.

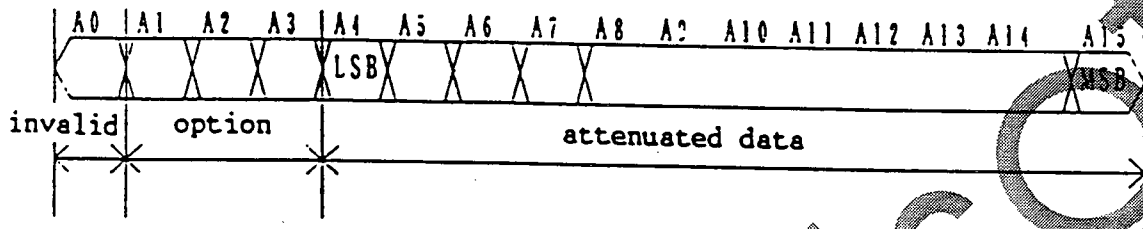
ATT, SHIFT, LATCH pins should be fixed to "H" or "L".

At MODE pin "L" (serial data transfer mode)

EMPH1, EMPH2 and D/N pins should be fixed to "H" or "L" for serial data transfer mode.

15. ATT Data Format In Use Of Serial Data Transfer Mode

Normal & double speed, de-emphasis and attenuation can be manipulated by input of the following data by timing described in electric characteristics section.



A 1 : speed flag. "L" normal speed, "H" double speed

A 2, A 3 : de-emphasis flag

A 2	A 3	de-emphasis
L	L	OFF
L	H	Fs=32KHz
H	L	Fs=44.1KHz
H	H	Fs=48KHz

ATT data should be set 4000H ("1" only for A14) when initializing.

ATTenuation

Since coefficient bit length of internal multiplier is 10 bit, normally upper 10 bit (A15-A6) of attenuated data are valid.

And the attenuation :
$$-20 \log \left(\frac{\text{upper 10bit}}{256} \right) \text{ dB}$$

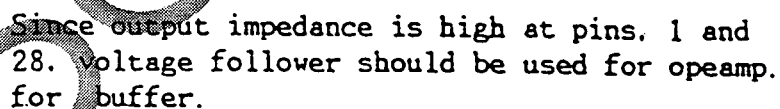
When upper 10bit of attenuated data become all "0", lower 2bit (A5 & A4) become valid and there will be attenuation by barrel sifter.

attenuation												attenuation level [dB]
MSB	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	LSB A5 A4	
0	1	0	0	0	0	0	0	0	0	0	0	0
0	0	1	1	1	1	1	1	1	1	1	1	-0.034
0	0	1	1	1	1	1	1	1	1	1	0	-0.034
0	0	1	1	1	1	1	1	1	1	0	1	-0.034
0	0	1	1	1	1	1	1	1	1	0	0	-0.034
0	0	1	1	1	1	1	1	1	1	0	1	-0.068
0	0	1	1	1	1	1	1	1	1	0	0	-0.068
.
.
.
0	0	0	0	0	0	0	0	0	0	1	0	-48.16
0	0	0	0	0	0	0	0	0	0	0	1	-50.66
0	0	0	0	0	0	0	0	0	0	0	1	-54.19
0	0	0	0	0	0	0	0	0	0	0	0	-60.21
0	0	0	0	0	0	0	0	0	0	0	0	-∞

Softmute after attenuation data change from 400H to 000H

Softmute time : $1/F_s \times 1.024$

Attenuation varying period is also on the linear of varying period of the softmute.



LPF: LOW PASS FILTER($F_c=20000\text{Hz}$)

DVDD = 5.0V

$$AVDD = 5.0V$$
$$V_{refH} = 5.0V$$
$$\text{AGND} = 0.0\text{V}$$
$$\text{Verfl} = 0.0V$$

PHYSICAL DIMENSIONS

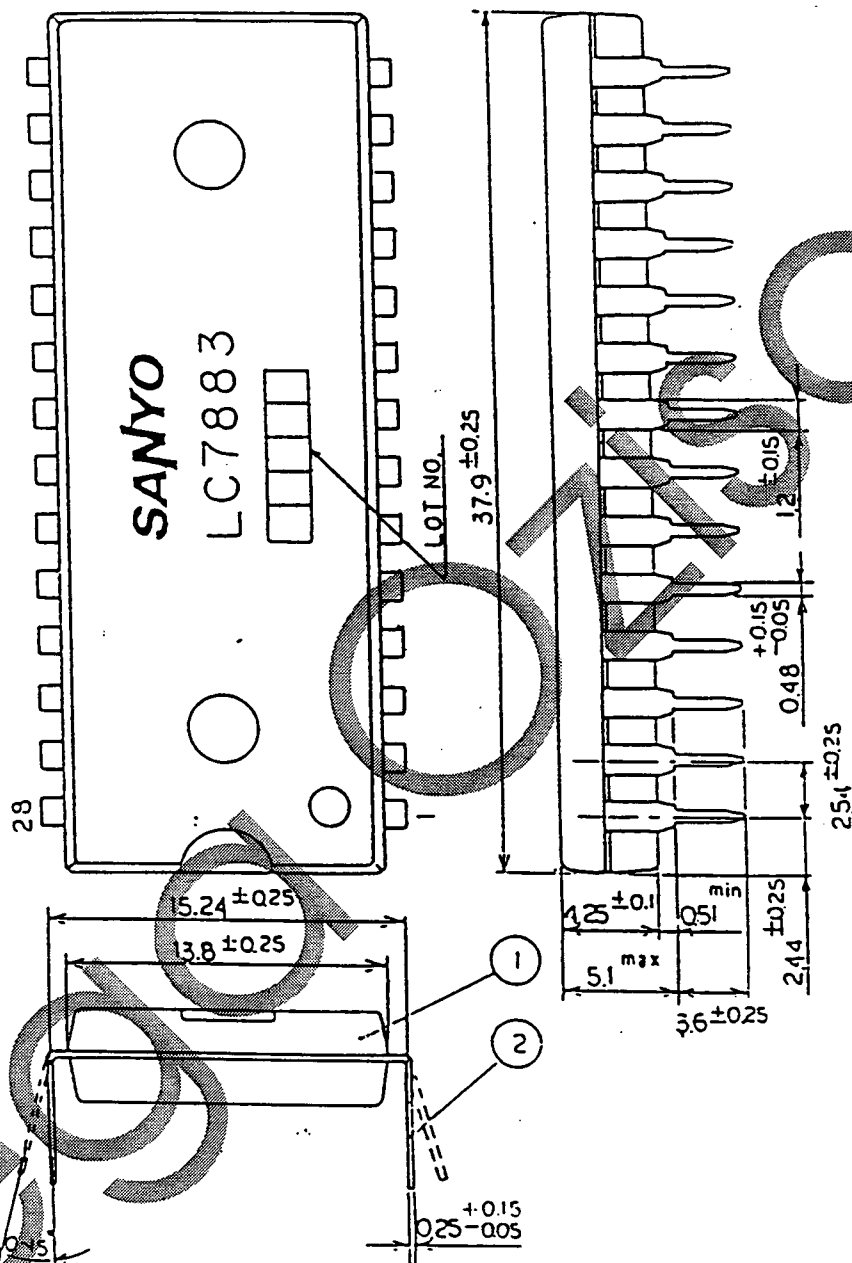
SCALE

3/1

DIMENSIONS

mm

MODEL LC7883



APPROVED BY

CHECKED BY

'90. 11. 13.

T. Akizawa

DRAWN BY

'90. 11. 9

	MATERIAL	FINISH
①	Epoxy Resins	—
②	42-ALLOY	Solder Plated