ICS25 FPGA

Version 1.9

7-1-2025

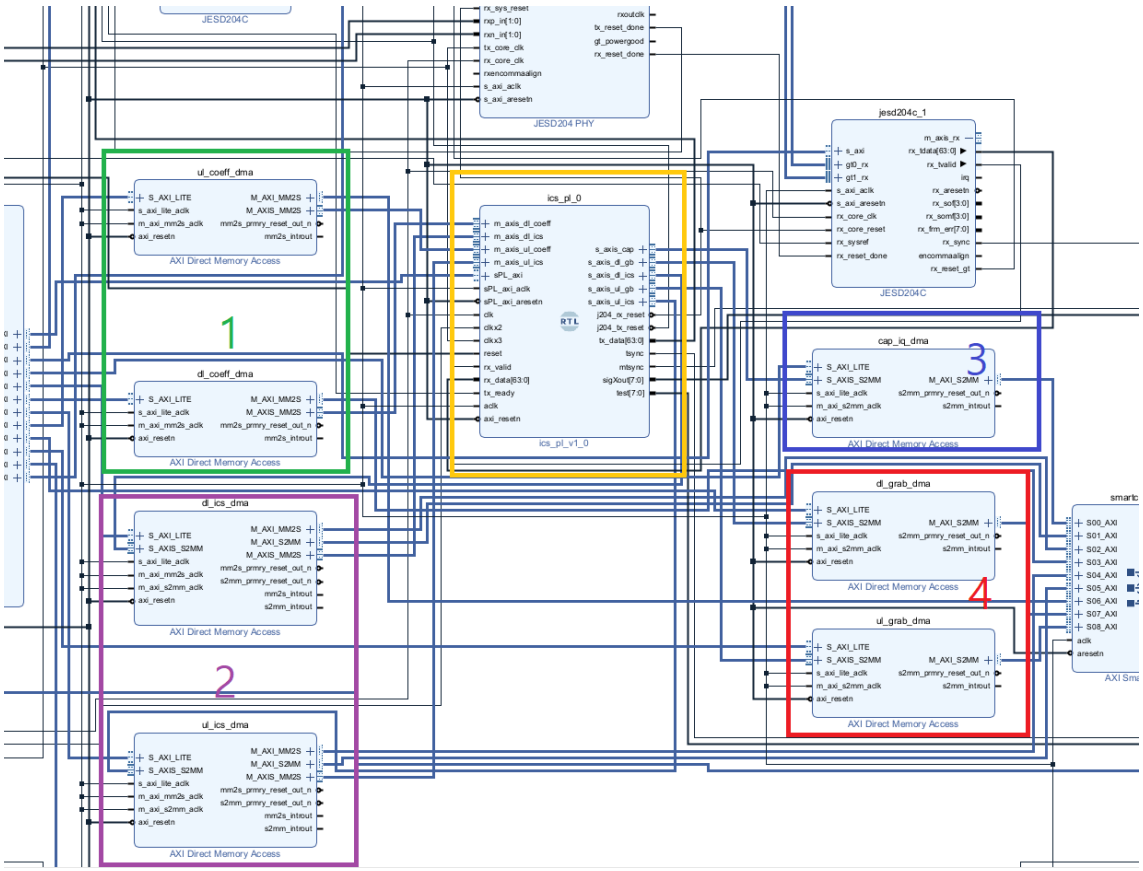
Contents

1 ICS_PL

다빈 시스템의 ICS 기능 블럭의 최상위 모듈은 'ICS_PL' 이다.

1.1 Connections in BD

아래 그림은 Xilinx Vivado project 의 block design 내에서 ICS_PL 부분을 발췌한 것이다.



1.2 ICS_PL 주요 Interface Signals 설명

Table 1: ICS_PL Interface Signals

Name	I/O	Description	Note
clk	I	122.88MHz clock	
clkx2	I	245.76MHz clock	unused now

<table>
<tr><td>clkx3</td><td>I</td><td>368.64MHz clock</td><td></td></tr>
<tr><td>reset</td><td>I</td><td>Active high reset input</td><td>aclk</td></tr>
<tr><td>rx_valid</td><td>I</td><td>A/D data valid, active high</td><td>synchronous to ‘clk’</td></tr>
<tr><td>rx_data[63:0]</td><td>I</td><td>A/D data input, 2’s complement signed integer
<table><tr><td>[63:48]</td><td>UL data path – Q</td></tr><tr><td>[47:32]</td><td>UL data path – I</td></tr><tr><td>[31:16]</td><td>DL data path – Q</td></tr><tr><td>[15:0]</td><td>DL data path – I</td></tr></table></td><td>synchronous to ‘clk’</td></tr>
<tr><td>aclk</td><td>I</td><td>PL clock, 125MHz</td><td></td></tr>
<tr><td>axi_resetn</td><td>I</td><td>Active low reset input</td><td>aclk</td></tr>
<tr><td>sPL_axi_aclk</td><td>I</td><td>PL registers control clock (= aclk)</td><td></td></tr>
<tr><td>sPL_axi_aresetn</td><td>I</td><td>Active low reset input (=axi_resetn)</td><td>aclk</td></tr>
<tr><td>sPL_axi</td><td>I/O</td><td>PL registers control bus</td><td>aclk</td></tr>
<tr><td>tx_ready[1]</td><td>I</td><td>JESD204C Tx ready input</td><td>Remove later</td></tr>
<tr><td>m_axis_dl(ul)_coeff</td><td>I/O</td><td>DMA I/F for DL(UL) channel filter coefficient download</td><td>GREEN(1)</td></tr>
<tr><td>m_axis_dl(ul)_ics</td><td>I/O</td><td>DMA I/F for DL(UL) ZCS data download</td><td>VIOLET(2)</td></tr>
<tr><td>s_axis_cap</td><td>I/O</td><td>DMA I/F for Timing module data capture</td><td>BLUE (3)</td></tr>
<tr><td>s_axis_dl(ul)_gb</td><td>I/O</td><td>DMA I/F for DL(UL) estimated data capture</td><td>RED(4)</td></tr>
<tr><td>s_axis_dl(ul)_ics</td><td>I/O</td><td>DMA I/F for Feedback data capture</td><td>VIOLET(2)</td></tr>
<tr><td>j204_tx(rx)_reset[1]</td><td>O</td><td>JESD204C block interface</td><td>Remove later</td></tr>
<tr><td>tx_data[63:0]</td><td>O</td><td>D/A data output, 2’s complement signed integer
<table><tr><td>[63:48]</td><td>UL data path – Q</td></tr><tr><td>[47:32]</td><td>UL data path – I</td></tr><tr><td>[31:16]</td><td>DL data path – Q</td></tr><tr><td>[15:0]</td><td>DL data path – I</td></tr></table></td><td>synchronous to ‘clkx3’</td></tr>
<tr><td>tsync</td><td>O</td><td>Timing information signal</td><td></td></tr>
</table>

mtsync	O	Timing information signal	
SigXout[7:0]	O	User defined timing information signals	
test[7:0]	O	Reserved for future test	

[1] Block design 에 JESD204C IP 를 포함하여 작성하는 과정에서 추가된 신호선이며, 향후 기산에서 Top level design 을 할 때는 필요 없음.