Specification For 4.2''EPD

Model NO.: E042A87

Product VER:A0

Customer Approval

Customer	
Approval By	
Date Of Approval	

It will be agreed by the receiver,if not sign back the Specification within 15days.

Prepared By	Checked By	Approval By
June		

Version	Content	Date	Producer
A0	New release	2020/11/26	June

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1.General Description

E042A87 is an Active Matrix Electrophoretic Display (AMEPD), with interface and a reference system design.The4.2 ” active area contains400×300 pixels, and has 1-bit B/W full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM and border are supplied with each panel.

2. Features

- 400×300 pixels display
- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable display
- Commercial temperature range
- Landscape, portrait modes
- Hard-coat antiglare display surface
- Ultra Low current deep sleep mode
- On chip display RAM
- Low voltage detect for supply voltage
- High voltage ready detect for driving voltage
- Internal temperature sensor
- 10-byte OTP space for module identification
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage
- I2C signal master interface to read external temperature sensor/ built-in temperature sensor

3. Application

Electronic Shelf Label System

4. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	4.2	Inch	
Display Resolution	400(H)×300(V)	Pixel	Dpi:119
Active Area	84.8(H)×63.6 (V)	mm	
Pixel Pitch	0.212×0.212	mm	
Pixel Configuration	Square		
Outline Dimension	91.00(H)× 77.00(V) × 1.15(D)	mm	Without masking film
Weight	15±0.5	g	

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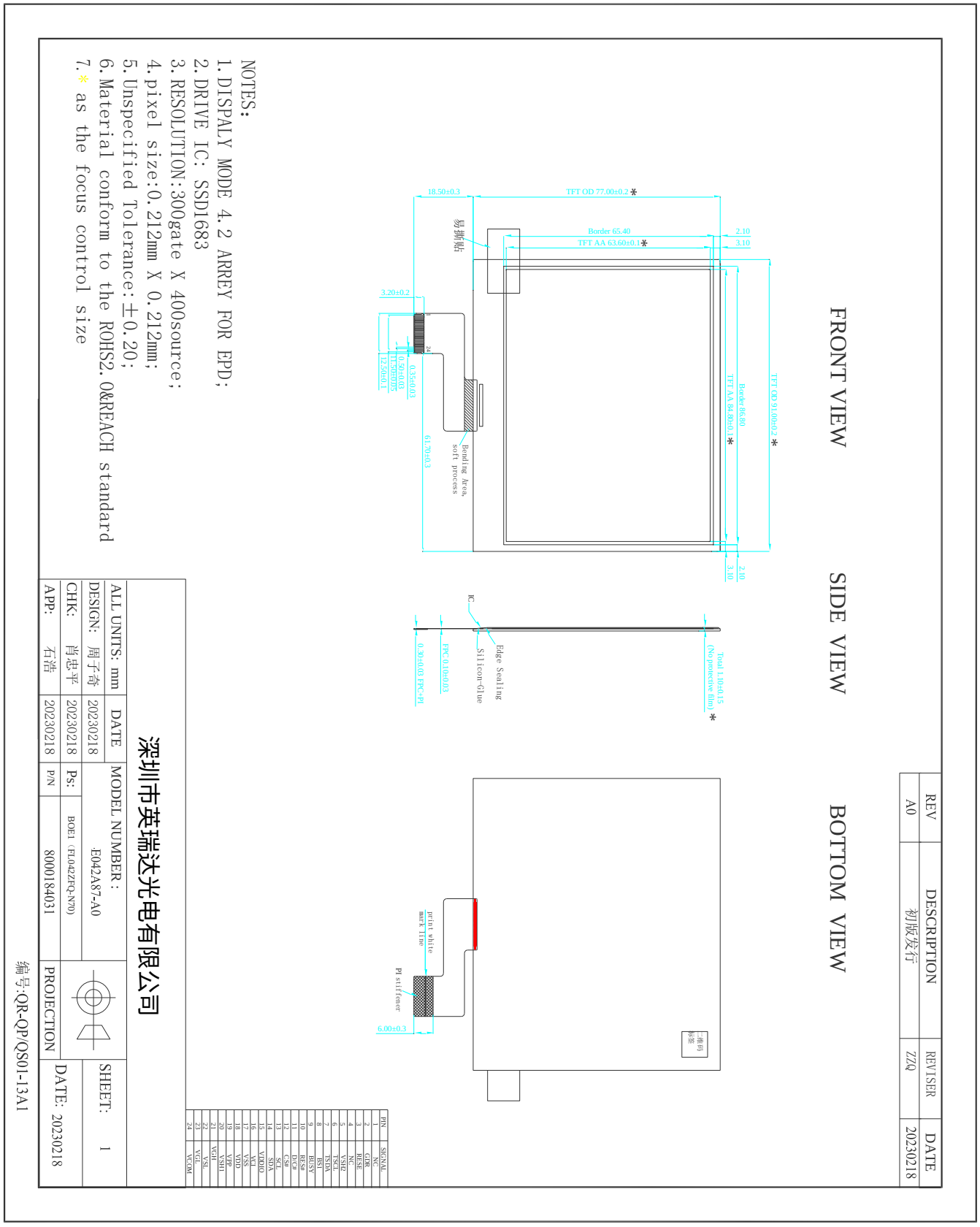
5. Mechanical Drawing of EPD module



6. Input/Output Terminals

Pin #	Single	Description	Remark
1	NC	No connection and do not connect with other NC pins NC	Keep Open
2	GDR	N-Channel MOSFET Gate Drive Control	
3	RESE	Current Sense Input for the Control Loop	
4	NC	No connection and do not connect with other NC pins	Keep Open
5	VSH2	Positive Source driving voltage	
6	TSCL	I2C Interface to digital temperature sensor Clock pin	
7	TSDA	I2C Interface to digital temperature sensor Date pin	
8	BS1	Bus selection pin	Note 6-5
9	BUSY	Busy state output pin	Note 6-4
10	RES #	Reset	Note 6-3
11	D/C #	Data /Command control pin	Note 6-2
12	CS #	Chip Select input pin	Note 6-1
13	SCL	serial clock pin (SPI)	
14	SDA	serial data pin (SPI)	
15	VDDIO	Power for interface logic pins	
16	VCI	Power Supply pin for the chip	
17	VSS	Ground	
18	VDD	Core logic power pin	
19	VPP	Power Supply for OTP Programming	
20	VSH1	Positive Source driving voltage	
21	VGH	Power Supply pin for Positive Gate driving voltage and VSH	
22	VSL	Negative Source driving voltage	
23	VGL	Power Supply pin for Negative Gate driving voltage, VCOM and VSL	
24	VCOM	VCOM driving voltage	

Note 6-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication: only when CS# is pulled LOW.
Note 6-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulle set is active low.
Note 6-4: This pin (BUSY) is Busy state output pin. When Busy is High the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin High when the driver IC is working such as:
- Outputting display waveform; or
- Communicating with digital temperature sensor

Note 6-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected.

7. MCU Interface

7.1 MCU Interface selection

The E042A87 can support 3-wire/4-wire serial peripheral. In the SSD1683, the MCU interface is pin selectable by BS1 shown in Table7-1.

Note

(1) L is connected to VSS

(2) H is connected to VDDIO

Table 7-1 : Interface pins assignment under different MCU interface

MCU Interface	Pin Name					
	BS1	RES#	CS#	D/C#	SCL	SDA
4-wire serial peripheral interface (SPI)	Connect to VSS	Required	Required	Required	SCL	SDA
3-wire serial peripheral interface (SPI) – 9 bits SPI	Connect to VDDIO	Required	Required	Connect to VSS	SCL	SDA

7.2 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA, D/C# and CS#. The control pins status in 4-wire SPI in writing command/data is shown in Table 7-2 and the write procedure 4-wire SPI is shown in Table 7-2

Table 7-2 : Control pins status of 4-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	L	L
Write data	↑	Data bit	H	L

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal

(3) SDA(Write Mode) is shifted into an 8-bit shift register on each rising edge of SCL in the order of D7, D6, ... D0. The level of D/C# should be kept over the whole byte. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/Data Byte register or command Byte register according to D/C# pin.

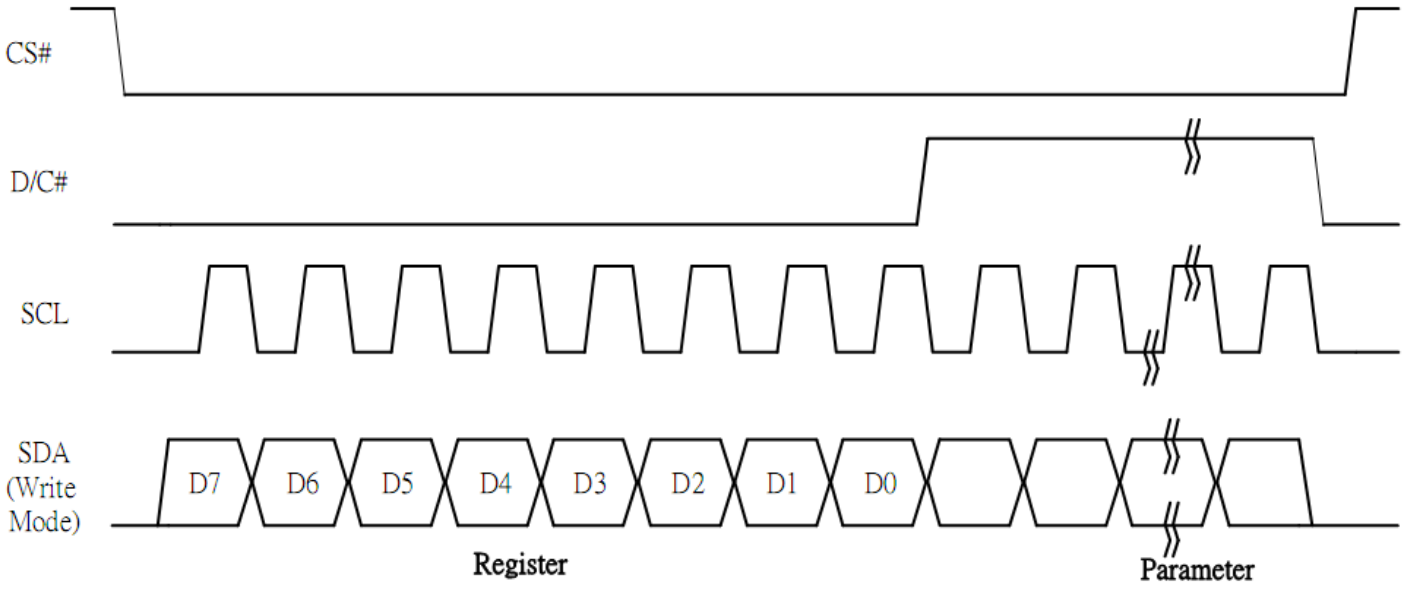


Figure 7-2 : Write procedure in 4-wire SPI mode

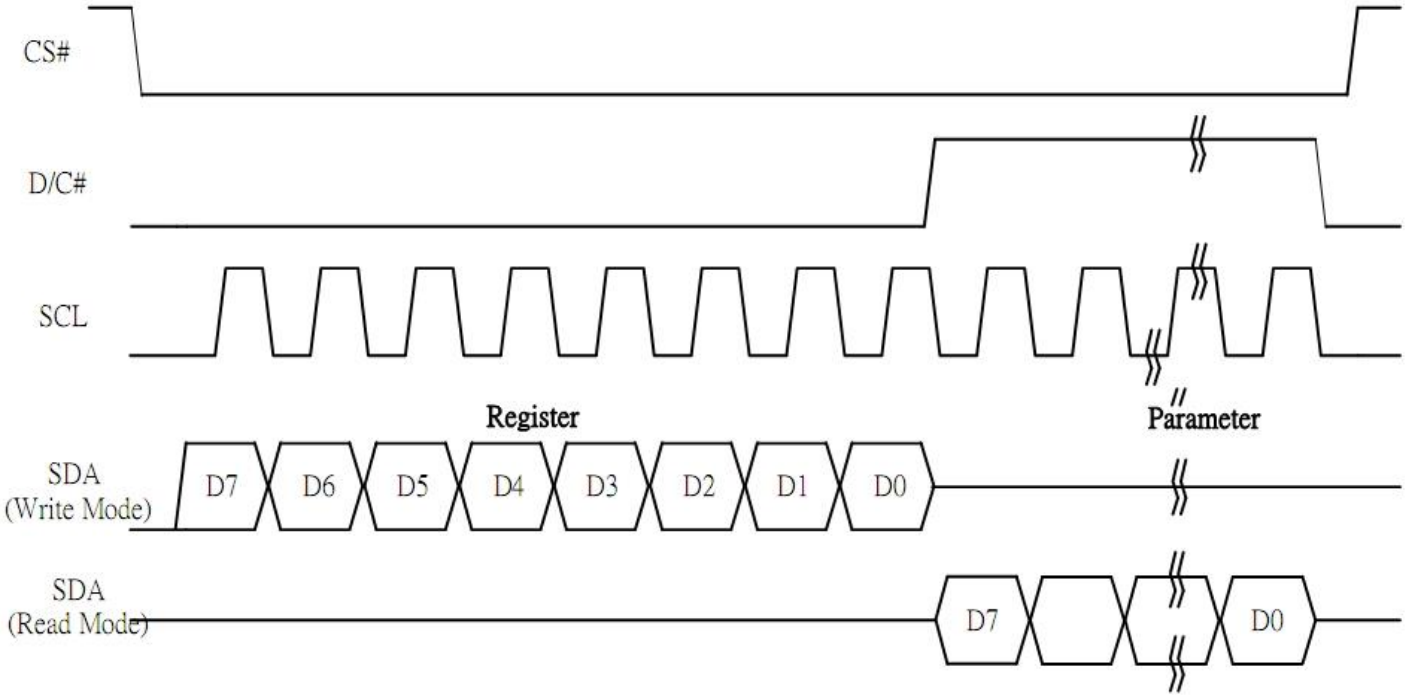


Figure 7-2 : Read procedure in 4-wire SPI mode

7.3 MCU Serial Peripheral Interface (3-wire SPI)

The 3-wire SPI consists of serial clock SCL, serial data SDA and CS#. The operation is similar to 4-wire SPI while D/C# pin is not used and it must be tied to LOW. The control pins status in 3-wire SPI is shown in Table7-3.

In the write operation, a 9-bit data will be shifted into the shift register on each clock rising edge. The bit shifting sequence is D/C# bit, D7 bit, D6 bit to D0 bit. The first bit is D/C# bit which determines the following byte is command or write data. When D/C# bit is 0, the following byte is command. When D/C# bit is 1, the following byte is data. Table 7-3 shows the write procedure in 3-wire SPI

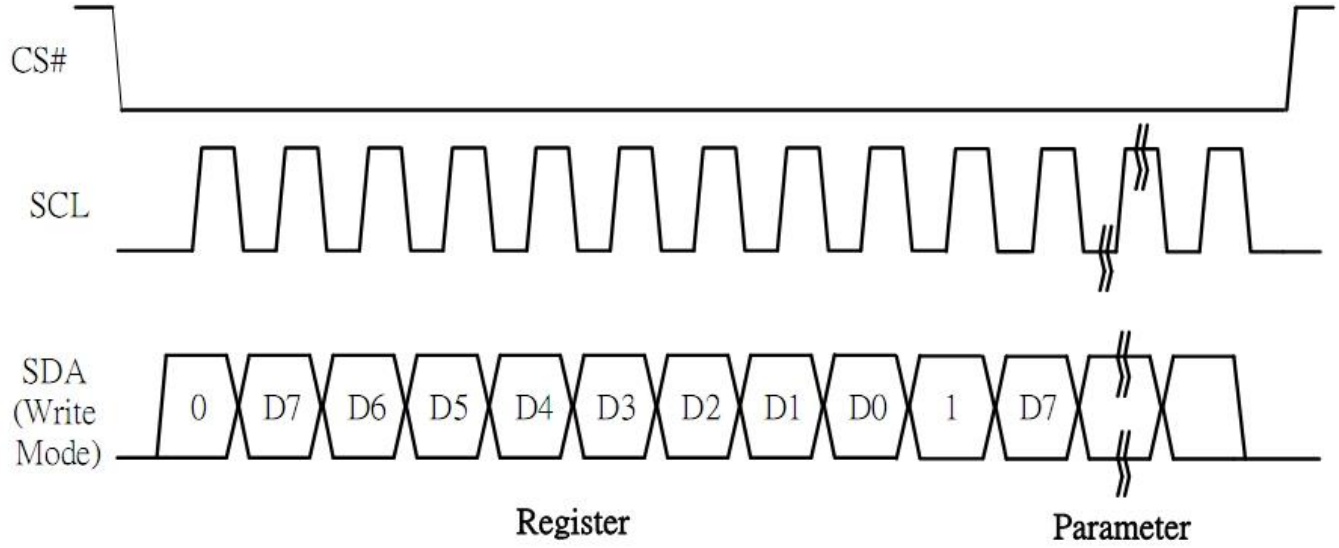
Table 7-3 : Control pins status of 3-wire SPI

Function	SCL pin	SDA pin	D/C# pin	CS# pin
Write command	↑	Command bit	Tie LOW	L
Write data	↑	Data bit	Tie LOW	L

Note:

(1) L is connected to VSS and H is connected to VDDIO

(2) ↑ stands for rising edge of signal



In the read operation (Register 0x1B, 0x27, 0x2D, 0x2E, 0x2F, 0x35), SDA data are transferred in the unit of 9 bits. After CS# pull low, the first byte is command byte, the D/C# bit is as 0 and following with the register byte. After command byte send, the following byte(s) are data byte(s), with D/C# bit is 1. After D/C# bit sending from MCU, an 8-bit data will be shifted out on each clock falling edge. The serial data SDA bit shifting sequence is D7, D6, to D0 bit. Figure 7-4 shows the read procedure in 3-wire SPI.

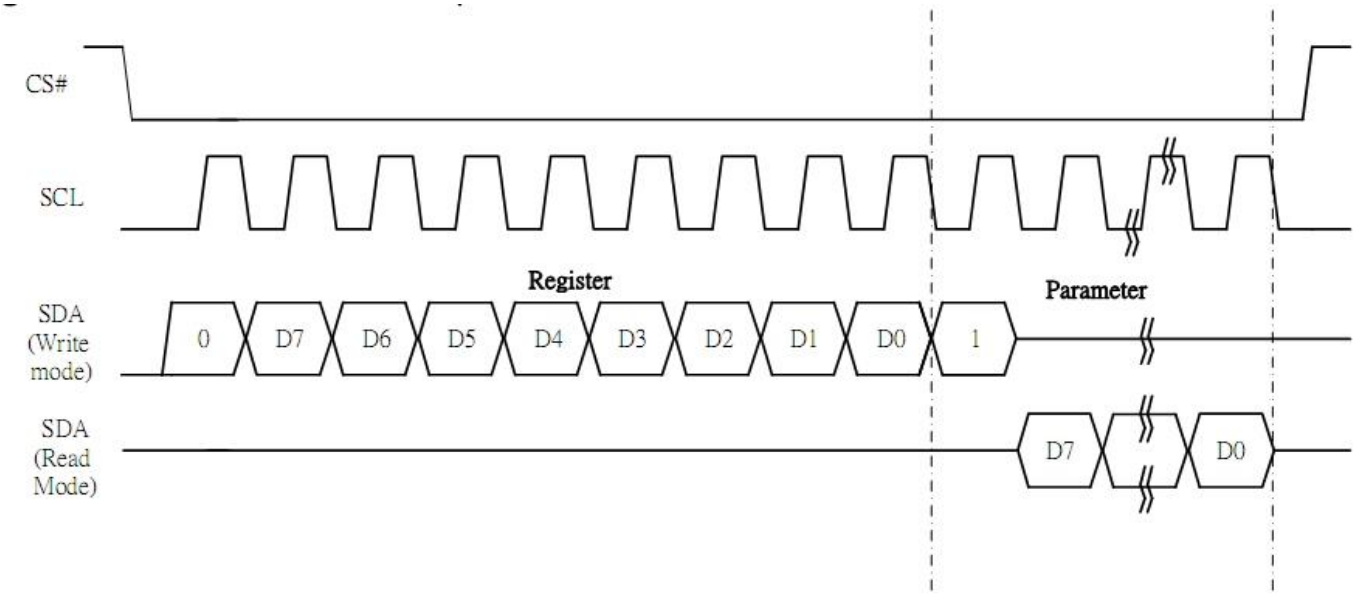


Figure 7-3 : Read procedure in 3-wire SPI mode

8. COMMAND TABLE

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	01	0	0	0	0	0	0	0	1	Driver Output Control	Set the number of gate. Setting for 300 gates is: Set A[8:0] = 12Bh Set B[7:0] = 00h
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	-	0	0	0	0	0	0	0	A_8		
0	1	-	0	0	0	0	0	B_2	B_1	B_0		
0	0	03	0	0	0	0	0	0	1	1	Gate Driving Voltage Control	Set Gate driving voltage. A[4:0] = 15h [POR], VGH at 19V
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	04	0	0	0	0	0	1	0	0	Source Driving voltage Control	Set Source output voltage. A[7:0] = 41h [POR], VSH1 at 15V B[7:0] = A8h [POR], VSH2 at 5V C[7:0] = 32h [POR], VSL at -15V
0	1	-	A7 B7 C7	A6 B6 C6	A5 B5 C5	A4 B4 C4	A3 B3 C3	A2 B2 C2	A1 B1 C1	A0 B0 C0		
0	0	0C	0	0	0	0	1	1	0	0	Soft start Control	Set Soft start setting A[7:0] = 8Eh B[7:0] = 8Ch C[7:0] = 85h D[7:0] = 3Fh
0	1	-	A7 B7 C7 D7	A6 B6 C6 D6	A5 B5 C5 D5	A4 B4 C4 D4	A3 B3 C3 D3	A2 B2 C2 D2	A1 B1 C1 D1	A0 B0 C0 D1		
0	0	10	0	0	0	1	0	0	0	0	Deep Sleep Mode	Deep Sleep mode Control
0	1	-	0	0	0	0	0	0	A1	A0		A[1:0] Description 00 Normal Mode [POR] 01 Enter Deep Sleep Mode1 11 Enter Deep Sleep Mode2
0	0	11	0	0	0	1	0	0	0	1	Data Entry mode setting	Define data entry sequence. A[2:0] = 3h [POR], A [1:0] = ID[1:0] Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 – Y decrement, X decrement, 01 – Y decrement, X increment, 10 – Y increment, X decrement, 11 – Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data is written to the RAM. When AM= 0, the address counter is updated in the X direction. [POR] When AM = 1, the address counter is updated in the Y direction.
0	1	-	0	0	0	0	0	A_2	A_1	A_0		
0	0	12	0	0	0	1	0	0	1	0	SW RESET	It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode During operation, BUSY pad will output high. Note: RAM are unaffected by this command.
0	0	14	0	0	0	1	0	1	0	0	HV Ready Detection	HV ready detection The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, HV Ready detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	15	0	0	0	1	0	1	0	1	VCI Detection	A[2:0] = 100 [POR] , Detect level at 2.3V A[2:0] : VCI level Detect A[2:0] VCI level 011 2.2V 100 2.3V 101 2.4V 110 2.5V 111 2.6V Other NA The command required CLKEN=1 and ANALOGEN=1 Refer to Register 0x22 for detail. After this command initiated, VCI detection starts. BUSY pad will output high during detection. The detection result can be read from the Status Bit Read (Command 0x2F).
0	1		0	0	0	0	0	A_2	A_1	A_0		
0	0	18	0	0	0	1	1	0	0	0	Temperature sensor control	Temperature Sensor Selection A[7:0] = 48h [POR], external temperature sensor A[7:0] = 80h Internal temperature sensor
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	1A	0	0	0	1	1	0	1	0	Temperature Sensor Control (Write to temperature register)	Write to temperature register. A[11:0] =7FFH[POR]
0	1	-	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
0	1	-	A_3	A_2	A_1	A_0	0	0	0	0		
0	0	1B	0	0	0	1	1	0	1	1	Temperature Sensor Control (Read from temperature register)	Read from temperature register.
1	1	-	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4		
1	1	-	A_3	A_2	A_1	A_0	0	0	0	0		
0	0	20	0	0	1	0	0	0	0	0	Master Activation	Activate Display Update Sequence. The Display Update Sequence Option is located at R22h BUSY pad will output high during operation. User should not interrupt this operation to avoid corruption of panel images.
0	0	21	0	0	1	0	0	0	0	1	Display Update Control 1	RAM content option for Display Update A[7:0] = 00h [POR] A[7:4] Red RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content A[3:0] BW RAM option 0000 Normal 0100 Bypass RAM content as 0 1000 Inverse RAM content
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
A[7:0]=FFh (POR)

<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then DISPLAY for display mode 1
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr><tr><td><u>Load LUT from OTP</u>
Enable Clock Signal,
Then Load LUT for display mode 1
Then Disable OSC</td><td>91</td></tr><tr><td><u>Load TS and then Load LUT from OTP</u>
Enable Clock Signal,
Then Load TS
Then Load LUT for display mode 1
Then Disable OSC</td><td>B1</td></tr></table>
<table><tr><th></th><th>Parameter (in Hex)</th></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then DISPLAY for display mode 2
Then Disable Analog
Then Disable OSC</td><td>CF</td></tr><tr><td><u>Load LUT from OTP</u>
Enable Clock Signal,
Then Load LUT for display mode 2
Then Disable OSC</td><td>99</td></tr><tr><td><u>Load TS and then Load LUT from OTP</u>
Enable Clock Signal,
Then Load TS
Then Load LUT for display mode 2
Then Disable OSC</td><td>B9</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>24</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write RAM(BW)</td><td>After this command, data entries will be written into the RAM until another command is written. Address pointers will advance accordingly.
For Write pixel:
Content of Write RAM(BW)=1
For Black pixel:
Content of Write RAM(BW)=0</td></tr>
<tr><td>0</td><td>0</td><td>26</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>Write RAM(RED)</td><td>After this command, data entries will be written into the RED RAM until another command is written. Address pointers will advance accordingly.
For Red pixel:
Content of Write RAM(RED)=1
For non-Red pixel[Black or White]:
Content of Write RAM(RED)=0</td></tr>
<tr><td>0</td><td>0</td><td>27</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>Read RAM</td><td>After this command, data read on the MCU bus will fetch data from RAM [According to parameter of Register 41h to select reading RAM(BW) / RAM(RED)], until another command is written. Address pointers will advance accordingly.
The 1st byte of data read is dummy data.</td></tr>
</table>

<table>
<tr><th>R/W#</th><th>D/C#</th><th>Hex</th><th>D7</th><th>D6</th><th>D5</th><th>D4</th><th>D3</th><th>D2</th><th>D1</th><th>D0</th><th>Command</th><th>Description</th></tr>
<tr><td>0</td><td>0</td><td>2B</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>ACVCOM setting</td><td>Set following values when ACVCOM is used, it will not affect DCVCOM
A[7:0] = 04h
B[7:0] = 63h</td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>2C</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Write VCOM register</td><td>Write VCOM register from MCU interface
A[7:0]=00h[POR]
<table><tr><th>A[7:0]</th><th>VCOM (V)</th><th>A[7:0]</th><th>VCOM (V)</th></tr><tr><td>08h</td><td>-0.2</td><td>44h</td><td>-1.7</td></tr><tr><td>0Bh</td><td>-0.3</td><td>48h</td><td>-1.8</td></tr><tr><td>10h</td><td>-0.4</td><td>4Bh</td><td>-1.9</td></tr><tr><td>14h</td><td>-0.5</td><td>50h</td><td>-2</td></tr><tr><td>17h</td><td>-0.6</td><td>54h</td><td>-2.1</td></tr><tr><td>1Bh</td><td>-0.7</td><td>58h</td><td>-2.2</td></tr><tr><td>20h</td><td>-0.8</td><td>5Bh</td><td>-2.3</td></tr><tr><td>24h</td><td>-0.9</td><td>5Fh</td><td>-2.4</td></tr><tr><td>28h</td><td>-1</td><td>64h</td><td>-2.5</td></tr><tr><td>2Ch</td><td>-1.1</td><td>68h</td><td>-2.6</td></tr><tr><td>2Fh</td><td>-1.2</td><td>6Ch</td><td>-2.7</td></tr><tr><td>34h</td><td>-1.3</td><td>6Fh</td><td>-2.8</td></tr><tr><td>37h</td><td>-1.4</td><td>73h</td><td>-2.9</td></tr><tr><td>3Ch</td><td>-1.5</td><td>78h</td><td>-3</td></tr><tr><td>40h</td><td>-1.6</td><td>Other</td><td>NA</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>2D</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>OTP Register Read</td><td>Read Register stored in OTP:
1. A[7:0]~ B[7:0]: VCOM Information
2. C[7:0]~F[7:0]: Display Mode
3. G[7:0]~H[7:0]: Module ID/ Waveform Version [2bytes]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td colspan="11">…</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>H7</td><td>H6</td><td>H5</td><td>H4</td><td>H3</td><td>H2</td><td>H1</td><td>H0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>2E</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>User ID read</td><td>Read 10 Byte User ID stored in OTP:
A[7:0]]~J[7:0]: UserID (R38, Byte A and Byte J) [10 bytes]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td>A5</td><td>A4</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td colspan="11">…</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td></td><td>J7</td><td>J6</td><td>J5</td><td>J4</td><td>J3</td><td>J2</td><td>J1</td><td>J0</td><td></td><td></td></tr>
<tr><td>0</td><td>0</td><td>2F</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>Status Bit Read</td><td>Read IC status Bit [POR 0x21]
A[5]: HV Ready Detection flag [POR=1]
0: Ready
1: Not Ready
A[4]: VCI Detection flag [POR=0]
0: Normal
1: VCI lower than the Detect level
A[3]: [POR=0]
A[2]: Busy flag [POR=0]
0: Normal
1: BUSY
A[1:0]: Chip ID [POR=01]
Remark:
A[5] and A[4] status are not valid after RESET, they need to be initiated by command 0x14 and command 0x15 respectively.</td></tr>
<tr><td>1</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>A4</td><td>0</td><td>0</td><td>A1</td><td>A0</td><td></td><td></td></tr>
<tr><td>0</td><td>1</td><td>-</td><td>0</td><td>0</td><td>0</td><td>0</td><td>A3</td><td>A2</td><td>A1</td><td>A0</td><td></td><td></td></tr>
</table>

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	32	0	0	1	1	0	0	1	0	Write LUT register	Write LUT register from MCU interface [70 bytes] (excluding the analog setting and frame setting)
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1	-	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1	-	:	:	:	:	:	:	:	:		
0	1	-	.	.	.	.	.	.	.	.		
0	0	36	0	0	1	1	0	1	1	0	Program OTP	Program OTP for User ID [R38h] The command required CLKEN=1. Refer to Register 0x22 for detail. BUSY pad will output high during operation
0	0	38	0	0	1	1	1	0	0	0	Write Register for User ID	Write Register for User ID A[7:0]]~J[7:0]: UserID [10 bytes]
0	1	-	A7	A6	A5	A4	A3	A2	A1	A0		
…												
1	1		J7	J6	J5	J4	J3	J2	J1	J0		
0	0	39	0	0	1	1	1	0	0	1	OTP program mode	OTP program mode A[1:0] = 11: for OTP programming Remark: User is required to EXACTLY follow the reference code sequences
0	1	-	0	0	0	0	0	0	A1	A0		
0	0	3A	0	0	1	1	1	0	1	0	Set dummy line period	Set A[7:0] = 2Ch
0	1	-	0	A6	A5	A4	A3	A2	A1	A0		
0	0	3B	0	0	1	1	1	0	1	1	Set Gate line width	Set A[3:0] = 0Ah
0	1	-	0	0	0	0	A3	A2	A1	A0		
0	0	3C	0	0	1	1	1	1	0	0	Border Waveform Control	Select border waveform for VBD A [7:6] Select VBD
0	1	-	A_7	A_6	A_5	A_4	0	0	A_1	A_0		

A[7:6]	Select VBD as
00[POR]	GS Transition Define A[1:0]
01	Fix Level Define A [5:4]
10	VCOM
11	HIZ

A [5:4] Fix Level Setting for VBD

A[5:4]	VBD level
00[POR]	VSS
01	VSH1
10	VSL
11	VSH2

A[1:0]) GS Transition setting for VBD

A[1:0]	VBD Transition
00 [POR]	LUT0
01	LUT1
10	LUT2
11	LUT3

R/W#	D/C#	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	0	41	0	1	0	0	0	0	1	0	Read RAM Option	Read RAM Option A[0]= 0 [POR] 0 : Read RAM corresponding to 24h 1 : Read RAM corresponding to 26h
0	1	-	0	0	0	0	0	0	0	A_0		
0	0	44	0	1	0	0	0	1	0	0	Set RAM X - address Start / End position	Specify the start/end positions of the window address in the X direction by an address unit A[4:0] = 00h B[4:0] = 31h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	1	-	0	0	0	B_4	B_3	B_2	B_1	B_0		
0	0	45	0	1	0	0	0	1	0	1	Set Ram Y- address Start / End position	Specify the start/end positions of the window address in the Y direction by an address unit A[7:0] = 12Bh B[7:0] = 0000h
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	1		0	0	0	0	0	0	0	A_8		
0	1	-	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		
0	1		0	0	0	0	0	0	0	B_8		
0	0	4E	0	1	0	0	1	1	1	0	Set RAM X - address counter	Make initial settings for the RAM X address in the address counter (AC) A[4:0] = 00h
0	1	-	0	0	0	A_4	A_3	A_2	A_1	A_0		
0	0	4F	0	1	0	0	1	1	1	1	Set RAM Y - address counter	Make initial settings for the RAM Y address in the address counter (AC) A[8:0] = 12Bh
0	1	-	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
			0	0	0	0	0	0	0	A_8		
0	0	74	0	1	1	1	0	1	0	0	Set Analog Block control	A[7:0] = 54h
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	7E	0	1	1	1	1	1	1	0	Set Digital Block control	A[7:0] = 3Bh
0	1		A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		

9.Reference Circuit

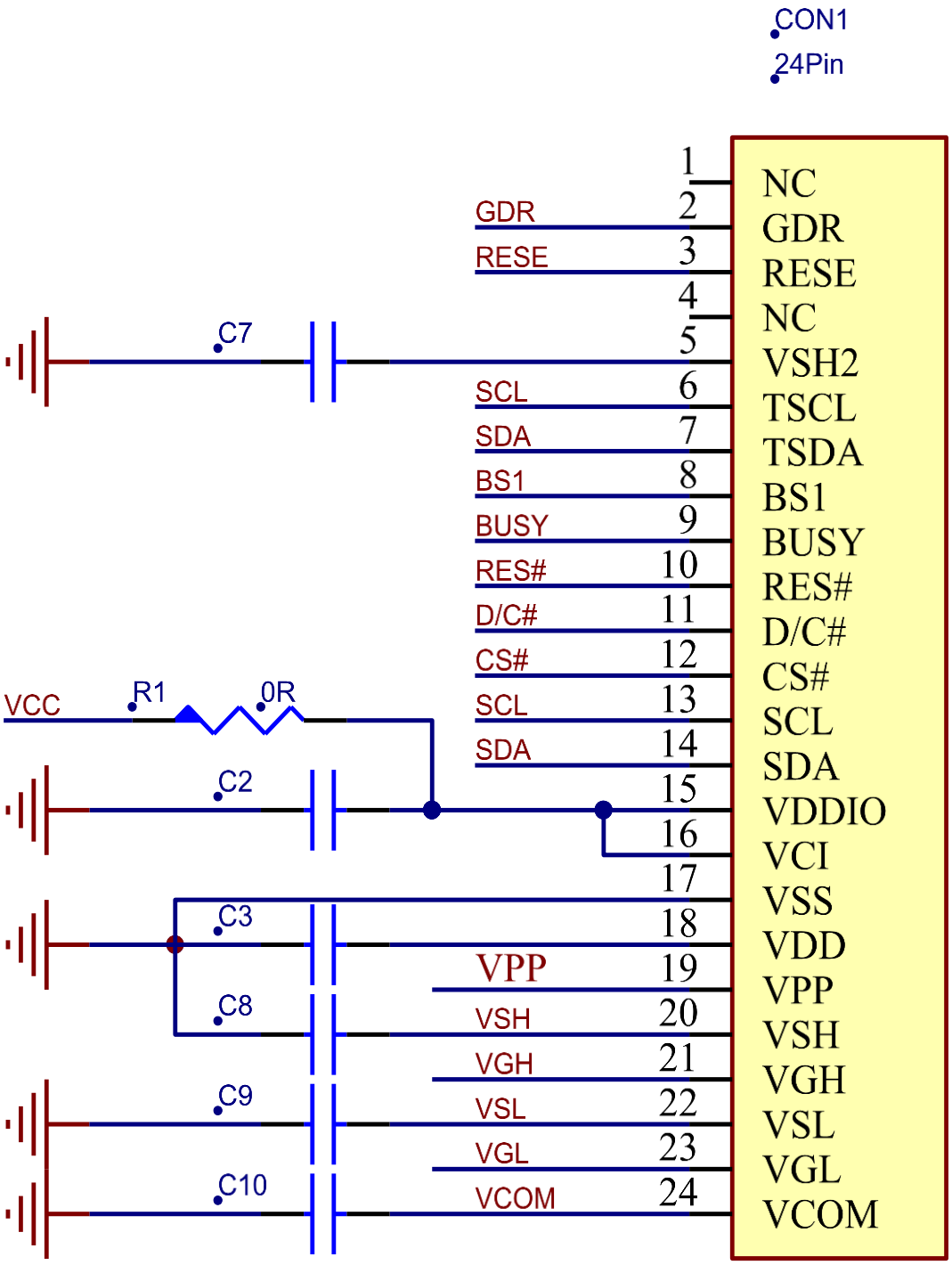


Figure. 9-1

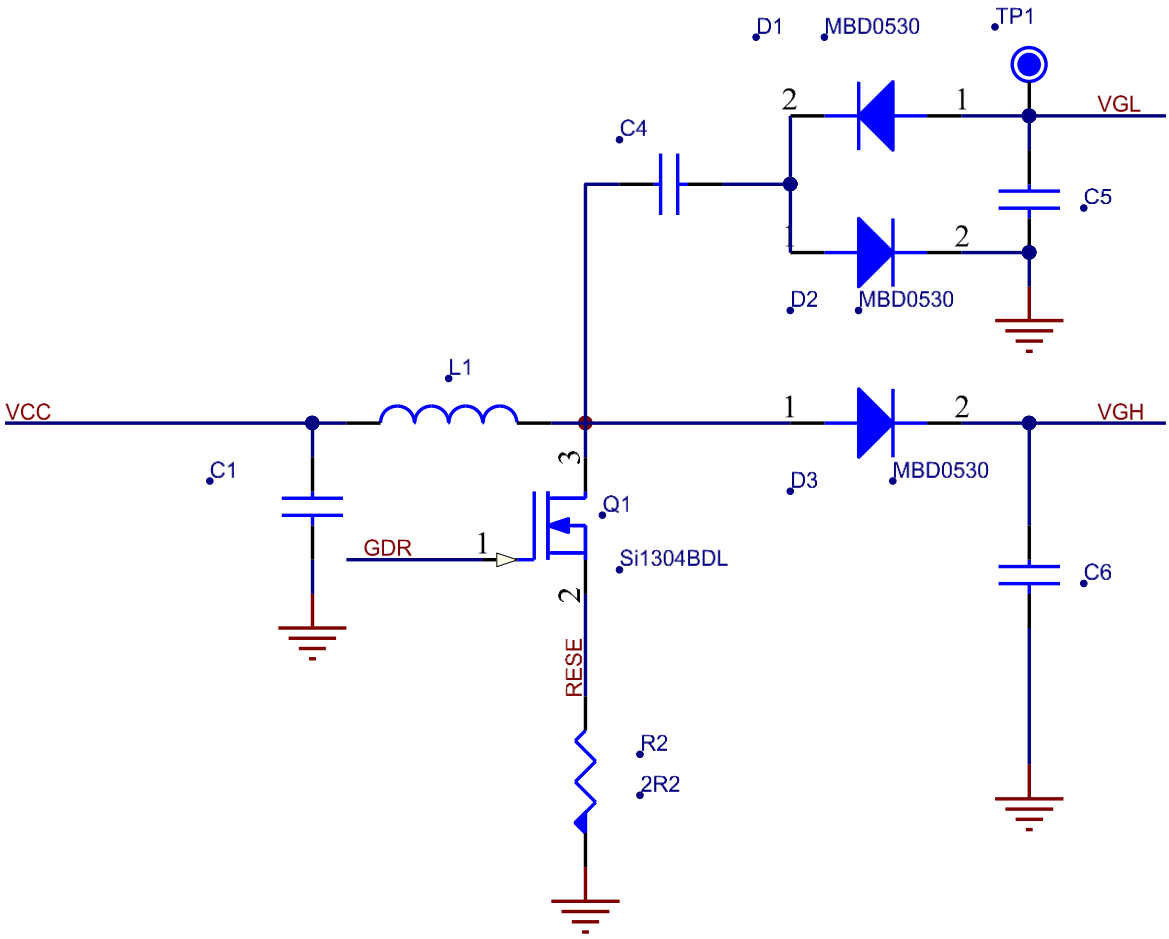


Figure. 9-2

Part Name	SSD1683Value /quirement/Reference Part
C1—C10	1uF/0603;X5R/X7R;Voltage Rating: 25V
C10	1uF/0603;X7R;Voltage Rating: 25V
D1—D3	MBR0530 1) Reverse DC voltage≥30V 2) Forward current≥500mA 3)Forward voltage≤430mV
R2	2.2 Ω/0603：1% variation
Q1	NMOS:Si1304BDL/NX3008NBK 1） Drain-Source breakdown voltage ≥30V 2） Vgs（th）=0.9（Typ），1.3V（Max） 3） Rds on≤ 2.1Ω @ Vgs=2.5V
L1	47uH/CDRH2D18、LDNP-470NC Maximum DC current~420mA Maximum DC resistance~650mΩ

10. Absolute Maximum Rating

Table 10-1 : Maximum Ratings

Symbol	Parameter	Rating	Unit	Humidity	Unit	Note
V_{CI}	Logic supply voltage	-0.5 to +6.0	V	-	-	
T_{OPR}	Operation temperature range	0 to 50	℃	35 to70	%	
Tttg	Transportation temperature range	-25 to 60	℃	-	-	Note11-2
Tstg	Storage condition	0 to 40	℃	35 to70	%	Maximum storage time: 5 years
-	After opening the package	0 to 40	℃	35 to70	%	

Note 10-1:Maximum ratings are those values beyond which damages to the device may occur.
Functional operation should be restricted to the limits in the Electrical Characteristics chapter.

Note10-2: Tttg is the transportation condition，the transport time is within 10 days for -25℃~0℃ or 50℃~60℃.

11. DC CHARACTERISTICS

The following specifications apply for: VSS=0V, VCI=3.3V, T_{OPR}=25℃.

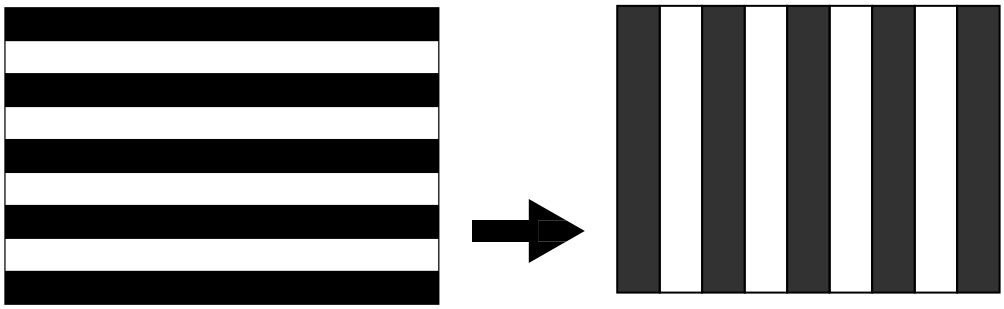
Table 11-1: DC Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
VCI	VCI operation voltage	-	2.5	3	3.7	V
VIH	High level input voltage	–	0.8VDDIO	-	-	V
VIL	Low level input voltage	–	-		0.2VDDIO	V
VOH	High level output voltage	IOH = -100uA	0.9VDDIO	-	-	V
VOL	Low level output voltage	IOL = 100uA	-		0.1VDDIO	V
Iupdate	Module operating current	-	-	6	-	mA
Isleep	Deep sleep mode	VCI=3.3V	-	-	3	uA

- The Typical power consumption is measured using associated 25℃ waveform with following pattern transition: from horizontal scan pattern to vertical scan pattern. (Note 11-1)
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by XingTai.
- Vcom value will be OTP before in factory or present on the label sticker.

Note 11-1

The Typical power consumption



12. AC Characteristics

The following specifications apply for: VDDIO - VSS = 2.5V to 3.7V, TOPR = 25℃

Write mode

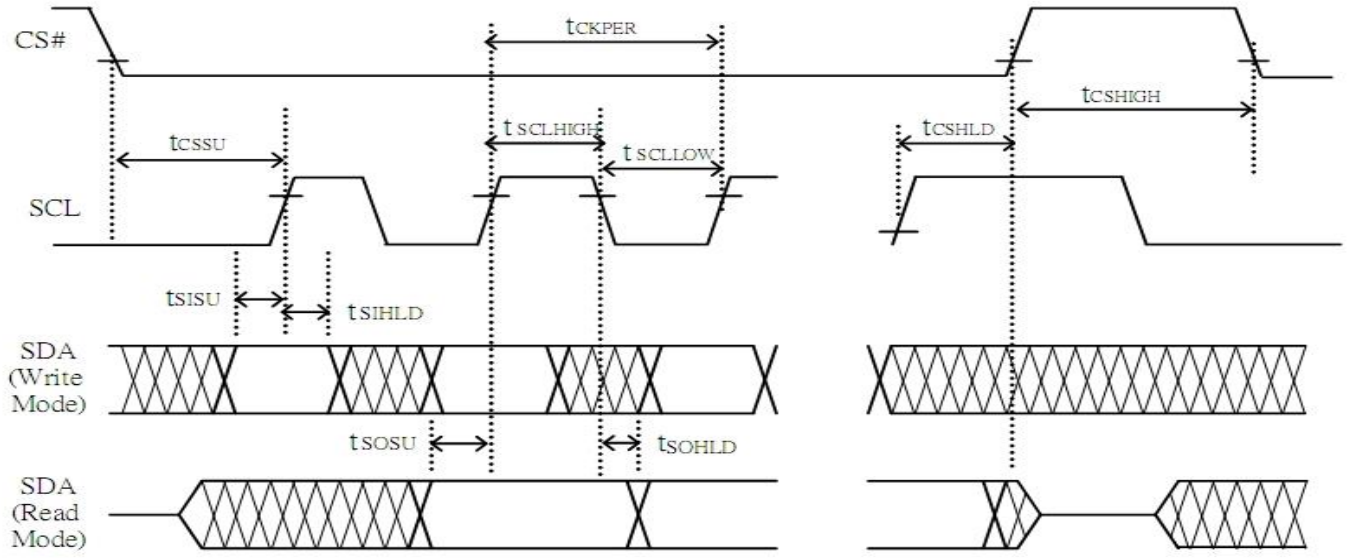
Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Write Mode)			20	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	20			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	20			ns
tCSHIGH	Time CS# has to remain high between two transfers	100			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	25			ns
tSCLLOW	Part of the clock period where SCL has to remain low	25			ns
tSISU	Time SI (SDA Write Mode) has to be stable before the next rising edge of SCL	10			ns
tSIHLD	Time SI (SDA Write Mode) has to remain stable after the rising edge of SCL	40			ns

Read mode

Symbol	Parameter	Min	Typ	Max	Unit
fSCL	SCL frequency (Read Mode)			2.5	MHz
tCSSU	Time CS# has to be low before the first rising edge of SCLK	100			ns
tCSHLD	Time CS# has to remain low after the last falling edge of SCLK	50			ns
tCSHIGH	Time CS# has to remain high between two transfers	250			ns
tSCLHIGH	Part of the clock period where SCL has to remain high	180			ns
tSCLLOW	Part of the clock period where SCL has to remain low	180			ns
tSOSU	Time SO(SDA Read Mode) will be stable before the next rising edge of SCL		50		ns
tSOHLD	Time SO (SDA Read Mode) will remain stable after the falling edge of SCL		0		ns

Note: All timings are based on 20% to 80% of VDDIO-VSS

Figure 12-2: SPI timing diagram



13. Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	-	30	mAs	-
Deep sleep mode	-	25℃	-	3	uA	-

MAs=update average current ×update time

14. Typical Operating Sequence

14.1 Normal Operation Flow

Sequence	Action by	Command	Action Description	Remark
1	User	-	Power on (VCI supply);	-
2	User	-	HW Reset	-
	IC	-	After HW reset, the IC will be ready for command input	-
	User	C 12	Command: SW Reset	--
	IC	-	After SW reset, the IC will have Registers load with POR value VCOM register loaded with OTP value IC enter idle mode	BUSY = H
	User	-	Wait until BUSY = L	-
3	-	-	Send initial code to driver including setting of	-
	User	C 74 D 54	Command: Set Analog Block Control	-
	User	C 7E D 3B	Command: Set Digital Block Control	-
	User	C 0C	Command: Set Softstart setting	-
	User	C 2B	Command: ACVCOM setting	
	User	C 01	Command: Driver Output Control (MUX, Source gate scanning direction)	-
	User	C 3A	Command: Set dummy line period	-
	User	C 3B	Command: Set Gate line width	-
	User	C 3C	Command: Border waveform control	-
4	-	-	Data operations for Black White	-
	User	C 11	Command: Data Entry mode setting	-
	User	C 44	Command: RAM X address start /end position	-
	User	C 45	Command: RAM Y address start /end position	-
	User	C 4E	Command: RAM X address counter	-
	User	C 4F	Command: RAM Y address counter	-
	User	C 24	Command: write BW RAM	-
	-	-	Ram Content for Display	-
5	-	-	Data operations for RED	-
	User	C 11	Command: Data Entry mode setting	-
	User	C 44	Command: RAM X address start /end position	-
	User	C 45	Command: RAM Y address start /end position	-
	User	C 4E	Command: RAM X address counter	-
	User	C 4F	Command: RAM Y address counter	-
	User	C 26	Command: write RED RAM	-
			Ram Content for Display	-
6	User	C 22	Command: Display Update Control 2	BUSY=H
	User	C 20	Command: Master Activation	
	IC	-	Booster and regulators turn on	
	IC	-	Load LUT register with corresponding waveform setting stored in OTP)	
	IC	-	Send output waveform according RAM content and LUT.	

	IC	-	Booster and Regulators turn off	
	IC	-	Back to idle mode	
	User	-	Wait until BUSY = L	-
7	User	-	IC power off;	-

15. Optical characteristics

15.1 Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detection is perpendicular unless otherwise specified.

T=25℃

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT	Note
R	Reflectance	White	30	35	-	%	Note 16-1
Gn	2Grey Level	-	-	DS+(WS-DS)×n(m-1)	-	L*	-
CR	Contrast Ratio	-	-	10	-	-	-
KS	Black State L* value	-	-	18	-	-	Note 16-1
	Black State a* value	-	-	0.2	-	-	Note 16-1
WS	White State L* value	-	-	67	-	-	Note 16-1
Panel's life	-	0℃～30℃	-	5years	-	-	Note 16-2
Panel	Image Update	Storage and transportation	-	Update the white screen	-	-	-
	Update Time	Operation	-	Suggest Updated once a day	-	-	-

WS : White state, KS : Black State

Note 16-1 : Luminance meter : Eye - One Pro Spectrophotometer ;

Note 16-2: We guarantee display quality from 0℃～30℃ generally,If operation ambient temperature from 0～50℃， will Offer special waveform by Xingtai.

We don't guarantee 5 years pixels display quality for humidity below 45%RH or above 70%RH

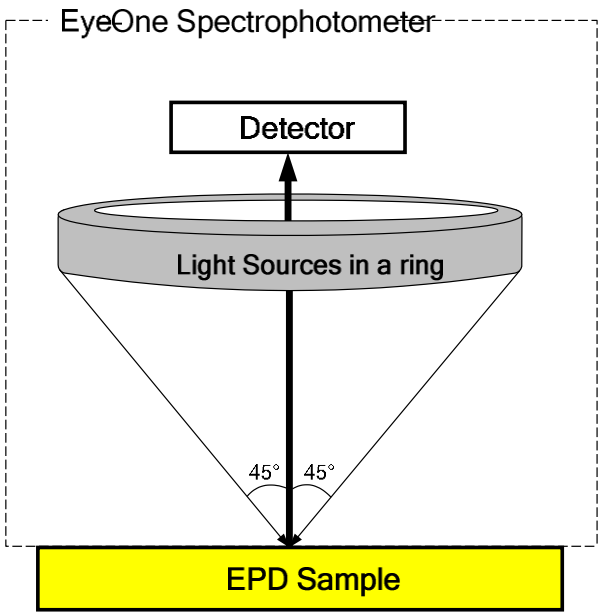
Suggest Updated once a day;

Note: It's only with the 25℃ and 51% RH for 5 years.

15.2 Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd)：

CR = Rl/Rd

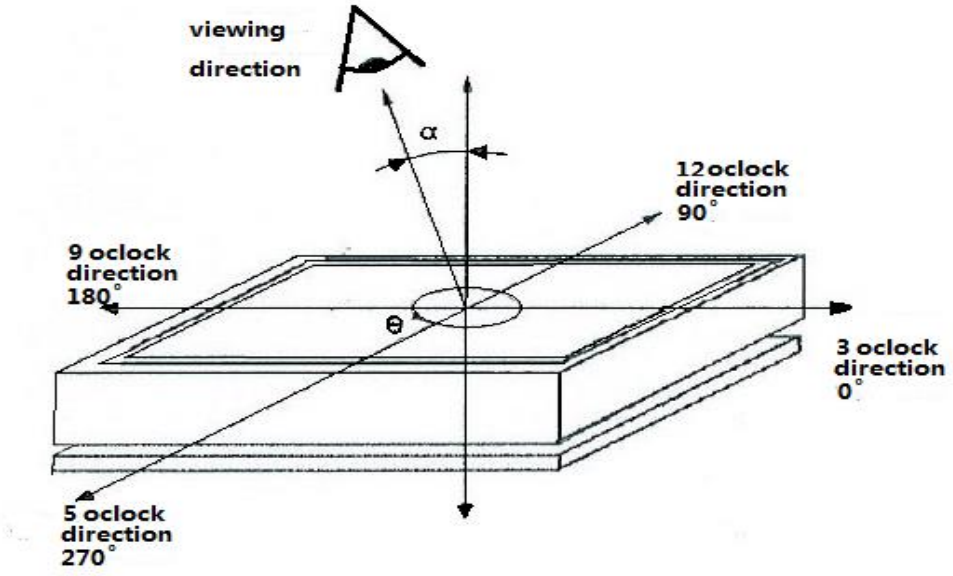


15.3 Reflection Ratio

The reflection ratio is expressed as:

R = Reflectance Factor $_{\text{white board}}$ x (L_{center} / $L_{\text{white board}}$)

L_{center} is the luminance measured at center in a white area (R=G =B=1). $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.



16. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS

WARNING
The display module should be kept flat or fixed to a rigid, curved support with limited bending along the long axis. It should not be used for continual flexing and bending. Handle with care. Should the display break do not touch any material that leaks out. In case of contact with the leaked material then wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.
Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged . Moreover the display is sensitive to static electricity and other rough environmental conditions.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	The data sheet contains final product specifications.

Limiting values
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.
Application information
Where application information is given, it is advisory and dose not form part of the specification.

Product Environmental certification
ROHS
REMARK
All The specifications listed in this document are guaranteed for module only. Post-assembled operation or component(s) may impact module performance or cause unexpected effect or damage and therefore listed specifications is not warranted after any Post-assembled operation.

17. Reliability test

	TEST	CONDITION	REMARK
1	High-Temperature Operation	T=40℃，RH=35%RH，For 240Hr	
2	Low-Temperature Operation	T = 0℃ for 240 hrs	
3	High-Temperature Storage	T=50℃ RH=35%RH For 240Hr	Test in white pattern
4	Low-Temperature Storage	T = -25℃ for 240 hrs	Test in white pattern
5	High Temperature, High-Humidity Operation	T=40℃，RH=90%RH，For 168Hr	
6	High Temperature, High-Humidity Storage	T=50℃，RH=80%RH，For 240Hr Test in white pattern	Test in white pattern
7	Temperature Cycle	-25℃(30min)~60℃(30min)，50 Cycle	Test in white pattern
8	Package Vibration	1.04G,Frequency : 20~200Hz Direction : X,Y,Z Duration: 30 minutes in each direction	Full packed for shipment
9	Package Drop Impact	Drop from height of 100 cm on Concrete surface Drop sequence:1 corner, 3edges, 6face One drop for each.	Full packed for shipment
10	UV exposure Resistance	765 W/㎡ for 168hrs,40℃	
11	Electrostatic discharge	Machine model: +/-250V,0Ω,200pF	

Actual EMC level to be measured on customer application.

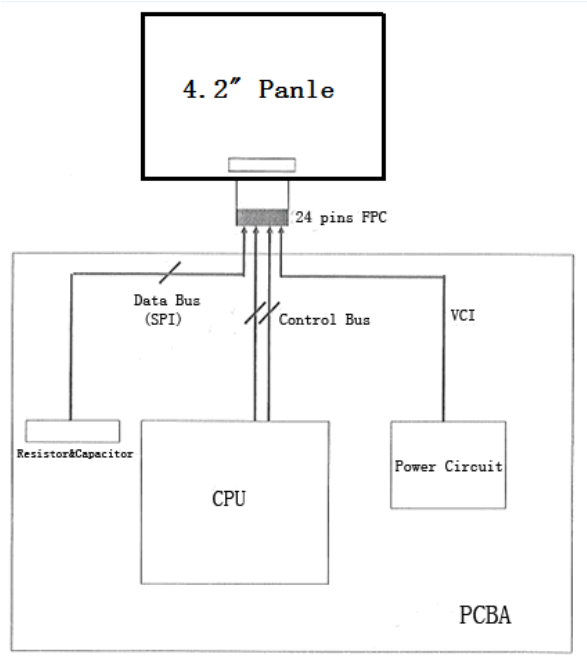
Note1：Stay white pattern for storage and non-operation test.

Note2：Operation is black/white/red pattern , hold time is 150S.

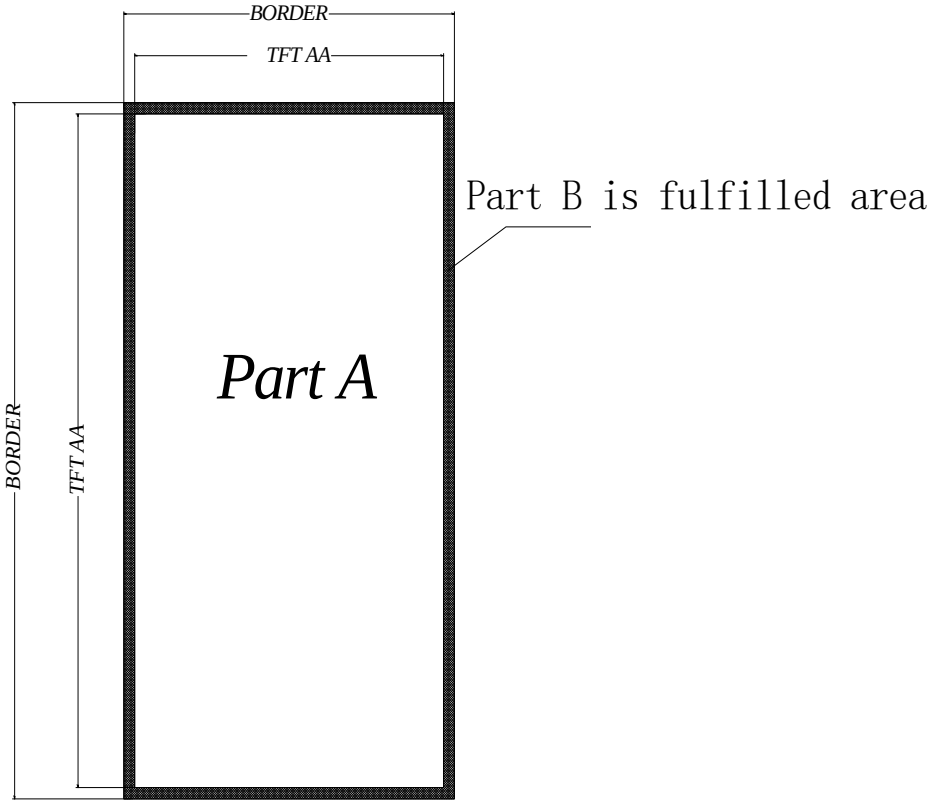
Note3：The function, appearance, opticals should meet the requirements of the test before and after the test.

Note4：Keep testing after 2 hours placing at 20℃-25℃.

18.Block Diagram



19.PartA/PartB specification



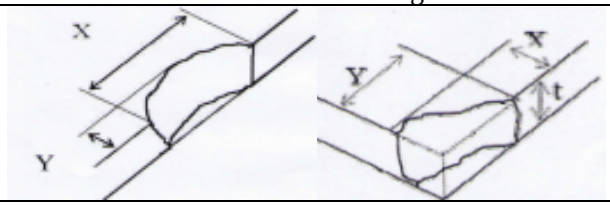
20. Point and line standard

File Name	Specification For 4.2" EPD	Module Number	E042A87
Version	A2	Page Number	27 of 33

Shipment Inspection Standard

Equipment：Electrical test fixture, Point gauge

Outline dimension	91.00(H)× 77.00(V) × 1.1(D)	Unit：㎜	Part-A	Active area	Part-B	Border area
Environment	Temperature	Humidity	Illuminance	Distance	Time	Angle
	19℃～25℃	55%±5%RH	800～1300Lux	300 ㎜	35Sec	

Defect type	Inspection method	Standard	Part-A	Part-B
Spot	Electric Display	D≤0.25 ㎜	Ignore	Ignore
		0.25 ㎜＜D≤0.4 ㎜	N≤4	Ignore
		D＞0.4 ㎜	Not Allow	Ignore
Display unwork	Electric Display	Not Allow	Not Allow	Ignore
Display error	Electric Display	Not Allow	Not Allow	Ignore
Scratch or line defect(include dirt)	Visual/Film card	L≤2 ㎜,W≤0.2 ㎜	Ignore	Ignore
		2.0mm＜L≤5.0mm,0.2＜W≤ 0.3mm,	N≤2	Ignore
		L＞5 ㎜,W＞0.3 ㎜	Not Allow	Ignore
PS Bubble	Visual/Film card	D≤0.2mm	Ignore	Ignore
		0.2mm≤D≤0.35mm & N≤4	N≤4	Ignore
		D＞0.35 mm	Not Allow	Ignore
Side Fragment	Visual/Film card	X≤6mm,Y≤0.4mm, Do not affect the electrode circuit (Edge chipping) X≤1mm,Y≤1mm, Do not affect the electrode circuit((Corner chipping) Ignore		
				
Remark	1.Cannot be defect & failure cause by appearance defect；			
	2.Cannot be larger size cause by appearance defect；			
	L=long W=wide D=point size N=Defects NO			

Note20-1： OQC inspection: One-time sampling plan for GB/T 2828.1-2012 , Inspection Level II, CR: AC/Re=0/1, MA=0.4, MI=0.65.

Note 20-2: Spot define: That only can be seen under White State or Dark State defects

Note 20-3: Any defect which is visible under gray pattern or transition process but invisible under black and white is disregarded.

Note 20-4:Any defect must be judged by Optical Microscope.

Note 20-5:Here is definition of the “Spot” and “Scratch or line defect”

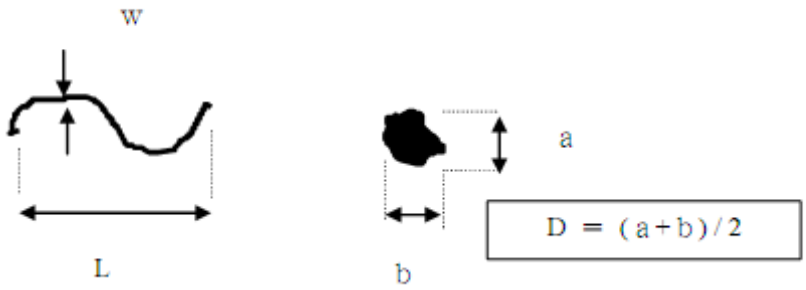
Spot: W>1/4L

Scratch or line defect :W ≤ 1/4L

Note 20-6:Definition for L/W and D （major axis）

Note 20-7：FPC bonding area pad doesn’t allowed visual inspection

Note 20-8：



21.Barcode

21.1 label appearance

ABBBBBBBCC
DDDEEEFGGG

21.2 QR scanned information（Total 28 code number+ 2 blank spaces）

A BBBBBBB CC ✐ DDD EEE F GGG ✐ H III J KKK
① ② ③ ④ ⑤ ⑥ ⑦ ⑧ ⑨ ⑩ ⑪

① A——The factory code
② BBBBBBB——Module name of EPD
③ CC——FPL model name
④ DDD——Date of production
⑤ EEE——Production lot
⑥ F——Separator
⑦ GGG——FPL Lot
⑧ H——Normal Lot
⑨ III——TFT、PS、EC.
⑩ J——IC
⑪ KKK——Serial NO.
✐ blank spaces

22.Packing

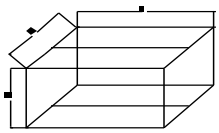
Packing Spec

Sheet No：

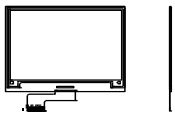
	Part No	E042A74	DATE	2020.05.21	VER	A0	Page	2-1

一, Package Type: Box

Box No	Holitech shipping box
Box size	515*322*170
Containment	96PCS



PRODUCT DRAWING



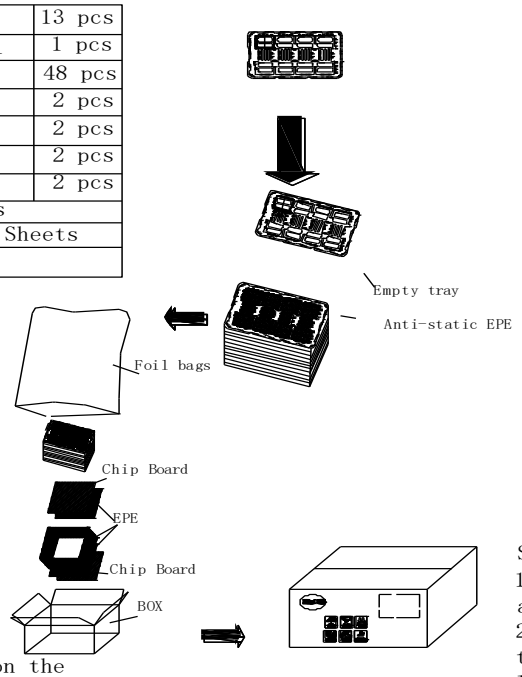
二,Inside package type:Plastic Tray unit: mm

Plastic Tray	465*280*15	13 pcs
Anti-static foil bags	700*530*0.1	1 pcs
EPE(inside)	88*221.5*2	48 pcs
EPE(Up-Down)	485*145*10	2 pcs
EPE(Left-Right)	285*480*10	2 pcs
EPE(Front-back)	310*145*10	2 pcs
Chip board	500*306*5	2 pcs
Quantity/tray	8 pcs	
Tray number/sheet	12+1 Sheets	
Box	1	

Step 1:
Material: Tray, EPE
Put the product in to the tray and keep the dispaly side up. Then put anti-static EPE in to each holes.

Step 2:
1) Must keep the angle 180 degree placed between the neighboring Plastic trays.
2) There are 12 layers product, total 8*12=96 pcs。
3) An empty Plastic tray intersects put on the top of the plastic trays.

Step 3:
1) In each case, put 2 bags of desiccant. then seal the trays with adhesive tapes.
2) Put the trays into foil bags.
3) heat seal the foil bags.



Step 4:
1)First put a chip board on the buttom of the box, then placed the down EPE, the left - right and front -back EPE.
2) Placed the sealed products into the box.
3) The last placed the up EPE on the top of the trays, and place a chip board on it.

Step 5:
1) Seal the box with adhensive tapes 。
2) Paste the lable onto the exterior box, and the lable can't cover the safety ,
transfer and RoSH sign。

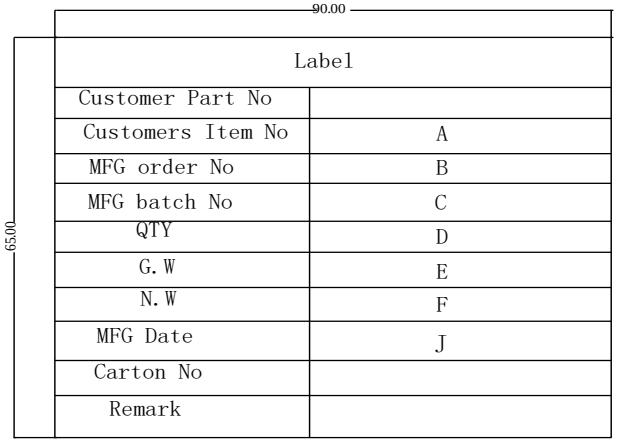
Design	X.Z.P	Approve	H.Z.P	Confirm	X.X.M
Date	2020.05.21	Date	2020.05.21	Date	2020.05.21

Packing Spec

Sheet No

	Part No	E042A74	Date	2020.05.21	VER	A0	Page	2-2

The label outside the carton print as below



Label	
Customer Part No	
Customers Item No	A
MFG order No	B
MFG batch No	C
QTY	D
G.W	E
N.W	F
MFG Date	J
Carton No	
Remark	

NOTE:

1. "A" Print customer Item No
2. "B" Print customer Order No
3. "C" Print MFG Batch No(Separate packing for different batch products. Mixed packing available for the odd number of different batch print all the batch NO&QTY accordingly if happened.
4. "D"Print product qty
5. "E"Print the G.W
6. "F"Print the N.W
7. "J"Print the MFG date
8. Before packing make sure the FPL batch ,item and qty are the same as which on the Final passed card.

Design	X.Z.P	Approve	H.Z.P	Confirm	X.X.M
Date	2020.05.21	Date	2020.05.21	Date	2020.05.21