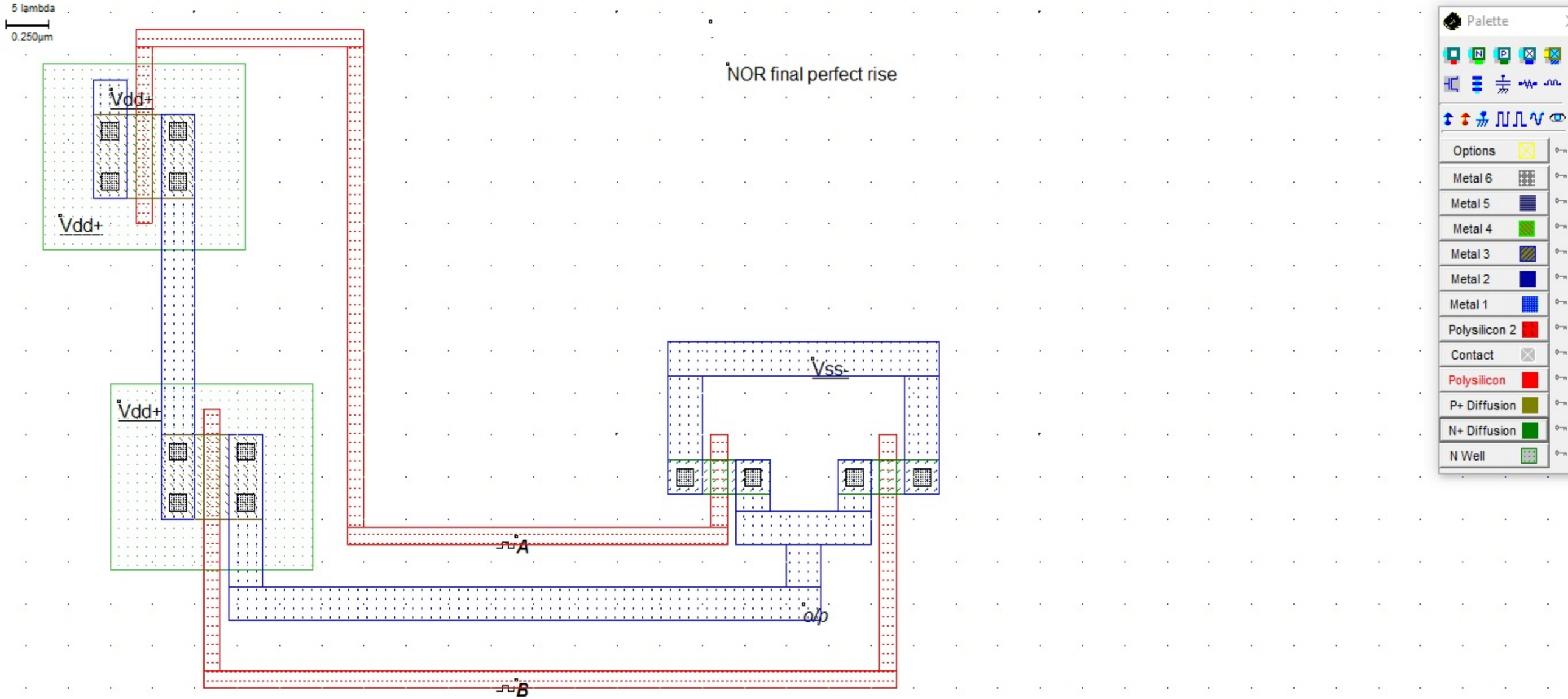
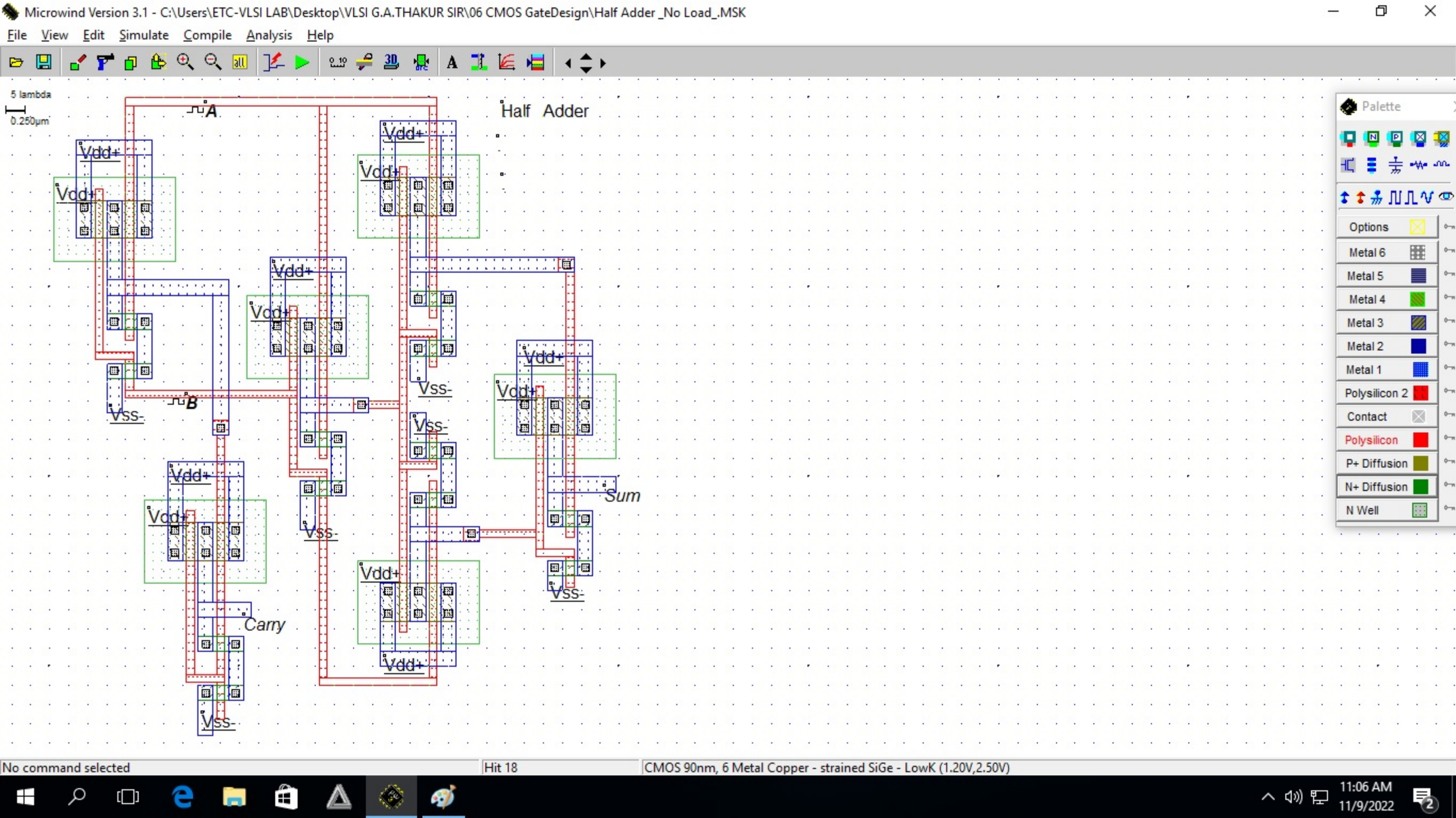
Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\NOR final perfect rise fall 5ps.MSK

File View Edit Simulate Compile Analysis Help



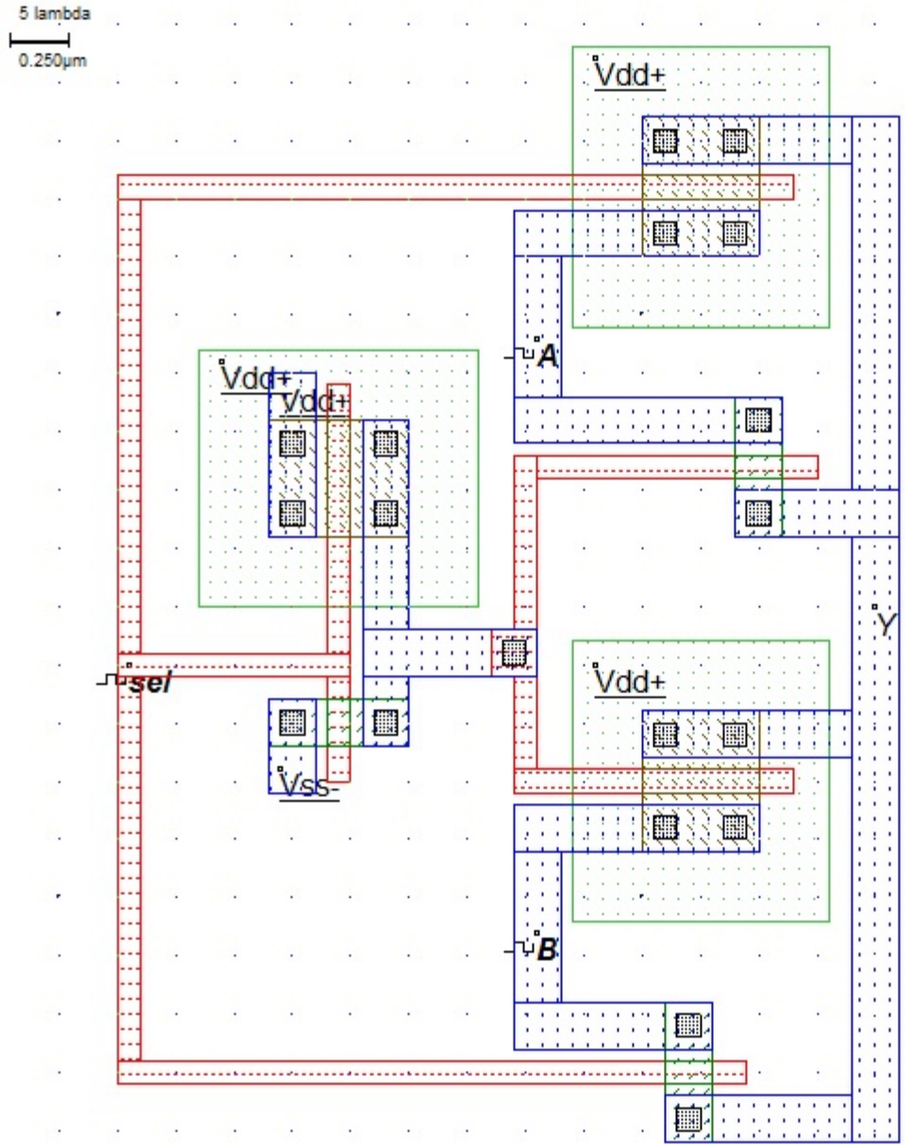
No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

11:01 AM
11/9/2022

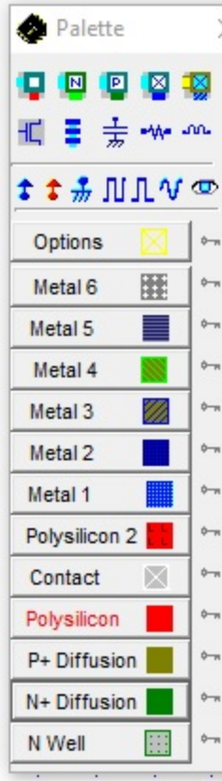

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\Half Adder _No Load_.MSK
File View Edit Simulate Compile Analysis Help
5 lambda
0.250µm
Half Adder
A
B
Sum
Carry
Vdd+
Vss-
Palette
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
No command selected
Hit 18
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)
11:06 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\07 CMOS Mux\mux by txgates sk.MSK

File View Edit Simulate Compile Analysis Help



MUX using Tx Gate

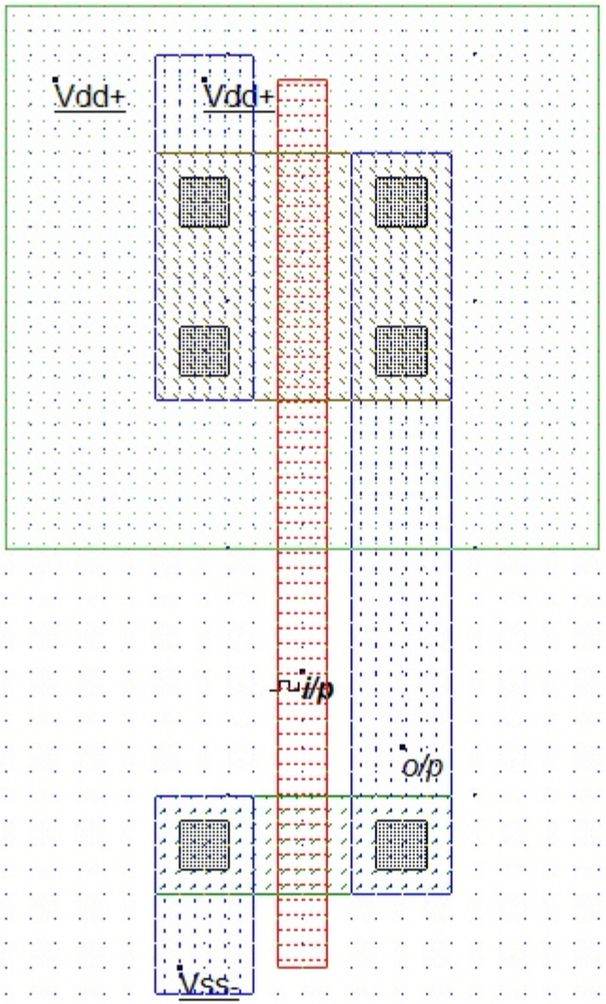


No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\Inverter No Load SK.MSK

File View Edit Simulate Compile Analysis Help

1 lambda
0.050µm



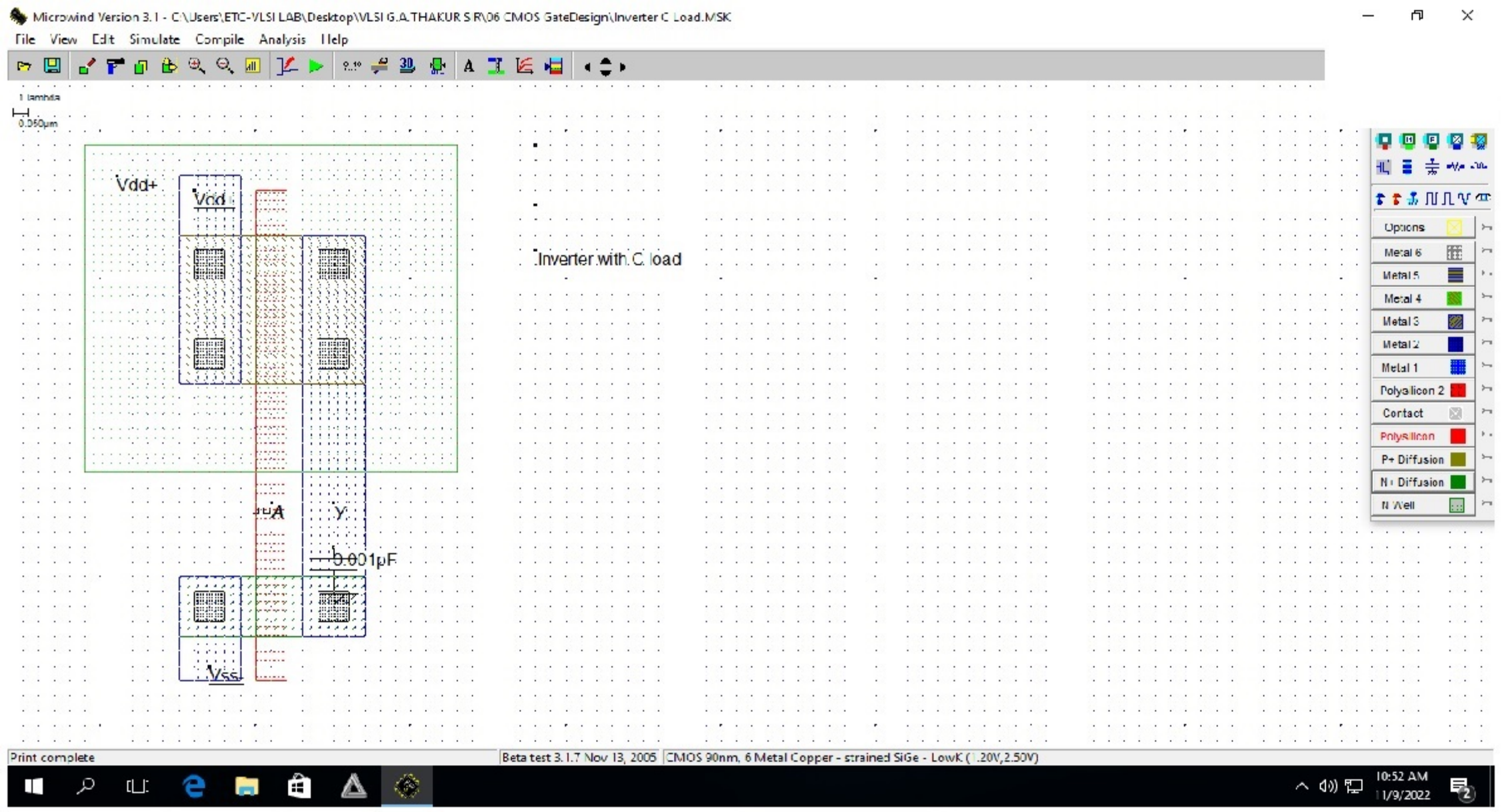
Inverter with no load

Palette

Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well

No command selected | Beta test 3.1.7 Nov 13, 2005 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

10:56 AM
11/9/2022

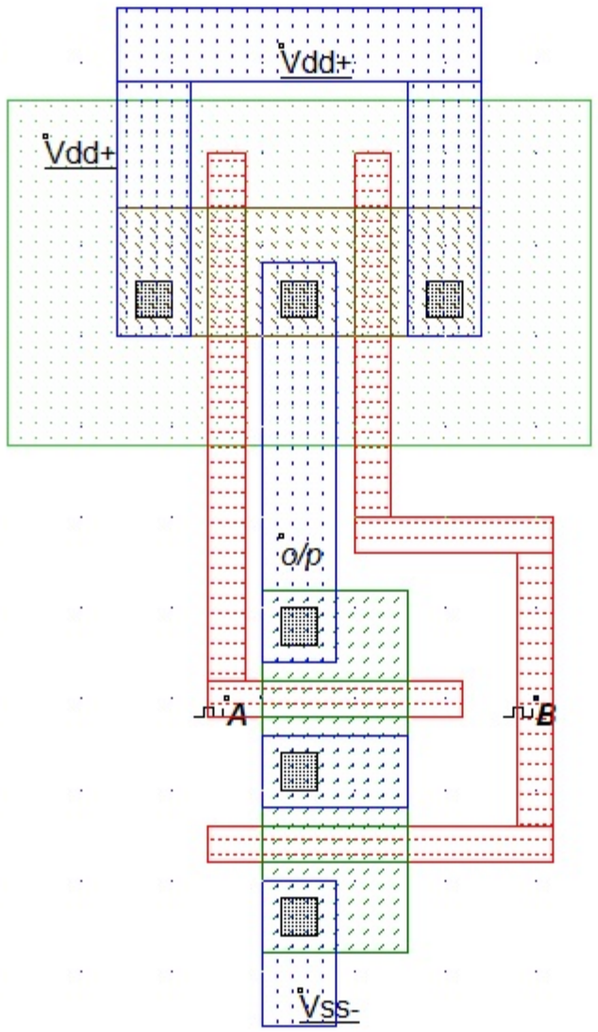

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR S R\06 CMOS GateDesign\Inverter C Load.MSK
File View Edit Simulate Compile Analysis Help
Vdd+
Vdd
Inverter with C load
A
Y
0.001pF
Vss
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well
Print complete
Beta test 3.1.7 Nov 13, 2005
CMOS 90nm, 6 Metal Copper - strained SiGe - LowK
10:52 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\NAND SK final 1ps rise fall 90d rotated.MSK

File View Edit Simulate Compile Analysis Help

5 lambda
0.250µm

NAND Gate



Palette

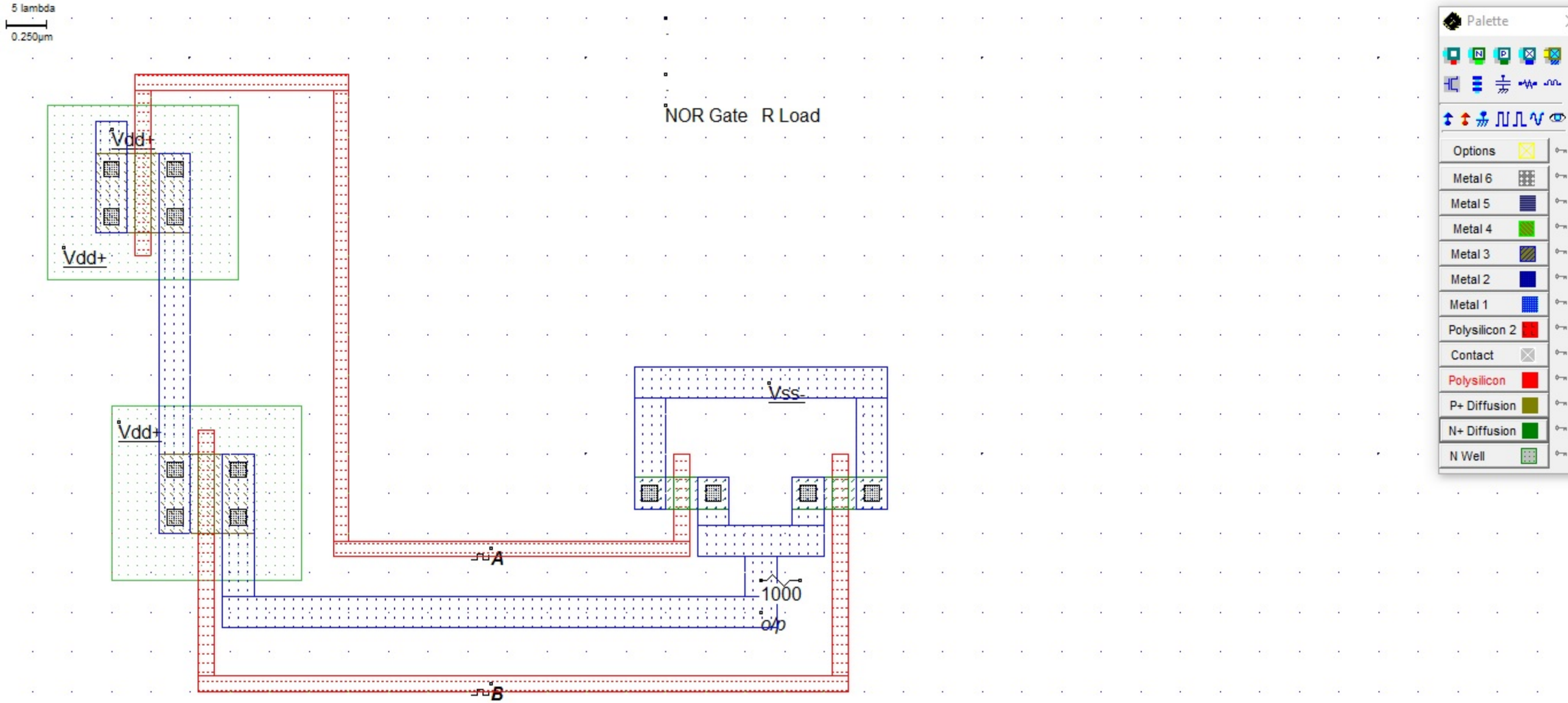
Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well

No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

11:00 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\NOR R Load SK.MSK

File View Edit Simulate Compile Analysis Help

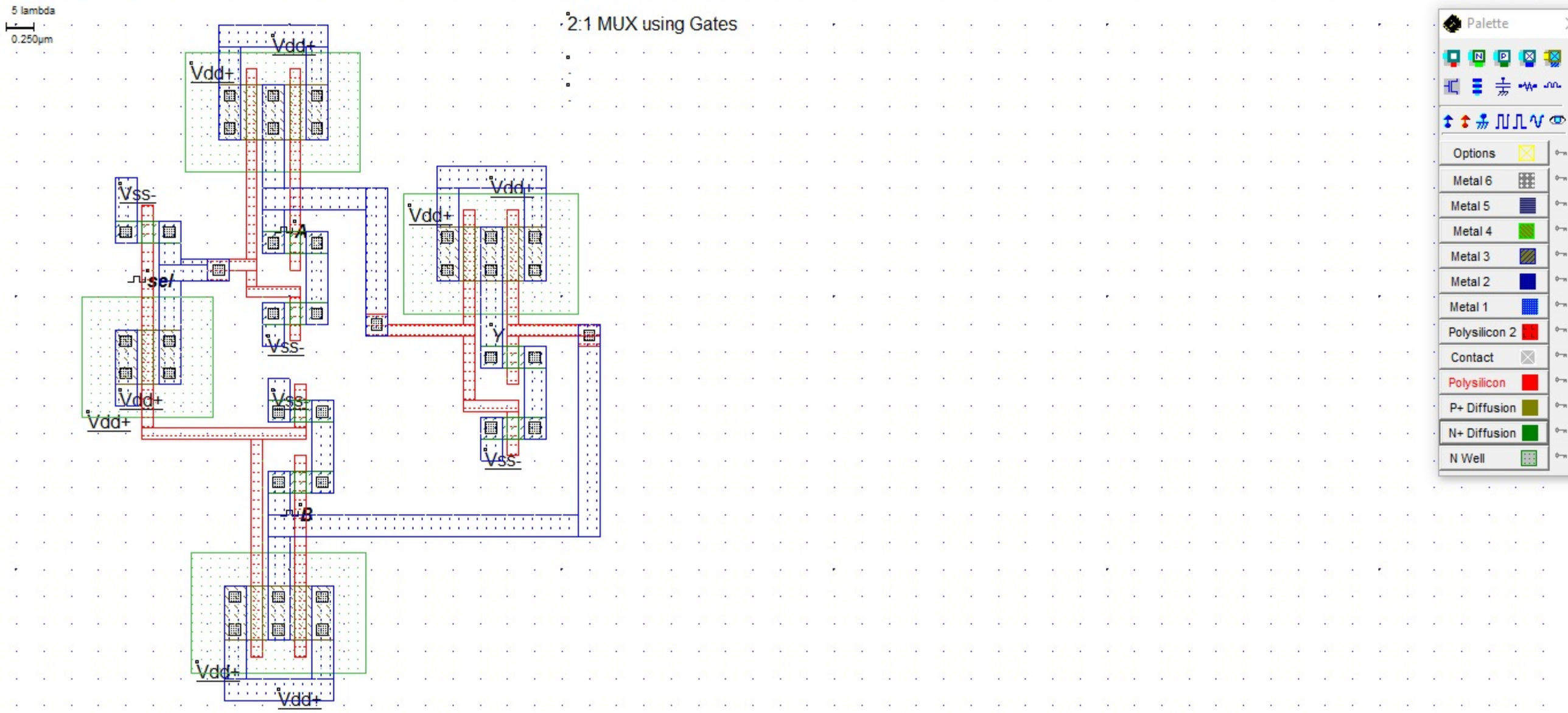


No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

11:02 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\07 CMOS Mux\mux by nand skfinal.MSK

File View Edit Simulate Compile Analysis Help



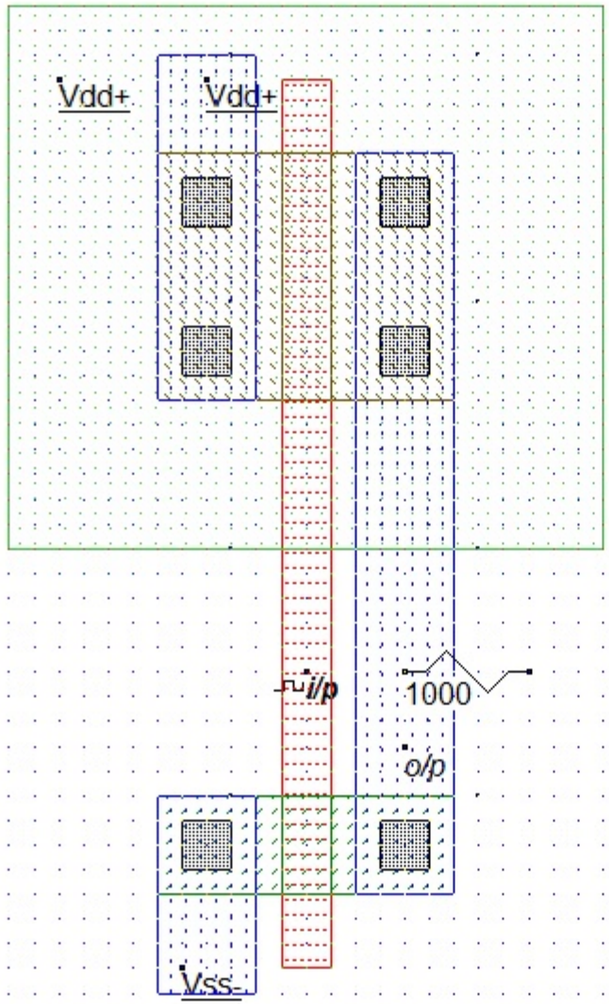
No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

11:03 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\Inverter R Laod SK.MSK

File View Edit Simulate Compile Analysis Help

1 lambda
0.050µm



Inverter R Load

Palette

Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well

No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

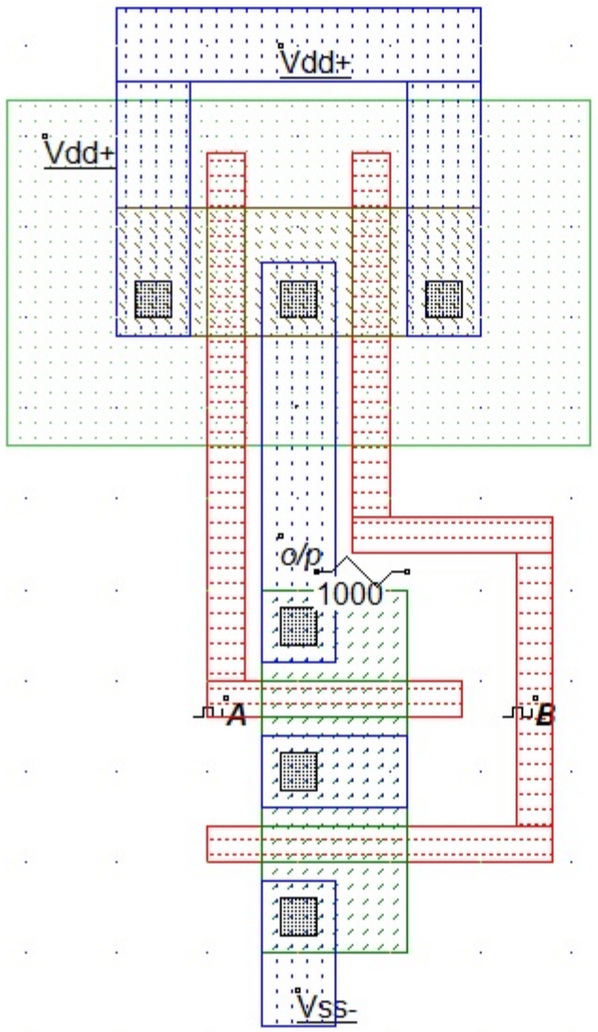
10:58 AM
11/9/2022

Microwind Version 3.1 - C:\Users\ETC-VLSI LAB\Desktop\VLSI G.A.THAKUR SIR\06 CMOS GateDesign\NAND R Load SK.MSK

File View Edit Simulate Compile Analysis Help

5 lambda
0.250µm

NAND Gate R Load



Palette

Options
Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Polysilicon 2
Contact
Polysilicon
P+ Diffusion
N+ Diffusion
N Well

No command selected | Hit 18 | CMOS 90nm, 6 Metal Copper - strained SiGe - LowK (1.20V,2.50V)

10:59 AM
11/9/2022