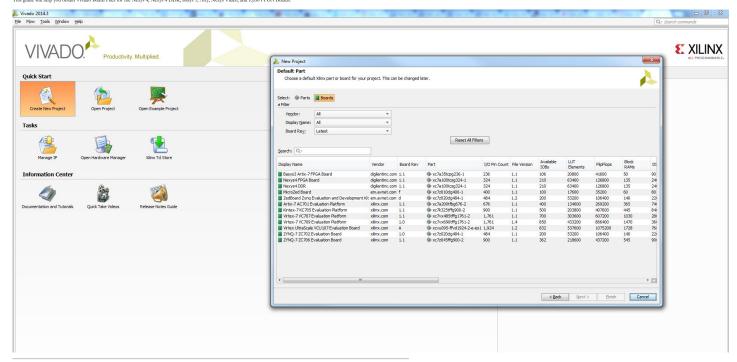


Vivado Version 2015.1 and Later Board File Installation

Board Files: Download [https://github.com/Digilent/vivado-boards/archive/master.zip]

Description



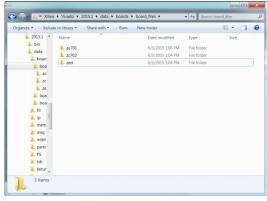
What you need before proceeding with this guide

Follow this Wiki guide on how to install and activate Vivado on your PC. Installing Vivado

What are Board Files and why do you need them

After installing Vivado, the default installation directory on your drive folder can be found here: C:\Xilinx\Vivado\2015.1\data\boards. ain a folder called board_files. If Vivado is installed in the C drive (usually record

By default this folder contains XML files for different FPGA boards ma

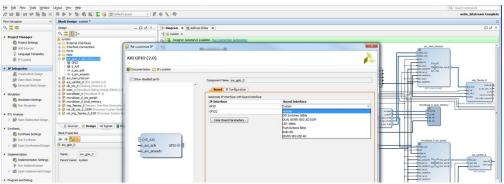


XML files define different interfaces on the board. Interfaces such as Slide Switches, Push Buttons, LEDs, USB-UART, DDR Memory, Ether

Digilent has created XML files for the Artix 7 FPGA boards

- Basys 3
 Nexys 4
 Nexys 4 DDR
 Arty
 Nexys Video
 Zybo

- In the AXI GPIO IP customiz



Vivado Version 2015.1 and Later Board File Installation [Reference.Digilentinc]

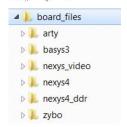


Installation

 $Download \ and \ extract \ this \ Zip \ file: \ https://github.com/Digilent/vivado-boards/archive/master.zip \ [https://github.com/Digilent/vivado-boards/archive/master.zip]$

 $You \ can \ also \ check \ out \ the \ repository \ for \ the \ board \ files \ on \ github \ located \ \underline{here} \ [\underline{https://github.com/Digilent/vivado-boards/[left]}]$

This zip file will contain a folder called new/hourd_files. Save this in your user documents folder. We will copy this hourd_files folder, navigate to the board_files folder inside the Vivado Installation directory, and menge them both.



- Copy the contents of the band_files folder
 Navigate to the board_files folder in the Vivado Installation directory (C:\Xilmx\Vivado\2015.1\data\boards\board_files)
 Passe the contents into the board_files folder
 Restart Vivado

The newly added files will each contain a sub-folder for the current board revision. This sub-folder contains the respective XML files for each FPGA board.

The sub-folder for the nexys4_ddr will contain an additional file called mig.prj which is the Xilinx Memory Interface Generator description file for customizing the DDR2 component on the Nexys 4 DDR.

You are now ready to start a new IP Integrator based Vivado project for the Digilent Nexys 4, Nexys 4 DDR and Basys 3 FPGA Boards.

vivado/boardfiles2015.txt · Last modified: 2016/01/20 16:56 by Thomas Kappenman