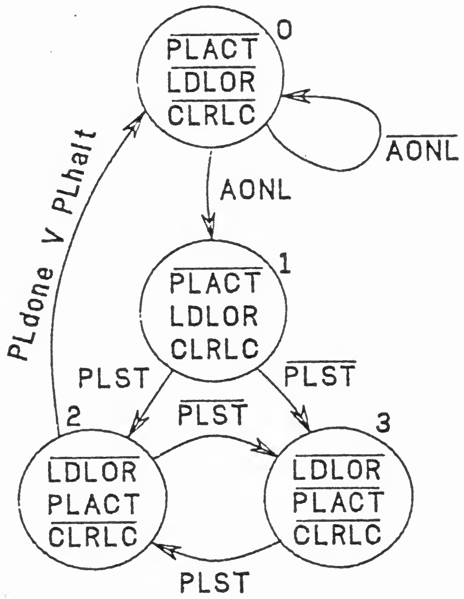
PARAMETER LOAD SEQUENCER STATE TABLE



State 0 - No Object Requires Load
State 1 - Initialization for Parameter Load
State 2 - Parameter Load currently Active
State 3 - Parameter Load currently Suspended

AONL = Any Object Needs Load
PLST = Parameter Load Active Status {from Gold Chip}
PLDONE = Parameter Load Done {Link Counter increments to one plus last parameter offset}
PLHALT = Parameter Load Halted {Half root written - Currently active object}
ENLOR = Enable Loading Object Register {Select OSELe Mux to L.O.Reg.}
PLACT = Parameter Load Active {Parameter memory fetch control to memory arbiter}
LDLOR = Load Loading Object Register from priority encoder
CLRLC = Clear Link Address Counter

State Definitions for Rainbow

Pixel Fetch States

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FERC: {Fetch Even Run Code}
    If Load RunCode (LRC) and Last FE then
          Select Object Select mux from OSEL to RCSEL
          Pixel Word Counter selected by RCSEL
          Pixel Data RAM selected by RCSEL
          Select Pixel Word Counter mux to Current Address (CADR)
          Enable Address Buffer (ENA)
          Assert Address Strobe (AS)
          Next state
          Deassert Address Strobe (AS)
          Increment Pixel Word Counter
          Assert Data Strobe (DS)
          Assert Data Load (Dld)
          Test and Wait for Data Acknowledge (DA) to assert
          Deassert Data Strobe (DS)
          Deassert Data Load (Dld).

FORC: {Fetch Odd Run Code}
    If Load RunCode (LRC) and Last FO then
          Select Object Select mux from OSEL to RCSEL
          Pixel Word Counter selected by RCSEL
          Pixel Data RAM selected by RCSEL
          Select Pixel Word Counter mux to Current Address (CADR)
          Enable Address Buffer (ENA)
          If OSELe=RCSEL then Assert Even Shadow Register Load (LDES)
          Assert Address Strobe (AS)
          Next state
          Deassert Address Strobe (AS)
          If OSELe=RCSEL then Deassert Even Shadow Register Load (LDES)
          If OSELe=RCSEL then Select mux to Even Shadow (ENES)
          Increment Pixel Word Counter
          Assert Data Strobe (DS)
          Assert Data Load (Dld)
          Test and Wait for Data Acknowledge (DA) to assert
          Deassert Data Strobe (DS)
          Deassert Data Load (Dld).

De: {read even word - OSELe}
          Pixel Word Counter selected by OSELe
          Pixel Data RAM selected by OSELe
          Select Pixel Word Counter mux to Current Address (CADR)
          Enable Address Buffer (ENA)
          Assert Address Strobe (AS)
          Next state
          Deassert Address Strobe (AS)
          Assert Data Strobe (DS)
          Assert Data Load (Dld)
          Test and Wait for Data Acknowledge (DA) to assert
          Deassert Data Strobe (DS)
          Deassert Data Load (Dld).

Do: {read odd word - OSELo}
          Pixel Word Counter selected by OSELo
          Pixel Data RAM selected by OSELo
          Select Pixel Word Counter mux to Current Address (CADR)
          Enable Address Buffer (ENA)
          Assert Address Strobe (AS)
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        Next state
        Deassert Address Strobe (AS)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld).

De & Do: {Read even word - OSELe then read Odd word - OSELo}
        Pixel Word Counter selected by OSELe
        Pixel Data RAM selected by OSELe
        Select Pixel Word Counter mux to Current Address (CADR)
        Enable Address Buffer (ENA)
        Assert Address Strobe (AS)
        Next state
        Deassert Address Strobe (AS)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld)
        Pixel Word Counter selected by OSELo
        Pixel Data RAM selected by OSELo
        Select Enable Pixel Word Counter mux to Current Address (CADR)
        Enable Address Buffer (ENA)
        Assert Address Strobe (AS)
        Next state
        Deassert Address Strobe (AS)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld).

S: {Shadow cycle - OSELo}
        Pixel Data RAM even output selected by OSELe
        Pixel Counter selected by OSELe
        Select Pixel Word Counter mux to Current Address (CADR)
        Enable Address Buffer (ENA)
        Assert Even Shadow Register Load (LDES)
        Assert Address Strobe (AS)
        Next state
        Deassert Even Shadow Register Load (LDES)
        Deassert Address Strobe (AS)
        Select Mux to Even Shadow Register (ENES)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld).

T: {Even Pixel Data load, Shadow Even Pixel & then Odd Pixel load}
        Pixel Word Counter selected by OSELe
        Pixel Data RAM selected by OSELe
        Select Pixel Word Counter mux to Last Address (LADR)
        Enable Address Buffer (ENA)
        Assert Address Strobe (AS)
        Next state
        Deassert Address Strobe (AS)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld).
        Select Pixel Word Counter mux to Current Address (CADR)
        Enable Address Buffer (ENA)
        Assert Even Shadow Register Load (LDES)
        Assert Address Strobe (AS)
        Next state
        Deassert Even Shadow Register Load (LDES)
        Deassert Address Strobe (AS)
        Select Mux to Even Shadow Register (ENES)
        Assert Data Strobe (DS)
        Assert Data Load (Dld)
        Test and Wait for Data Acknowledge (DA) to assert
        Assert Data Valid
        Deassert Data Strobe (DS)
        Deassert Data Load (Dld).

Refresh Memory Cycle:  {Gold}
        Test and wait for refresh active status
        Enable Refresh Address Buffer (ENRA)
        Assert Address Strobe (AS)
        Next State
        Deassert Address Strobe (AS)
        Test and Wait for Data Acknowledge (DA) to assert.

Write Root Memory Cycle: {Silver}
        Test Processor Request (PR)
        If Processor Request (PR) is asserted then
                If Link Load not Active or no Object Requires load then
                        Tristate Address Strobe (AS), set as input
                        Tristate Data Strobe (DS), set as input
                        Set Data Acknowledge (DA) as an output
                        Set Address/Data Bus as an input
                        Assert Processor Grant (PG)
                        Test and wait for Address Strobe (AS) to assert
                        Latch address into internal address registers
                        Test and wait for Address Strobe (AS) to deassert
                        Test and wait for Data Strobe (DS) to assert
                        Set Muxr to pass address latch to Link RAM
                        Latch data into Link RAM
                        Assert Data Acknowledge (DA)
                        Test and Wait Data Strobe (DS)
                        Deassert Data Acknowledge (DA)
                        Deassert Processor Grant (PG).
                        Set address strobe (AS) as an output
                        Set data strobe (DS) as an output
                        Set Data Acknowledge (DA) as an input
                        Set address/data bus as an output
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Link Load:
        While Link Load Status is active {Gold Chip} and any Object Requires
            Load do
                Arbitrate Highest Priority Object
                Select all register arrays with OSEL or OSELX
                Clear Link Load Shift Register stages 1 through 8
                Set stage 0 of Link Load Shift Register
                Load Link Counter from Link Register Array
                Select Address Mux to Link Load Counter
                While Link Load Shift Register, Stage 8 is low
                  do
                        Perform Read Memory Cycle
                        Enable Data on to Pbus during Data Strobe active
                        Load Parameter Registers 0..7 from Pbus strobed by
                          Pload 0..7 which is Data Strobe and Link Load Shift
                          Register Output Stages 0..7
                        Clock Link Load Shift Register
                        Increment Link Load Counter
                Delete current selected object from Priority Encoder
                  Input Register.
```

Interchip Status

S2	S1	S0	Description
0	0	0	Refresh Active
0	0	1	NOP
0	1	0	Abort Cycle
0	1	1	Reset
1	0	0	Even Field Top Of Screen
1	0	1	Odd Field Top Of Screen
1	1	0	Pixel Active
1	1	1	Link Load Active