Lab 2 Report

1st Skyler Cook
Electrical and Computer Engineering
Utah State University
Logan, USA
A02304185@aggies.usu.edu

2nd Jaron Seedal
Electrical and Computer Engineering
Utah State University
Logan, USA
a02358703@aggies.usu.edu

3rd Dr. Jonathan Philips
Electrical and Computer Engineering
Utah State University
Logan, USA
jonathan.phillips@usu.edu

***Abstract*—This document is a written report of the laboratory work performed to simulate a stopwatch that counts while a button is pressed, and resets when another button is pressed at any point, accurate to the tens of milliseconds.**

I. Introduction

This project implements a stopwatch on the DE10-Lite FPGA board using VHDL. The stopwatch displays time in MM.SS.HH format on the six seven-segment displays, with push buttons for reset and go control. The design achieves hundredth of a second accuracy using counters and nested assignment statements.

II. Objectives

The objectives of the project, as defined by the instructor, were: Implement a stopwatch on your DE-10 Lite development board. The stopwatch should meet the following criteria:

1) The stopwatch shall be accurate to hundredths of a second.
2) The 6 seven-segment displays will be used to represent minutes, seconds, and hundredths of seconds following the format MM.SS.HH (notice the decimal points).
3) Use the 2 push buttons as a ”reset” and a ”go” button. Reset sets the time back to zero. The stopwatch starts when go is pressed and stops when go is released.
4) Do not use a gated or register-driven clock in your design. In other words, no clock dividers!
5) Complete the entire project in VHDL.

III. Procedure

The students started the assignment by writing out their logic for how the stopwatch assignments would be made. The students decided to use a custom variable defined to be an array of hexadecimal values from 0 to 9 (10 entries). The students decided to split the memory into two sections, one with decimal points and one without decimal points. The students elected to use nested if-else statements to increment integers for each time location (MM:SS:HH). At the end of the logic, the students would then make assignments to the seven-segment displays by accessing the hexadecimal values stored in the array at the position associated with the integer value.

The students then simulated their design, which surprisingly worked perfectly the first time. The stopwatch was accurate to a hundredth of a second and the system responded to inputs properly. The students then moved on to programming the DE10-Lite. This is where the students ran into a multitude of issues. The first issue the students found was that their top module did not define the stopwatch entity, so the assignments were never being mapped to the board. After this change, the students were stumped for nearly 2 hours as they read through the compiler errors on Quartus Prime. It turned out that the students had named their project differently than their top module, making it so the compiler could not find the proper port mappings and assignments.

The students fixed the compiler issue by changing the .qsf file to look at the correct .vhd file where the top module was located. Once this change was made, the output went to the board properly. However, the seven-segment displays did not show the correct values based on the students attempt to interpret the schematic. The students then defined their custom array to only turn one segment on at a time to determine which segments corresponded to which bit in the 8-bit array. The students then calculated the associated hexadecimal values for the array with and without the decimal point. Once these values were updated, the stopwatch functioned perfectly.

IV. Results

The students successfully simulated the function of the stopwatch. The students then programmed the DE10-Lite. After some debugging, the students had a fully-functional stopwatch, as defined by the project objectives. Fig 1 shows the stopwatch after running for 31 seconds in parallel to a calibrated stopwatch, with the small error between the two being a result of imperfect human start and stopping button presses.

The project also simulated as expected, as shown in Fig 2 and Fig 3. Fig 2 shows signals were reset to their base hex value corresponding to 0 when a reset signal is given. Fig 3 shows that when the stopwatch start signal is low, the counter pauses and resumes onces the start signal goes high, simulating a button press.

V. Discussion and Conclusions

The stopwatch design successfully met the requirements by displaying minutes, seconds, and hundredths of a sec-

Fig. 1. Thirty-one Second Stopwatch Run

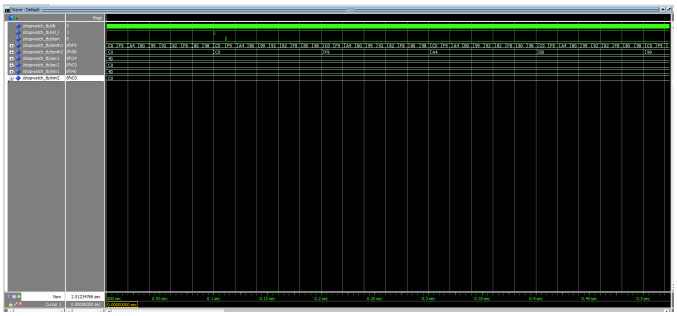

Fig. 2. Counter Resetting in Simulation

ond on the DE10-Lite's six seven-segment displays. Using counters ensured accurate timing without gated clocks, while the push buttons provided reliable reset and go functions. Simulation confirmed correct operation, and hardware testing demonstrated consistent performance on the FPGA. The main issues that were presented arose from learning how to program VHDL in multiple files to understand better how to make modular designs, and the necessary implementation for this. Overall, the project reinforced concepts of synchronous digital design, clock management, and practical FPGA implementation.

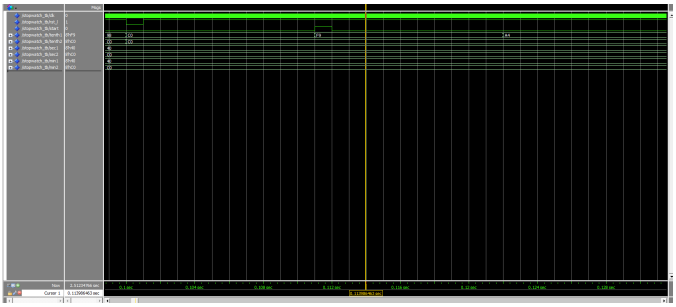

Fig. 3. Simulation count being delayed for 10 ms