Leader of Microcontroller Technology
A Fabless Semiconductor Company

ABOV SEMICONDUCTOR

Hardware Design Guide for Noise Immunity

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Contents

1. Filter & Bypass Capacitor

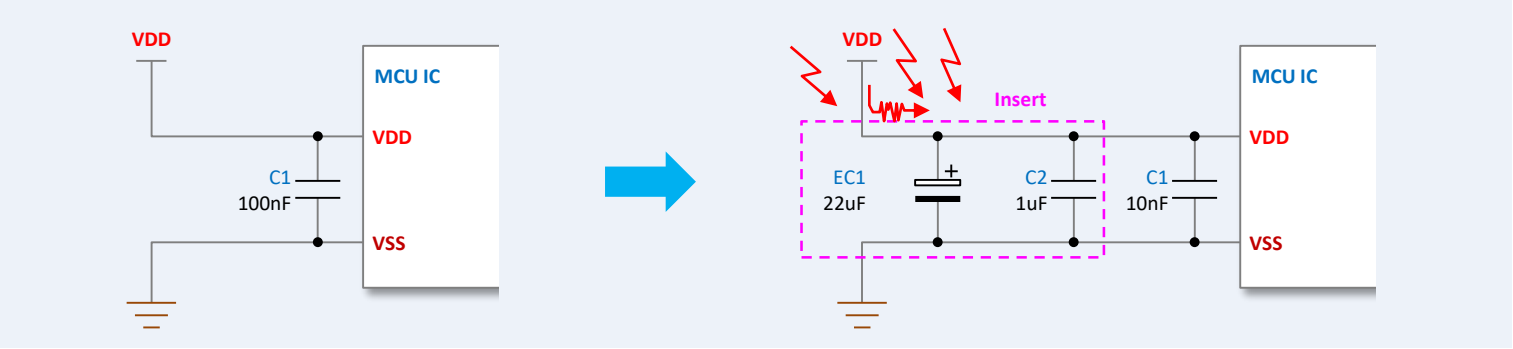
Filter Capacitor: EC1 (Electrolytic Capacitor)

- External noise (e.g. EFT) is reduced first by a capacitor of a power source.
- In case of an electrolytic capacitor with leads, values of ESL (Equivalent Series Inductance) and ESR (Equivalent Series Resistance) are high, and thus SRF (Self Resonant Frequency) value is low.
- The filter capacitor EC1 is used to block low frequency noise. It should be placed close to a Host (IC) or a connector (within 30mm) rather than to an MCU.

Bypass Capacitor: C1, C2

- Chip Ceramic Capacitors are recommended.
- Two capacitors are used often in a Decoupling Capacitor structure (Typ. use 100-fold difference).
- Since they block high frequency noise, the bypass capacitors should be placed close to an MCU's power pin (within 10mm).

Item	Component	Value
Bypass Capacitor (Decoupling)	C1	10nF (0.01uF) to 100nF (0.1uF)
	C2	1uF
Filter Capacitor	EC1	Typ. 22uF

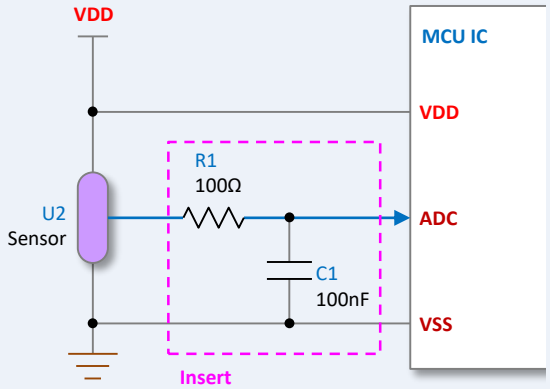


2. ADC Input

Power Selection

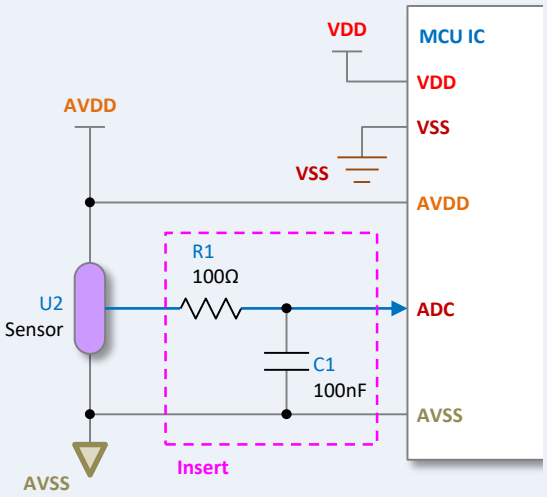
- Analog power should be used for a circuit design if analog power (AVDD and AVSS) and digital power (VDD and VSS) are separated in an MCU.
- Single power should be used if an MCU supports single power internally. It should be sure that the analog power and the input trace are not affected by external noise.
- Additionally, an RC filter (Low Pass Filter) can be used on the ADC input trace. When using the RC Filter, RC Time Constant value should be 3-times the stabilization time.

1. For only single power



$$f_c = \frac{1}{2\pi RC}$$

2. For supporting analog power



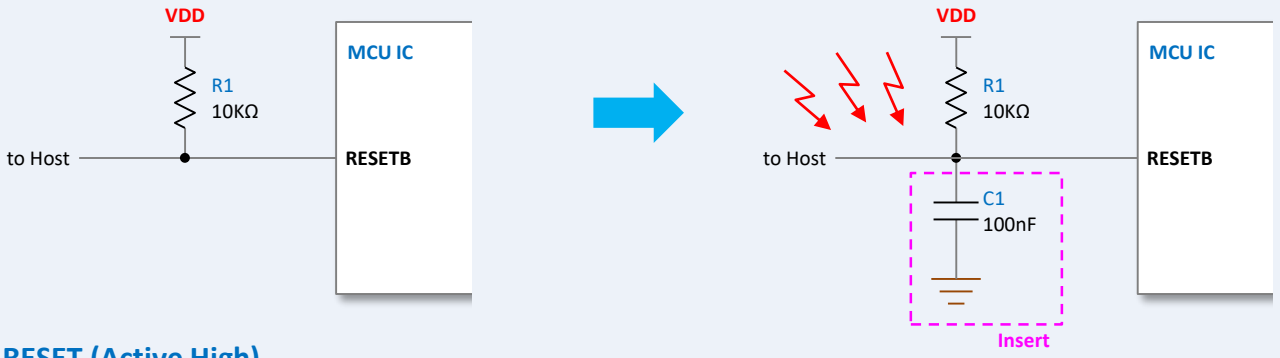
3. Reset Pin

Filters used on a Reset Pin

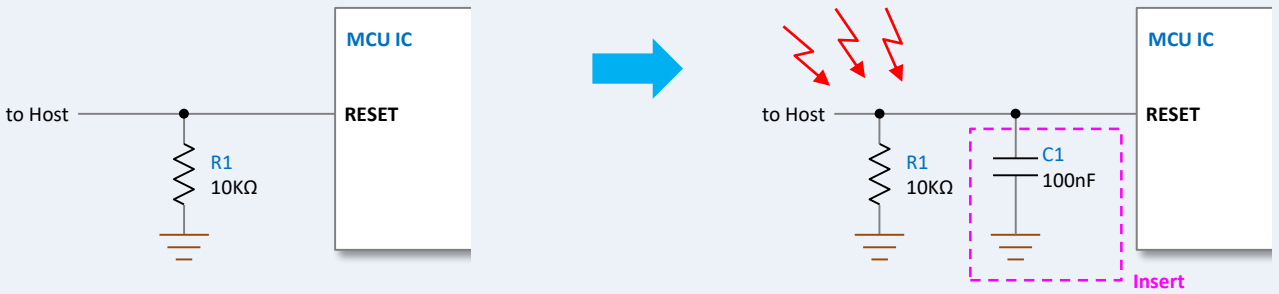
- Regardless of whether to use a Reset pin, Resistors and Capacitors must be placed at a Reset pin for stability.
- A circuit must be carefully selected depending on Reset pin characteristics.

Item	Component	Value
Pull-up/down Resistor	R1	10KΩ
Filter Capacitor	C1	Typ. 100nF (0.1uF, Example)

1. RESETB (Active Low)



2. RESET (Active High)

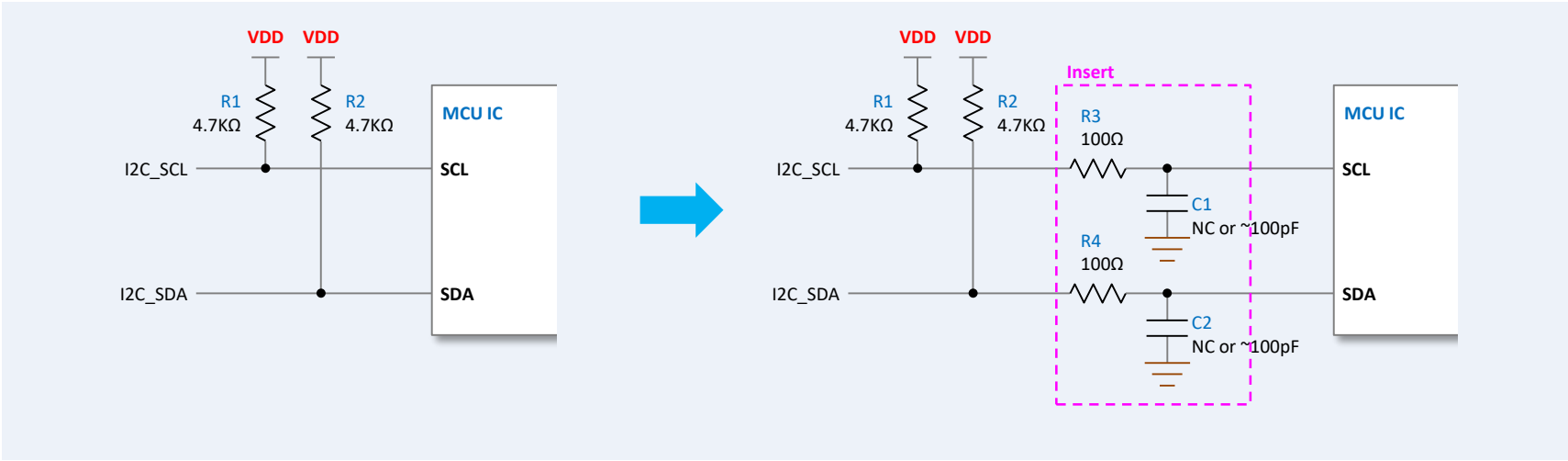


4. I2C Lines

Filters used on I2C Lines

- Pull-up Resistors, Series Resistors, and Filter Capacitors are available for use of the filters.
- Ordering of the sequence of the filter parts is critical to performance.
  → A Series Resistor reduces noise and a Filter Capacitor bypasses the noise to GND.
- Filter (R1~R4, C1, C2) parts must be placed close to a Host (IC) or a Connector (within 30mm) rather than to an MCU.
- The same guideline is applied to SPI Lines.

Item	Component	Value
Pull-up Resistor	R1, R2	4.7KΩ ~ 10KΩ
Series Resistor	R3, R4	100Ω ~ 330Ω
Filter Capacitor	C1, C2	NC or ~100pF

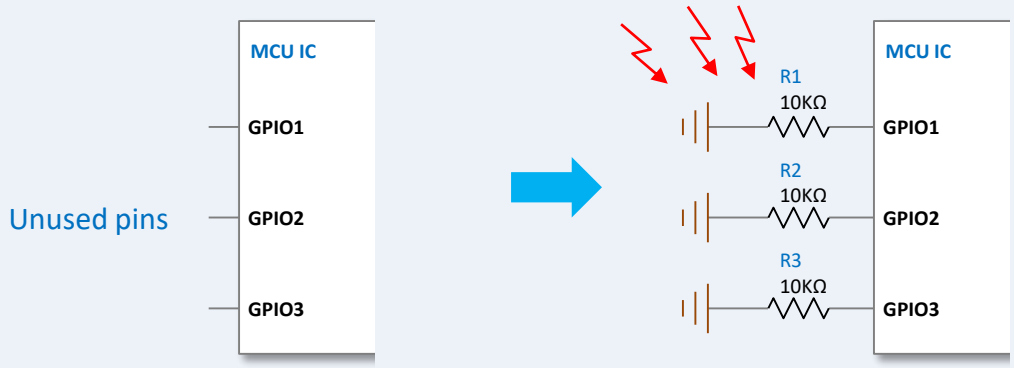


5. Unused Pins

Filters used on Unused Pins

- Terminate unused pins by connecting Pull-down Resistors. This improves Noise Immunity.
- Resistors should be placed close to an MCU (within 20mm).

Item	Component	Value
Pull-down Resistor	R1	1KΩ ~ 10KΩ



- NC pins must be set as a Push-pull Output Low or an Input and Pull-up (Internal).

6. Power Lines

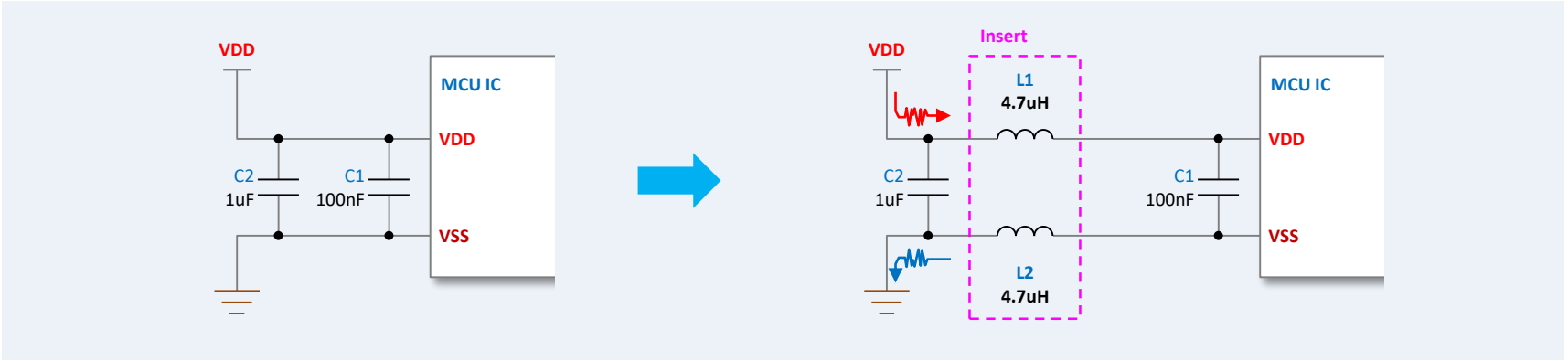
Filter Circuit for Power Lines

- Filters on power lines enhance performance of the boards that failed tests.

Filters used on an MCU Power Input

- Filter (L1, L2) parts must be placed close to noise sources (e.g. within 30mm of the Connector) rather than to an MCU.

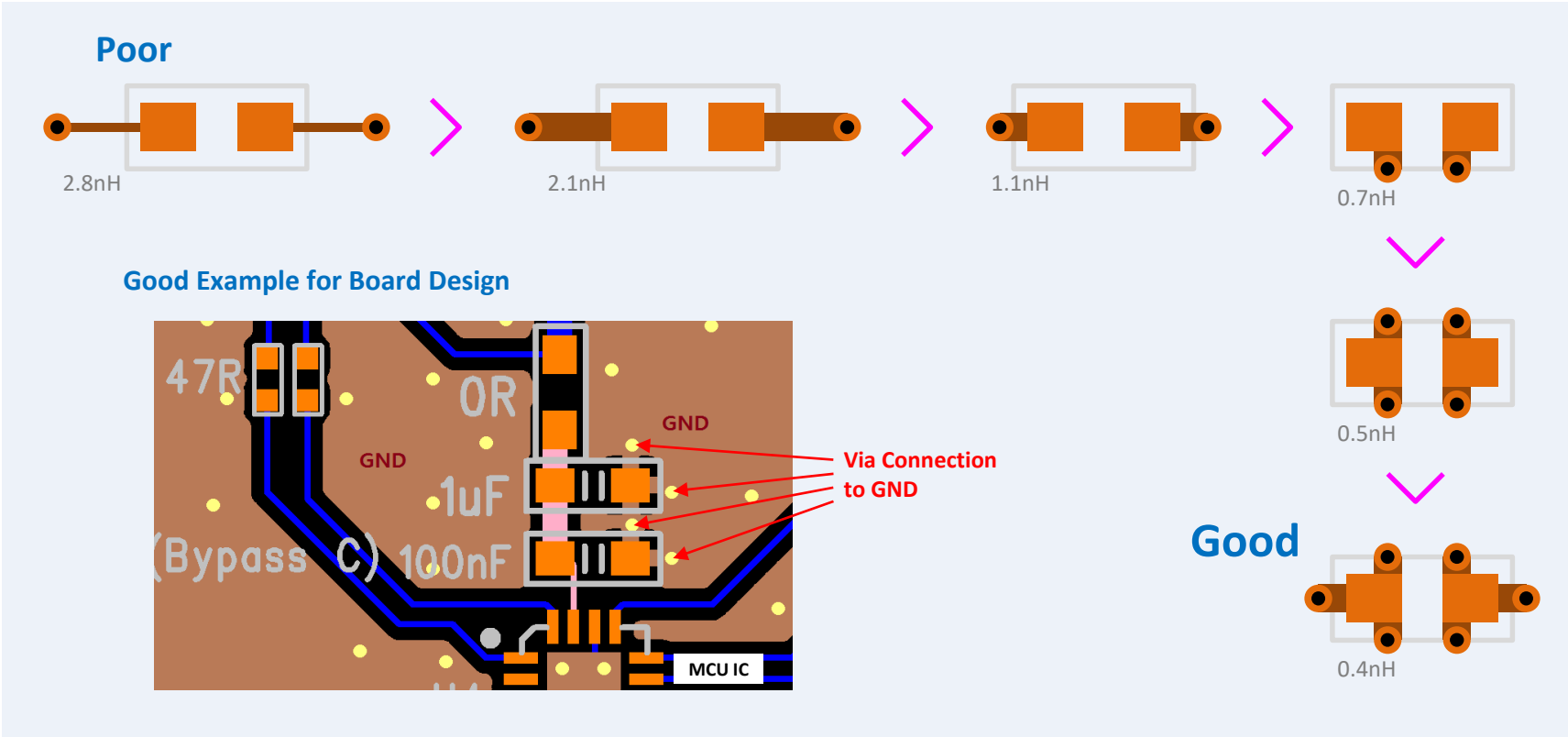
Item	Component	Value
Decoupling Capacitor	C1	10nF (0.01uF) ~ 100nF (0.1uF)
	C2	1uF
Series Inductor	L1, L2	Typ. 4.7uH



7. Via Connection (1 of 3)

Case 1: Via Connection to Power/Ground(GND) Plane.

1. Use a Via to connect a Bypass & Filter Capacitor to Power or GND of other layer when designing a circuit board.
2. At this point, traces connecting the Capacitor through the Via form a single Inductance value.
3. The bigger the Inductance value (unwanted) is, the more external noise affects.
4. Therefore, by widening the trace width while using multiple Vias, the Inductance value becomes smaller and filtered noise can pass to GND easily.

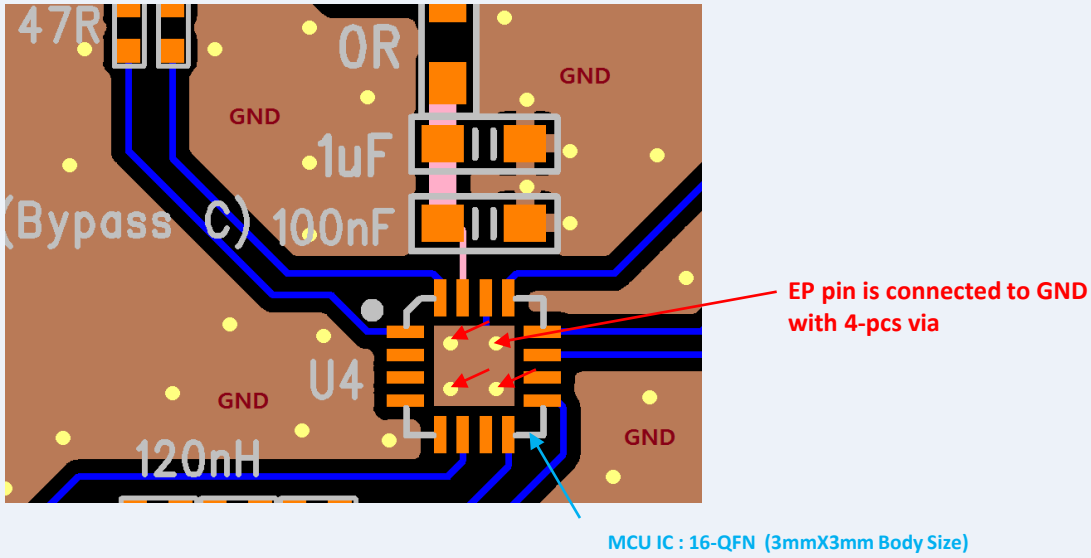


7. Via Connection (2 of 3)

Case 2: Via Connection to EP (Exposed Pad) of an MCU

- Packages such as QFN have Exposed Pads (Bottom Pads) on a device. These pads normally connect to GND.
- Place as many Vias as possible on an EP pin.
  e.g. For 16-pin QFN (3mm X 3mm), place at least 2 Vias within an EP.

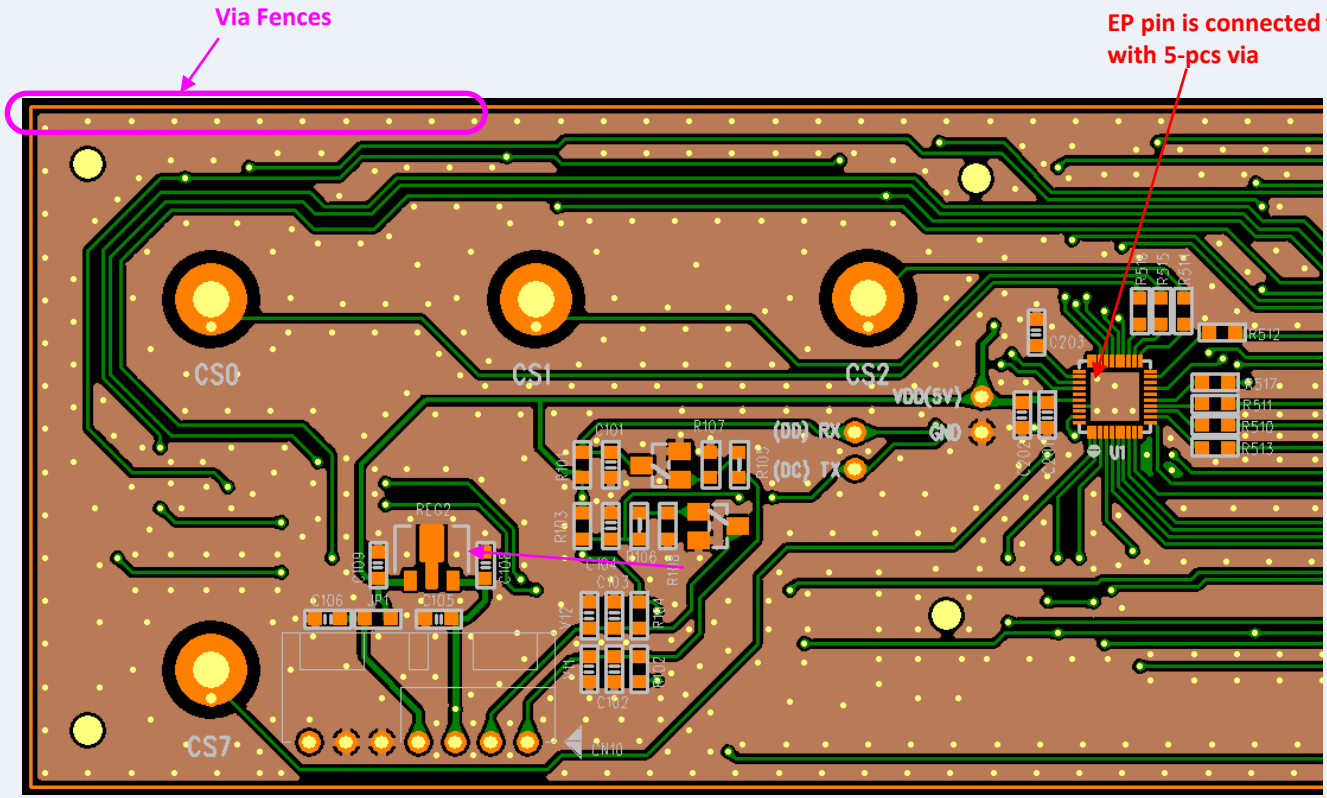
Good Example for Board Design



7. Via Connection (3 of 3)

Case 3: Via Fences

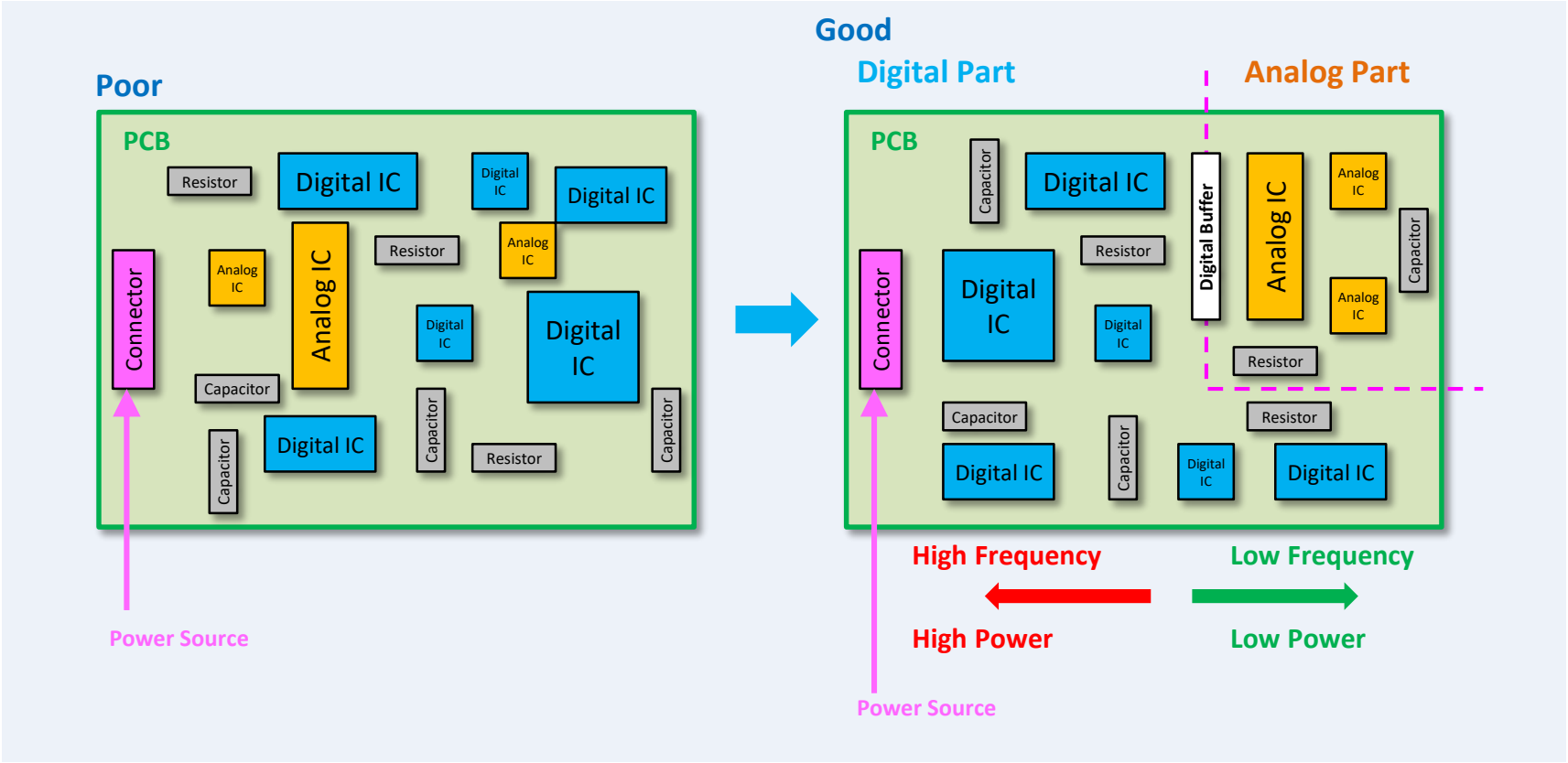
1. Place GND Vias in fixed intervals on boundaries of a board (Typ. 5mm Pitch).
2. Place GND Vias in fixed intervals on internal GND pattern too.
3. External Noise and EMI emission effects can be reduced by executing steps 1 and 2.



8. Component Placement

Component Placement Guidelines

1. A reference point is the location where power is supplied (‘Connector’ in figures below).
2. Classify parts into digital and analog. Place a digital part consuming the most power and having the highest operation frequency closest to the ‘Connector’.
3. If an analog part is placed closest to the ‘Connector’ instead, high frequency and large current will pass through the analog part and affect the performance.

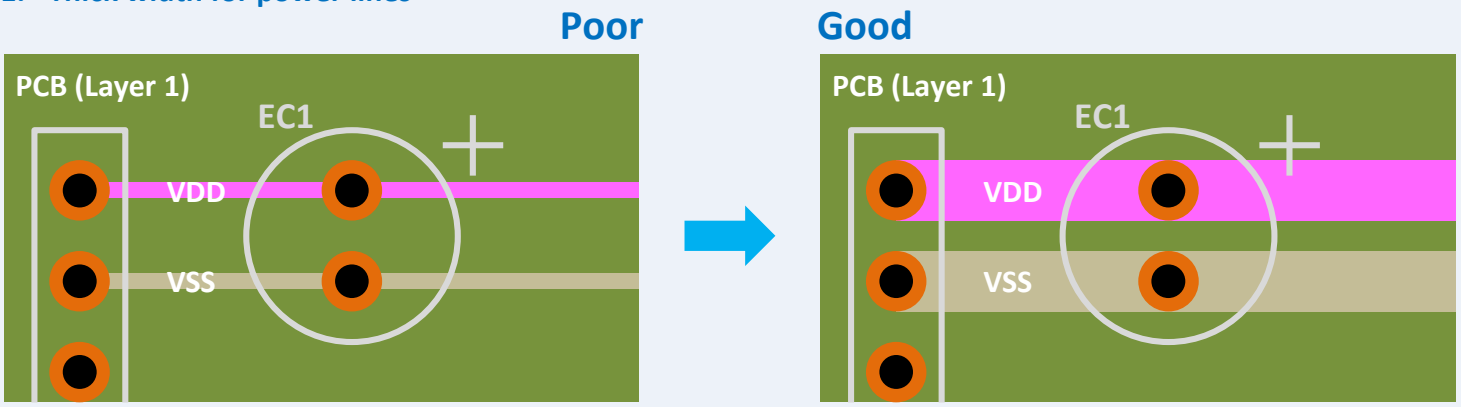


9. Power Line Routing (1 of 4)

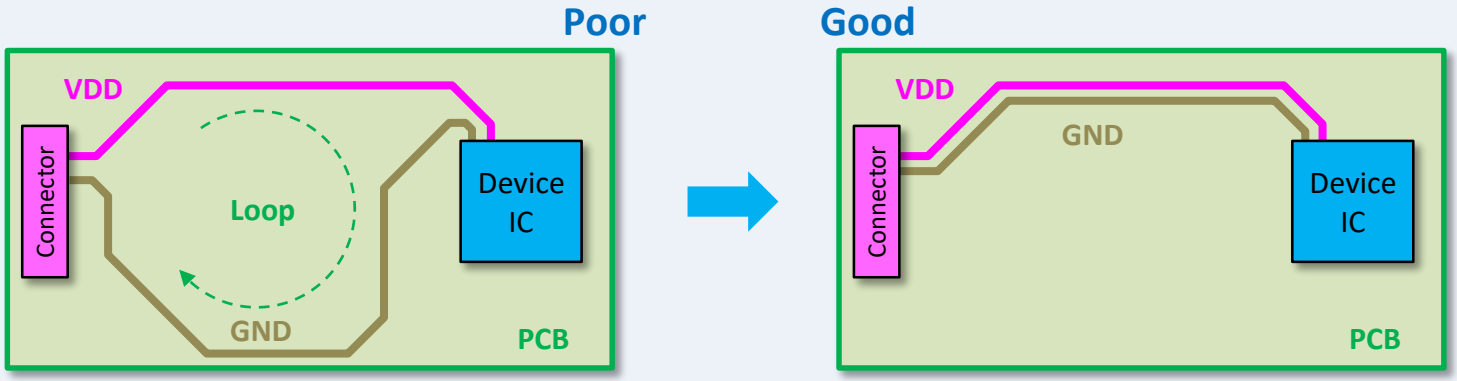
Case 1: Basic Tracing for Power Lines (VDD & GND)

- Trace wide in parallel without jumpers (Recommend filling GND with copper pattern).
- VDD and GND power lines must be placed in vicinity and in parallel. Minimize the surface area of a loop that VDD and GND created.

1. Thick width for power lines



2. Minimized loop size for power lines

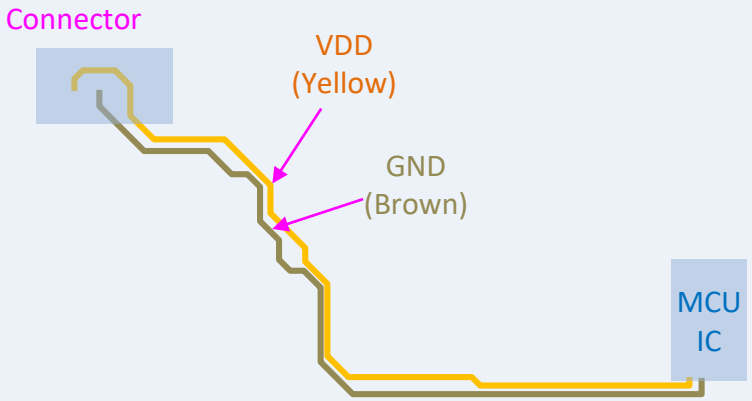


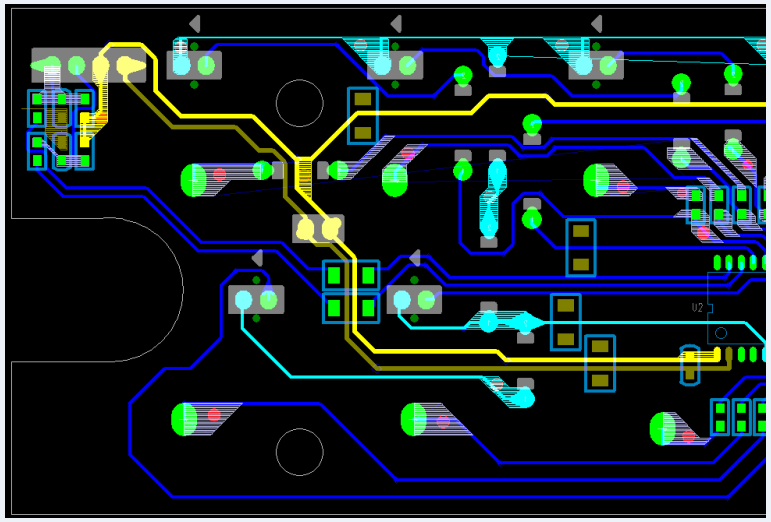
9. Power Line Routing (2 of 4)

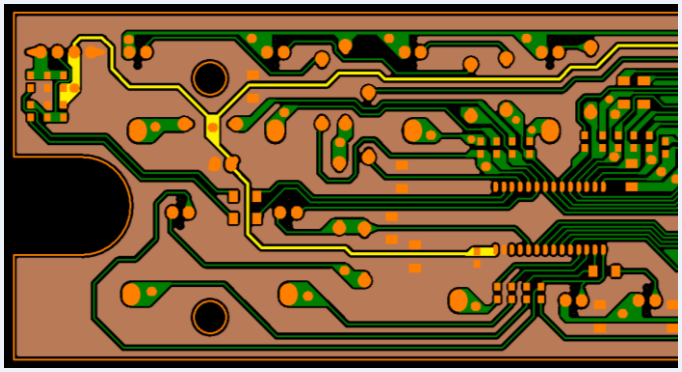
Case 1 (continued): Basic Tracing for Power Lines (VDD & GND)

- Example: Single-layer Board Design

1. Power Lines (VDD & GND) traced in parallel without jumpers





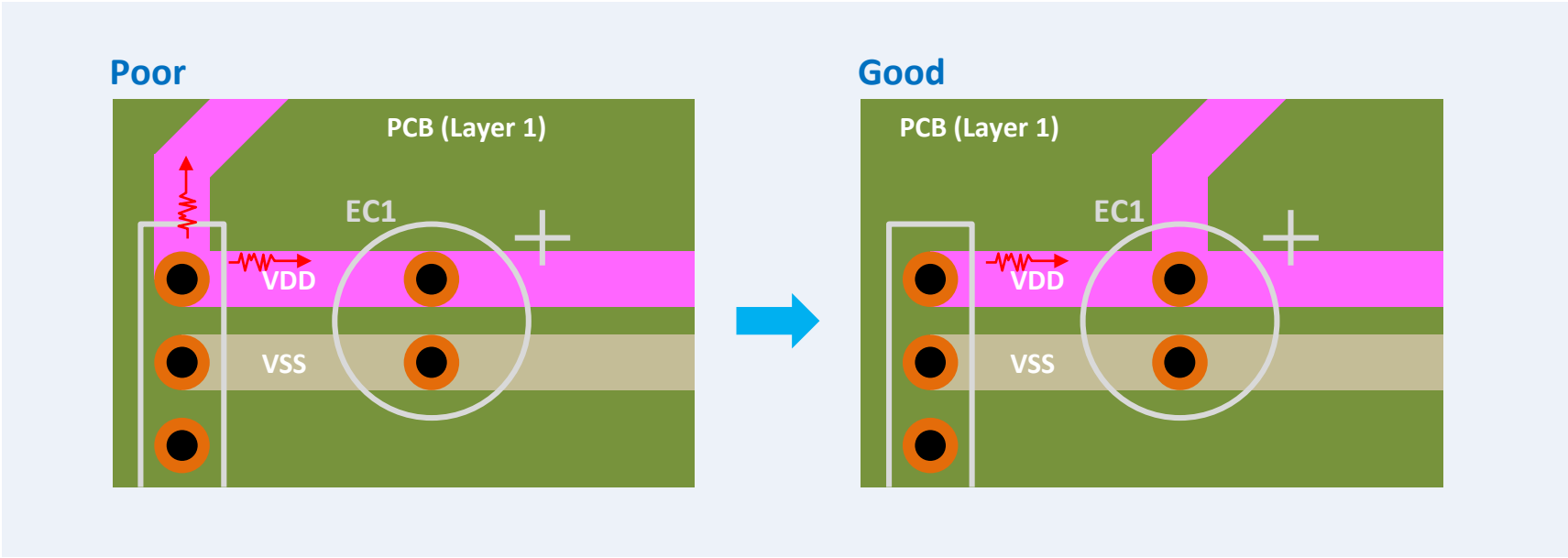


2. GND Copper Pattern is filled (poured).

9. Power Line Routing (3 of 4)

Case 2: When Power Lines are Separately Traced at Multiple Locations

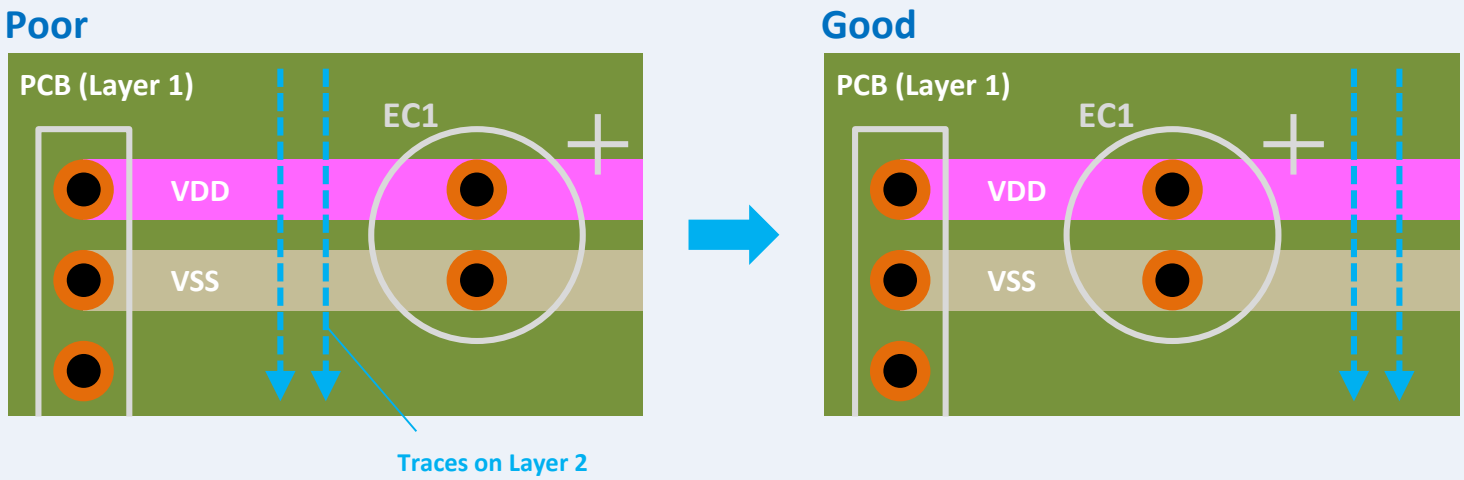
- Power Lines must be filtered first and then divided.
- In a figure of Poor Case shown below, tracing without EC1 (Filter Capacitor) is not filtered sufficiently and can be affected by external noise flowing into the power line.



9. Power Line Routing (4 of 4)

Case 3: When Traces Overlap with Power Lines

- Traces should not overlap with any parts if possible. However, in case of overlap with Power Lines, it must be filtered before the overlap.
- In a figure of Poor Case shown below, when signal traces overlap with unfiltered power lines, they can be affected by external noise flowing into the power line.
- Overlapping traces not only account for Power Lines but also Communication Lines.

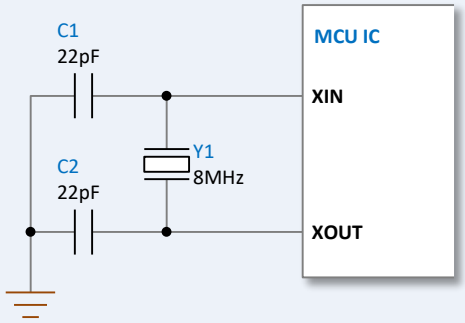


10. External Clock (1 of 2)

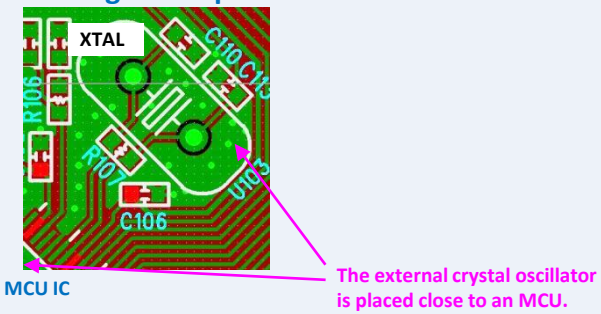
Guideline 1: GND Shielding

- In case of using an External Clock Source (Crystal Oscillator or Ceramic Resonator)
- Form GND Shielding (Ground Guard) pattern around the Clock Source GND Shielding (Ground Guard).
  - It minimizes EMI Emission, and in turn minimizes external noise effect.
  - Clock Source GND pin and MCU GND pin should be connected properly. If a different GND on an other layer is connected, the connection will be used as an inflow route of external noise and unwanted oscillation and offset can be generated by the external noise.

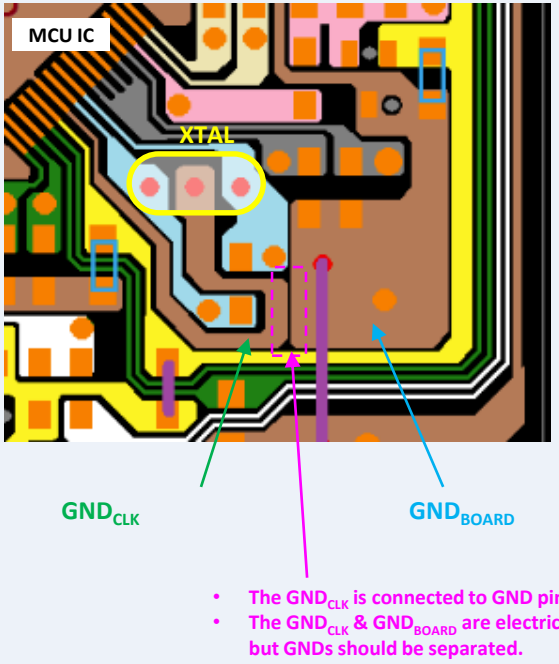
1. Basic Schematic Diagram



2. Board Design: Component Placement



3. Board Design: GND Pattern (Single-layer Board)

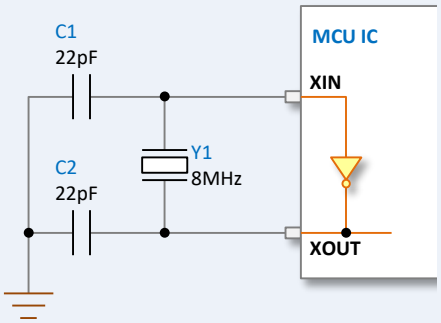


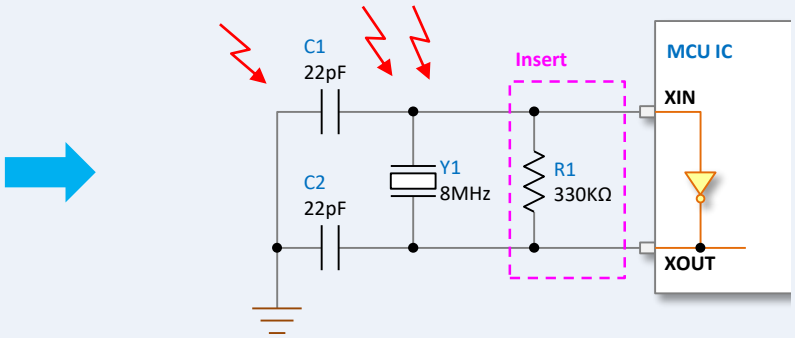
10. External Clock (2 of 2)

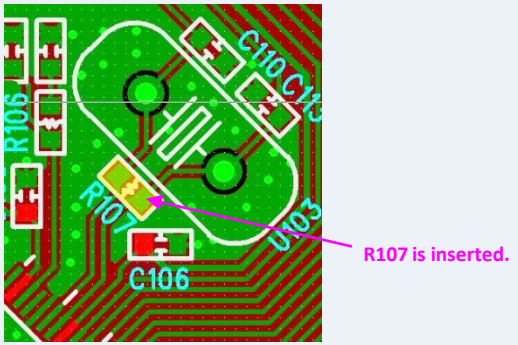
Guideline 2: Increase Current to Reduce External Noise

- If a noise issue related to the XTAL pin is not resolved, the following method may help.
  - Add a resistor between XIN pin and XOUT pin to reduce resistance on the Oscillator Feedback.

Item	Component	Value
External Feedback Resistor	R1	330KΩ ~ 750KΩ



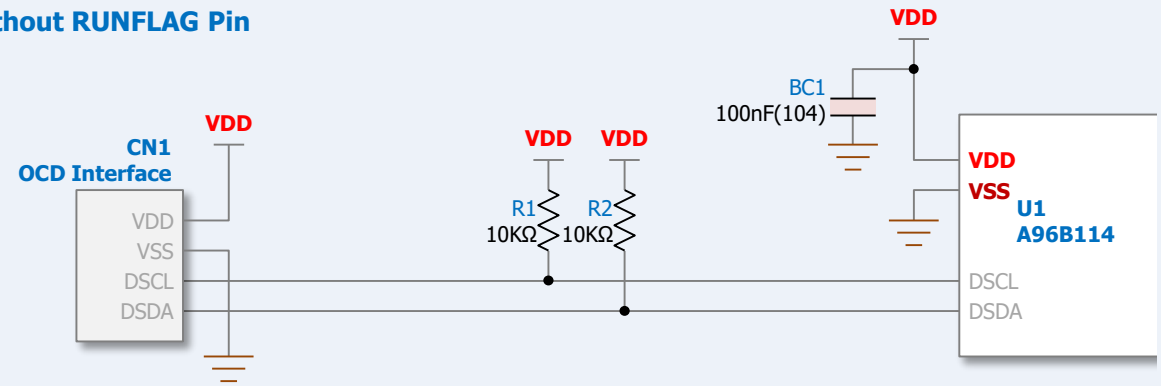




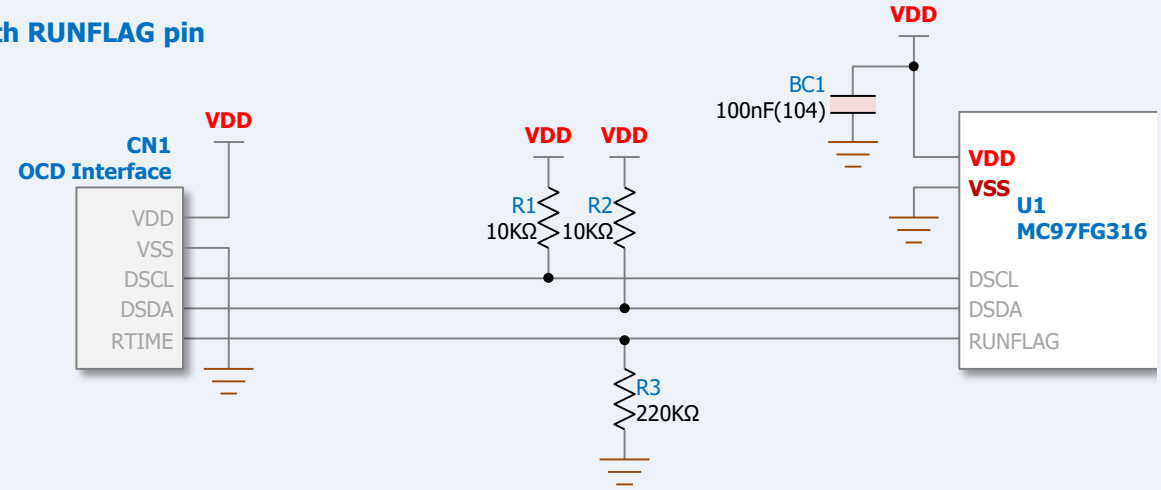
11. Debugging Interface (1 of 5) – OCD 8bit MCU

Guideline 1: OCD/OCD II (On-chip Debugger) Interface

1. In case, without RUNFLAG Pin



2. In case, with RUNFLAG pin



- A 220KΩ pull-down resistor must be placed on the RUNFLAG pin.
- The RUNFLAG has an internal pull-down resistor (typ. 20KΩ @ 5V).
- This is the reason that RUNFLAG pin must be set to Low during User Code operation.

11. Debugging Interface (2 of 5) – JTAG 32bit MCU

Guideline 2: JTAG Interface

- JTAG interface is used for firmware update or debugging.
- When using the JTAG interface, a pull-up/pull-down resistor must follow the specification shown in a table below:

	nTRST	TDI	TMS	TCK	TDO	BOOT
AC33M4064	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 1MΩ	Pull-up 10KΩ
AC33M8128	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 1MΩ	Pull-up 10KΩ
A33G526	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 1MΩ	Pull-down 10KΩ

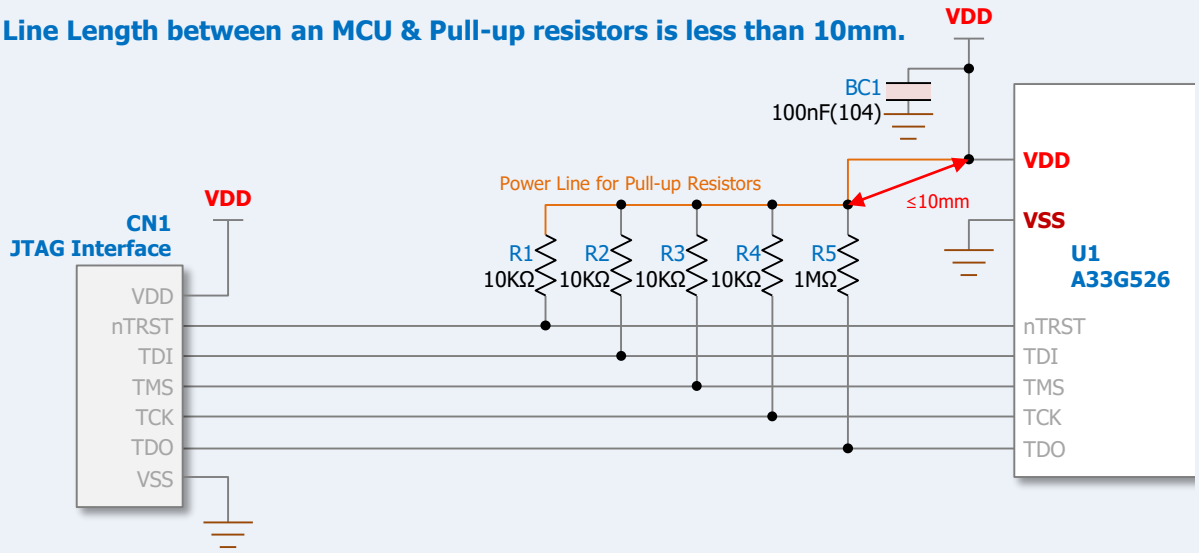
- Even after development stage, if the JTAG pins are left in unconnected state, they can be affected by external noise. For this reason, the pull-up resistors and the pull-down resistors are required in production boards.
- As a reference, a device supporting both JTAG interface and SWD interface is introduced:
  - The device's interface that is not used under the development state can be set to NC.
  - Because the firmware can fix it to Output Low or Output High.
- Resistors should be placed close to the JTAG pins (within 10mm).
- Pull-up resistor power must be connected to MCU's VDD power.
- If power connection of the pull-up resistor is far from MCU's VDD power (over 10mm), add a bypass capacitor of 0.1uF between MCU's VDD pin and GND. In addition, the bypass capacitor's GND pin and the MCU's GND pin must be connected very well.

NOTE: When nTRST pin is connected to GND (using a 0Ω Resistor), the JTAG is disabled.

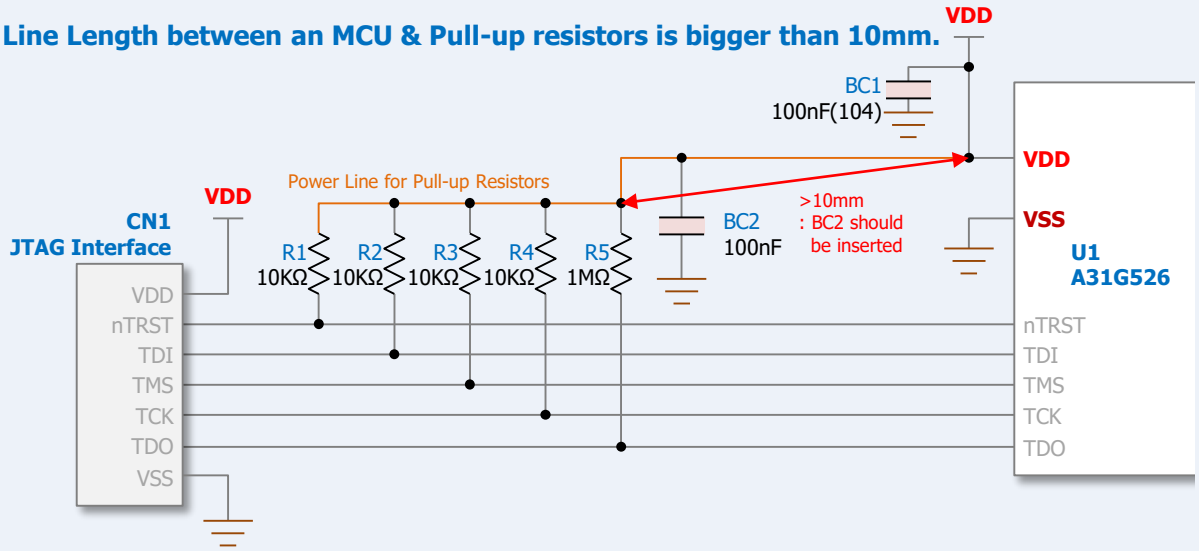
11. Debugging Interface (3 of 5) – JTAG 32bit MCU

Guideline 2 (continued): JTAG Interface - Example (A33G526)

1. Power Line Length between an MCU & Pull-up resistors is less than 10mm.



2. Power Line Length between an MCU & Pull-up resistors is bigger than 10mm.



11. Debugging Interface (4 of 5) – SWD 32bit MCU

Guideline 3: SWD (Serial Wire Debugger) Interface

- SWD Interface is used for firmware update or debugging.
- When using the SWD interface, a pull-up/pull-down resistor must follow the specification shown in a table below:

	SWDIO	SWCLK	nRESET	BOOT
AC30M1x64	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
AC33Mx064	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
AC33Mx128	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
A31G11x	Pull-up 10KΩ	Pull-down 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
A31G12x	Pull-up 10KΩ	Pull-down 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
A31G213	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
A31G314	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-up 10KΩ
A33G526	Pull-up 10KΩ	Pull-up 10KΩ	Pull-up 10KΩ with Shunt C	Pull-down 10KΩ

- Even after development stage, if the SWD pins are left in unconnected state, they can be affected by external noise. For this reason, the pull-up resistors and the pull-down resistors are required in production boards.

11. Debugging Interface (4 of 5) – SWD 32bit MCU

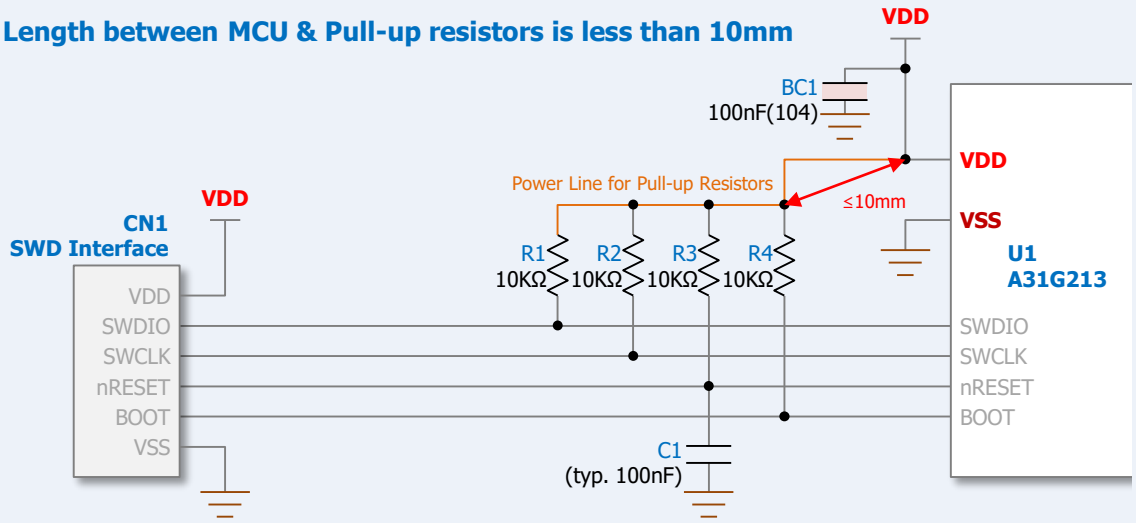
Guideline 3 (continued): SWD (Serial Wire Debugger) Interface

- As a reference, a device supporting both JTAG interface and SWD interface is introduced:
  - The device's interface that is not used under the development state can be set to NC.
  - Because the firmware can fix it to Output Low or Output High.
- Resistors should be placed close to the SWD pins (within 10mm).
- Pull-up resistor power must be connected to MCU's VDD power.
- If the power connection of the pull-up resistor is far from MCU's VDD power (over 10mm), add a bypass capacitor of 0.1uF between MCU's VDD pin and GND. In addition, the capacitor's GND and the MCU's GND pin must be connected very well.
- Pull-up Resistor of 10KΩ and Shunt Capacitor (typical 0.1uF) must be placed on nRESET pin.

11. Debugging Interface (5 of 5) – SWD 32bit MCU

Guideline 3 (continued): SWD (Serial Wire Debugger) Interface - Example (A31G213)

1. Power Line Length between MCU & Pull-up resistors is less than 10mm



2. Power Line Length between MCU & Pull-up resistors is bigger than 10mm