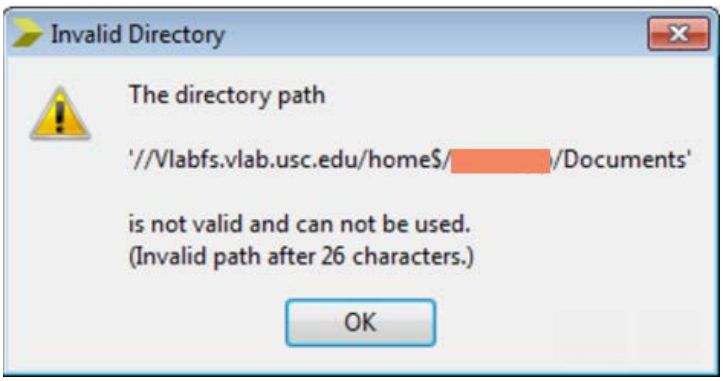
4/7/2017, 3/1/2020

Picoblaze Demo

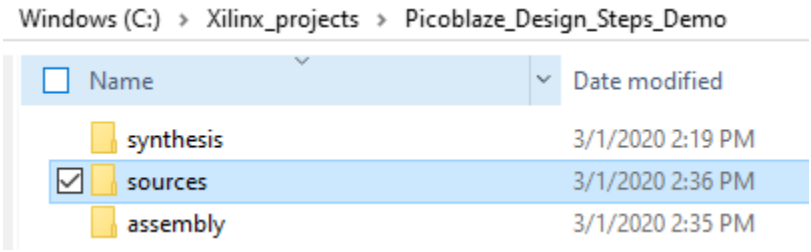
1. If you have not created a Xilinx_project folder under C:\, please create one.
C:\Xilinx_projects\

This folder path should not contain spaces. Though Windows has the bad habit of creating folder and file names with spaces, no CAD tool designer likes or supports such names.

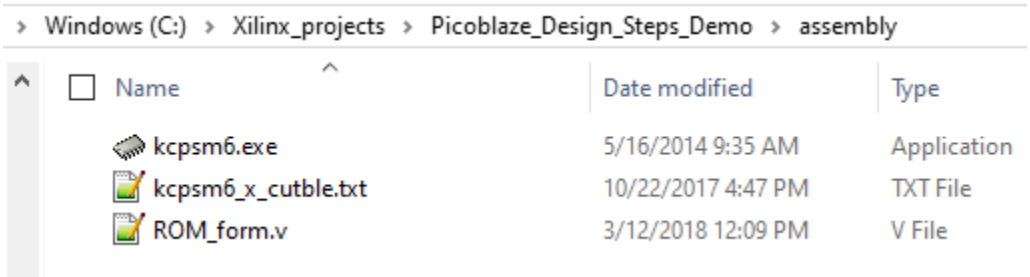
If you are using VDI, do not create your directory under the VDI-suggested Documents folder (or the desktop) as it has a weird network folder path and you get an error like the one below.



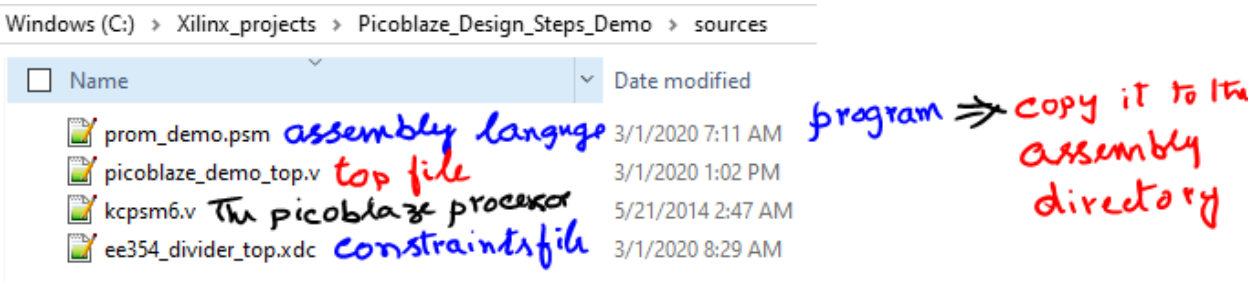
2. Create a demo folder with three subfolders under this
C:\Xilinx_projects\Picoblaze_Design_Steps_Demo



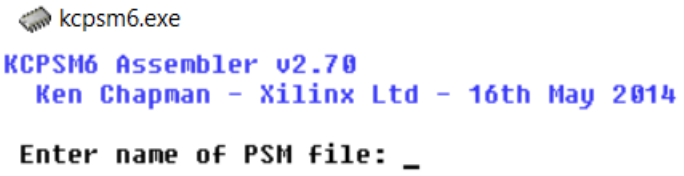
3. Gather the assembler executable (kcpsm6.exe) and the assembler format file given to you (ROM_form.v) under the assembly subdirectory.

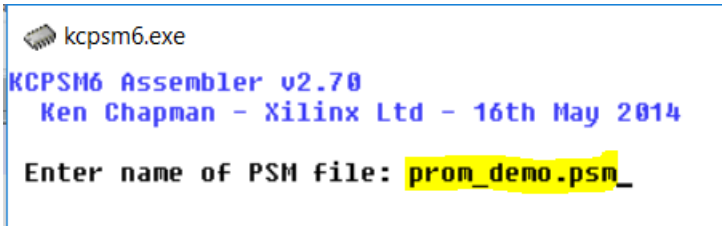


3.1 Create your assembly program (.psm file) by editing a similar file given to you. Keep a copy under sources subdirectory and also under the assembly subdirectory.
The sources directory also consists of the top file.



4. Go to the “assembly” subdirectory and invoke (double-click) the assembler executable (kcpsm6.exe) and provide to it your .psm file and the format file.

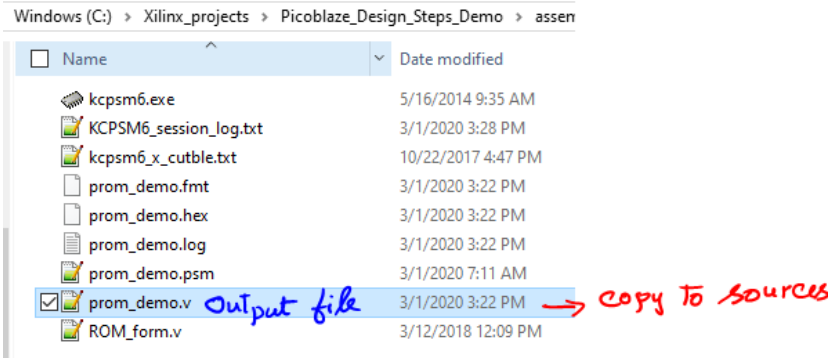




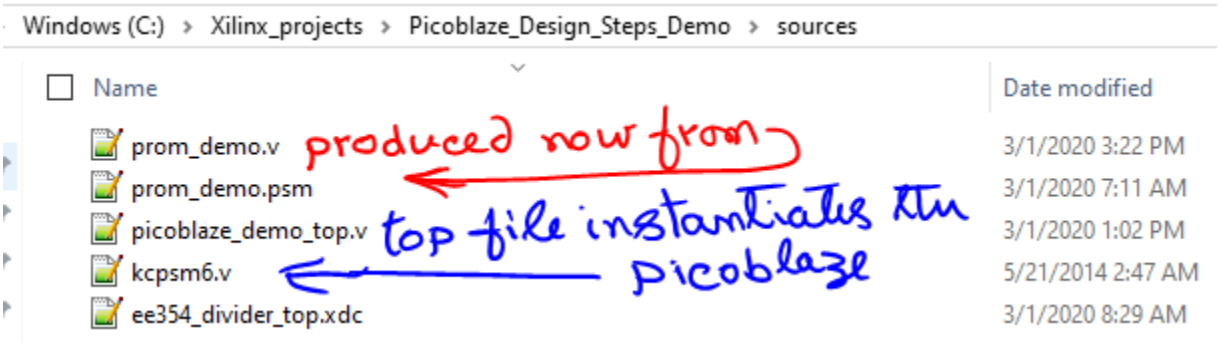
```
Enter name of PSM file: prom_demo.psm

Reading top level PSM file...
  C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\assembly\prom_demo.psm

A total of 36 lines of PSM code have been read

Checking line labels
Checking CONSTANT directives
Checking STRING directives
Checking TABLE directives
Checking instructions

Writing formatted PSM file...
  C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\assembly\prom_demo.fmt

Expanding text strings
Expanding tables
Resolving addresses and Assembling Instructions
  Last occupied address: 002 hex
  Nominal program memory size: 1K (1024)     address(9:0)
  Occupied memory locations: 3
  Assembly completed successfully

Writing LOG file...
  C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\assembly\prom_demo.log
Writing HEX file...
  C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\assembly\prom_demo.hex
Writing Verilog file...
  C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\assembly\prom_demo.v

KCPSM6 Options.....
         R - Repeat assembly with 'prom_demo.psm'
         N - Assemble new file.
         Q - Quit
```

Type “Q” to quit and look at the contents of your directory.

5. Note the highlighted parts. Since our programs are small, it assembles into a BRAM of 1K location (1K instructions) . It has produced an output file of prom_demo.v (name based on the fact that our assembly language program is named as prom_demo.psm.



6. copy prom_demo.v to source directory



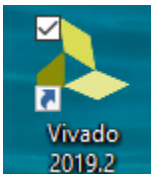
7. Create or use the given top file picoblaze_demo_top.v. Add the .xdc file with the needed pin definitions. Add the kcpsm6.v file (the picoblaze processor file) provided by Xilinx (which is provided by us to you via the demo zip file to the source subdirectory

The top file (here picoblaze_demo_top.v) contains the picoblaze soft processor instantiation.

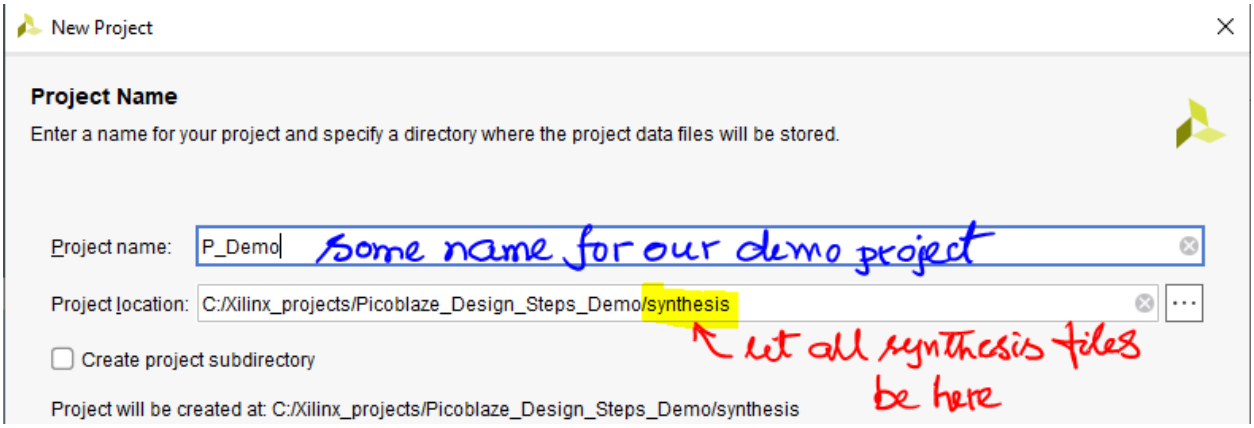
"7s" stands for the Xilinx 7-series FPGAs. Artix-7 is a 7-series FPGA.

```
prom_demo #(
  // .C_FAMILY          ("S6"),   // Nexys-3
  .C_FAMILY           ("7S"),      // Nexys-4
  .C_RAM_SIZE_KWORDS   (1),
  .C_JTAG_LOADER_ENABLE    (1))
  program_rom (
  .rdl               (rdl),
  .enable            (bram_enable),
  .address           (address),
  .instruction       (instruction),
  .clk               (board_clk));
```

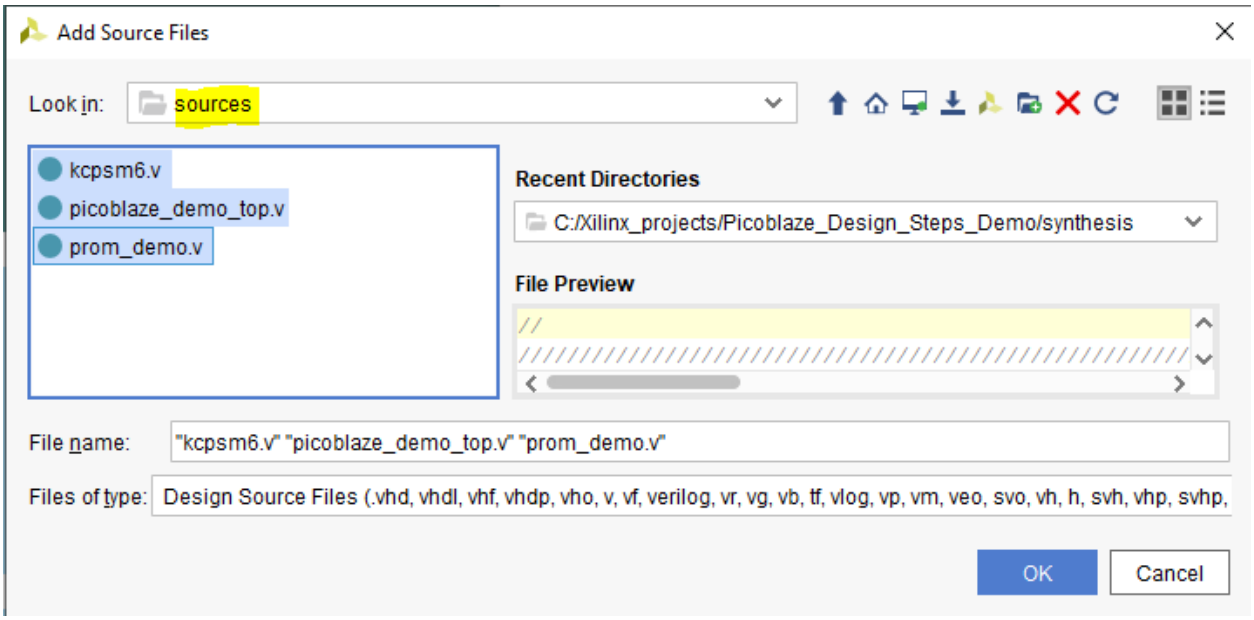
8. Invoke Vivado

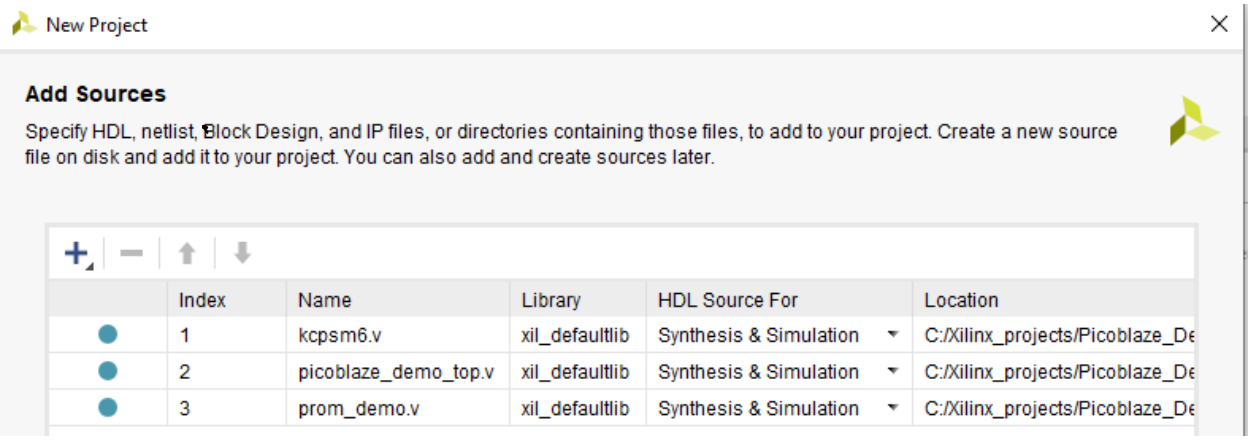


9. Setup the project (project properties, etc.)

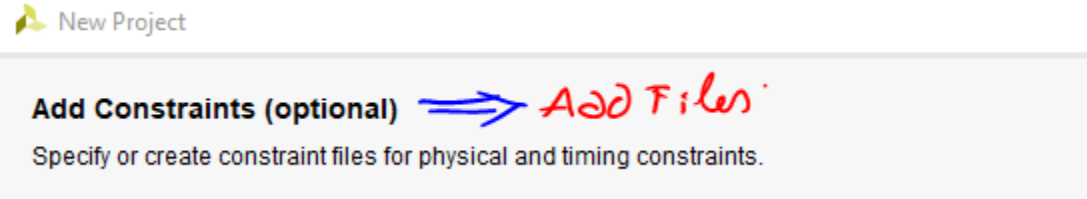


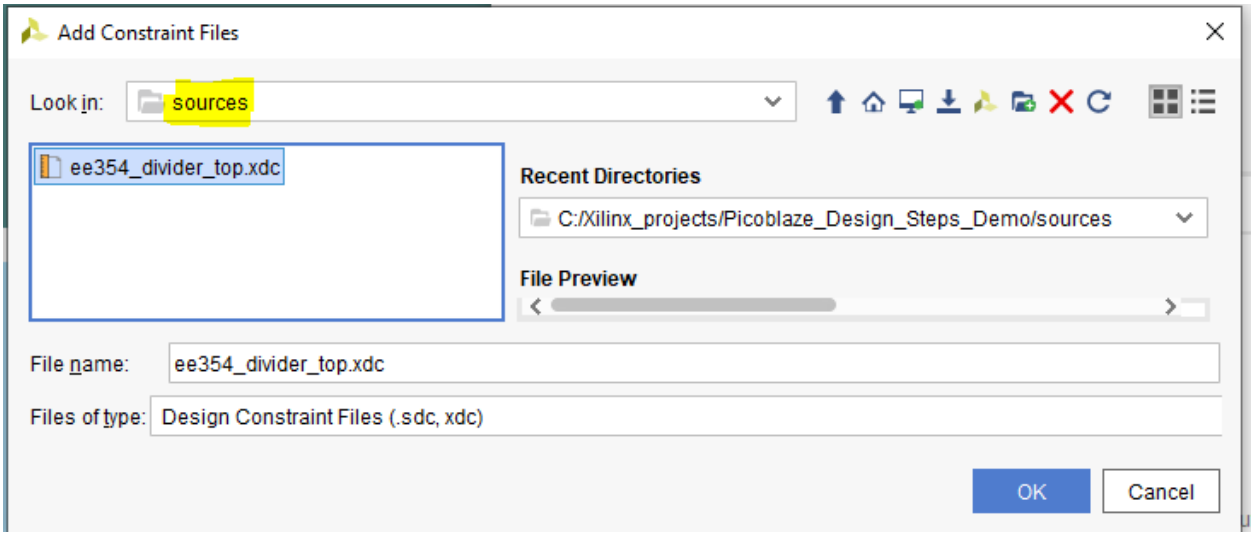
Add Sources => Add Files

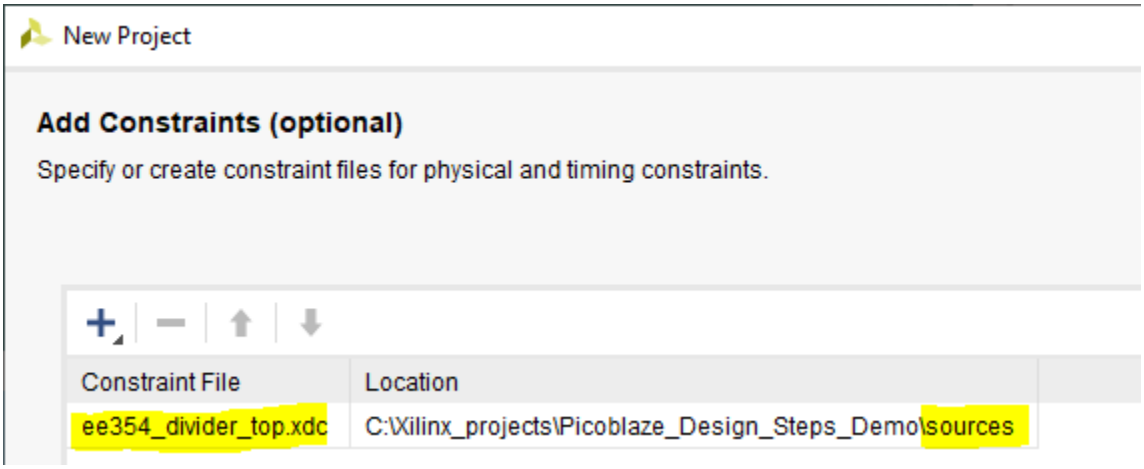



New Project
Add Sources
Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.
Index
Name
Library
HDL Source For
Location
1
kcpsm6.v
xil_defaultlib
Synthesis & Simulation
C:/Xilinx_projects/Picoblaze_De
2
picoblaze_demo_top.v
xil_defaultlib
Synthesis & Simulation
C:/Xilinx_projects/Picoblaze_De
3
prom_demo.v
xil_defaultlib
Synthesis & Simulation
C:/Xilinx_projects/Picoblaze_De

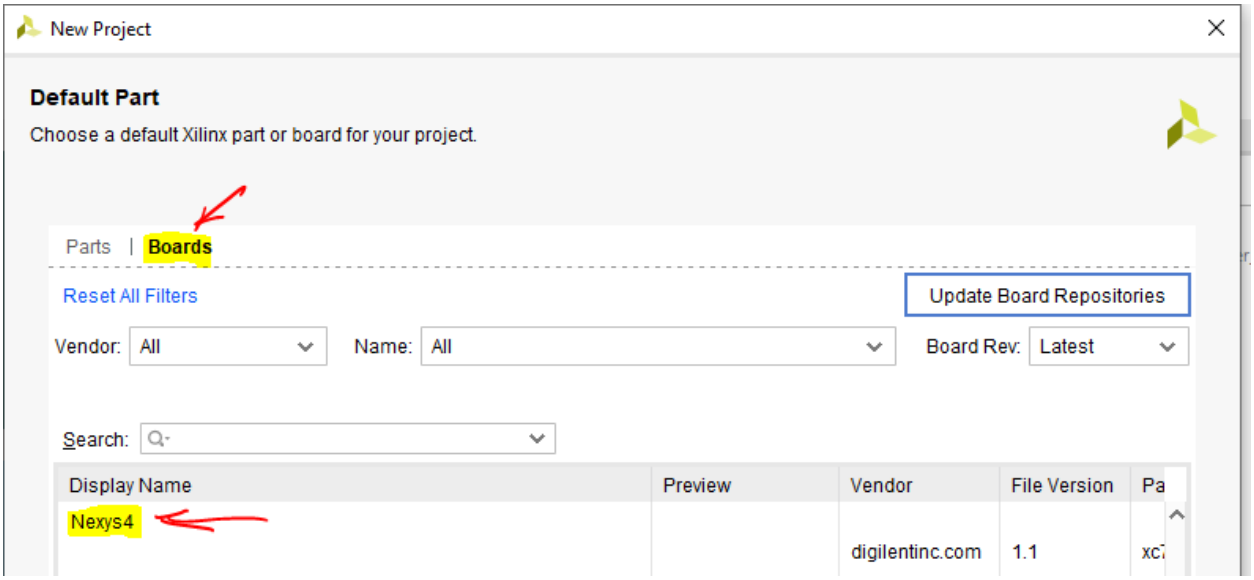
Next

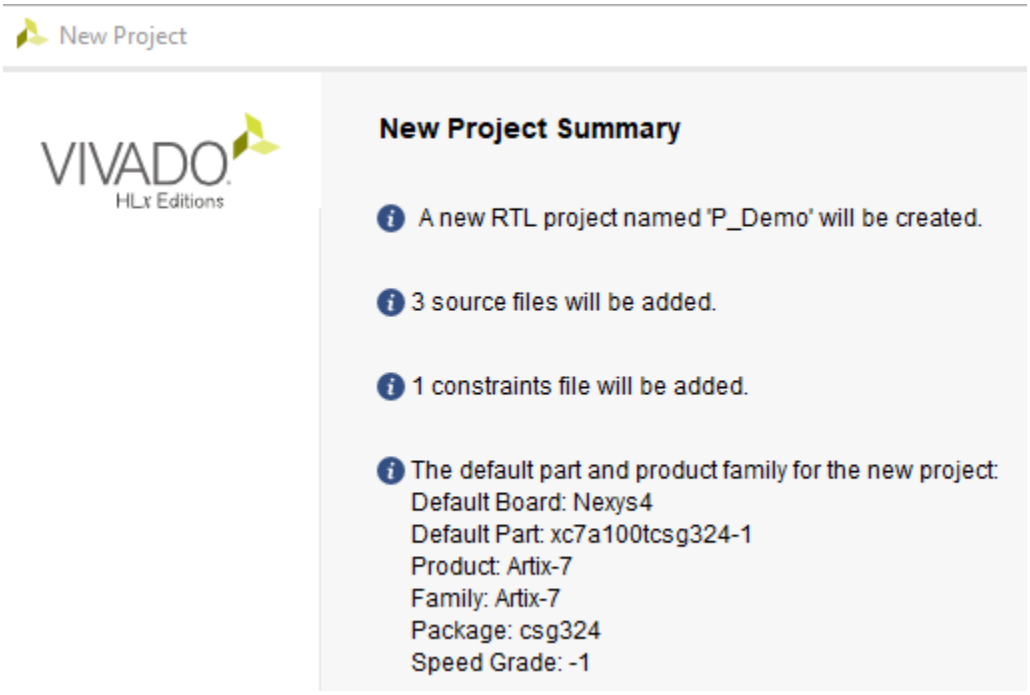

New Project
Add Constraints (optional)
Add Files
Specify or create constraint files for physical and timing constraints.


Add Constraint Files
Look in:
sources
ee354_divider_top.xdc
Recent Directories
C:/Xilinx_projects/Picoblaze_Design_Steps_Demo/sources
File Preview
File name:
ee354_divider_top.xdc
Files of type:
Design Constraint Files (.sdc, xdc)
OK
Cancel

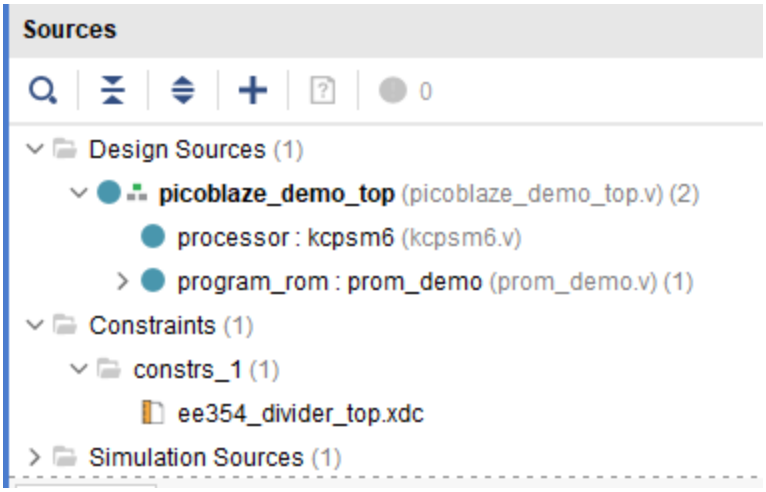

New Project
Add Constraints (optional)
Specify or create constraint files for physical and timing constraints.
Constraint File
Location
ee354_divider_top.xdc
C:\Xilinx_projects\Picoblaze_Design_Steps_Demo\sources

Next


New Project
Default Part
Choose a default Xilinx part or board for your project.
Parts | Boards
Reset All Filters
Update Board Repositories
Vendor: All
Name: All
Board Rev: Latest
Search:
Display Name
Preview
Vendor
File Version
Nexys4
digilentinc.com
1.1


New Project
VIVADO
HLx Editions
New Project Summary
A new RTL project named 'P_Demo' will be created.
3 source files will be added.
1 constraints file will be added.
The default part and product family for the new project:
Default Board: Nexys4
Default Part: xc7a100tcsg324-1
Product: Artix-7
Family: Artix-7
Package: csg324
Speed Grade: -1

Finish



10.

Run Synthesis

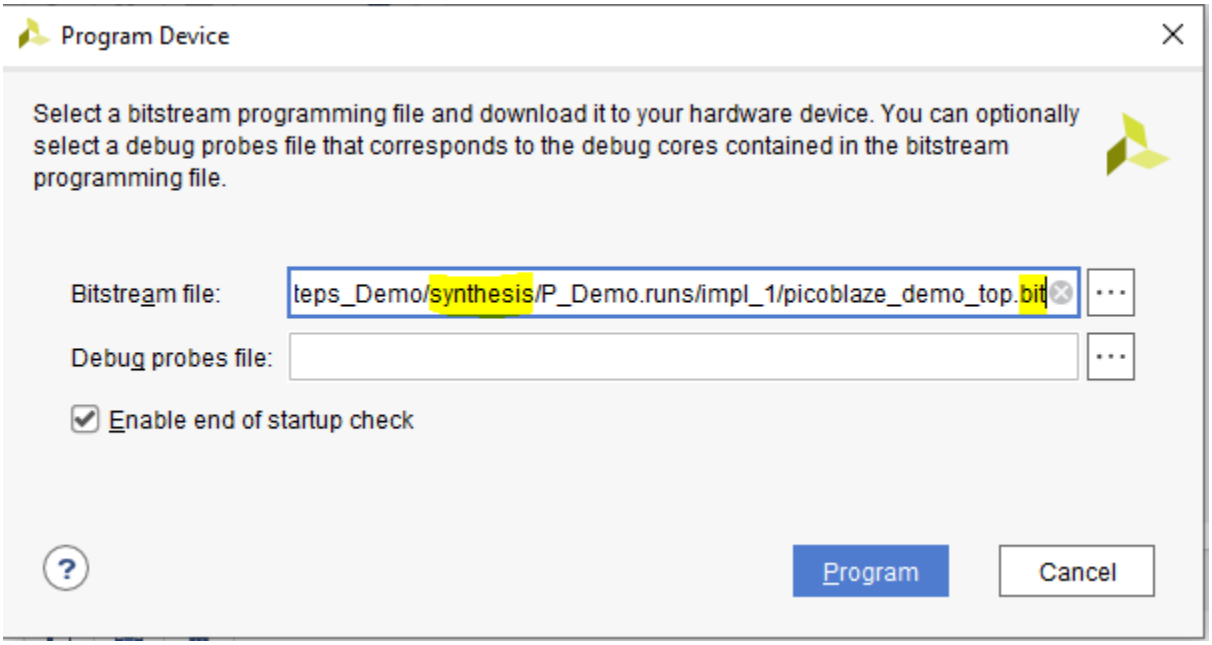
Run Implementation

Generate Bit stream

Open Hardware Manager

Open Target => Auto-connect

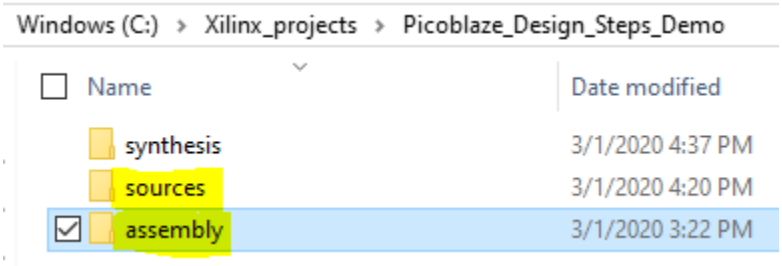
Program Device =>



Program

Verify on the board, that the 8 LEDs
{Ld7, Ld6, Ld5, Ld4, Ld3, Ld2, Ld1, Ld0}
follow the 8 switches
{Sw7, Sw6, Sw5, Sw4, Sw3, Sw2, Sw1, Sw0}

11. Notice directory structure, where we gather the source files under sources subdirectory, assembler related files under assembly subdirectory and synthesis-related files under synthesis subdirectory.



This facilitates carrying the sources files easily to another project. Actually, carry the sources subdirectory and the assembly subdirectory to another project as you need the assembler executable (kcpsm6.exe) and the ROM format file (ROM_form.v) for the next project.