CPE 322
Digital Hardware Design Fundamentals

Electrical and Computer Engineering
UAH

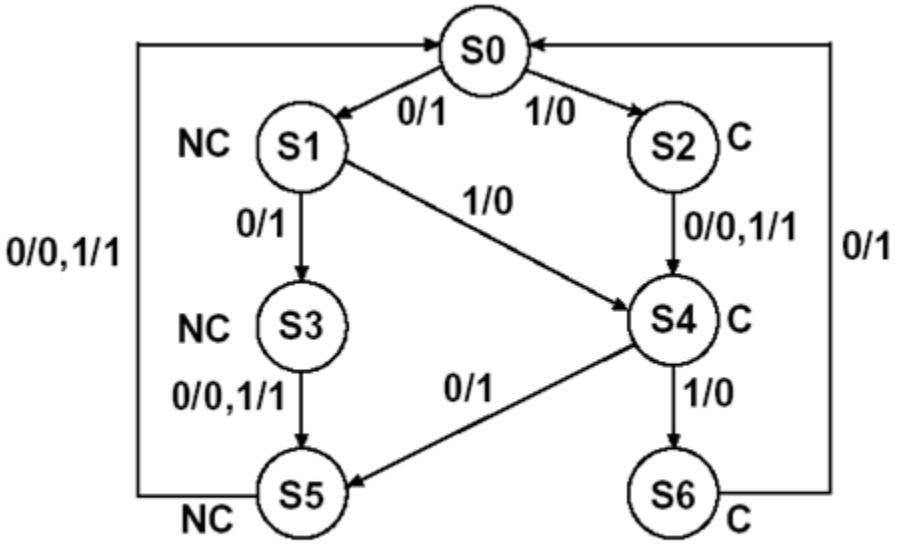
Extended State Graph Finite State Machine Representations

Extended State Graph

- Similarities to basic State (Transition) Graph
  - Nodes represent states
  - Arcs (or edges) represent transition between states
  - Labelling on arcs represent Inputs/Outputs on Mealy Machines
  - Labelling on arcs represent Inputs and labelling on nodes represent Outputs on Moore Machines
- Differences with basic State (Transition) Graph
  - To reduce Clutter
    - Only Inputs that impact a transition from one state to another are present on the graph – others are ignored.
    - Only Outputs that are TRUE (logic high) for a given transition are listed.

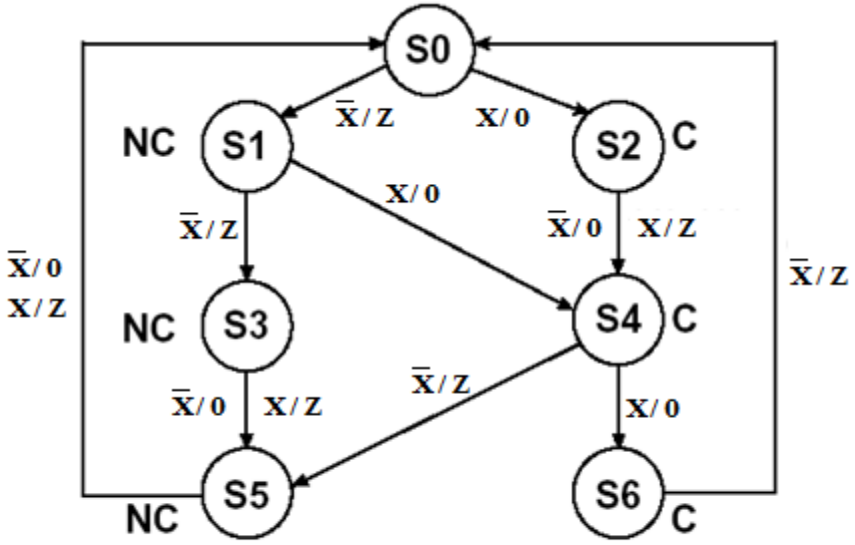
BCD to Excess 3 Mealy FSM Example

X/Z



Standard State Graph Notation

BCD to Excess 3 Mealy FSM Example



Extended State Graph Notation

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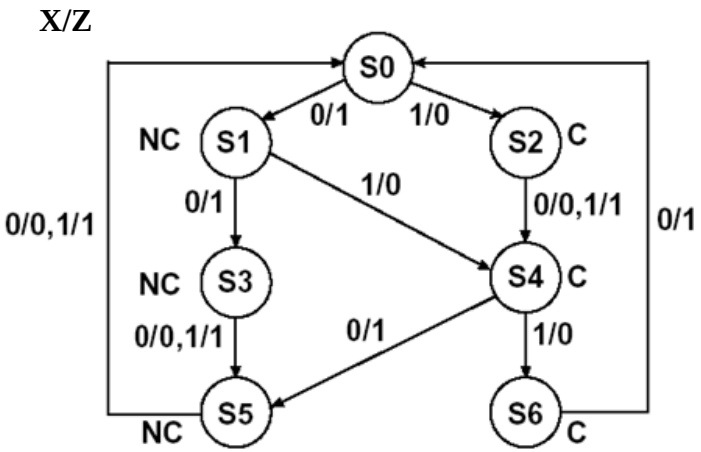
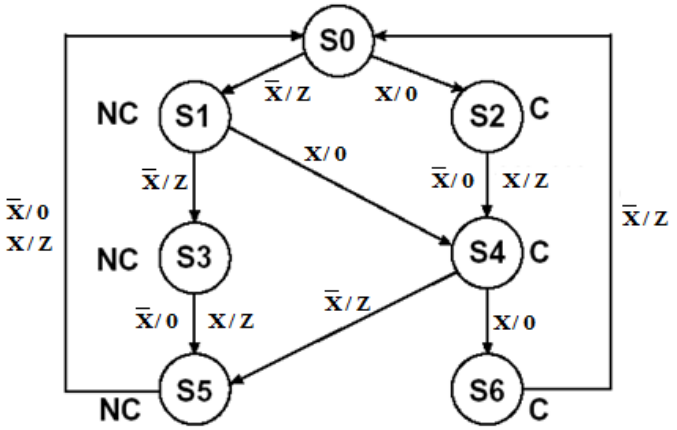
BCD to Excess 3 Mealy FSM Example

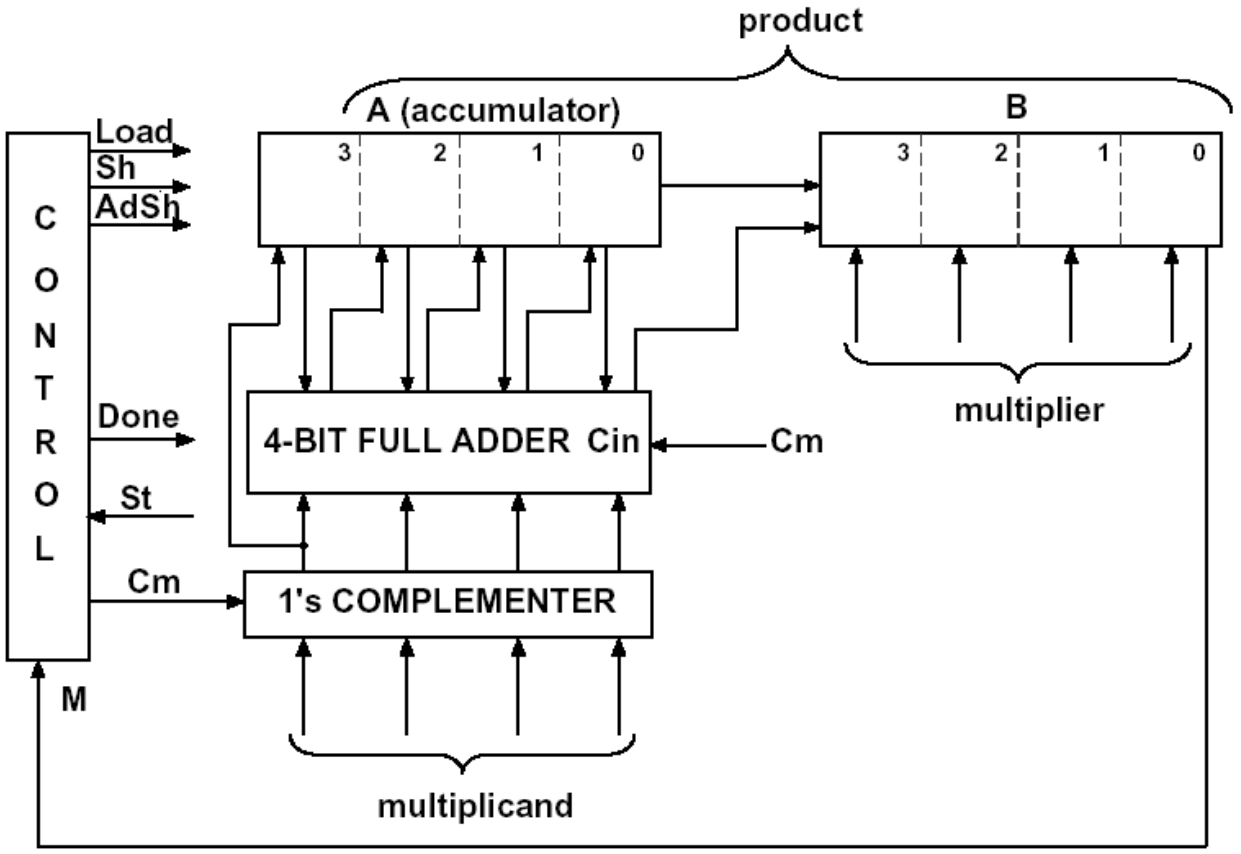


Standard State Graph Notation



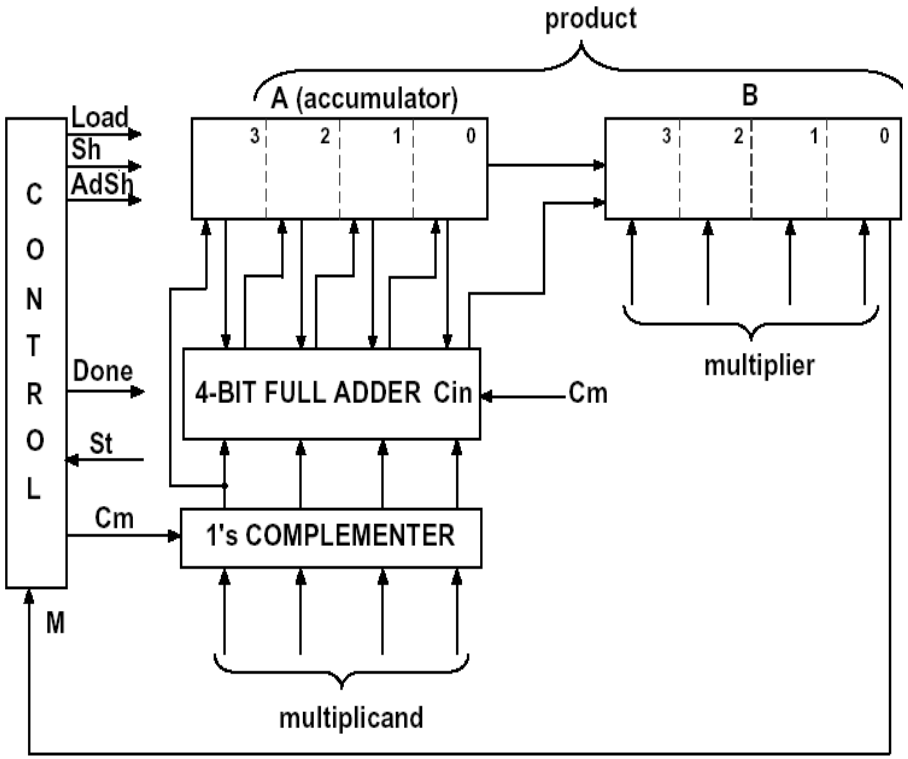
Extended State Graph Notation

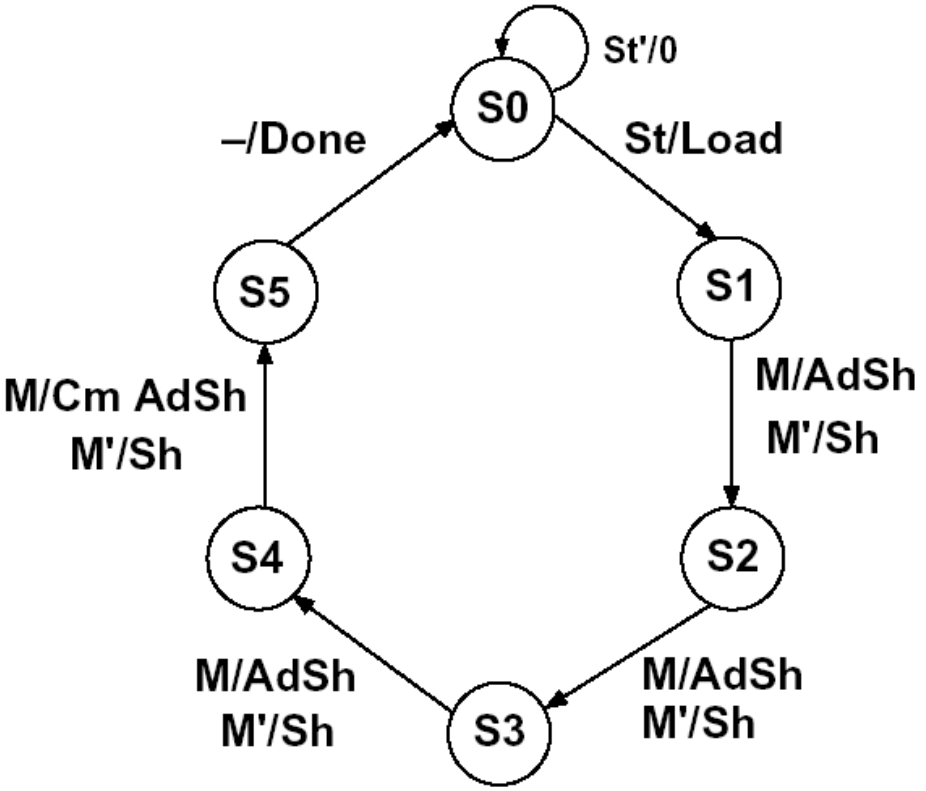
Example: Faster Multiplier



- Move wires from the adder outputs one position to the right => add and shift can occur at the same clock cycle

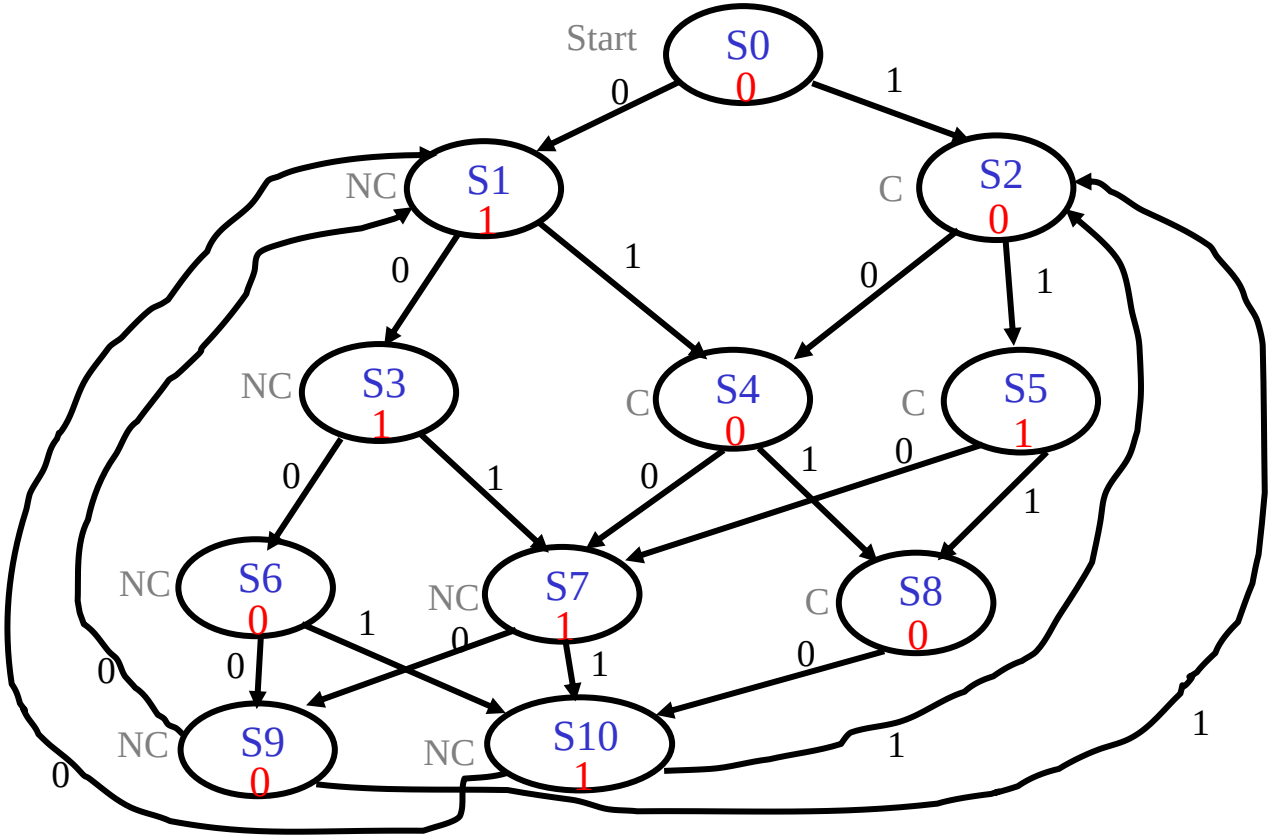
Extended State Graph for Fast Multiplier



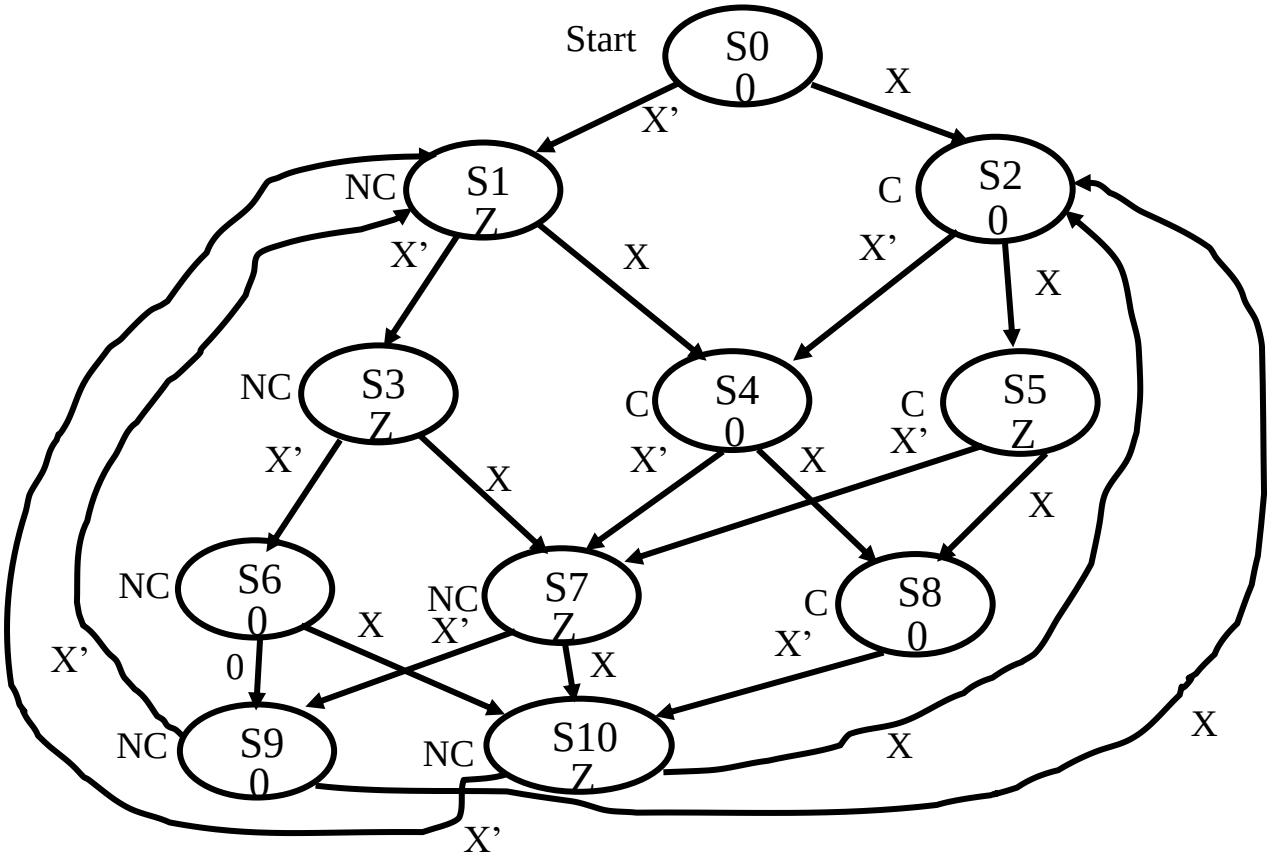


- Note: '-' on the input means no inputs are monitored and transition occurs to the next state no matter what the inputs are

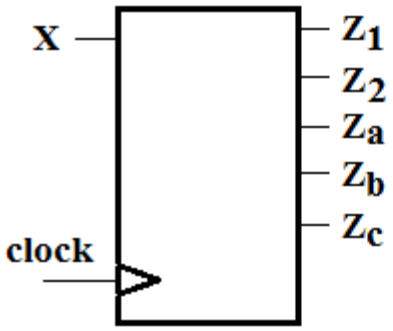
BCD to Excess 3 Moore FSM Example
(Standard State Graph Representation)

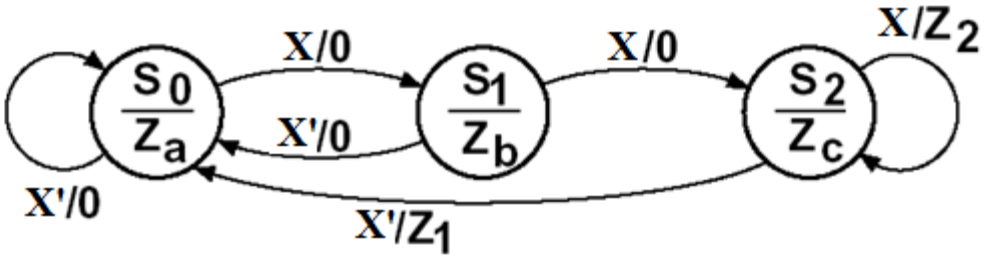


BCD to Excess 3 Moore FSM Example
(Extended State Graph Representation)



Combined Mealy/Moore FSM
(Extended State Graph Representation)





Input:

X

Outputs:

Z_a, Z_b, Z_c { Moore Outputs

Z_1, Z_2 { Mealy Outputs