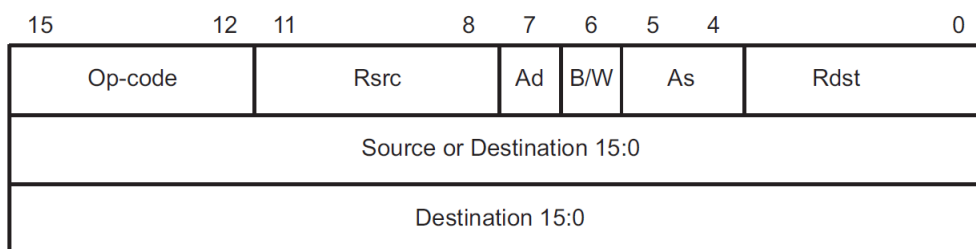


## MSP430 Instruction Set

### Double Operand Instructions



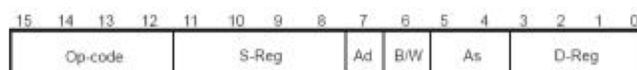
**Figure 6-22. MSP430 Double-Operand Instruction Format**

**Table 6-4. MSP430 Double-Operand Instructions**

| Mnemonic  | S-Reg,<br>D-Reg | Operation                       | Status Bits <sup>(1)</sup> |   |   |   |
|-----------|-----------------|---------------------------------|----------------------------|---|---|---|
|           |                 |                                 | V                          | N | Z | C |
| MOV (.B)  | src,dst         | src → dst                       | —                          | — | — | — |
| ADD (.B)  | src,dst         | src + dst → dst                 | *                          | * | * | * |
| ADDC (.B) | src,dst         | src + dst + C → dst             | *                          | * | * | * |
| SUB (.B)  | src,dst         | dst + .not.src + 1 → dst        | *                          | * | * | * |
| SUBC (.B) | src,dst         | dst + .not.src + C → dst        | *                          | * | * | * |
| CMP (.B)  | src,dst         | dst - src                       | *                          | * | * | * |
| DADD (.B) | src,dst         | src + dst + C → dst (decimally) | *                          | * | * | * |
| BIT (.B)  | src,dst         | src .and. dst                   | 0                          | * | * | Z |
| BIC (.B)  | src,dst         | .not.src .and. dst → dst        | —                          | — | — | — |
| BIS (.B)  | src,dst         | src .or. dst → dst              | —                          | — | — | — |
| XOR (.B)  | src,dst         | src .xor. dst → dst             | *                          | * | * | Z |
| AND (.B)  | src,dst         | src .and. dst → dst             | 0                          | * | * | Z |

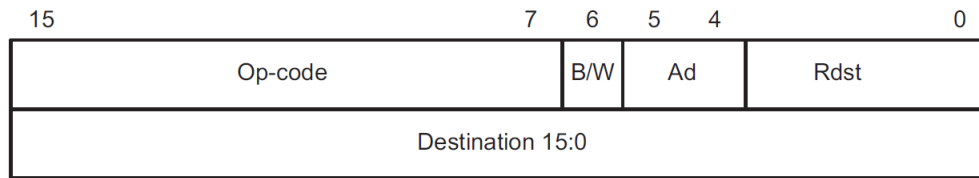
(1) \* = Status bit is affected.  
 — = Status bit is not affected.  
 0 = Status bit is cleared.  
 1 = Status bit is set.

MSP430: 16, 16-bit registers  
 R0 - Program counter  
 R1 - Stack pointer (SP) *last full location on TOS*  
 R2 - Status register (SR)  
 R3 - Constant generator



| As | Ad | Addressing Mode                      | Syntax | Description   |
|----|----|--------------------------------------|--------|---|
| 00 | 0  | Register Mode $\rightarrow$          | Rn     | Register contents are operand   |
| 01 | 1  | Indexed Mode $\uparrow$              | X(Rn)  | (Rn + X) points to the operand.<br>X is stored in the next word   |
| 01 | 1  | Symbolic Mode $\downarrow$           | ADDR   | (PC + X) points to the operand.<br>X is stored in the next word. Indexed Mode X(PC) is used                       |
| 01 | 1  | Absolute Mode $\uparrow$ /           | &ADDR  | The word following the instruction contains the absolute address.   |
| 10 | -  | Indirect Register Mode $\rightarrow$ | @Rn    | Rn is used as a pointer to the operand  |
| 11 | -  | Indirect Autoincrement $\rightarrow$ | @Rn+   | Rn is used as a pointer to the operand.<br>Rn is incremented afterwards   |
| 11 | -  | Immediate Mode $\#$                  | #N     | The word following the instruction contains the immediate constant N.<br>Indirect Autoincrement Mode @PC+ is used |

## Single Operand Instructions



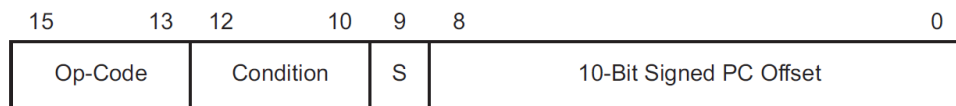
**Figure 6-23. MSP430 Single-Operand Instructions**

**Table 6-5. MSP430 Single-Operand Instructions**

| Mnemonic    | S-Reg,<br>D-Reg | Operation  | Status Bits <sup>(1)</sup> |   |   |   |
|-------------|-----------------|--|----------------------------|---|---|---|
|             |                 |  | V                          | N | Z | C |
| RRC ( . B)  | dst             | C → MSB → .....LSB → C   | 0                          | * | * | * |
| RRA ( . B)  | dst             | MSB → MSB → ....LSB → C  | 0                          | * | * | * |
| PUSH ( . B) | src             | SP - 2 → SP, src → SP  | —                          | — | — | — |
| SWPB        | dst             | bit 15...bit 8 ↔ bit 7...bit 0   | —                          | — | — | — |
| CALL        | dst             | Call subroutine in lower 64KB  | —                          | — | — | — |
| RETI        |                 | TOS → SR, SP + 2 → SP  | *                          | * | * | * |
|             |                 | TOS → PC, SP + 2 → SP  |                            |   |   |   |
| SXT         | dst             | Register mode: bit 7 → bit 8...bit 19<br>Other modes: bit 7 → bit 8...bit 15 | 0                          | * | * | Z |

(1) \* = Status bit is affected.  
 — = Status bit is not affected.  
 0 = Status bit is cleared.  
 1 = Status bit is set.

## Jump Instructions



**Figure 6-24. Format of Conditional Jump Instructions**

**Table 6-6. Conditional Jump Instructions**

| Mnemonic | S-Reg,<br>D-Reg | Operation                            | decimal | hexadecimal | binary |
|----------|-----------------|--------------------------------------|---------|-------------|--------|
|          |                 |                                      |         |             |        |
| JEQ, JZ  | Label           | Jump to label if zero bit is set     | 0       | 0           | 0000   |
| JNE, JNZ | Label           | Jump to label if zero bit is reset   | 1       | 1           | 0001   |
|          |                 |                                      | 2       | 2           | 0010   |
|          |                 |                                      | 3       | 3           | 0011   |
| JC       | Label           | Jump to label if carry bit is set    | 4       | 4           | 0100   |
|          |                 |                                      | 5       | 5           | 0101   |
| JNC      | Label           | Jump to label if carry bit is reset  | 6       | 6           | 0110   |
|          |                 |                                      | 7       | 7           | 0111   |
| JN       | Label           | Jump to label if negative bit is set | 8       | 8           | 1000   |
|          |                 |                                      | 9       | 9           | 1001   |
| JGE      | Label           | Jump to label if (N .XOR. V) = 0     | 10      | A           | 1010   |
|          |                 |                                      | 11      | B           | 1011   |
| JL       | Label           | Jump to label if (N .XOR. V) = 1     | 12      | C           | 1100   |
|          |                 |                                      | 13      | D           | 1101   |
| JMP      | Label           | Jump to label unconditionally        | 14      | E           | 1110   |
|          |                 |                                      | 15      | F           | 1111   |

.bss uninitialized  
.data initialized  
.text executable  
.long 32 bit  
.word 16 bit  
.string 16 bit  
.int 16 bit  
words: .word 2, -1, 3, 4 (4 16 bit words)  
Instruction length in words is +1 for all that are not indirect or autoincrement

## Emulated Instructions

Table 6-7. Emulated Instructions

| Instruction   | Explanation                | Emulation         | Status Bits <sup>(1)</sup> |   |   |   |
|---------------|----------------------------|-------------------|----------------------------|---|---|---|
|               |                            |                   | V                          | N | Z | C |
| ADC (.B) dst  | Add Carry to dst           | ADDC (.B) #0, dst | *                          | * | * | * |
| BR dst        | Branch indirectly dst      | MOV dst, PC       | —                          | — | — | — |
| CLR (.B) dst  | Clear dst                  | MOV (.B) #0, dst  | —                          | — | — | — |
| CLRC          | Clear Carry bit            | BIC #1, SR        | —                          | — | — | 0 |
| CLRN          | Clear Negative bit         | BIC #4, SR        | —                          | 0 | — | — |
| CLRZ          | Clear Zero bit             | BIC #2, SR        | —                          | — | 0 | — |
| DADC (.B) dst | Add Carry to dst decimally | DADD (.B) #0, dst | *                          | * | * | * |
| DEC (.B) dst  | Decrement dst by 1         | SUB (.B) #1, dst  | *                          | * | * | * |
| DECD (.B) dst | Decrement dst by 2         | SUB (.B) #2, dst  | *                          | * | * | * |
| DINT          | Disable interrupt          | BIC #8, SR        | —                          | — | — | — |
| EINT          | Enable interrupt           | BIS #8, SR        | —                          | — | — | — |
| INC (.B) dst  | Increment dst by 1         | ADD (.B) #1, dst  | *                          | * | * | * |
| INCD (.B) dst | Increment dst by 2         | ADD (.B) #2, dst  | *                          | * | * | * |

- (1) \* = Status bit is affected.  
— = Status bit is not affected.  
0 = Status bit is cleared.  
1 = Status bit is set.

| Mnemonic and Syntax  | Description  | See                           |
|--|--|-------------------------------|
| <b>.bss</b> symbol, size in bytes[, alignment]                       | Reserves size bytes in the .bss (uninitialized data) section                                   | <a href="#">.bss topic</a>    |
| <b>.data</b>   | Assembles into the .data (initialized data) section  | <a href="#">.data topic</a>   |
| <b>.intvec</b>   | Creates an interrupt vector entry in a named section that points to an interrupt routine name. | <a href="#">.intvec topic</a> |
| <b>.sect "section name"</b>  | Assembles into a named (initialized) section   | <a href="#">.sect topic</a>   |
| <b>.text</b>   | Assembles into the .text (executable code) section   | <a href="#">.text topic</a>   |
| <b>symbol .usect "section name", size in bytes<br/>[, alignment]</b> | Reserves size bytes in a named (uninitialized) section   | <a href="#">.usect topic</a>  |

Table 6-7. Emulated Instructions (continued)

| Instruction  | Explanation                            | Emulation          | Status Bits <sup>(1)</sup> |   |   |   |
|--------------|--|--------------------|----------------------------|---|---|---|
|              |  |                    | V                          | N | Z | C |
| INV (.B) dst | Invert dst                             | XOR (.B) #-1, dst  | *                          | * | * | * |
| NOP          | No operation                           | MOV R3, R3         | —                          | — | — | — |
| POP dst      | Pop operand from stack                 | MOV @SP+, dst      | —                          | — | — | — |
| RET          | Return from subroutine                 | MOV @SP+, PC       | —                          | — | — | — |
| RLA (.B) dst | Shift left dst arithmetically          | ADD (.B) dst, dst  | *                          | * | * | * |
| RLC (.B) dst | Shift left dst logically through Carry | ADDC (.B) dst, dst | *                          | * | * | * |
| SBC (.B) dst | Subtract Carry from dst                | SUBC (.B) #0, dst  | *                          | * | * | * |
| SETC         | Set Carry bit                          | BIS #1, SR         | —                          | — | — | 1 |
| SETN         | Set Negative bit                       | BIS #4, SR         | —                          | 1 | — | — |
| SETZ         | Set Zero bit                           | BIS #2, SR         | —                          | — | 1 | — |
| TST (.B) dst | Test dst (compare with 0)              | CMP (.B) #0, dst   | 0                          | * | * | 1 |

| Dec | Hx | Oct | Char | Dec                      | Hx | Oct | Htmi | Chr   | Dec | Hx | Oct | Htmi | Chr | Dec | Hx | Oct | Htmi | Chr |
|-----|----|-----|------|--------------------------|----|-----|------|-------|-----|----|-----|------|-----|-----|----|-----|------|-----|
| 0   | 0  | 000 | NUL  | (null)                   | 32 | 20  | 040  | Space | 64  | 40 | 100 | 64   | 8   | 96  | 60 | 140 | 64   | 96  |
| 1   | 1  | 001 | SOH  | (start of heading)       | 33 | 21  | 041  | 32    | 65  | 41 | 101 | 65   | A   | 97  | 61 | 141 | 65   | A   |
| 2   | 2  | 002 | STX  | (start of text)          | 34 | 22  | 042  | 33    | 66  | 42 | 102 | 66   | B   | 98  | 62 | 142 | 66   | B   |
| 3   | 3  | 003 | ETX  | (end of text)            | 35 | 23  | 043  | 34    | 67  | 43 | 103 | 67   | C   | 99  | 63 | 143 | 67   | C   |
| 4   | 4  | 004 | END  | (end of transmission)    | 36 | 24  | 044  | 35    | 68  | 44 | 104 | 68   | D   | 100 | 64 | 144 | 68   | D   |
| 5   | 5  | 005 | ENQ  | (enquiry)                | 37 | 25  | 045  | 36    | 69  | 45 | 105 | 69   | E   | 101 | 65 | 145 | 69   | E   |
| 6   | 6  | 006 | ACK  | (acknowledge)            | 38 | 26  | 046  | 37    | 70  | 46 | 106 | 70   | F   | 102 | 66 | 146 | 70   | F   |
| 7   | 7  | 007 | BEL  | (bell)                   | 39 | 27  | 047  | 38    | 71  | 47 | 107 | 71   | 10  | 103 | 67 | 147 | 71   | 10  |
| 8   | 8  | 010 | BS   | (backspace)              | 40 | 28  | 050  | 40    | 72  | 48 | 110 | 72   | H   | 104 | 68 | 150 | 72   | H   |
| 9   | 9  | 011 | TAB  | (horizontal tab)         | 41 | 29  | 051  | 41    | 73  | 49 | 111 | 73   | I   | 105 | 69 | 151 | 73   | I   |
| 10  | A  | 012 | LF   | (NL line feed, new line) | 42 | 2A  | 052  | 42    | 74  | 4A | 112 | 74   | J   | 106 | 6A | 152 | 74   | J   |
| 11  | B  | 013 | VT   | (vertical tab)           | 43 | 2B  | 053  | 43    | 75  | 4B | 113 | 75   | K   | 107 | 6B | 153 | 75   | K   |
| 12  | C  | 014 | FF   | (NP form feed, new page) | 44 | 2C  | 054  | 44    | 76  | 4C | 114 | 76   | L   | 108 | 6C | 154 | 76   | L   |
| 13  | D  | 015 | CR   | (carriage return)        | 45 | 2D  | 055  | 45    | 77  | 4D | 115 | 77   | M   | 109 | 6D | 155 | 77   | M   |
| 14  | E  | 016 | SO   | (shift out)              | 46 | 2E  | 056  | 46    | 78  | 4E | 116 | 78   | N   | 110 | 6E | 156 | 78   | N   |
| 15  | F  | 017 | SI   | (shift in)               | 47 | 2F  | 057  | 47    | 79  | 4F | 117 | 79   | O   | 111 | 6F | 157 | 79   | O   |
| 16  | 10 | 020 | DLE  | (data link escape)       | 48 | 30  | 060  | 48    | 80  | 50 | 120 | 80   | P   | 112 | 70 | 160 | 80   | P   |
| 17  | 11 | 021 | DC1  | (device control 1)       | 49 | 31  | 061  | 49    | 81  | 51 | 121 | 81   | Q   | 113 | 71 | 161 | 81   | Q   |
| 18  | 12 | 022 | DC2  | (device control 2)       | 50 | 32  | 062  | 50    | 82  | 52 | 122 | 82   | R   | 114 | 72 | 162 | 82   | R   |
| 19  | 13 | 023 | DC3  | (device control 3)       | 51 | 33  | 063  | 51    | 83  | 53 | 123 | 83   | S   | 115 | 73 | 163 | 83   | S   |
| 20  | 14 | 024 | DC4  | (device control 4)       | 52 | 34  | 064  | 52    | 84  | 54 | 124 | 84   | T   | 116 | 74 | 164 | 84   | T   |
| 21  | 15 | 025 | NAK  | (negative acknowledge)   | 53 | 35  | 065  | 53    | 85  | 55 | 125 | 85   | U   | 117 | 75 | 165 | 85   | U   |
| 22  | 16 | 026 | STB  | (synchronous idle)       | 54 | 36  | 066  | 54    | 86  | 56 | 126 | 86   | V   | 118 | 76 | 166 | 86   | V   |
| 23  | 17 | 027 | ETB  | (end of trans. block)    | 55 | 37  | 067  | 55    | 87  | 57 | 127 | 87   | W   | 119 | 77 | 167 | 87   | W   |
| 24  | 18 | 030 | CAN  | (cancel)                 | 56 | 38  | 070  | 56    | 88  | 58 | 130 | 88   | X   | 120 | 78 | 170 | 88   | X   |
| 25  | 19 | 031 | EM   | (end of medium)          | 57 | 39  | 071  | 57    | 89  | 59 | 131 | 89   | Y   | 121 | 79 | 171 | 89   | Y   |
| 26  | 1A | 032 | SUB  | (substitute)             | 58 | 3A  | 072  | 58    | 90  | 5A | 132 | 90   | Z   | 122 | 7A | 172 | 90   | Z   |
| 27  | 1B | 033 | ESC  | (escape)                 | 59 | 3B  | 073  | 59    | 91  | 5B | 133 | 91   | [   | 123 | 7B | 173 | 91   | [   |
| 28  | 1C | 034 | FS   | (file separator)         | 60 | 3C  | 074  | 60    | 92  | 5C | 134 | 92   | \   | 124 | 7C | 174 | 92   | \   |
| 29  | 1D | 035 | GS   | (group separator)        | 61 | 3D  | 075  | 61    | 93  | 5D | 135 | 93   | ]   | 125 | 7D | 175 | 93   | ]   |
| 30  | 1E | 036 | RS   | (record separator)       | 62 | 3E  | 076  | 62    | 94  | 5E | 136 | 94   | ^   | 126 | 7E | 176 | 94   | ^   |
| 31  | 1F | 037 | US   | (unit separator)         | 63 | 3F  | 077  | 63    | 95  | 5F | 137 | 95   | _   | 127 | 7F | 177 | 95   | _   |