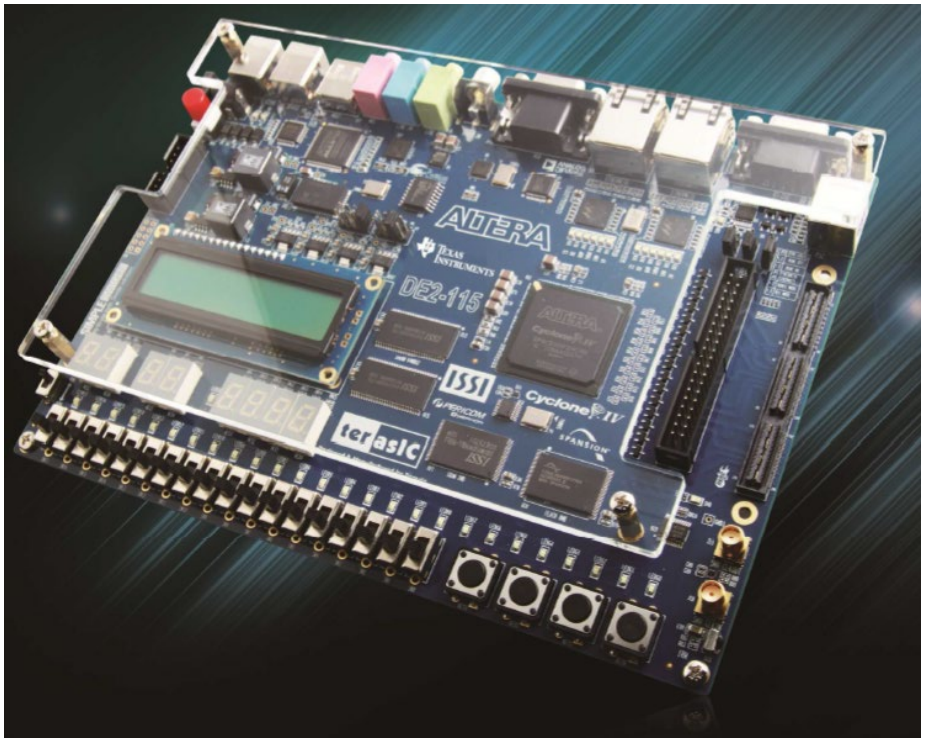
CPE 322
Digital Hardware Design Fundamentals

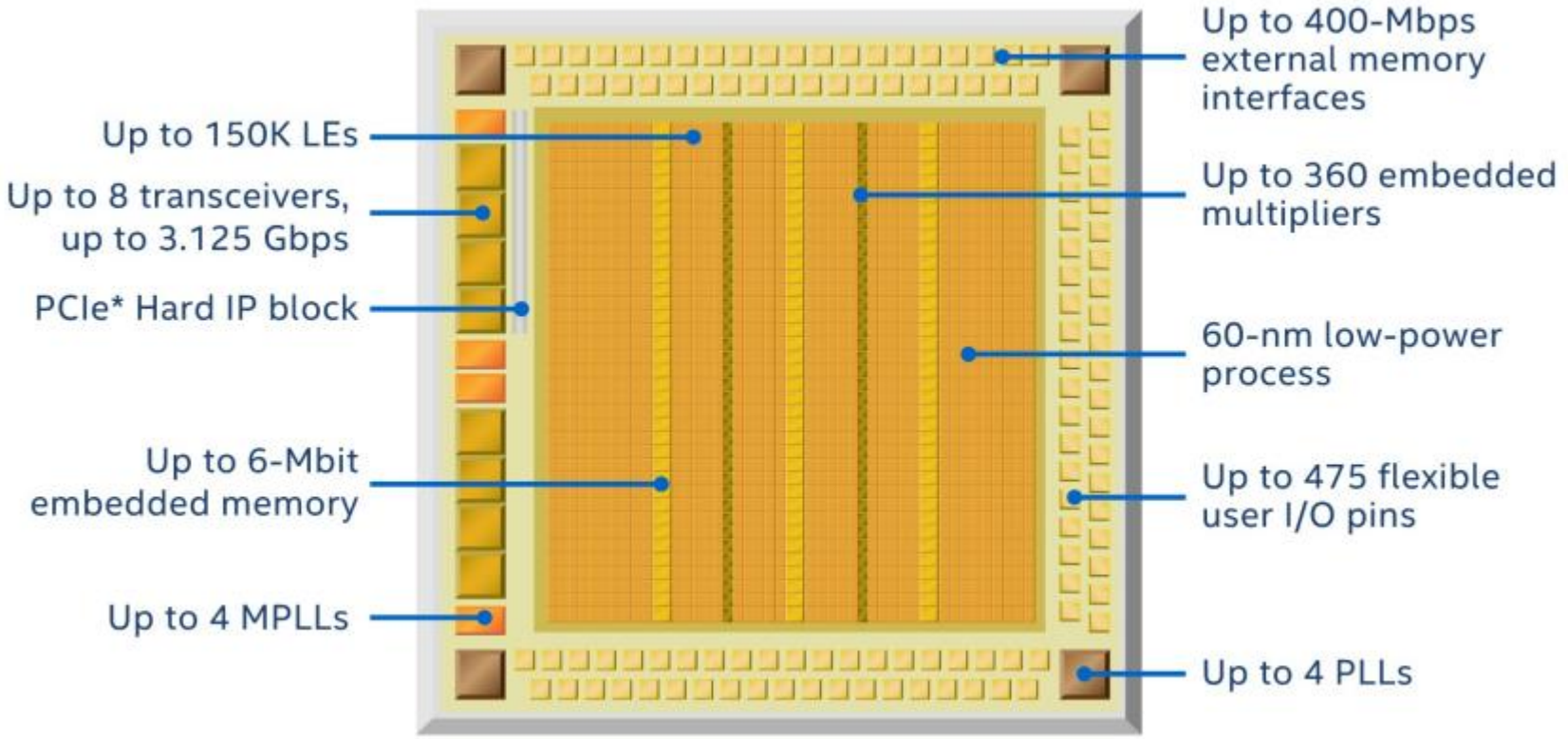
Non CLB FPGA Building Blocks:

Dedicated Memory Blocks &

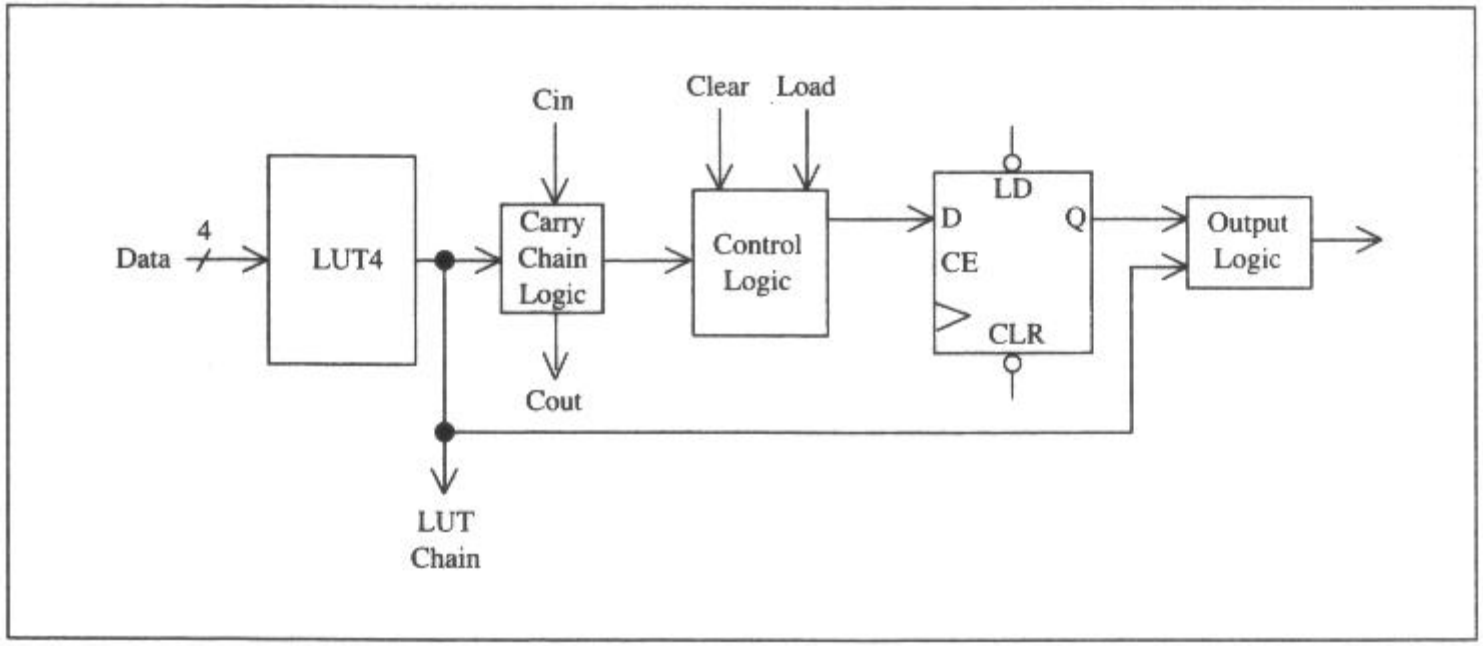
Dedicated Multipliers



Cyclone IV E Family FPGA Layout



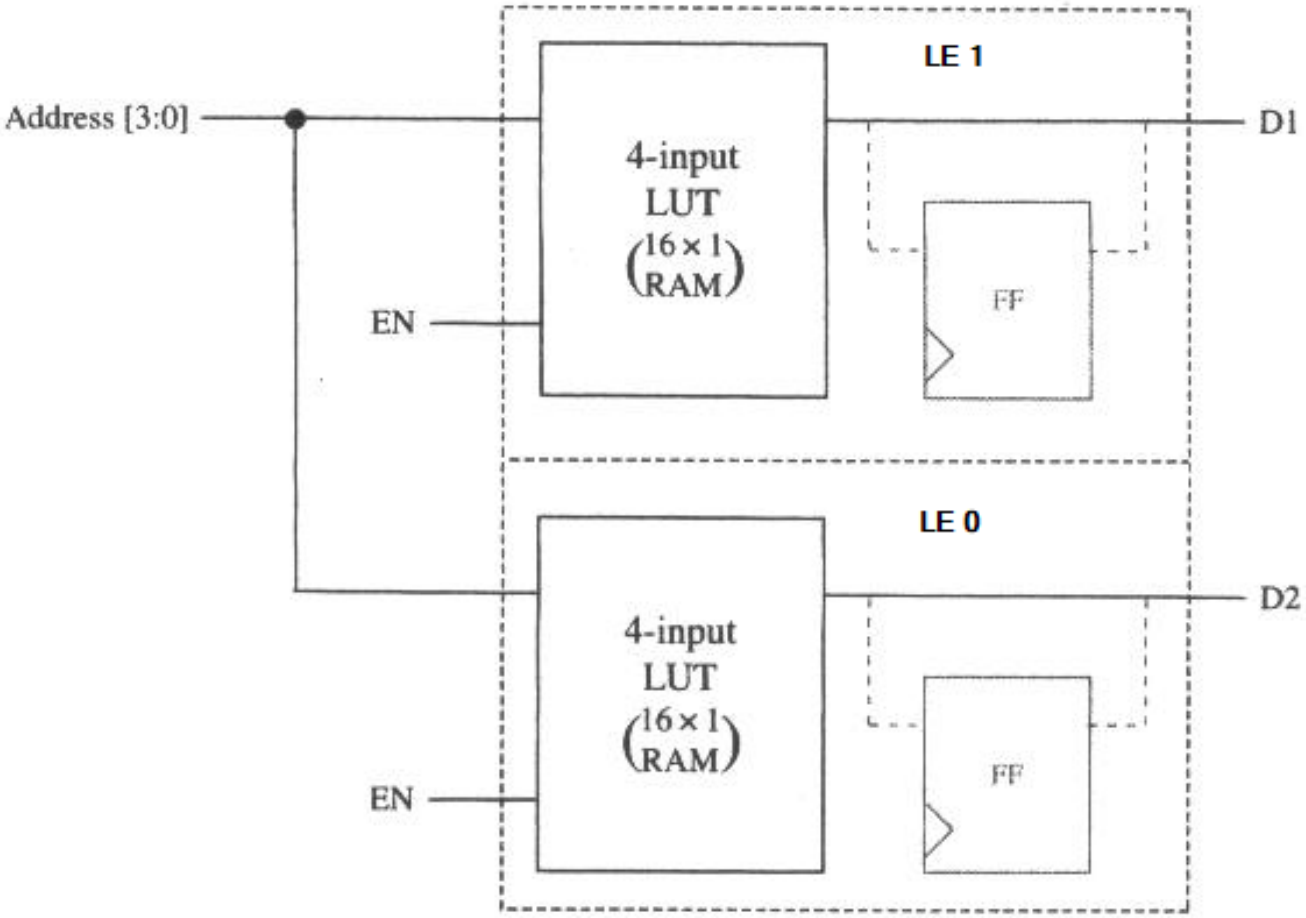
IntelFPGA's Configurable Logic Block (Cyclone IV E Logic Element -- LE)



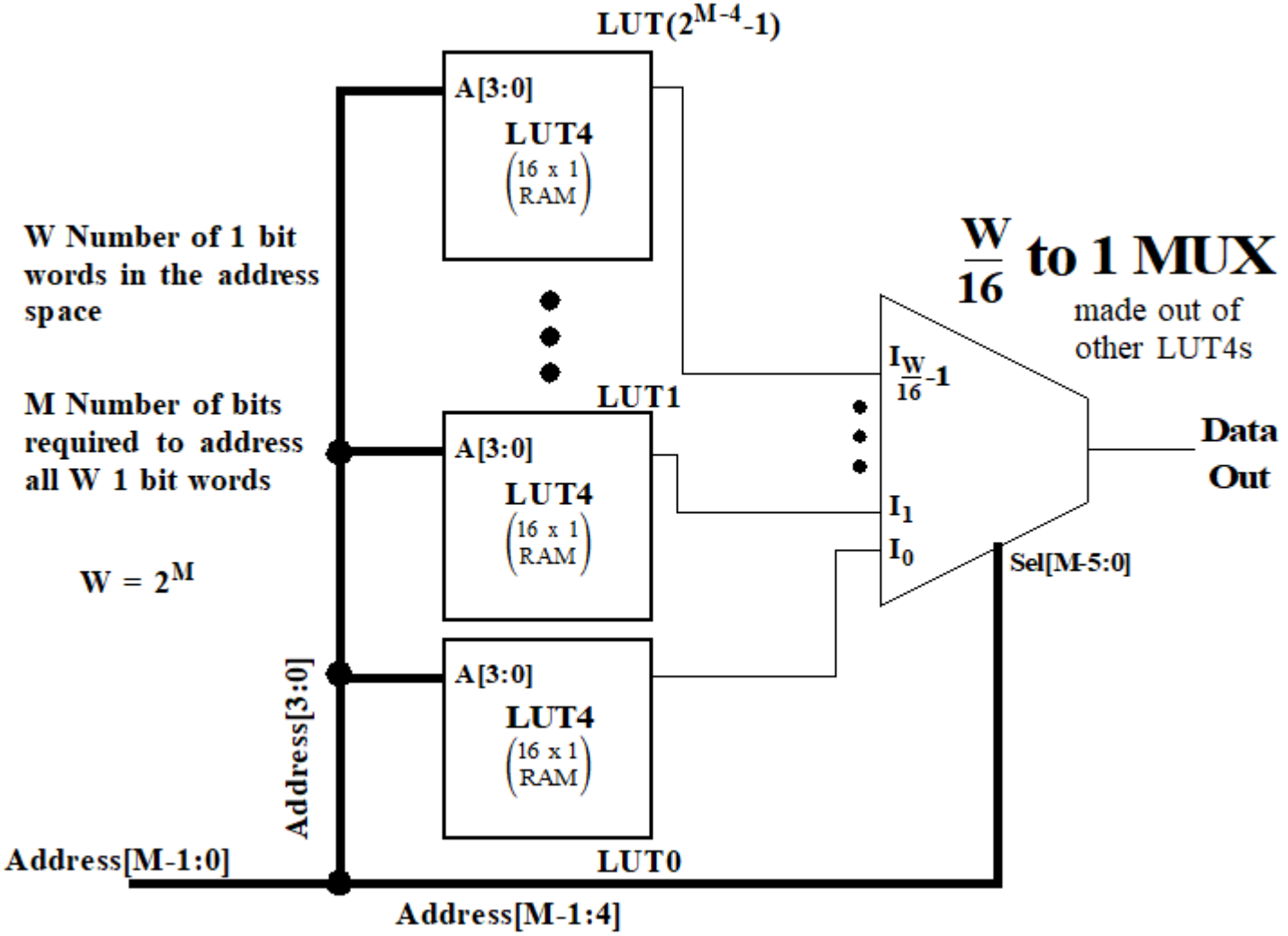
114,480 LEson the IntelFPGA EP4CE115 FPGA in the DE2-115

Creating Memory from LUTs

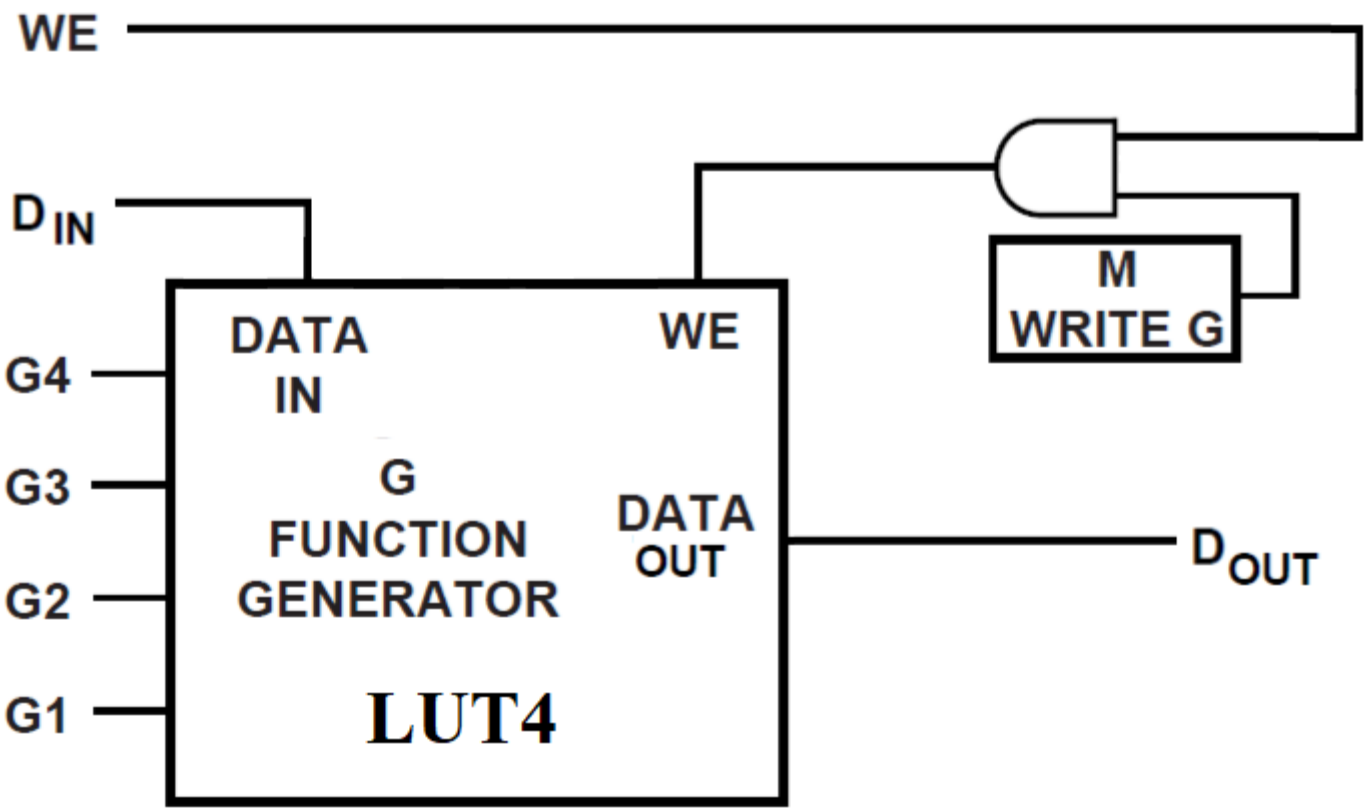
(16 x 2 memory)



Creating Memory from LUTs
(W x 1 Rom Memory)



LUTs as a Read/Write Memory Cell



Creating Memory from LUTs

Verilog HDL Model that typically infers LUT-based memory

```
// Synchronous write Asynchronous Read Read/Write Memory
// Made from LUTs of the LUT Register Resources
module Memory  (input CLK, MemWrite, input [12:0] Address,
                input [7:0] Data_In, output [7:0] DATA_OUT);

   reg [7:0] DataMEM[0:8191]; // 8 K bytes of memory

   initial
      begin
         $readmemh("initial_ram.txt",DataMEM);
      end

   always @ (posedge CLK)
      begin
         if (MemWrite) DataMEM[Address] = Data_In;   // Synchronous Write
      end

   assign DATA_OUT = DataMEM[Address];               // Asynchronous Read

endmodule
```

Creating Memory from LUTs

Verilog HDL Model that typically infers LUT-based memory

Flow Summary

<<Filter>>

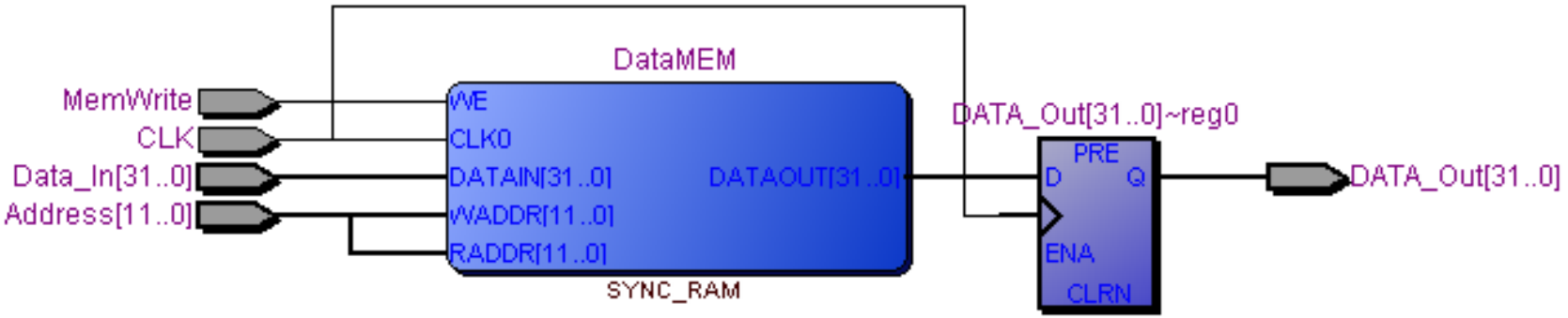
Flow Status	Successful - Sun Apr 19 13:15:09 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	Memory
Top-level Entity Name	Memory
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	84,363 / 114,480 (74 %)
Total registers	65536
Total pins	31 / 529 (6 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Took 74% of the 114,480 LEs on the IntelFPGA EP4CE115 FPGA in the DE2-115

Took 30 minutes to Synthesize/Optimize/Place and Route using Quartus Prime CAD tool

Creating Memory Regions using Dedicated Embedded FPGA Synchronous RAM Memory

```
module Memory (input CLK, MemWrite, input [11:0] Address,
               input [31:0] Data_In, output reg [31:0] DATA_Out);
```




```
endmodule
```

Both inputs and outputs are activated by the clock

Dedicated Memory – Variable Data Widths (Cyclone IV E)

Width	Depth	Addr Bus	Data Bus
1	8192	13	1
2	4096	12	2
4	2048	11	4
8	1024	10	8
9	1024	10	9
16	512	9	16
18	512	9	18
32	256	8	32
36	256	8	36

Dedicated Memory – Variable Data Widths (Cyclone IV E – Modes of Operation)

- Single Port
  - supports non-simultaneous read and write operations from a single address
- Simple Dual-Port
  - supports simultaneous read and write operations to different memory locations
- True Dual-Port
  - supports any combination of two-port operations: two reads, two writes, or one read and one write, at two different clock frequencies.
- Shift-register

Using the Embedded Dedicated Memory

Verilog Model that typically infers Dedicated memory

```
// Synchronous Read/Write Memory
// Quartus will use Dedicated Memory instead of LUTs because
// the Dedicated Memory in our targeted FPGA has the same attributes
module Memory (input cLK, MemWrite, input [12:0] Address,
                  input [7:0] Data_In, output reg [7:0] DATA_OUT);

   reg [7:0] DataMEM[0:8191]; // 8 K bytes of memory

   initial
      begin
         $readmemh("initial_ram.txt",DataMEM);
      end

   always @ (posedge cLK)
      begin
         if (MemWrite) DataMEM[Address] = Data_In; // Synchronous Write
         DATA_OUT = DataMEM[Address];              // Synchronous Read
      end

endmodule
```

Using the Embedded Dedicated Memory

Verilog Model that typically infers Dedicated memory

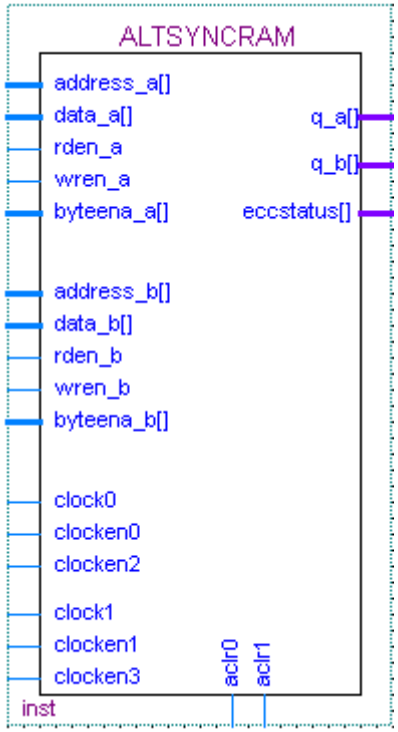
Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 20 00:24:55 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	Memory
Top-level Entity Name	Memory
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	9 / 114,480 (< 1 %)
Total registers	9
Total pins	31 / 529 (6 %)
Total virtual pins	0
Total memory bits	65,536 / 3,981,312 (2 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Structural Technique for Implementing Memory Elements in the FPGA's Dedicated Block RAM Memory

```
// Memory module in Verilog HDL in a manner that explicitly utilizes
// the Altera Megafunction library in Quartus. This will utilize
// 64 M4K dedicated memory elements for a total storage of
// 262144 bits (It also uses 48 LE's).
module rom (input [14:0] address, input clock, output [7:0] q);
   altsyncram   C1 (
      .clock0 (clock),
      .address_a (address),
      .q_a (q),
      .aclr0 (1'b0),
      .aclr1 (1'b0),
      .address_b (1'b1),
      .addressstall_a (1'b0),
      .addressstall_b (1'b0),
      .byteena_a (1'b1),
      .byteena_b (1'b1),
      .clock1 (1'b1),
      .clocken0 (1'b1),
      .clocken1 (1'b1),
      .clocken2 (1'b1),
      .clocken3 (1'b1),
      .data_a ({8{1'b1}}),
      .data_b (1'b1),
      .eccstatus (),
      .q_b (),
      .rden_a (1'b1),
      .rden_b (1'b1),
      .wren_a (1'b0),
      .wren_b (1'b0));
```




```
defparam
   C1.clock_enable_input_a = "BYPASS",
   C1.clock_enable_output_a = "BYPASS",
   C1.init_file = "E:/example/rom.hex",
   C1.intended_device_family = "Cyclone IV",
   C1.lpm_hint = "ENABLE_RUNTIME_MOD=NO",
   C1.lpm_type = "altsyncram",
   C1.numwords_a = 32768,
   C1.operation_mode = "ROM",
   C1.outdata_aclr_a = "NONE",
   C1.outdata_reg_a = "UNREGISTERED",
   C1.power_up_uninitialized = "FALSE",
   C1.ram_block_type = "M9K",
   C1.widthad_a = 15,
   C1.width_a = 8,
   C1.width_byteena_a = 1;

endmodule
```

Multiplication in FPGAs

Using LUTS to Implement a 4x4 Multiplier
(using LUTs)

```
module LUTmult(input [3:0] Mplier, Mcand, output reg [7:0] Product);

   reg [7:0] prod_rom [0:255];

   initial
      begin:ROM_LOAD
      reg [8:0] i;
      for (i=0;i<256;i=i+1)
         prod_rom[i] = {4'b0000,i[7:4]}*{4'b0000,i[3:0]};
      end
```

columns

rows

```
(x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00",
x"00", x"01", x"02", x"03", x"04", x"05", x"06", x"07", x"08", x"09", x"0A", x"0B", x"0C", x"0D", x"0E", x"0F",
x"00", x"02", x"04", x"06", x"08", x"0A", x"0C", x"0E", x"10", x"12", x"14", x"16", x"18", x"1A", x"1C", x"1E",
x"00", x"03", x"06", x"09", x"0C", x"0F", x"12", x"15", x"18", x"1B", x"1E", x"21", x"24", x"27", x"2A", x"2D",
x"00", x"04", x"08", x"0C", x"10", x"14", x"18", x"1C", x"20", x"24", x"28", x"2C", x"30", x"34", x"38", x"3C",
x"00", x"05", x"0A", x"0F", x"14", x"19", x"1E", x"23", x"28", x"2D", x"32", x"37", x"3C", x"41", x"46", x"4B",
x"00", x"06", x"0C", x"12", x"18", x"1E", x"24", x"2A", x"30", x"36", x"3C", x"42", x"48", x"4E", x"54", x"5A",
x"00", x"07", x"0E", x"15", x"1C", x"23", x"2A", x"31", x"38", x"3F", x"46", x"4D", x"54", x"5B", x"62", x"69",
x"00", x"08", x"10", x"18", x"20", x"28", x"30", x"38", x"40", x"48", x"50", x"58", x"60", x"68", x"70", x"78",
x"00", x"09", x"12", x"1B", x"24", x"2D", x"36", x"3F", x"48", x"51", x"5A", x"63", x"6C", x"75", x"7E", x"87",
x"00", x"0A", x"14", x"1E", x"28", x"32", x"3C", x"46", x"50", x"5A", x"64", x"6E", x"78", x"82", x"8C", x"96",
x"00", x"0B", x"16", x"21", x"2C", x"37", x"42", x"4D", x"58", x"63", x"6E", x"79", x"84", x"8F", x"9A", x"A5",
x"00", x"0C", x"18", x"24", x"30", x"3C", x"48", x"54", x"60", x"6C", x"78", x"84", x"90", x"9C", x"A8", x"B4",
x"00", x"0D", x"1A", x"27", x"34", x"41", x"4E", x"5B", x"68", x"75", x"82", x"8F", x"9C", x"A9", x"B6", x"C3",
x"00", x"0E", x"1C", x"2A", x"38", x"46", x"54", x"62", x"70", x"7E", x"8C", x"9A", x"A8", x"B6", x"C4", x"D2",
x"00", x"0F", x"1E", x"2D", x"3C", x"4B", x"5A", x"69", x"78", x"87", x"96", x"A5", x"B4", x"C3", x"D2", x"E1");
```

```
   always @ (Mplier or Mcand)
      Product = prod_rom[{Mplier,Mcand}]; // read Product LUT

endmodule
```

Using LUTS to Implement a 4x4 Multiplier
(using LUTs)

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 20 00:52:44 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	LUTmult
Top-level Entity Name	LUTmult
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	67 / 114,480 (< 1 %)
Total registers	0
Total pins	16 / 529 (3 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Using Dedicated Block RAM to Implement a 4x4 Multiplier

```
module LUTmult(input clk, input [3:0] Mplier, Mcand, output reg [7:0] Product);

   reg [7:0] prod_rom [0:255];

   initial
      begin:ROM_LOAD
      reg [8:0] i;
      for (i=0;i<256;i=i+1)
         prod_rom[i] = {4'b0000,i[7:4]}*{4'b0000,i[3:0]};
      end
```

columns

rows

```
      (x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00", x"00",
      x"00", x"01", x"02", x"03", x"04", x"05", x"06", x"07", x"08", x"09", x"0A", x"0B", x"0C", x"0D", x"0E", x"0F",
      x"00", x"02", x"04", x"06", x"08", x"0A", x"0C", x"0E", x"10", x"12", x"14", x"16", x"18", x"1A", x"1C", x"1E",
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      x"00", x"0C", x"18", x"24", x"30", x"3C", x"48", x"54", x"60", x"6C", x"78", x"84", x"90", x"9C", x"A8", x"B4",
      x"00", x"0D", x"1A", x"27", x"34", x"41", x"4E", x"5B", x"68", x"75", x"82", x"8F", x"9C", x"A9", x"B6", x"C3",
      x"00", x"0E", x"1C", x"2A", x"38", x"46", x"54", x"62", x"70", x"7E", x"8C", x"9A", x"A8", x"B6", x"C4", x"D2",
      x"00", x"0F", x"1E", x"2D", x"3C", x"4B", x"5A", x"69", x"78", x"87", x"96", x"A5", x"B4", x"C3", x"D2", x"E1");

   always @ (posedge clk)
      Product = prod_rom[{Mplier,Mcand}]; // read Product LUT
                                          // synchronously

endmodule
```

Using Dedicated Block RAM to Implement a 4x4 Multiplier

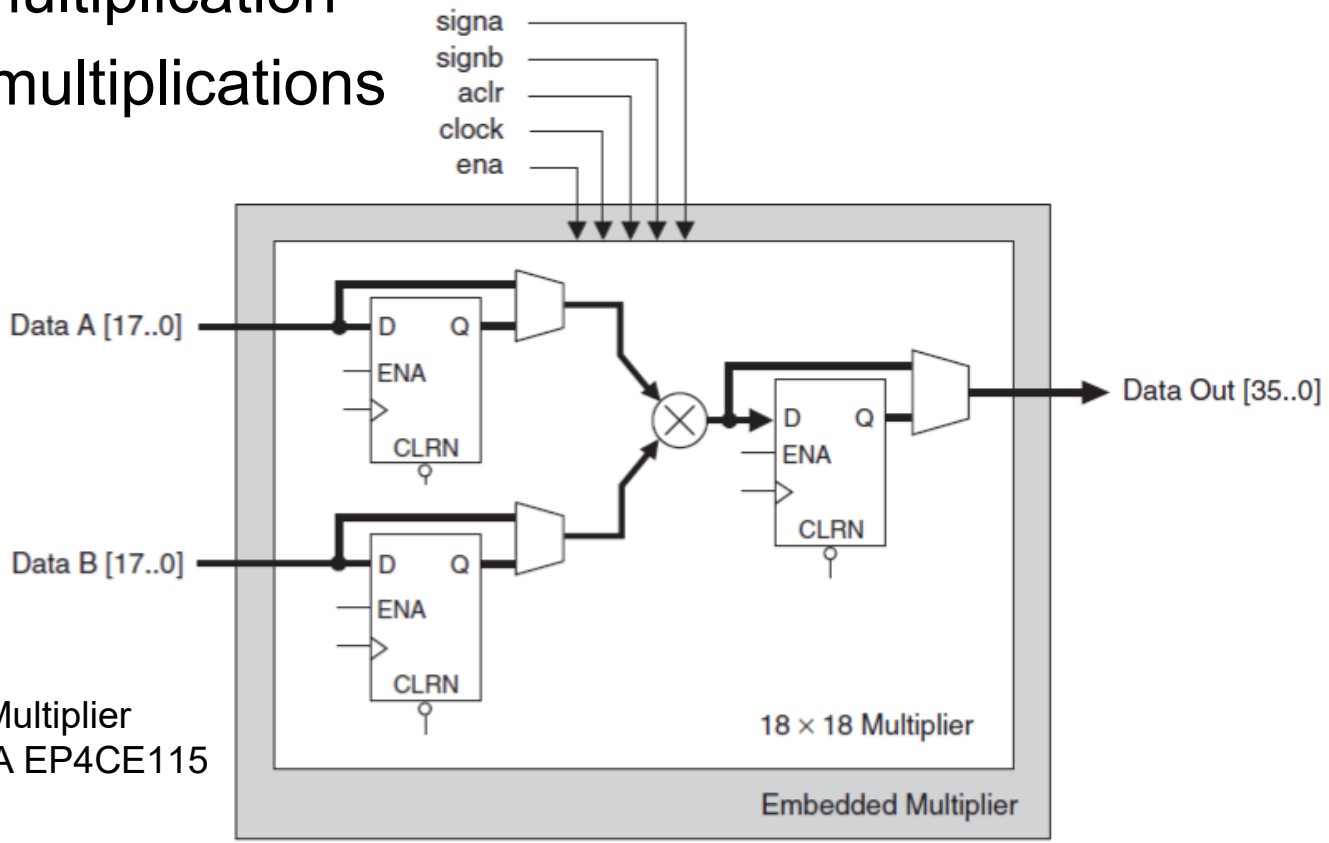
Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 20 01:09:21 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	LUTmult
Top-level Entity Name	LUTmult
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	0 / 114,480 (0 %)
Total registers	0
Total pins	17 / 529 (3 %)
Total virtual pins	0
Total memory bits	2,048 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Embedded Multiplier Blocks
(Cyclone IV E – 18x18 bit mode)

- Two Modes for each 18x18 bit multiplier
  - 18x18 bit multiplication
  - Two 9 x 9 multiplications



266 Embedded 18x18 Multiplier Blocks on the IntelFPGA EP4CE115 FPGA in the DE2-115

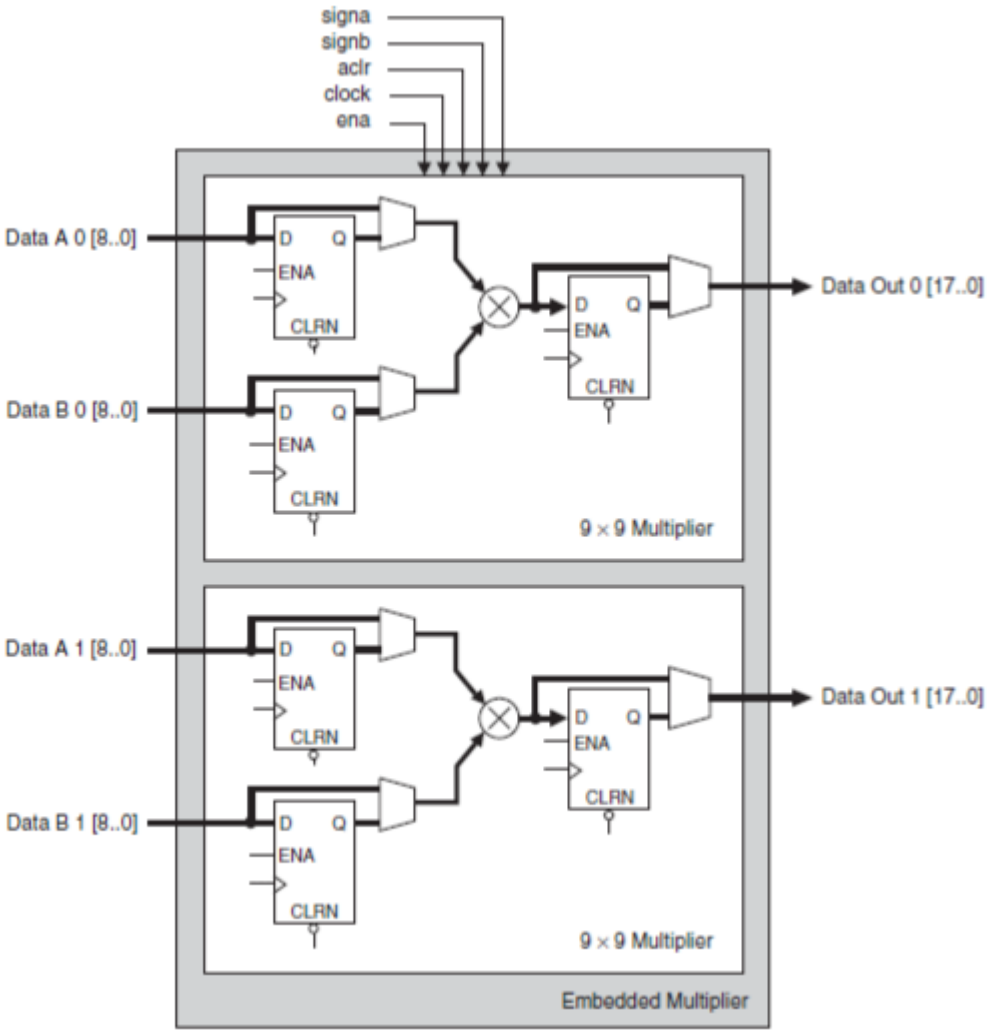
Embedded Multiplier Blocks (Cyclone IV E – Dual 9x9 bit mode)

266 Embedded 18x18 Multiplier Blocks on the IntelFPGA EP4CE115 FPGA in the DE2-115

OR

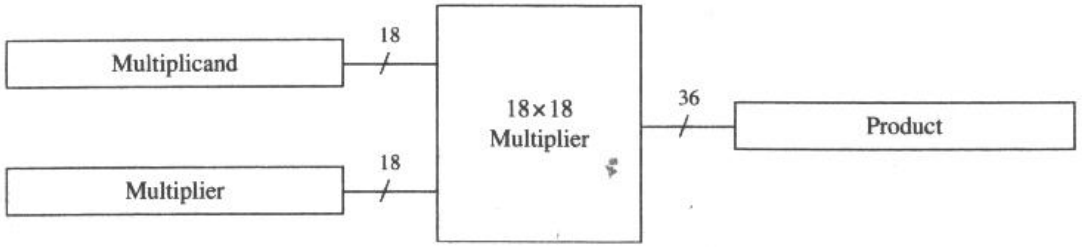
532 Embedded 9x9 Multiplier Blocks on the IntelFPGA EP4CE115 FPGA in the DE2-115

(when all are operated in the 9x9 mode)



Using Embedded Multiplier Blocks to Implement a 32 x 32 bit Multiplication

```
module mult_embedded (input [31:0] A,B, output [63:0] C);
    assign C = A * B;
endmodule
```



Flow Summary

<<Filter>>

Flow Status	Successful - Mon Apr 20 02:47:39 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	mult_embedded
Top-level Entity Name	mult_embedded
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	79 / 114,480 (< 1 %)
Total registers	0
Total pins	128 / 529 (24 %)
Total virtual pins	0
Total memory bits	0 / 3,981,312 (0 %)
Embedded Multiplier 9-bit elements	8 / 532 (2 %)
Total PLLs	0 / 4 (0 %)