The University of Alabama in Huntsville
ECE Department
CPE 221 01
Fall 2019
Homework #8 Solution

9.52 Consider a computer with a 256-byte address space and a two-way 64-byte set associative cache. The computer word size is a byte and each cache line contains four bytes. If the cache is initially empty and the following sequence of hexadecimal addresses is read, show the cache contents and the the corresponding sequence of hits and misses.

48, 0C, 48, 4C, 5C, 3A, 20, 21, 22, 24, 81, 49, 30, 34, 27, 3E, 24, 28, 2C, 40

64 bytes x 1 word/1 byte x 1line/4 words x 1 set/2 lines = 8 sets

	Index Block Offset		
48	010 010 00 miss	81	100 000 01 miss
0C	000 011 00 miss	49	010 010 01 hit
48	010 010 00 hit	30	001 100 00 miss
4C	010 011 00 miss	34	001 101 00 miss
5C	010 111 00 miss	27	001 001 11 hit
3A	001 110 10 miss	3E	001 111 10 miss
20	001 000 00 miss	24	001 001 00 hit
21	001 000 01 hit	28	001 010 00 miss
22	001 000 10 hit	2C	001 011 00 miss
24	001 001 00 miss	40	010 000 00 miss

Set	Tag*	Data	Tag	Data
0	001, 010	M[20..23], M[40..43]	100	M[80..83]
1			001	M[24..27]
2	001	M[28..2B]	010	M[48..4B]
3	000, 001	M[0C..0F], M[2C..2F]	010	M[4C..4F]
4	001	M[30..33]		
5			001	M[34..37]
6	001	M[38..3B]		
7	001	M[3C..3F]	010	M[5C..5F]

9.57 A computer with a 24-bit address bus has a main memory of size 16 MB and a cache size of 32 KB. The word length is four bytes.

a. What is the address format for a direct-mapped cache with a line size of 8 words?
32 KB x 1 word/4 bytes x 1 line/8 words x 1 set/1 line = 1 k sets
Byte offset = 2 bits, Block offset = 3 bits, Index = 10 bits, Tag = 9 bits

b. What is the address format for a fully associative cache with a line size of 16 words?
Byte offset = 2 bits, Block offset = 4 bits, Index = 0 bits, Tag = 18 bits

c. What is the address format for a four-way set-associative cache with a line size of 8 words?
32 KB x 1 word/4 bytes x 1 line/8 words x 1 set/4 lines = 256 sets
Byte offset = 2 bits, Block offset = 3 bits, Index = 8 bits, Tag = 11 bits