LABORATORY # 07 & 08
Characteristics of BJT and Amplification Behavior

Purpose

The concept and characteristics of bipolar junction transistors (BJTs) is introduced. The basic concepts investigated for BJTs carries over into future labs, especially for MOSFETs. Both NPN and PNP constructions will be considered. Constants and variables relating to BJTs will be discussed and utilized in the procedure section.

Theoretical Background

Construction - A BJT has three parts: a collector region, a base region, and an emitter region. The base is also at times referred to as the channel if the BJT is field affected to allow current to flow through the collector and emitter. For an NPN the base is a P-type material (material with extra holes), the collector and emitter regions are an N-type material (material with extra electrons). For an NPN the emitter region contains a higher density of electrons than the collector which allows current to flow from the collector to the emitter. For a PNP the base is an N-type material, while the collector and emitter regions are P-type. For a PNP the emitter region contains a higher density of holes than the collector region allowing current to flow from the emitter to the collector. Thus, all BJTs have two junctions; one emitter-base and the other collector-base.

Operation - Current flows through the base region if the transistor is in "forward" or "reverse-active mode". That is to say, DC current in the transistor is flowing through the base but only a small amount is coming from the base. "Forward-active mode" means the DC current is flowing in the direction of the base-collector junction and in the opposite direction of the base-emitter junction. "Reverse-active-mode" means the DC current is flowing opposite of the base-collector junction and in the same direction as the base-emitter junction. Maximum current flow is achieved in "saturation mode". No current flows in "cut-off mode".

Appearance –BJT circuit symbols vary so refer to the data sheet provided by the manufacturer for the specific BJT you are using. Some examples are provided below.

NPN

PNP

Physical Appearance

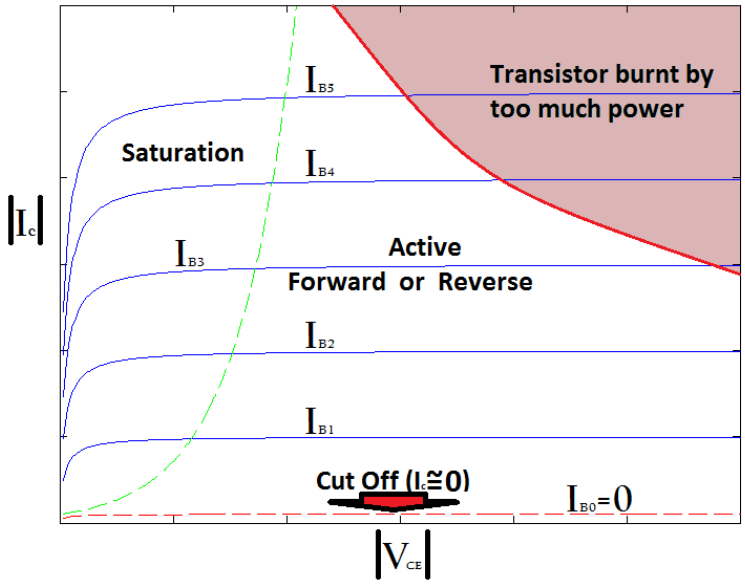


Figure 7.1 Output characteristic of BJT

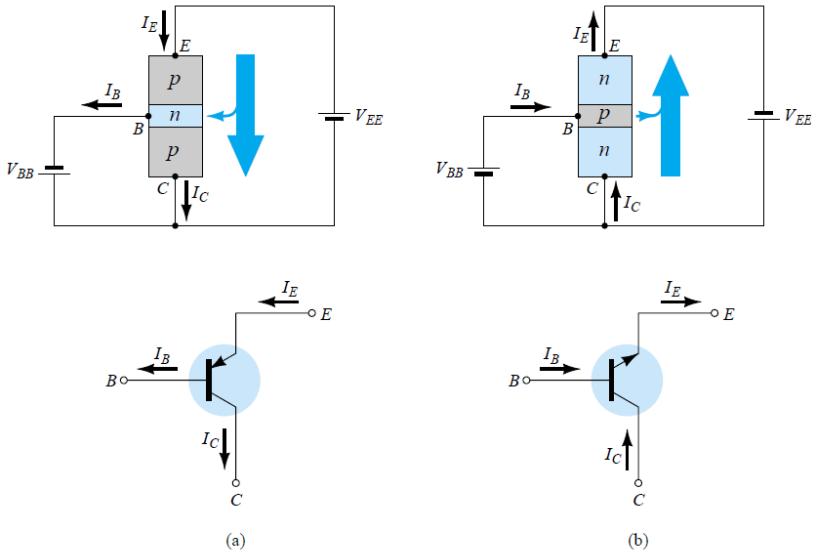


Figure 7.2 Common Collector Configuration* (a) PNP (b) NPN

BJT Kirchoff's Voltage Law: $V_{CE} = V_{CB} + V_{BE}$

BJT Kirchoff's Current Law: $I_E = I_C + I_B$

Common Emitter Configuration: $\alpha = {I_C}/{I_E}$, $\beta = {I_C}/{I_B}$, $\alpha = {\beta}/{\beta+1}$ and $\beta = {\alpha}/{1-\alpha}$

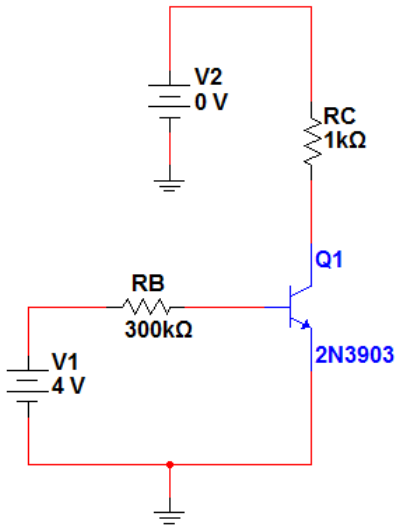


Figure 7.3 Common Collector Circuit

Procedure (Simulation and Experimental):

1. Construct the circuit as shown in Fig. 7.3. Set R_B = 300kΩ, R_C=1kΩ and use the 2N3903 BJT transistor. Let V_1 = 4 V and then record the values of I_B, I_C, I_E, β, and V_{CE} while increasing the value of V_2 from 0 V (**do not measure I_E in the lab**). Repeat with V_1 = 6, 8, and 10 V. I_B will not change much for each value of V_1. To save time in the lab, only measure I_B two or three times for each V_1 value (use the average). Table 7.1 is provided as an example for how to organize your data. Use your own judgment for how many data points to collect for each value of V_1. Make sure to collect more data around the knee of the curves as shown in Fig. 7.4. For each curve stop collecting data once it is clear that I_C is no longer increasing rapidly. Pick your last V_2 value so that your last V_{CE} value is approximately the same for each curve.

2. Draw the output characteristic curves as shown in Fig. 7.1 and 7.4 using your results. Evaluate the Q-point behavior of the NPN transistor for each characteristic curve (Note: Q-point is dependent on I_B, I_C and V_{CC}). Identify the midpoint biasing Q-point.

3. Discuss your results in the conclusion section. Explain the information that is conveyed in your characteristic curve plot. Comment on the Q-point behavior with respect to I_B, I_C and V_{CC}. Discuss β and the significance of any tends you observe.

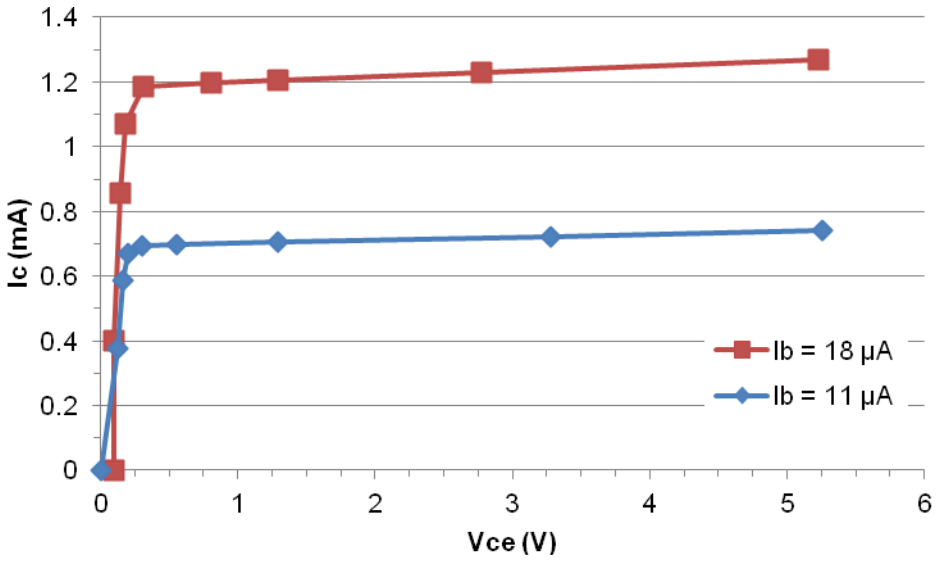


Figure 7.4 Characteristic curves for V_1 = 4V and V_1 = 6V. **You will have 4 I_B curves.**

Table 7.1 (this table is incomplete and requires additional rows for V1 = 4, 6, 8, and 10 V)

V_1 = 4V	I_B (µA)	I_C (mA)	I_E (mA)	V_{CE} (V)	β
V_1 = 6V					

BJT small signal amplification (Lab # 08):

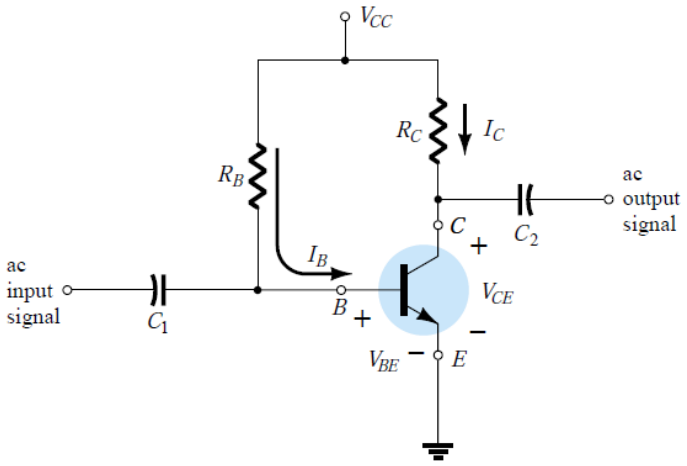


Figure 8.1 Common Collector Circuit

Procedure (Simulation and Experimental):

1. Apply a 500 mV peak-to-peak sinusoidal input signal at the given range of frequencies (see Table 8.1) to the circuit in Fig. 8.1. Use R_B = 300 kΩ, R_C = 1kΩ, C_1 = C_2 = 0.1 nF, V_{CC} = 16 V, and a 2N3903 BJT.

2. You may use a Bode plotter to find gain and then calculate V_{out} from gain. Alternatively use an oscilloscope to find V_{out} and then calculate gain (the Bode plotter is easier and faster). Plot gain in dB as a function of frequency. Make sure to label your axes and make sure that the frequency axis (the x-axis) is in log scale.

3. Provide oscilloscope displays of the input and output waveforms at the lowest and highest frequencies. Explain why the output is clipped at the higher frequencies. Identify (approximately) the frequency where clipping begins to occur. What changes to the circuit can be made to ensure no clipping occurs for the given input signal and frequency range (you may change component values and/or add or remove resistors and capacitors)? What happens to the gain of the circuit based on your answer to prevent clipping?

Table 8.1

Frequency	Vout	Gain (dB)
10		
30		
60		
100		
200		
500		
1 kHz		
2 kHz		
5 kHz		
10 kHz		
15 kHz		
20 kHz		
50 kHz		
75 kHz		
100 kHz		
150 kHz		
200 kHz		
500 kHz		
750 kHz		
1 MHz		
1.5 MHz		
2.0 MHz		

Reference:

Electronic Devices and Circuit Theory, 7th Ed. by Robert Boylestad and Louis Nashelsky.

LABORATORY # 09 and 10

Operating Characteristics of JFETs

Purpose

The concept of the junction field effect transistor (JFET) is introduced. Understanding the configuration and states of JFETs will aid in the understanding of MOSFETs which will be introduced in later labs. Both NPN and PNP constructions are considered. Constants and variables relating to JFETs are discussed and utilized to convey a full understanding of the material. JFETs have high input impedance and low output noise. These features make JFETs ideal for small signal amplification. Unlike BJTs current can flow from drain to source or vice versa equally.

Theoretical Background

Construction - A JFET is constructed with four parts: a gate region, a body region, a drain region and a source region. The body is referred to as the channel if voltage in the gate is field affected. This puts the JFET into active mode allowing current to flow through the body. For an N-channel JFET the body is a P-type material, while the drain and source are both N-type. For a P-channel JFET the body is N-type, the drain and source are both P-type. For ideal operation the material used to make the gate has no effect. Since the gate has no junctions, it can be modeled as a capacitor.

Operation - Current flows through the body/channel region if the transistor is in linear operating mode. To get the JFET into linear operating mode you must appropriately bias the gate. The gate bias creates a channel through the body allowing current to flow. The voltage needed on the gate to put a JFET into linear operating mode is known as the threshold voltage. This gate voltage can be kept close to the threshold voltage relative to the source-drain voltage in order to make the JFET act as a current controlled device. Thus, the current can be maintained regardless of the drain to source voltage.

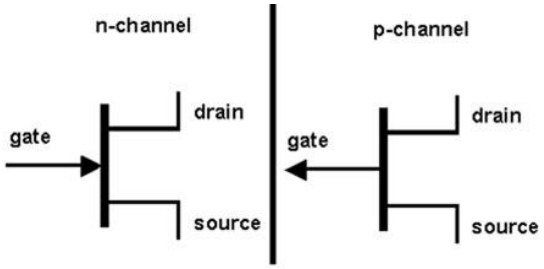


Figure 9.1 Symbolic representation

Terms

The terminals of JFETs use “D” to represent the drain, “S” to represent the source, “G” to represent the gate, and “B” to represent the body. The three operating states are known as Ohmic (linear), Saturation, and pinch-off. The threshold voltage (V_{TH}) is used to represent the minimum value of the voltage required between the gate and source (V_{GS}) in order to allow current to pass through the body. The pinch off voltage (V_P) is the voltage beyond which the source current is constant (JFET is in saturation). V_P is defined when the gate to source voltage is zero.

Output characteristic V-I curves of a typical JFET:

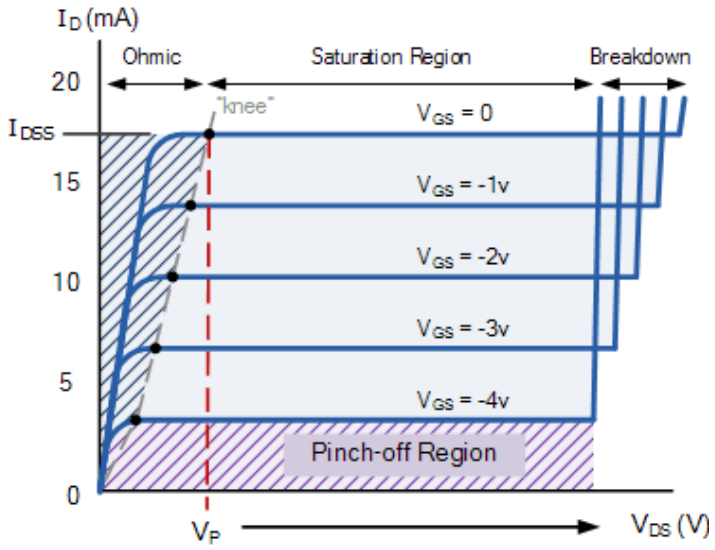


Figure 9.2 Drain Characteristics

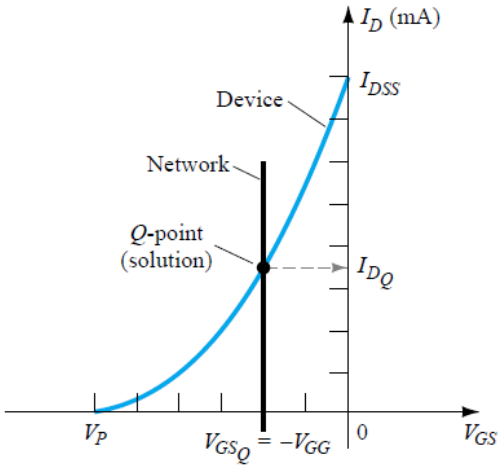


Figure 9.3 Transfer Characteristics

Circuit

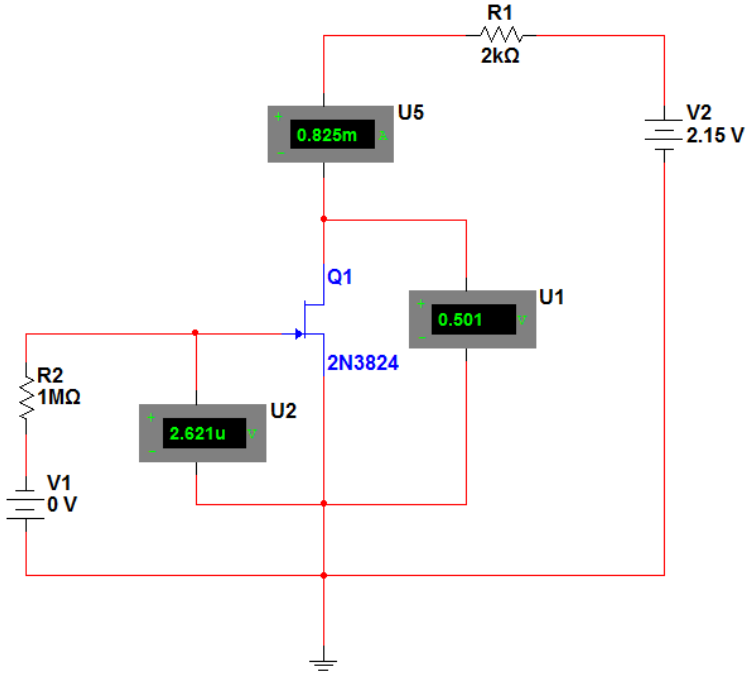


Figure 9.4 JFET (2N3824) circuit

Tables:

Table 9.1

Drain Characteristic (NPN 2N3824)			
	V_{GS} = 0 V	**V_{GS} = -0.5 V**	**V_{GS} = -1 V**
V_{DS} (V)	**I_d (mA)**	**I_d (mA)**	**I_d (mA)**
0			
0.5			
1			
2			
4			
8			
12			
16			
20			

Table 9.2

	V_{DS} = 6V
V_{GS} (V)	I_d (mA)
0	
-0.5	
-1	
-1.5	
-2	

Procedure

1) Construct the circuit provided in Fig 9.4 and use the n-channel JFET 2N3824 in Multisim and 2N3819 in lab.

2) Obtain data to produce drain characteristic curves:
   a) Measure I_d for the values of V_{DS} indicated in Table 9.1 (note: you need to adjust V_2 in order to set V_{DS} to the values in the table. Thus, V_2 does not equal V_{DS}). While you do this adjust the value of V_1 as needed to keep V_{GS} = 0V.
   b) Repeat with V_{GS} = -0.5V and -1.0V
   c) Plot the data you recorded in Table 9.1. Your results should look like Fig 9.2. Based on your plot, estimate V_P and V_{TH}. Mark V_P on your plot.

3) Obtain data to produce a transfer characteristic plot
   a) Set V_2 so that V_{DS} = 6V
   b) Adjust the value of V_1 to obtain the values of V_{GS} in Table 9.2. For each V_{GS} measure I_d. Your final value for I_d should be 0 mA. If you do not get I_d = 0 mA (or very close to it) then continue decreasing V_{GS} below -2V until I_d reaches 0 mA.
   c) Plot your results and estimate V_P. Mark V_P on your plot. Compare your estimation of V_P in your drain and transfer characteristic analyses.

Reference:

Electronic Devices and Circuit Theory, 7th Ed. by Robert Boylestad and Louis Nashelsky.

Small Signal Amplification with JFETs (Lab 10)

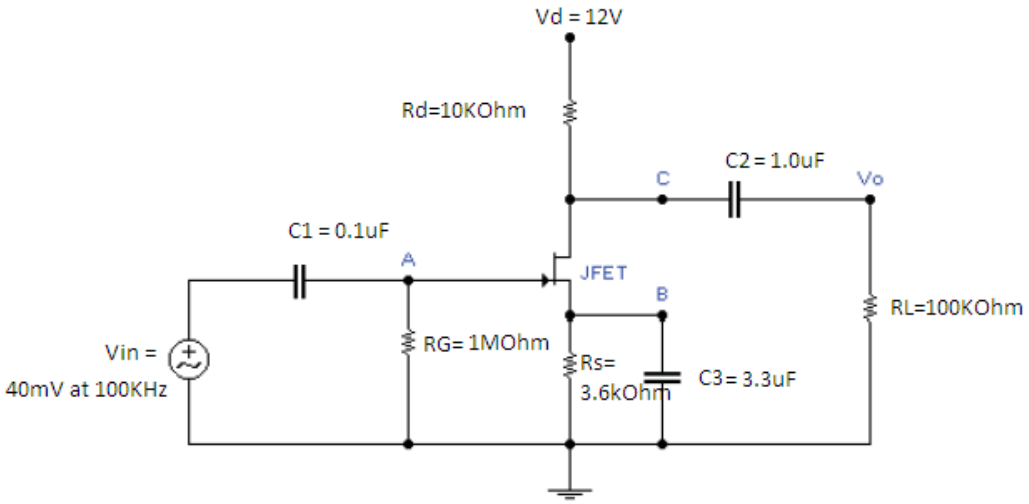


Figure 10.1

Procedure:

1 Build the circuit as shown in Fig. 10.1 in Multisim. Apply a small sinusoidal signal (Vpp=40mV) at the given frequency range (See table 10.1) using JFET 2N3824 (2N3819 in lab).

2 Based on your Table 10.1 results, plot voltage gain as a function of frequency and calculate the bandwidth. Identify the high and low cutoff frequencies. Note: plot frequency on a log scale.

   a. In the lab the frequency generator has a maximum output frequency of 3 MHz and a minimum output voltage greater than 40 mV peak-to-peak. However, the 2N3819 that you will use in the lab has a much smaller bandwidth than the 2N3824 that you will simulate.

   b. For the lab apply the minimum amplitude allowed by your frequency generator. Create your own table similar to Table 10.1 but with a maximum frequency of 3 MHz. Make sure you collect enough data points to plot the frequency response of the circuit in Fig. 10.1.

3 Comment on the phase relationship between the input and output waveforms

4 Compare and discuss your experimental and simulation results.

Table 10.1

Frequency (Hz)	Vout (mV)	Gain
30		
45		
60		
100		
200		
500		
1000		
10000 (10 kHz)		
100000 (100 kHz)		
500000		
1000000 (1MHz)		
1500000		
2000000		
3000000		
4000000		
5000000		
7000000		
10000000 (10MHz)		
11000000		
12000000		
15000000		
16000000		

Lab 11 and 12 MOSFETs

Lab 11

Introduction

The MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is a three terminal unipolar semiconductor. The MOSFET is a voltage controlled field effect transistor that differs from a JFET in that it has a metal oxide gate electrode which is electrically insulated from the main semiconductor N-channel or P-channel by a thin layer of insulating material. Thus, the gate terminal is isolated from the main current carrying channel, and no current flows into the gate. Just like the JFET, the MOSFET acts like a voltage controlled resistor where the current flowing through the main channel between the drain and source is proportional to the input voltage. MOSFETs operate in two different modes. In depletion mode, the transistor requires the Gate-Source voltage, (V_{GS}) to switch the device OFF. The depletion mode MOSFET is equivalent to a normally slosed switch. In the enhancement mode, the transistor requires a gate-source voltage, (V_{GS}) to switch the device ON. The enhancement mode MOSFET is equivalent to a normally open switch.

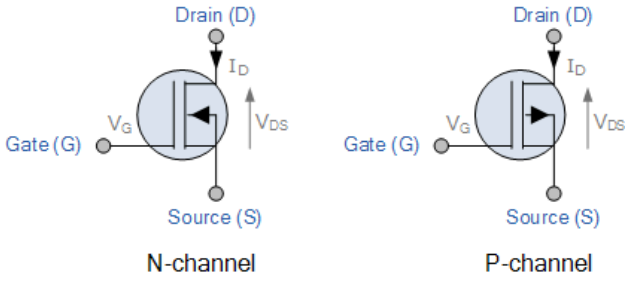


***Figure 11.1** Symbolic representation of MOSFET.

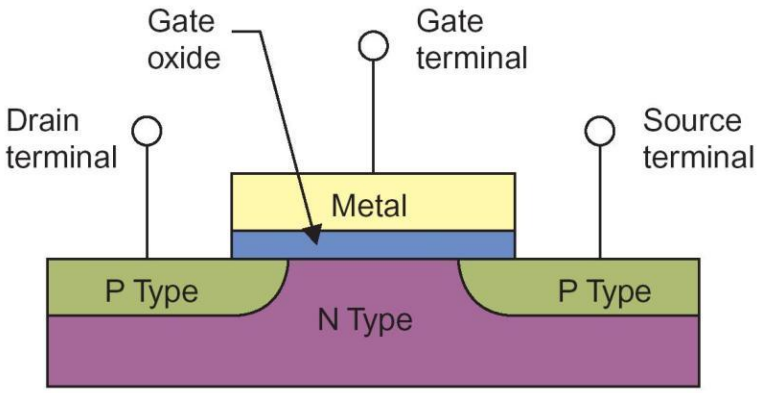
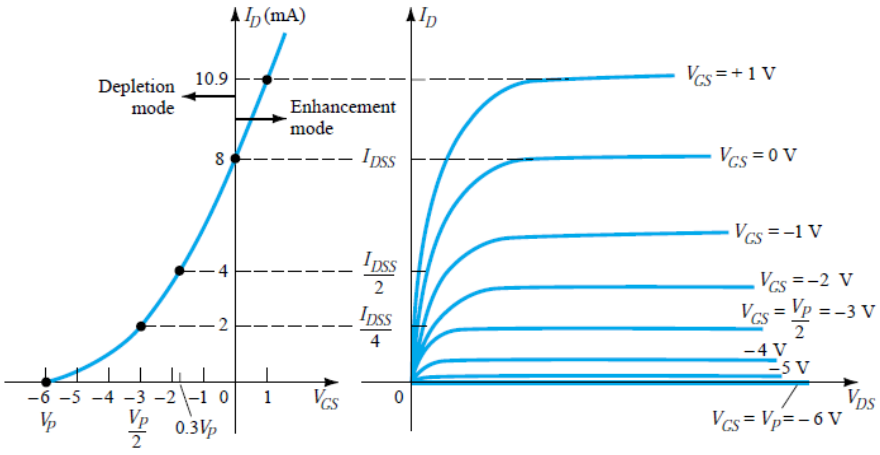
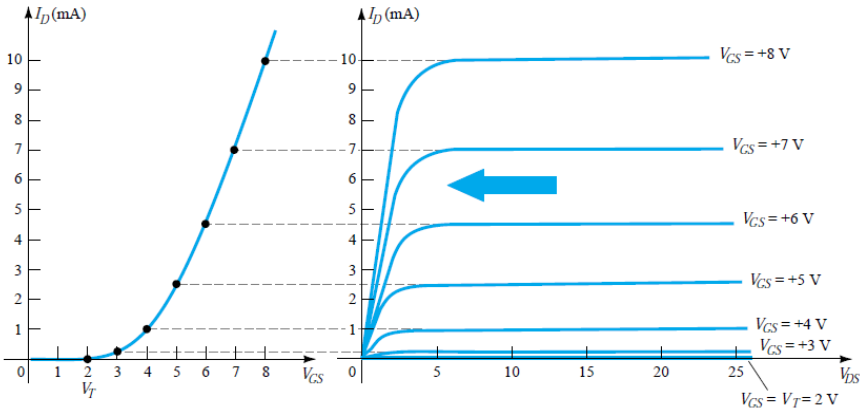


***Figure 11.2** Structural diagram of N-channel MOSFET

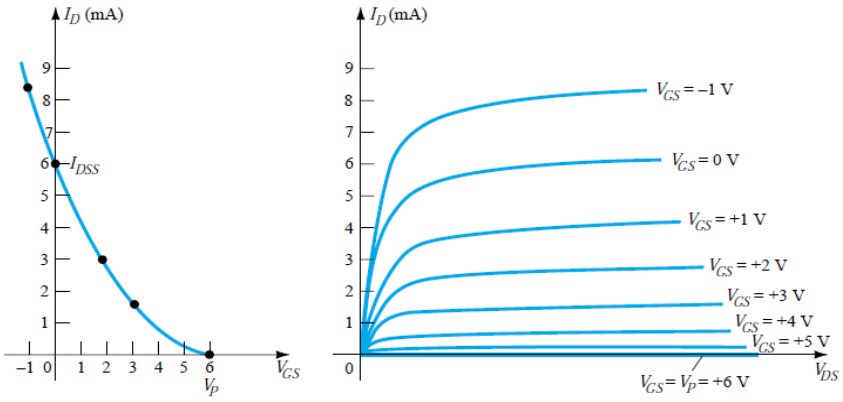


(a)

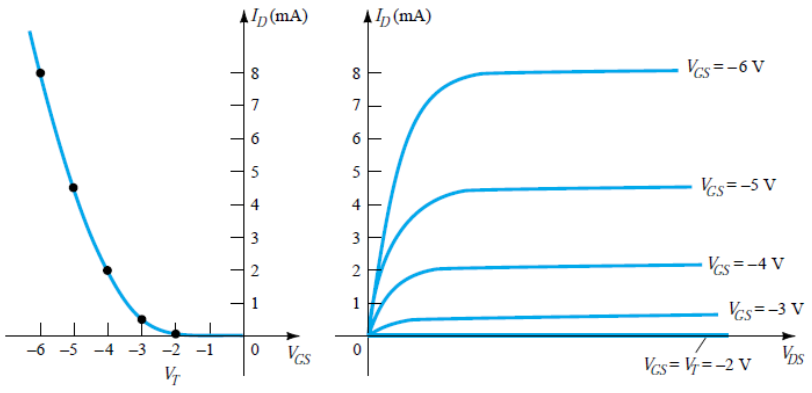


(b)

***Figure 11.3** N-Channel MOSFET (a) Depletion Mode (b) Enhancement Mode.



(a)



(b)

***Figure 11.4** P-Channel MOSFET (a) Depletion Mode (b) Enhancement Mode.

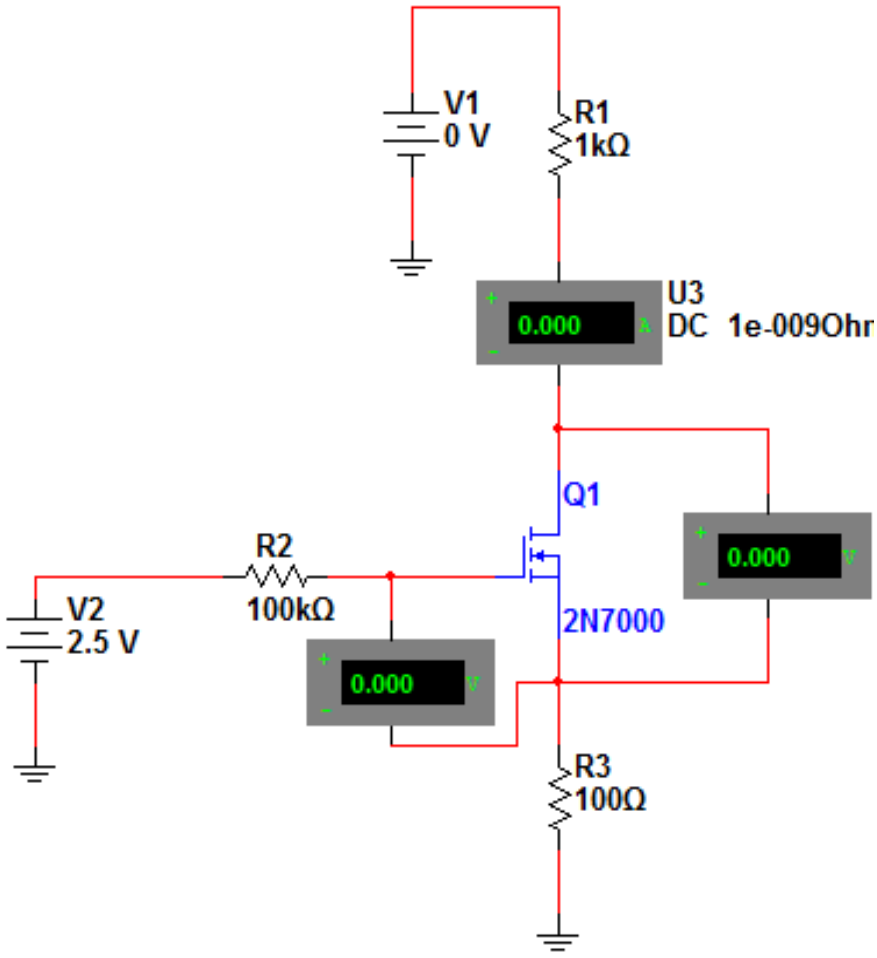


Figure 11.5

V_2 = 2.5V		V_2 = 3V		V_2 = 3.5V		V_2 = 4V	
V_{ds}	V_{gs} =	V_{ds}	V_{gs} =	V_{ds}	V_{gs} =	V_{ds}	V_{gs} =
(mV)	I_d (mA)	(mV)	Id (mA)	(mV)	Id (mA)	(mV)	Id (mA)

Table 11.1

V_{gs} (V)	I_d (mA)

Table 11.2

Part 1

- Construct the circuit in Figure 11.5 using the 2N70000 MOSFET.
- Set V_2 = 2.5V and then starting with V_1 = 0V, increase the value of V_1 until I_d saturates. While adjusting the value of V_1, measure V_{GS}, V_{DS}, and I_d and record your results in Table 11.1. Repeat with V_2 = 3, 3.5, and 4V. Note: V_{DS} is not equal to V_1, and V_{GS} is not equal to V_2. **Note: create your own table as you will need more rows than are provided in Table 11.1**. Use your best judgment for how many data points to collect. Make sure to collect more data points in the non-linear regions.
- Plot the results that you have recorded in Table 11.1.
- Using your plot for Table 11.1 for each V_{GS} value, identify the V_{DS} range for which the MOSFET is in the linear ohomic region (i.e. where the MOSFET behaves like a voltage controlled resistor).
- For each V_{GS} value, identify the minimum V_{DS} value that places the MOSFET in saturation.

Part 2

- Construct the circuit in Figure 11.5 and set V_1 = 22V.
- Record the value of V_{GS} and I_d in the first row of Table 11.2 when V_2 = 0V. Fill out the rest of Table 11.2 by varying the value of V_2 from 2V in 0.25V increments until I_d no longer increases.
- Plot the results that you have recorded in Table 11.2.
- Using your plot from Table 11.2, identify the threshold voltage (i.e. the minimum V_{GS} needed for the MOSFET to conduct). Mark the threshold voltage on your plot.

- Based on your plots and Figures 11.3-11.4, is the 2N7000 an enhancement or depletion mode MOSFET? Is it an n-channel or p-channel device (NMOS or PMOS)?

Bonus Points (up to 100): Compare your MOSFET, JEFT (lab 9), and BJT (lab 7) results and identify the reasons these devices behave differently. What are the MOSFET vs. JFET vs. BJT pros and cons?

Reference:

*Electronic Devices and Circuit Theory, 7th Ed. by Robert Boylestad and Louis Nashelsky.

Lab 12

The purpose of this lab is to examine the bandwidth of the 2N7000 MOSFET with a range of frequencies from 10Hz to 3MHz. For each frequency the input and output voltages of the circuit will be measured. Finally, after a plot of the frequency vs. the gain is made, the bandwidth will be measured.

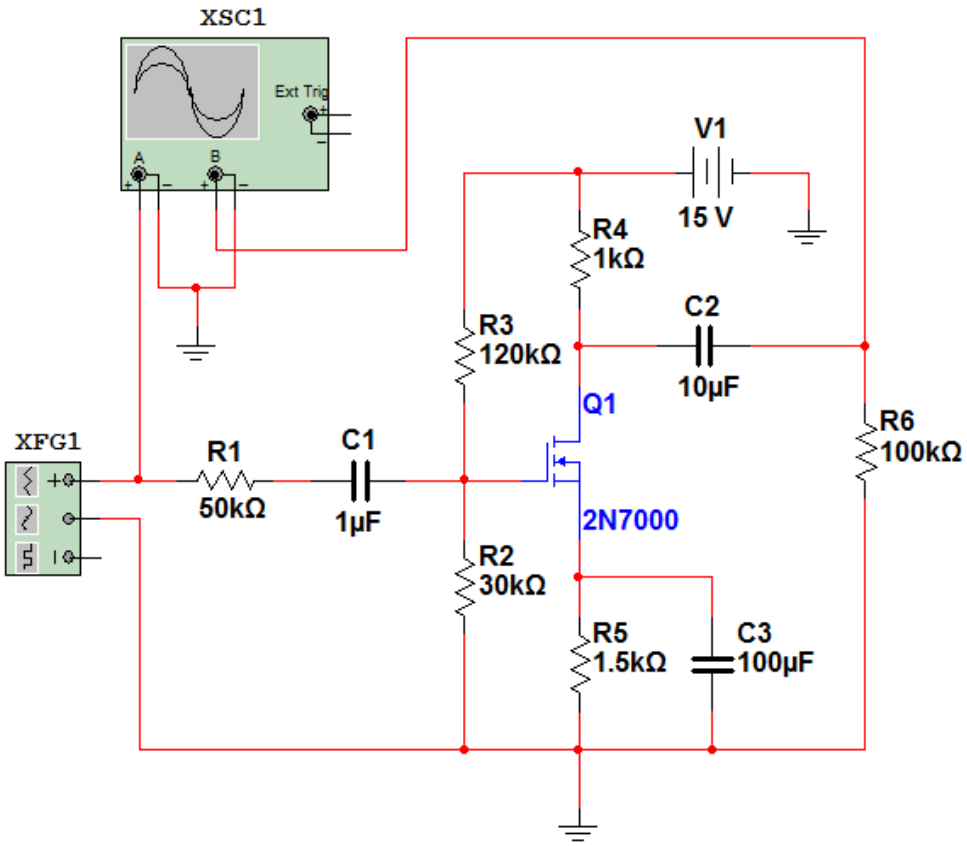


Figure 12.1

Procedure:

1. Build the circuit as shown in Figure 12.1 and amplify a sinusoidal signal with V_p = 100mV for the given frequency range (See table 12.1) using MOSFET (2N7000). In lab use the smallest amplitude that your function generator will output.

2. Based on Table 12.1 results, plot voltage gain as a function of frequency. Calculate the approximate bandwidth and identify f_{low} and f_{high}.

3. Comment on the phase relationship between the input and output waveforms.

Bonus (up to 50 points, simulation only): Connect a Bode plotter to the input and output. For Mode select Magnitude and for Horizontal and Vertical select Log. Under Horizontal set F to 3 MHz and I to 10 Hz. For Vertical set I to -30 dB and F to 30 dB (you may need to adjust the I and F settings for Vertical as you go). Modify the circuit to maximize the bandwidth **while keeping the gain above 10 dB** within the pass band of the circuit. You may change the value of V_1 or any of the capacitors or resistors (**except the load resistor**, R6). You may also add or remove resistors and capacitors. Use the oscilloscope to verify that the output is not clipped for input frequencies within the circuit's bandwidth. Two example Bode plots are provided for clarification. **Submit and discuss your modified circuit in the lab report (not the prelab). No credit will be given if you do not submit your modified circuit diagram.**

Bonus (up to 100 points): Compare MOSFET signal amplification to JFET (Lab # 10) and BJT (Lab # 08). What are the pros and cons of using MOSFETs, JFETs, and BJTs?

Table 12.1

Frequency	Vout	Voltage Gain
10		
30		
60		
100		
200		
500		
1 KHz		
2 kHz		
5 KHz		
10 KHz		
15 KHz		
20 KHz		
50 KHz		
75 KHz		
100 KHz		
150 KHz		
200 KHz		
500 KHz		
750 KHz		
1 MHz		
1.5 MHz		
2.0 MHz		
3.0 MHz		

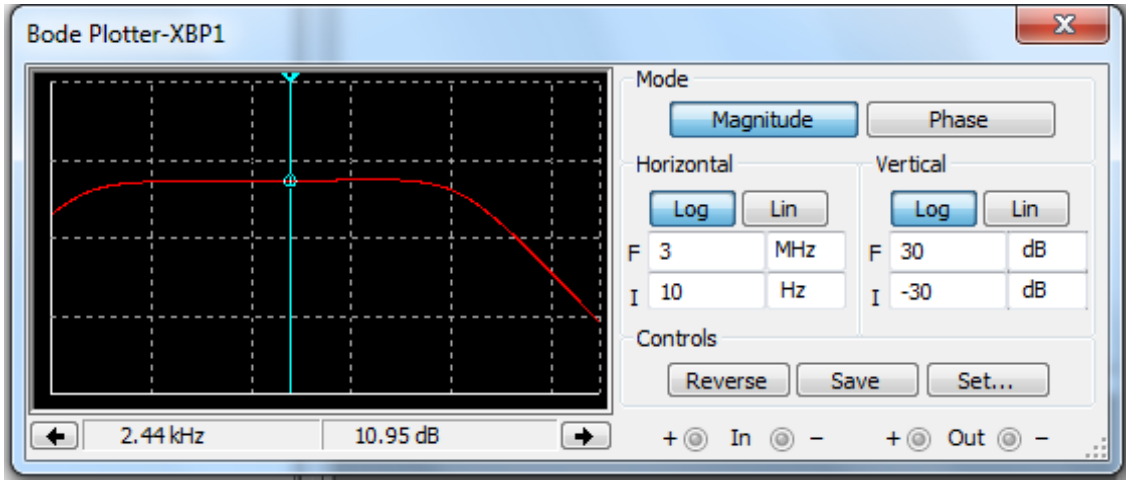


Figure 12.2 Bode plot for circuit as given

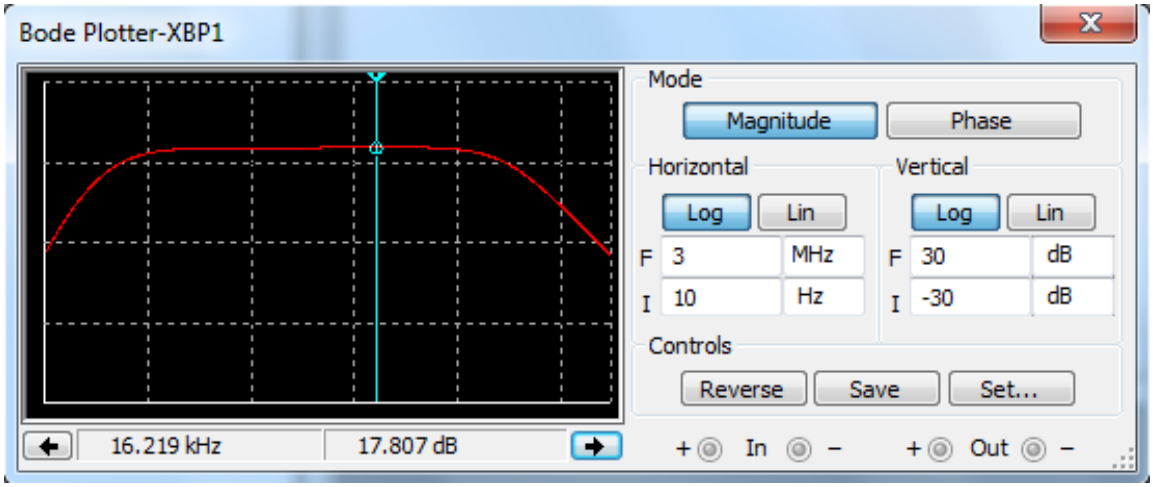


Figure 12.3 Bode plot for a modified circuit

The circuit that produced the Bode plot in Figure 12.3 has a bandwidth 162 kHz wider and a gain nearly 7 dB higher than the given circuit. You should be able to do better than Figure 12.3. Remember to use the oscilloscope to verify that the output is not clipped for input frequencies at f_{low} and f_{high}.