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CPE 324-02: Advance Logic Design Laboratory

Lab 1

Quartus tutorial and DE10-Lite setup.

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1. Introduction:

1.1 What is to be studied, what is the purpose, and how is this purpose accomplished?

The purpose of this experiment is to study the quartus tutorial PDF file on canvas using the lab1.bdf in lieu of the one provided in the tutorial. This is accomplished by reading and following the tutorial closely and replacing section 5 with lab1.bdf.

2. Experiment Description

2.1 Theory, analysis, and purpose:

No laboratory manual was provided to write theory or analysis on, however, the purpose is to learn how to use the Quartus software with the DE10-Lite board.

However, I will cover NAND gates and OR gates briefly as they are implemented in the design. A NAND gate will produce a false output IFF all the inputs are true. Or gates are true if one or more input is true, and false IFF all inputs are false.

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1
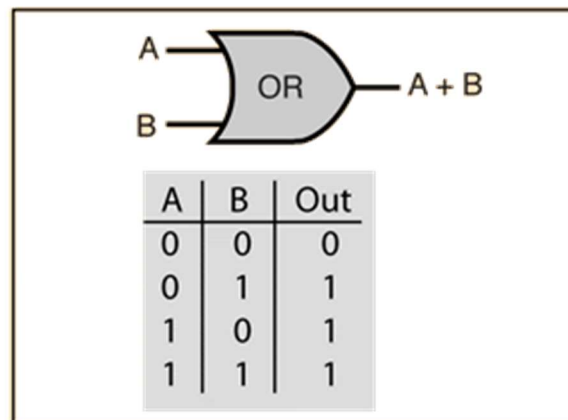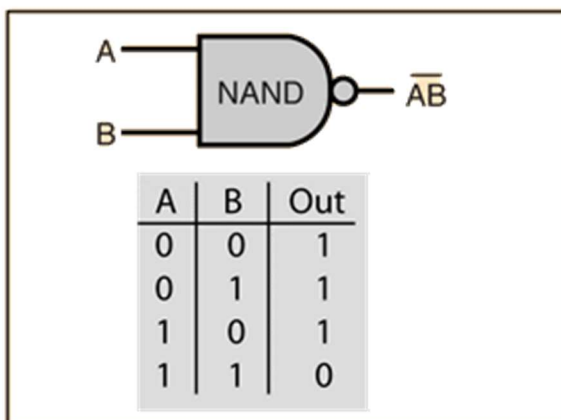
2.2 Design and implementation procedure:

The design for this laboratory is provided as lab1.bdf on canvas, therefore I have no design or implementation procedure. A screenshot of the design is provided below:
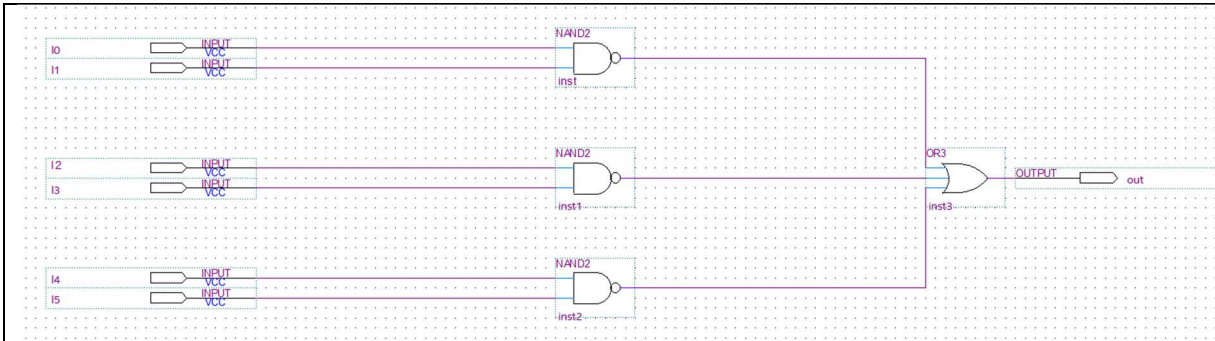

Figure 1.1

3. Demonstration

3.1 Implementation method:

Since there was little direction for this lab, I am inserting my own values for my Waveform file, as shown in the following screenshot:
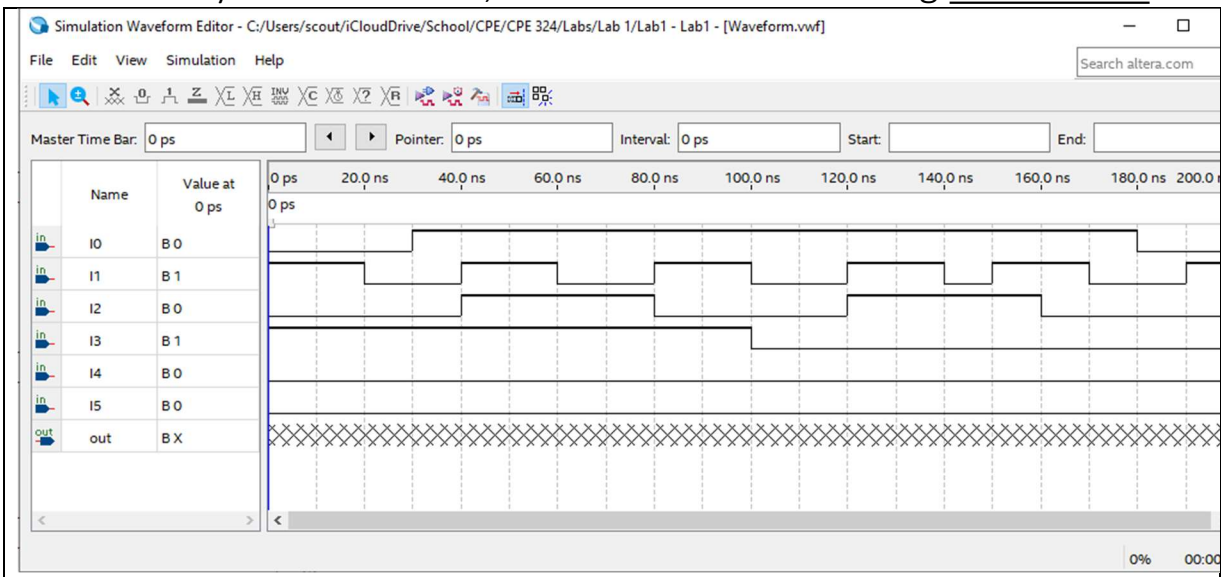

Figure 1.2

3.2 Video Link:

The following video provides a quick demonstration of the lab results:

https://drive.google.com/file/d/1Azg2ngL3d_TQ1Ro0ZX0vyw7z0uBXju
EF/view?usp=sharing

4. Experimental Results

4.1 Waveform Output:

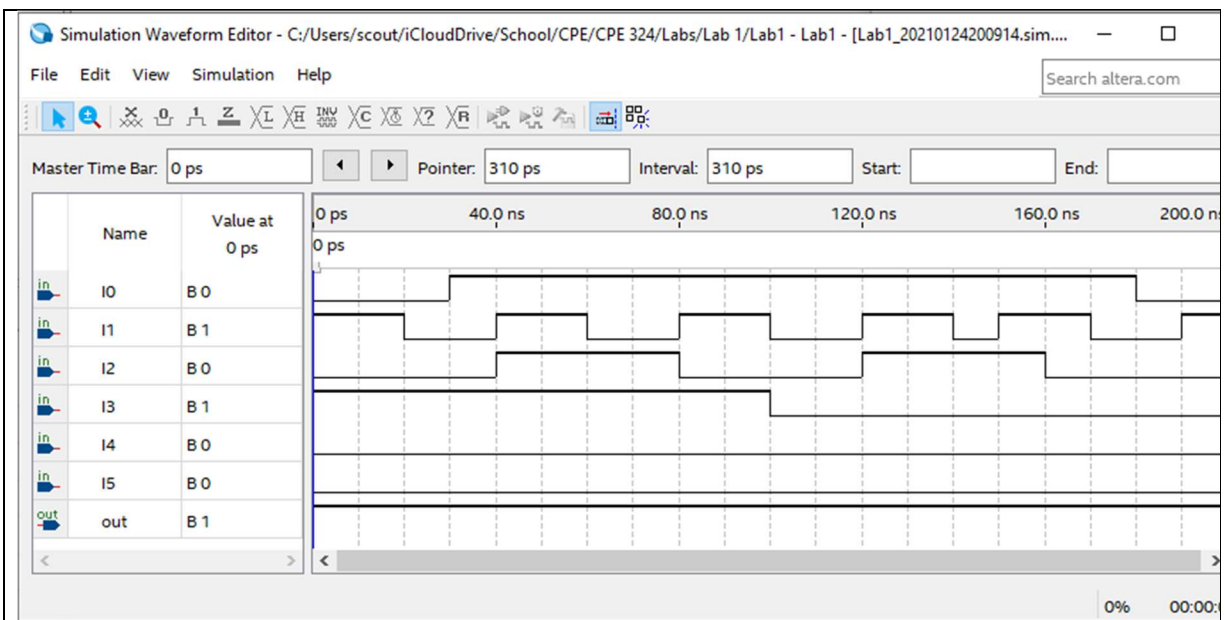The following output was produced using the inputs as shown in figure 1.2:

Figure 1.3

4.2 Observations:

Due to the OR gate, "inst3", on figure 1.1, if a value seen after inst, inst1, or inst2 is high, the output will always be high. On the contrary,

if and only if all three of the logic gates are low, then the output will also be low. Because one value is always high as shown in figure 1.3, the output will always be high. In summary, if you want a low output, every input value needs to be a one. I will now provide a screenshot to show this:
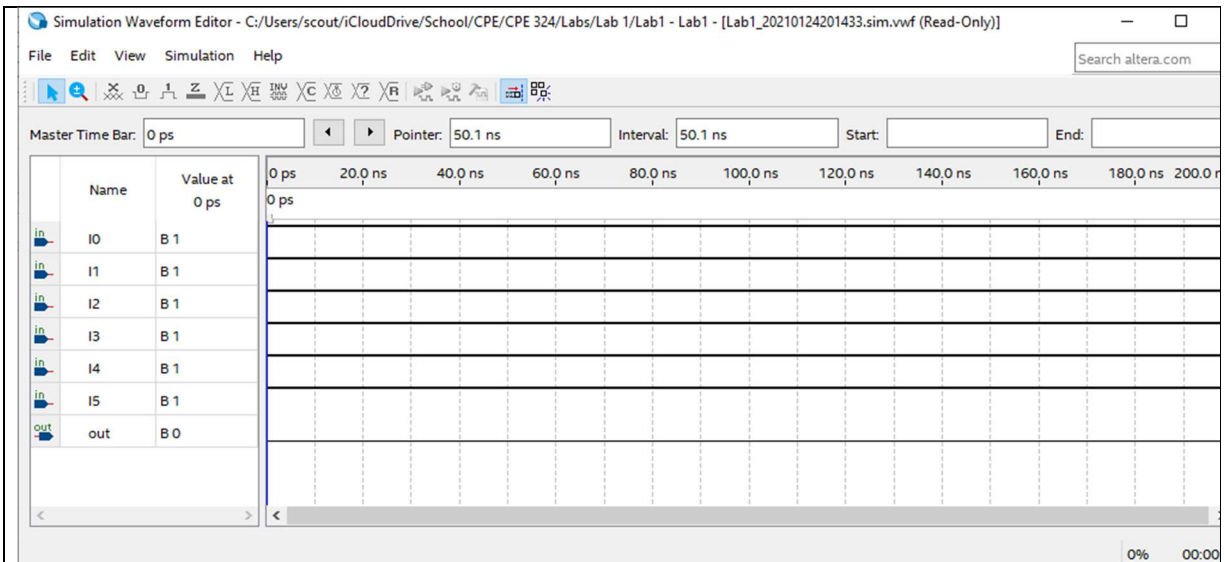

Figure 1.4.

As you can see in figure 1.4, if all input values are high, the output will be low. If any value is changed to low, at that point the output will be be high:
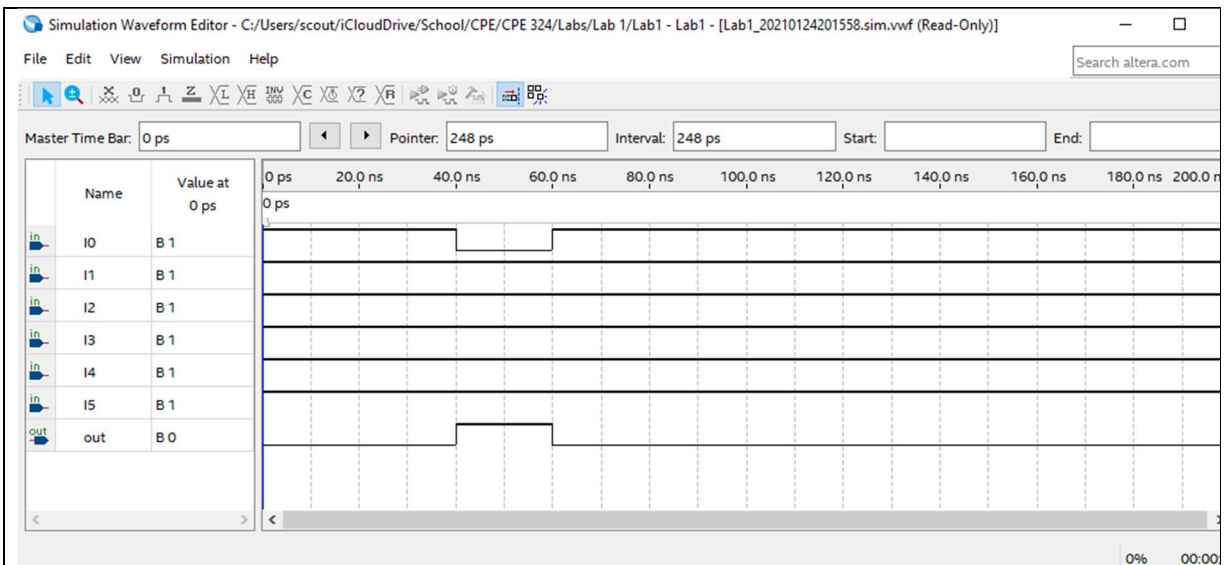
Figure 1.5

Functionally, this design would be useful for provided results under very specific guidelines. For example, a backup generator will only shut down if everyone one of the error messages are indicated. Otherwise, it is still safe to run.

4.3 Questions:

No laboratory manual was provided thus no questions were provided to be answered.

4.4 Pre-Laboratory results:

No laboratory manual was provided thus a pre-lab does not exist so I do not have results to provide.

4.5 Post lab questions:

No laboratory manual was provided thus no post lab questions were provided to be answered.

5. Conclusions

5.1 - Results and lessons learned:

During this lab, I learned how to create a Quartus project using my DE10-lite board. I also learned how to develop a waveform file to get an output for the design. I also refreshed my knowledge on logic gates, inputs, and outputs.