

# Cover Page

EE 316-08

## Electric Circuits & Electronics Design Lab

### **Lab 9 & 10: Operating Characteristics of JFETs**

By: Nolan Anderson

Lab Date: 04/4/2021

Lab Due: 04/6/2021

## 1. Introduction:

Labs 9 and 10 aim to build the students conceptual knowledge of field effect transistors. Understanding this material is imperative to understanding MOSFETs later on. JFETs have high input impedance and low output noise. These features make them ideal for small signal amplification. I will first cover the theory behind JFETs in section 2 and present my results in section 3. Finally, section 5-6 will discuss the results.

## 2. Theoretical Analysis:

### 2.1 Junction Field-Effect Transistors (JFETS)

These devices are used to control switches, voltage-controlled resistors, and amplifier controls. They consist of a gate (G), drain (D), and source (S) and have two configurations, n and p channel.

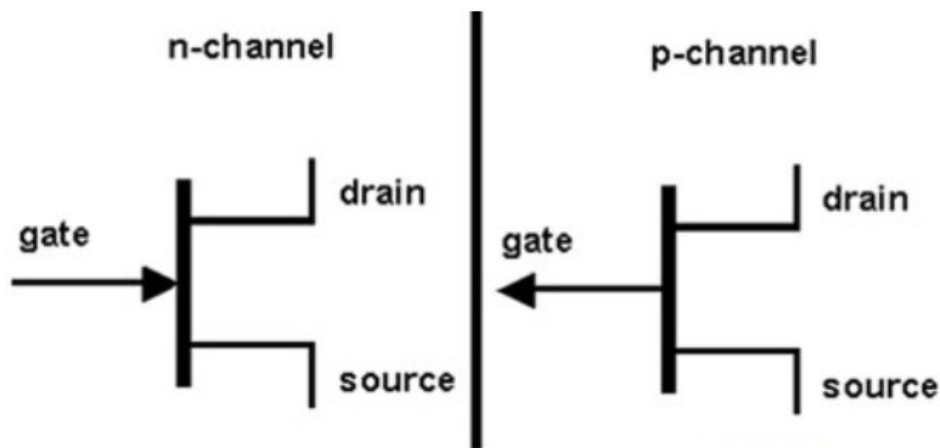


Figure 2.1 Symbolic Representation of JFETS

- N-channel: current flows into the channel region at the drain side and comes out at the source side. When a negative voltage is applied, the gate side reduces current flow from drain to source.
- P-channel: Current flows into the channel region at the source side and comes out the drain side. A positive voltage applied at the gate side reduces current flow from source to drain.
- Ohmic Behavior: JFET behaves like a voltage-controlled resistor. (1)
- Saturation Behavior: The drain current is strongly influenced by gate-source voltage but not influenced by drain-source voltage. (2)
- Pinch-off Behavior: Acts like an open circuit where no current is flowing through the device. (3)
- Breakdown behavior: Loses the ability to resist current because too much voltage applied across the drain-source terminals. (4)

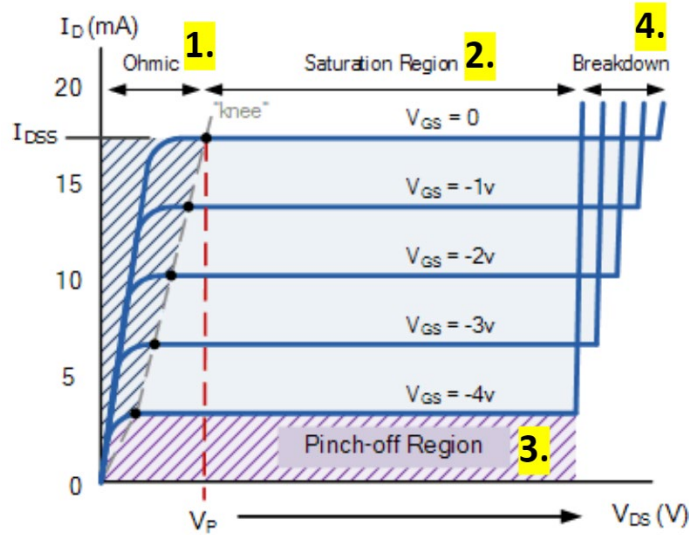
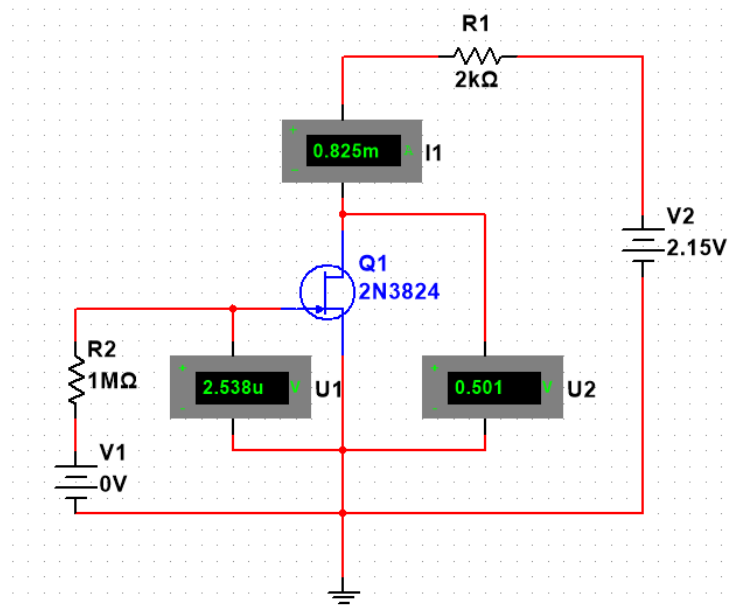


Figure 2.2 Operating states

- Threshold voltage: Used to represent the minimum voltage required between the gate and source in order to allow current to pass through the body.
- Pinch of voltage is the voltage beyond which the source current is constant. It is defined when the gate to source voltage is zero.

### 3. Simulations:

#### 3.1 Common collector circuit (Lab 7)



Circuit 9.1 JFET Circuit

VDS (V)	Id (mA) @ VGS = 0V	Id (mA) @ VGS = -0.5 V	Id (mA) @ VGS = -1 V
0	0	0	0
0.5	0.823	0.605	0.387
1	1.434	0.998	0.561
1.5	1.829	1.171	0.57
2	2.006	1.183	0.572
2.5	2.02	1.187	0.574
3	2.025	1.19	0.576
3.5	2.031	1.193	0.576
4	2.036	1.196	0.578
5	2.046	1.203	0.581
6	2.058	1.21	0.584
7	2.069	1.216	0.588
8	2.078	1.222	0.591
12	2.123	1.247	0.602
16	2.165	1.272	0.615
20	2.213	1.3	0.629

Table 9.1 Drain Characteristics

VGS (V)	Id (mA) @ VDS = 6V
0	2.058
-0.5	1.22
-1	0.593
-1.5	0.188
-2	0.011

Table 9.2 Transfer Characteristic

### 3.2 Small Signal Amplification

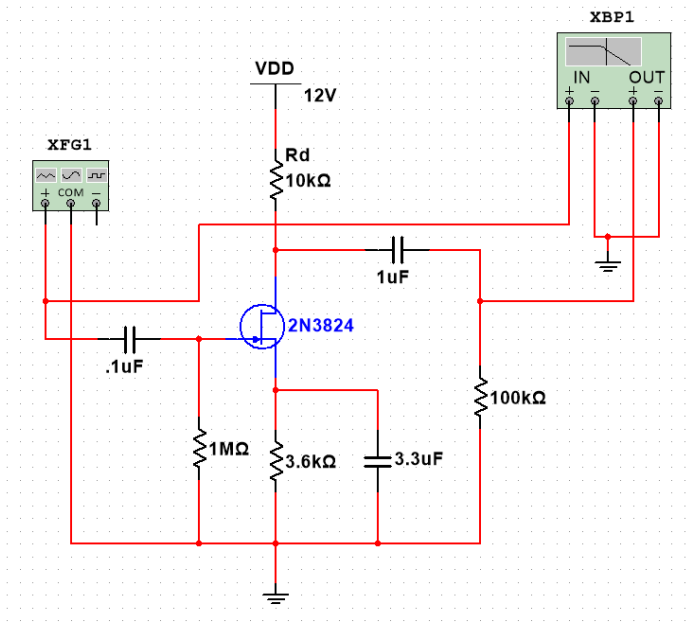


Figure 10.1 Small Signal Amplification

Frequency (Hz)	Vin (mV)	Vout (mV)	Gain
30	40	158.62	11.97
45	40	196.63	13.83
60	40	221.72	14.87
100	40	256.01	16.12
200	40	276.48	16.79
500	40	283.18	17.00
1000	40	284.39	17.04
10000	40	284.71	17.05
100000	40	284.71	17.05
500000	40	284.45	17.04
1000000	40	283.57	17.01
1500000	40	282.17	16.97
2000000	40	280.13	16.91
3000000	40	274.8	16.74
4000000	40	268.02	16.52
5000000	40	259.13	16.23
7000000	40	241.38	15.61
10000000	40	212.43	14.50
11000000	40	202.91	14.10
12000000	40	194.94	13.76
15000000	40	170.02	12.57

16000000	40	163.72	12.24
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Table 10.1 Gain as a Function of Frequency

#### 4. ~~Experimental:~~

We were not instructed to provide experimental results for this lab, see the following screenshot.

### Summary

- Lab 9 and 10 Report is due Tuesday 6<sup>th</sup> April 2021 by midnight.
- Prelab 11 and 12 is due Tuesday 13<sup>th</sup> April 2021 by midnight.
- Fill out Table 9.1, 9.2 and 10.1 with results from...
  - Simulation
  - • ~~Experimental results~~

## 5. Results and Discussion:

### 5.1 Lab 9 Plots

Figure 5.1 shows the plot for Table 9.1 and figure 5.2 shows the plot for Table 9.2.

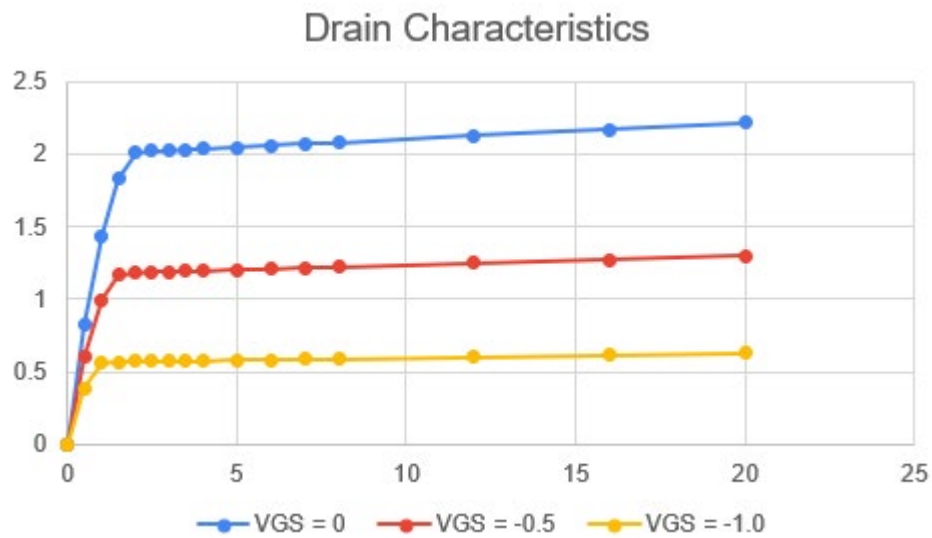


Figure 5.1: Drain Characteristics Curves

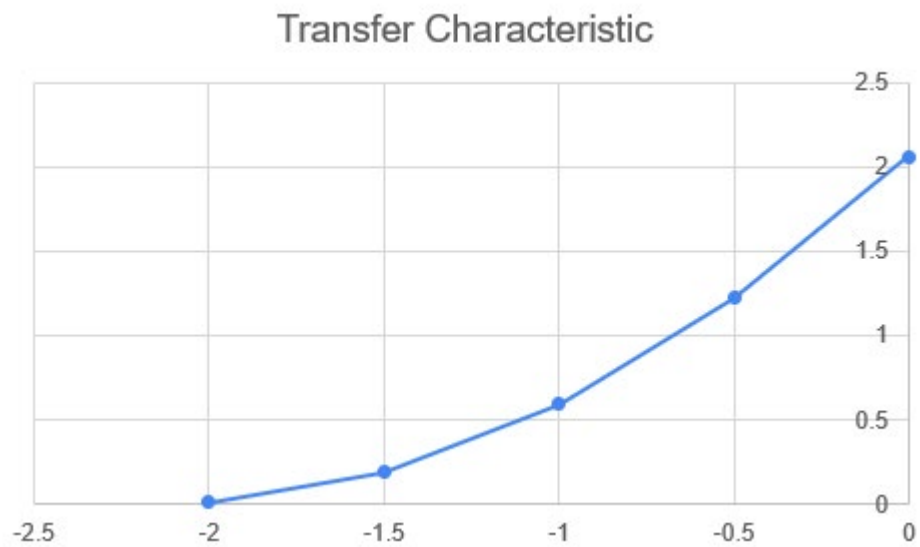


Figure 5.2: Transfer Characteristic Curves

## 5.2 Lab 10 Questions

Figure 5.3 shows the voltage gain plot for table 10.1, and questions 3 & 4 from the lab report are also answered below that.

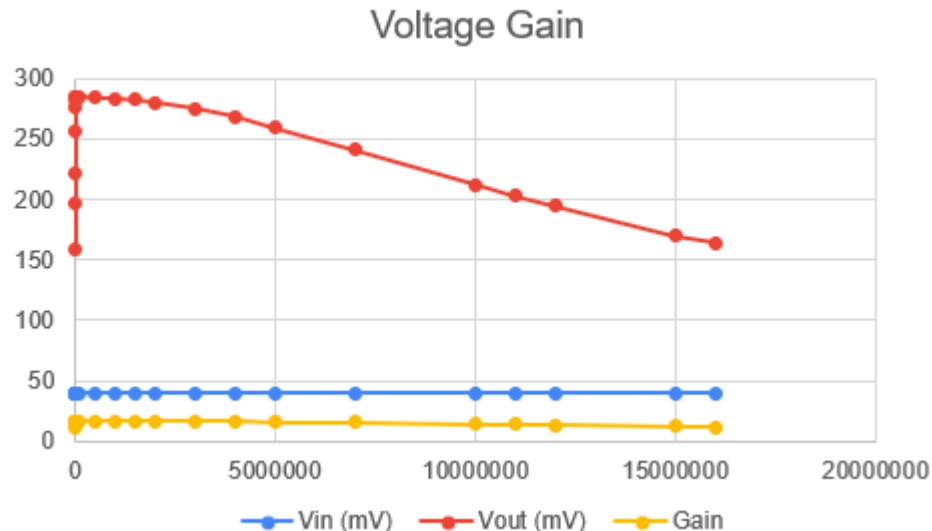


Figure 5.3, voltage gain plot for table 10.1

3: Comment on the phase relationship between the input and output waveforms.

As the frequency metric grew, the output voltage and gain became to fall. Gain did not fall the whole time, however (see table 10.1). Overall though, as the frequency increased, gain and output voltage decreased.

4. Compare and discuss your experimental and simulation results.

We did not do any experimental calculations, but the results lie closely with the expected output for a voltage gain plot for small signal amplification. As the frequency gets higher, the signal cannot keep up.

## 6. Conclusion:

Labs 9 and 10 increased my understanding of JFETS very well. Being able to see these circuits work with different inputs and analyzing the outputs made me realize how powerful these circuit elements can be.