CPE 323
Intro to Embedded Computer Systems
Interrupts (Exceptions)

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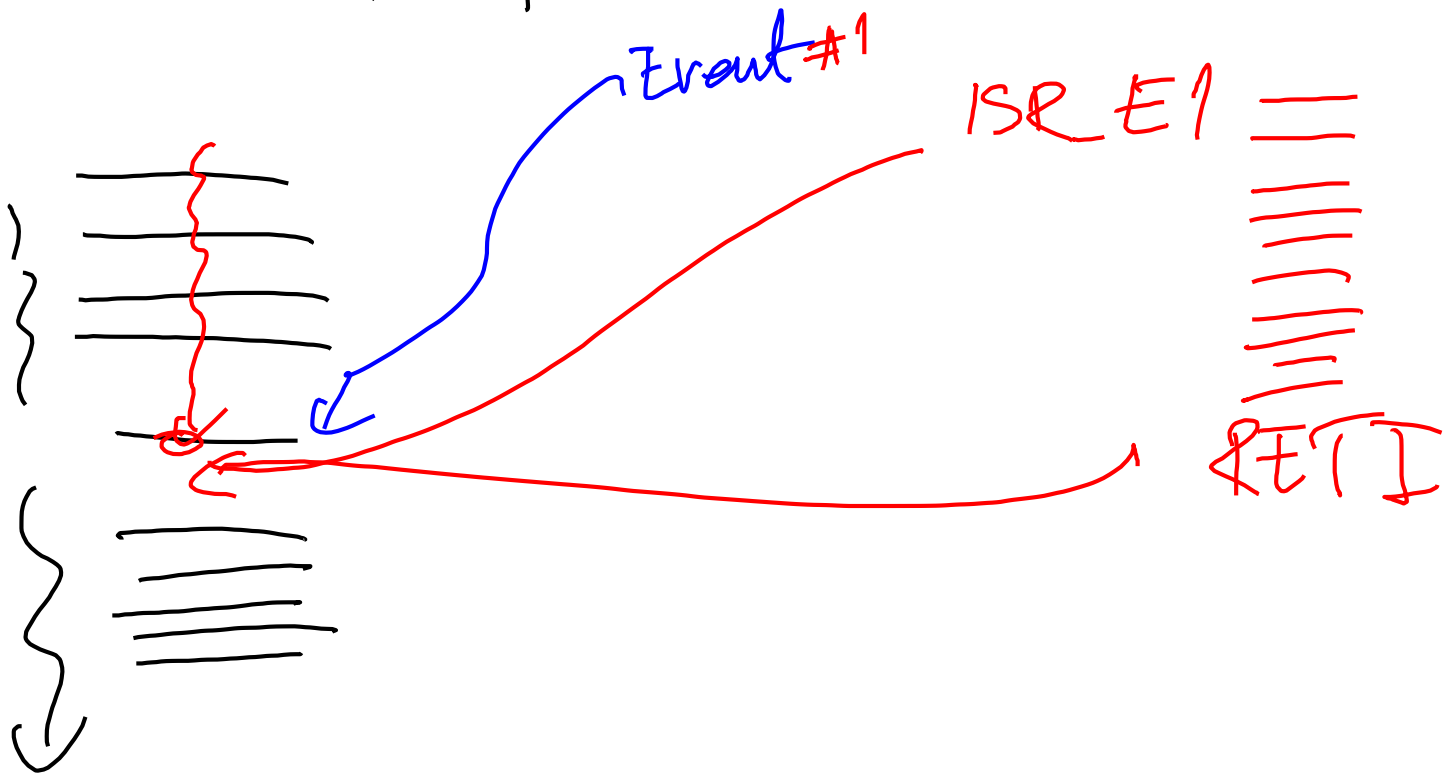
Admin

Instruction Execution Stages

- 1. Instruction Fetch
- 2. -11- Decode
- 3. Operand Fetch
- 4. Execute
- 5. Store Results
- 6. Exception Processing

What are Interrupts?

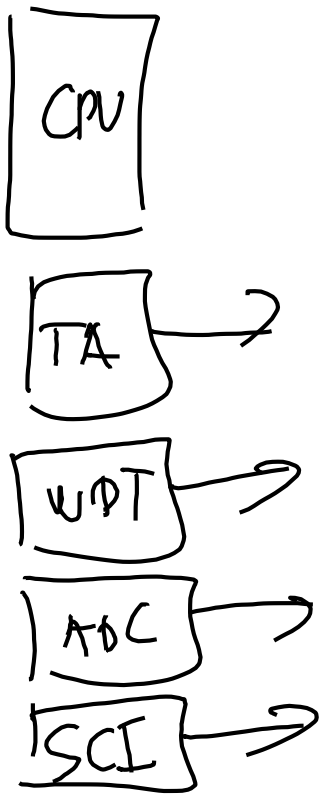
→ Events (asynchronous) triggered in hardware



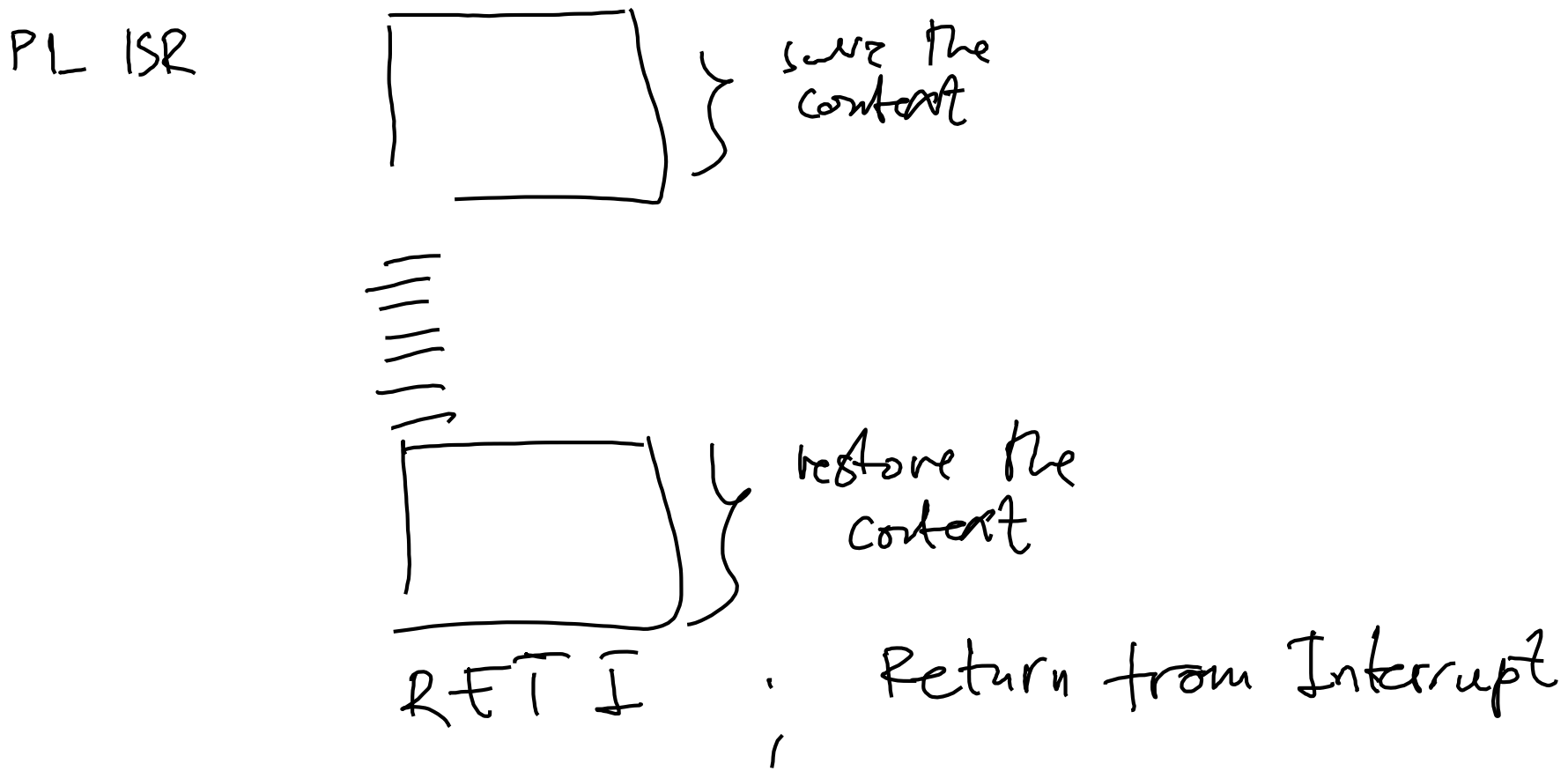
Sources of Interrupts

→ internal to CPU

→ external (peripherals) → polling
→ interrupt



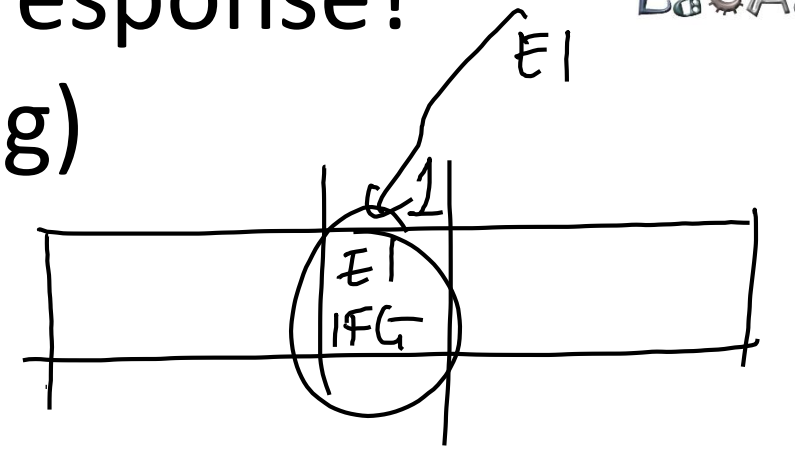
Interrupt Service Routine (ISRs)



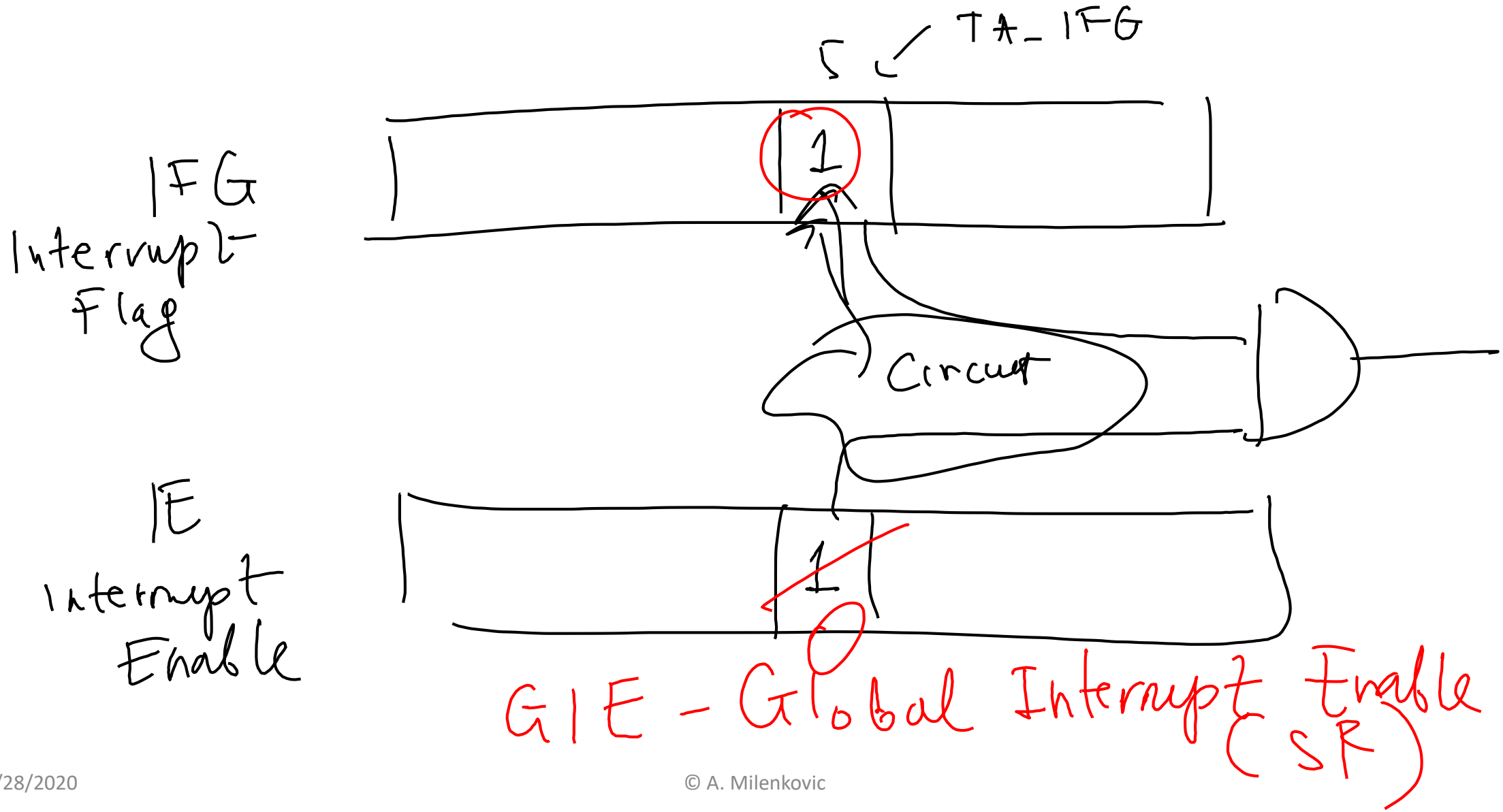
What does MSP430 do as a response? (Exception Processing)

- 1. Finish instruction execution
- 2. Push PC + SR
- 3. Clear SR
- 4. Select highest prority interrupt
- 5. Clear IFG bit for single-source interrupts
- 6. Read the starting address of the corresponding ISR from the IVT (interrupt vector table)
- 7. Move into PC

IFG



Tracking Interrupts? (IFG bits)



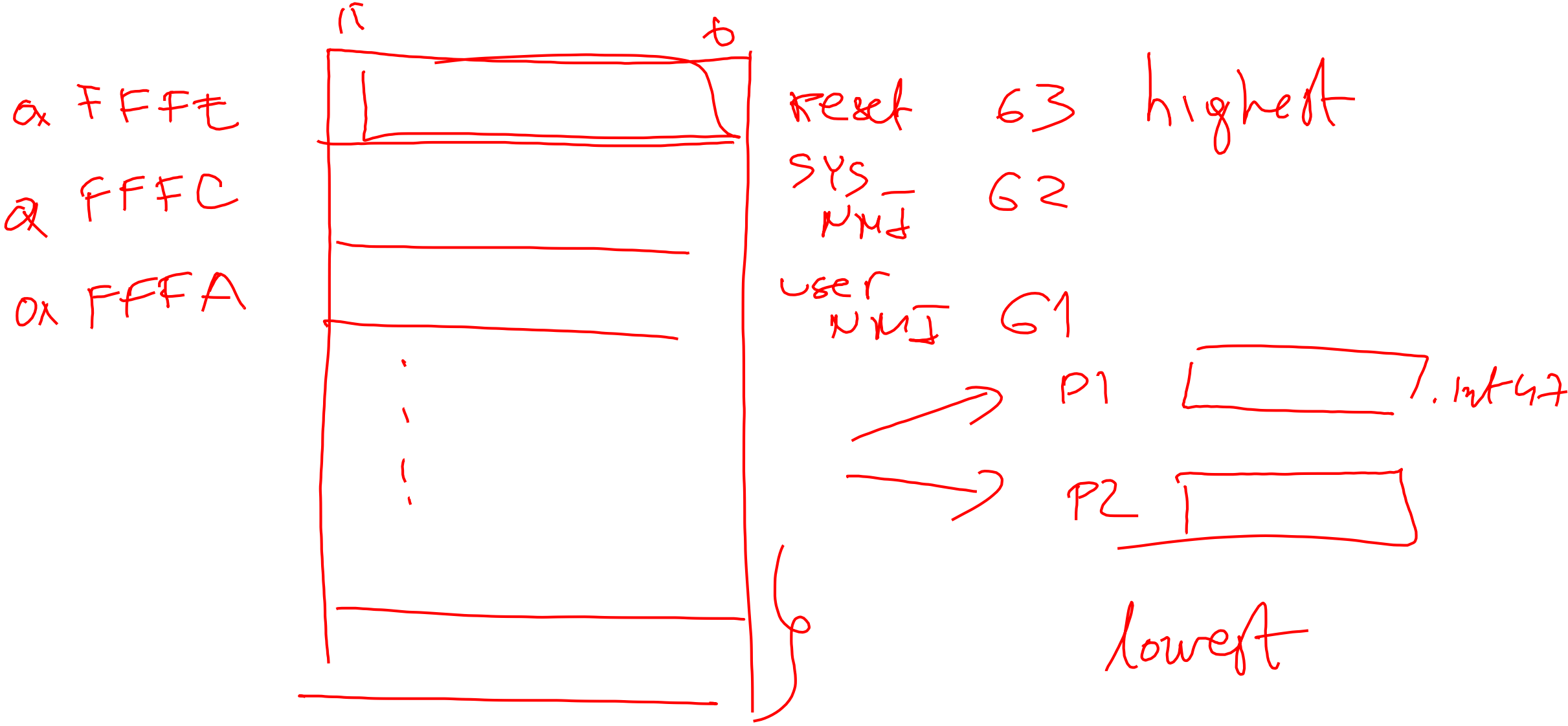
Masking Interrupts (IE Bits)

→ Selective masking

→ Global masking (GIE)

→ NMI – Non-Maskable Interrupt

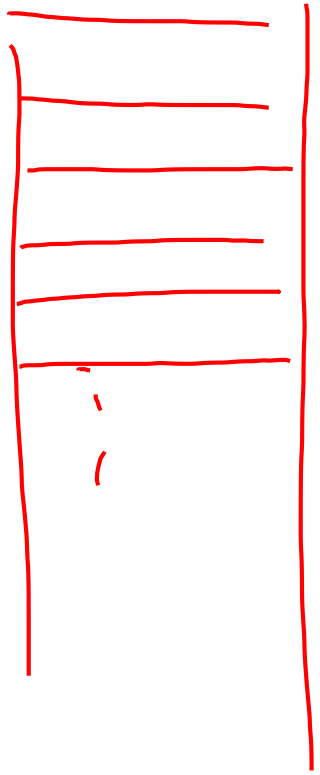
Interrupt Vector Table



Interrupt Priorities

→ Vectored

→ Fixed priorities



Parallel Ports and Interrupts

- P1 and P2 have interrupt capability
- P1IFG
- P1IE
- P1IES
- P2IFG
- P2IE
- P2IES