The University of Alabama in Huntsville
ECE Department
CPE 221 01
Spring 2020
Homework #6

Due March 20, 2020: 7.97(20), 7.98(10), 7.99a,b(20)

7.97 A processor executes an instruction in the following six stages. The time required by each stage in picoseconds (1,000 ps = 1 ns) is given for each stage.

IF	Instruction fetch	220 ps
ID	Instruction decode	150 ps
OF	Operand fetch	180 ps
OE	Execute	240 ps
M	Memory access	350 ps
OS	Operand store (writeback)	180 ps

a. What is the time to execute an instruction if the processor is not pipelined?
b. What is the time taken to fully execute an instruction assuming that this structure is pipelined in six stages and that there is an additional 10 ps per stage due to the pipeline latches?
c. Once the pipeline is full, what is the average instruction execution time?
d. Suppose that 35% of instructions are branch instructions that are taken and cause a 5-cycle penalty, what is the effective instruction execute time?

7.98 A RISC processor executes the following code. There are no data dependencies.

```
ADD  r0, r1, r2
ADD  r3, r4, r5
ADD  r6, r7, r8
ADD  r9, r10, r11
ADD  r12, r13, r14
ADD  r15, r16, r17
```

a. Assuming a four-stage pipeline (fetch, operand fetch, execute, and write) what registers are being read during the seventh clock cycle and what register is being written?
b. Assuming a five-stage pipeline (fetch, operand fetch, execute, memory, and write register) what registers are being read in the fifth clock cycle and what register is being written?

7.99 Consider the following code:

```
LDR    r1, [r6]       ; Load r1 from memory. r6 is a pointer
ADD    r1, r1, #1     ; Increment r1 by 1
LDR    r2, [r1, #4]   ; Load r2 from memory
ADD    r2, r6, #1     ; Increment r2 by 1
ADD    r3, r1, r2     ; Add r1 and r2 with total in r3
ADD    r8, r2, #4     ; Increment r8 by 4
STR    r3, [r6, #8]   ; Store r2 in memory
SUB    r2, r8, #64    ; Subtract 64 from r2
```

The processor has a five-stage pipeline F O E M S; that is, instruction fetch, operand fetch, execute, memory access, and operand writeback to register file. Assume that the register file is not capable of writing and reading in the same cycle.

a. How many cycles does this code take to execute assuming internal forwarding is not used?
b. How many cycles does the code take to execute assuming internal forwarding is used?