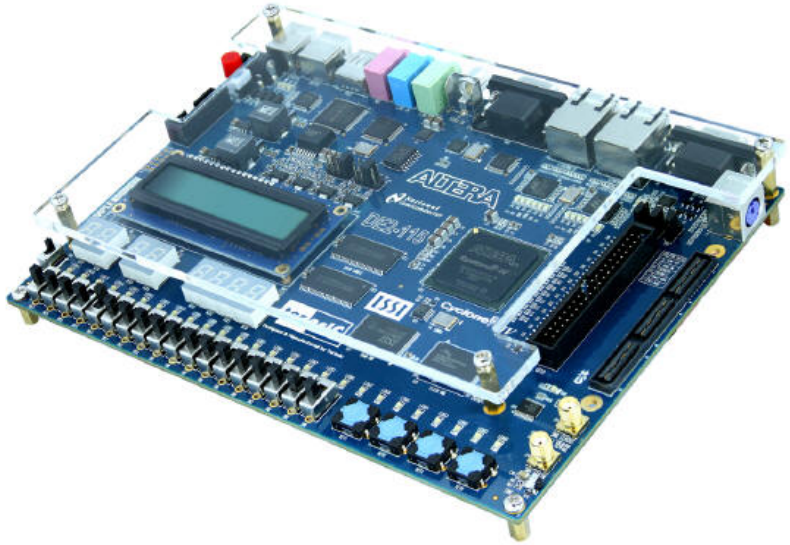
CPE/EE 422/522

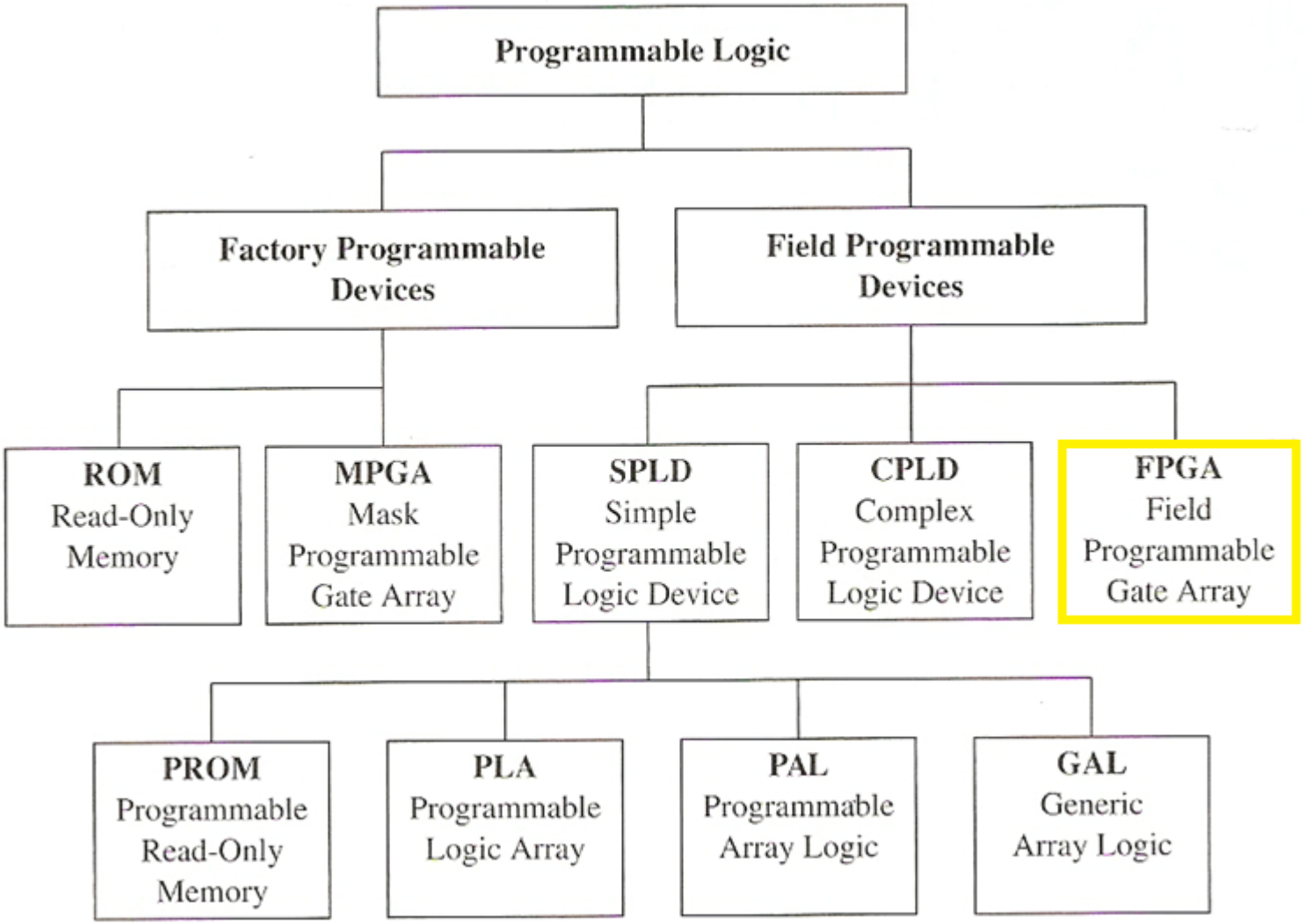
Advanced Logic Design

Electrical and Computer Engineering
UAH

Overview of FPGA Architectures & Technology Considerations



Types of Programmable Logic Devices



Field Programmable Gate Arrays

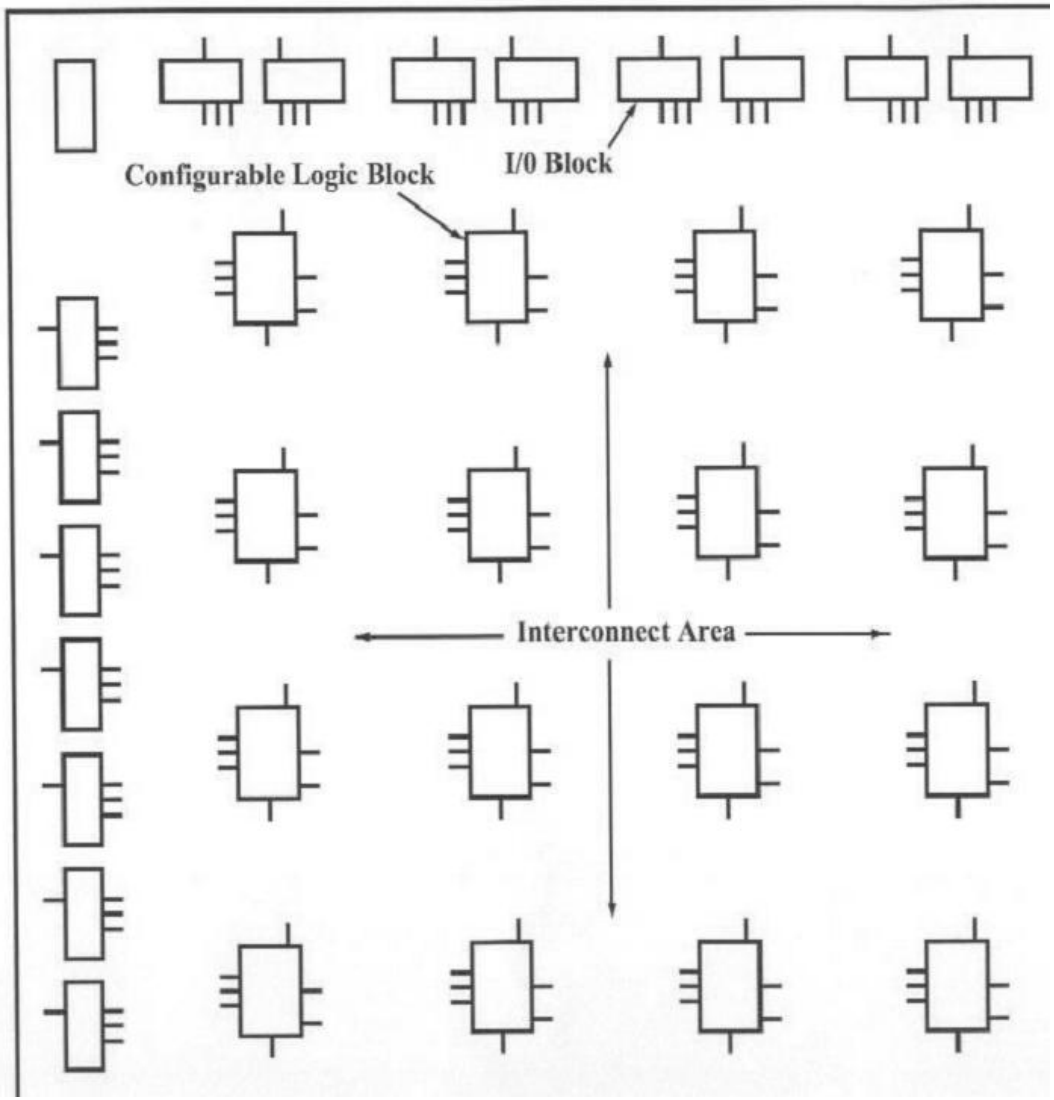
- FPGAs are pre-fabricated integrated circuits that can be configured after fabrication to emulate the functionality of a wide variety of digital systems
- Uses Include:
  - Rapid Prototyping of new hardware designs
  - Faster time to market for low to medium volume productions than Application Specific Integrated Circuits
  - Adaptable/Evolutionary Designs
    - Easy upgrade of hardware
    - Nonintrusive updates through partial reconfiguration
  - Reconfigurable Computing
    - Non-Instruction Set Architecture approaches to High-Performance or Energy Aware Computing

FPGA

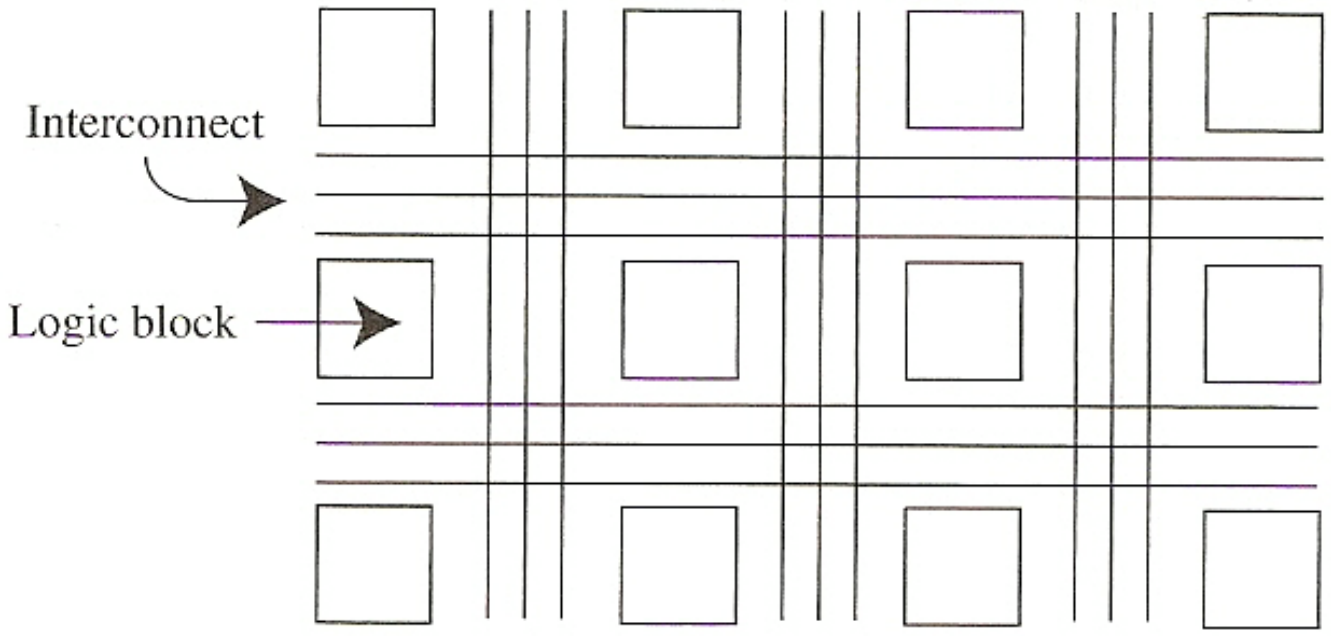
Field programmable Gate Arrays are large programmable logic devices that are comprised of

- Configurable logic blocks where small sequential and combinational logic elements of the design can be implemented.
- Programmable routing channels that interconnects these logic blocks.
- I/O blocks that are connected to logic blocks through routing interconnect and that make off-chip connections

Typical FPGA Layout



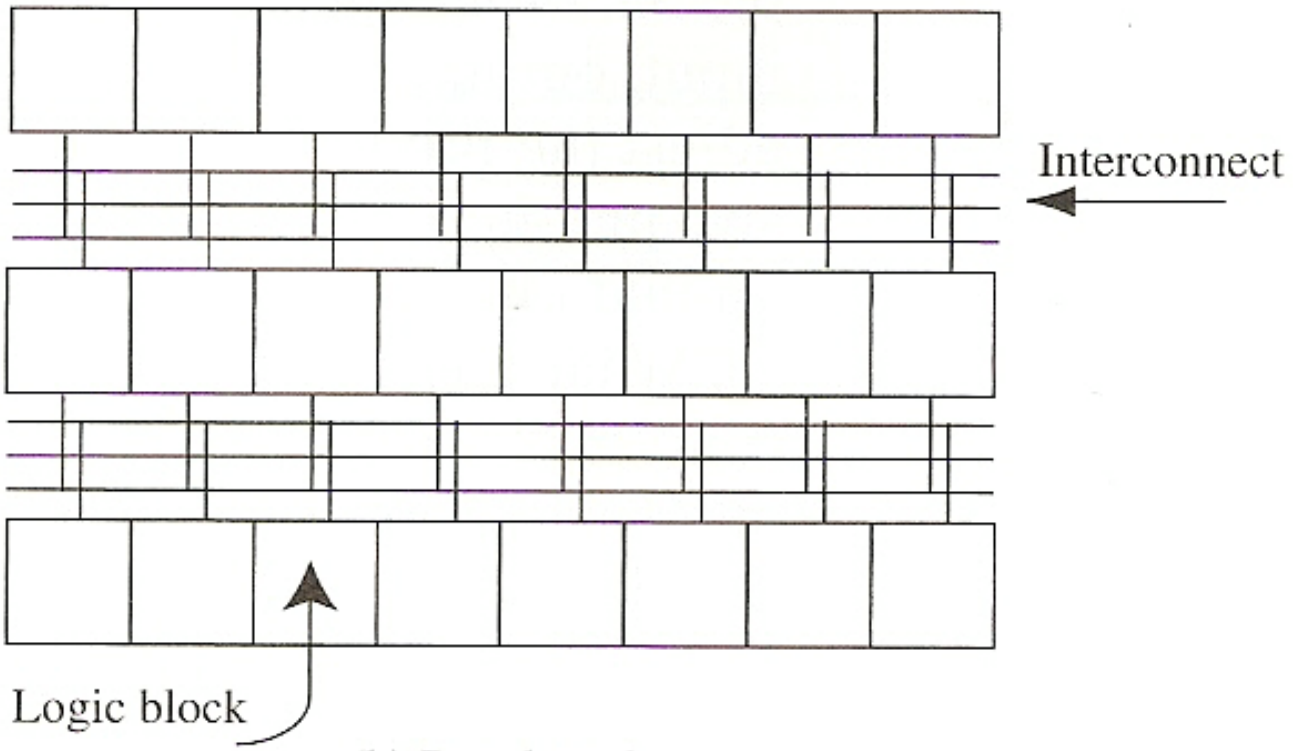
Typical FPGA Architectures



(a) Matrix based (symmetrical array)

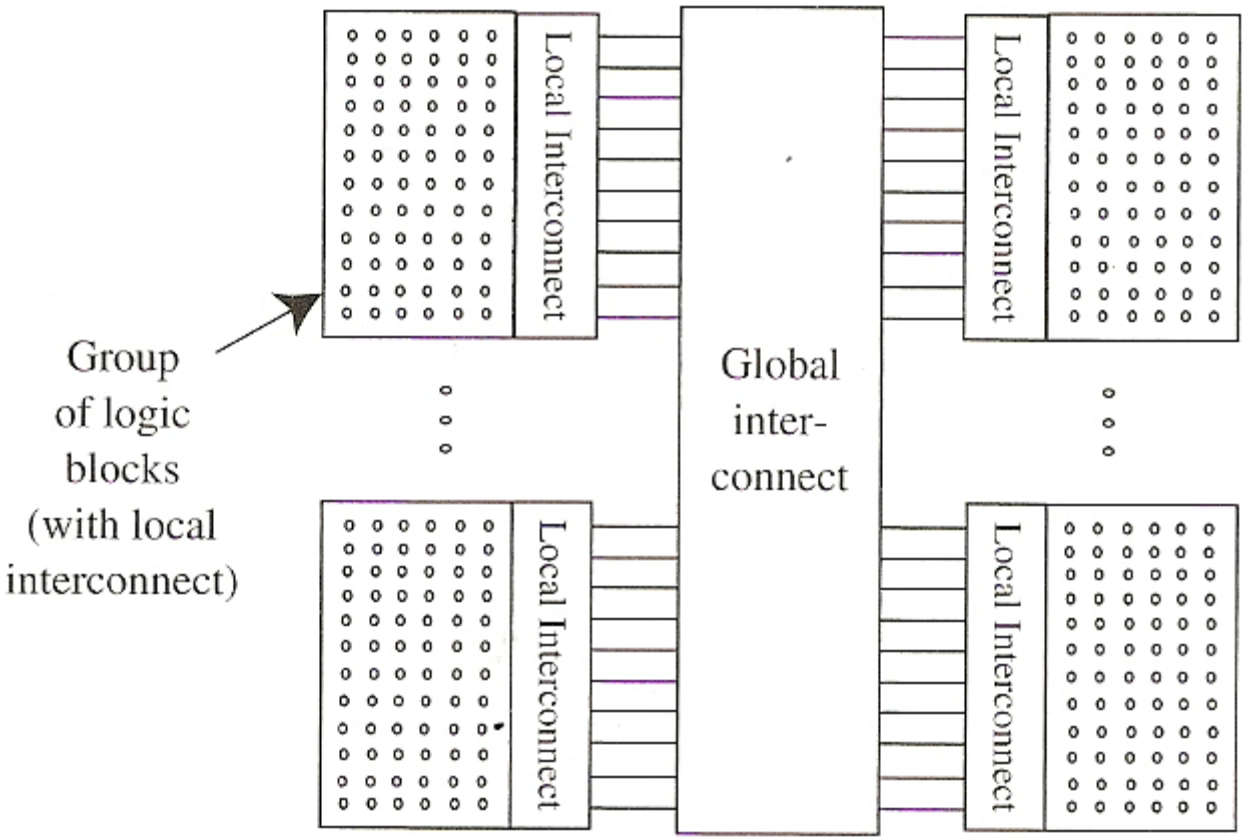
Also called Island Style Architecture

Typical FPGA Architectures



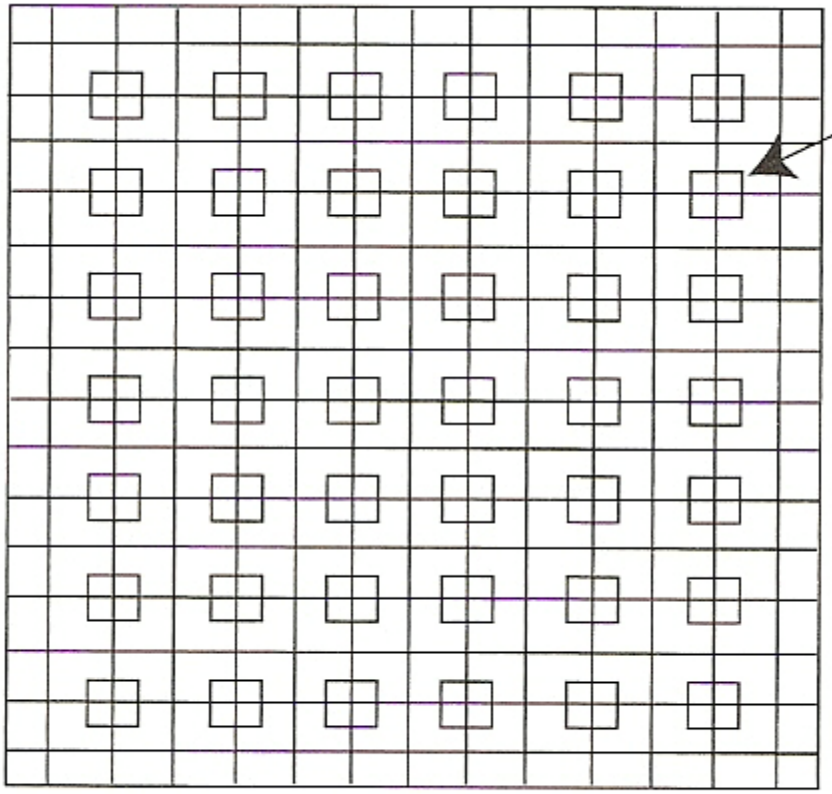
(b) Row based

Typical FPGA Architectures



(c) Hierarchical

Typical FPGA Architectures



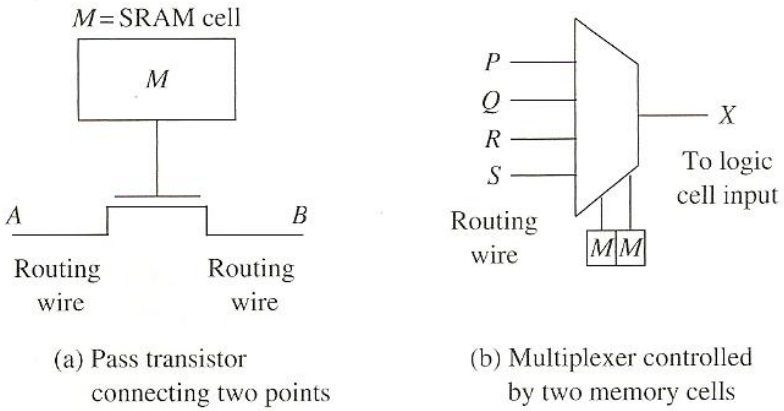
(d) Sea of gates

FPGA Configuration Technologies

Programming Technology	Volatility	Programmability	Area Overhead	Resistance	Capacitance
SRAM	Volatile	In-circuit reprogrammable	Large	Medium to high	High
EPROM	Nonvolatile	Out-of-circuit reprogrammable	Small	High	High
EEPROM	Nonvolatile	In-circuit reprogrammable	Medium to high	High	High
Antifuse	Nonvolatile	Not reprogrammable	Small	Small	Small

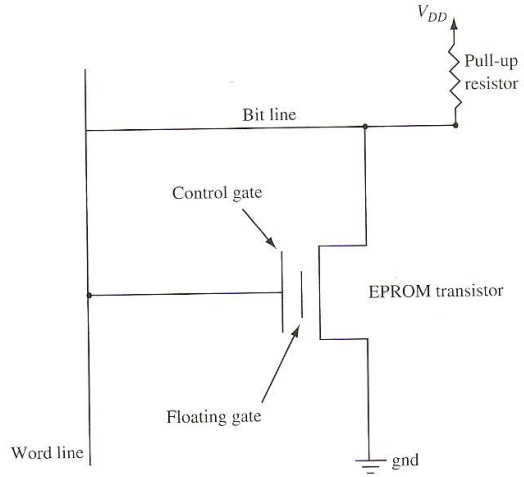
- Configuration Technology is used to
  - Configure the routing interconnect of the FPGA
  - Configure the Configurable Logic Blocks and the IO blocks

FPGA Routing Technology

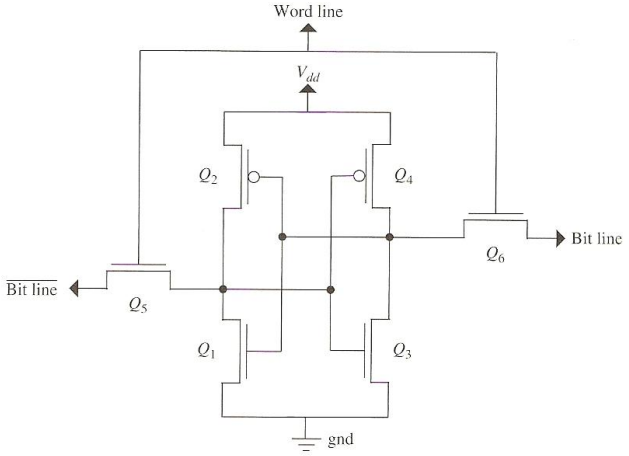


(a) Pass transistor connecting two points

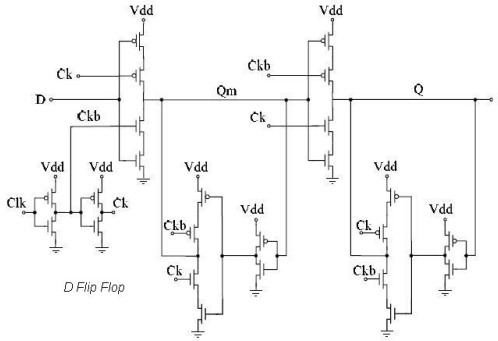
(b) Multiplexer controlled by two memory cells



EPROM, EEPROM, FLASH

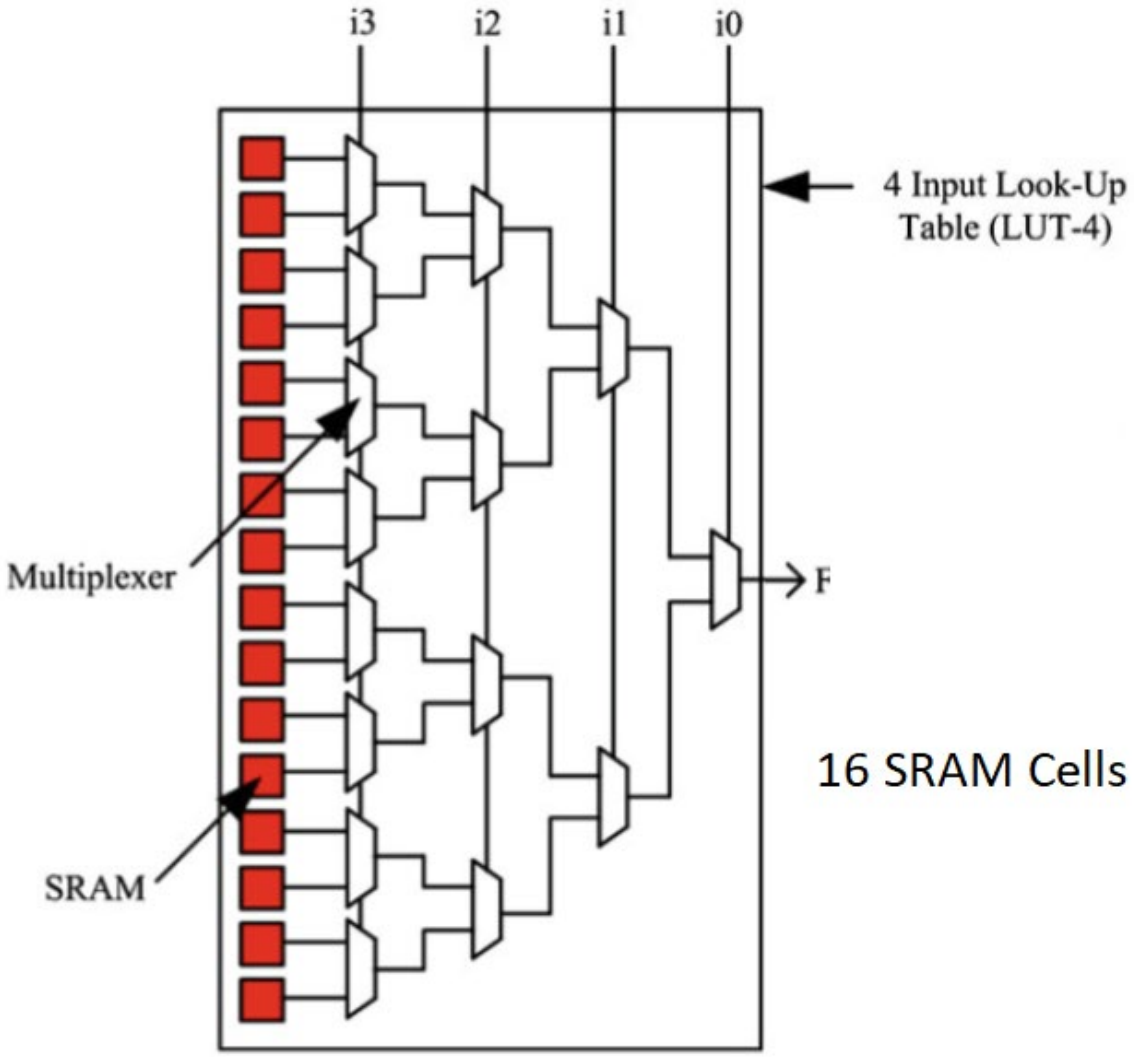


SRAM



D-Flip Flop

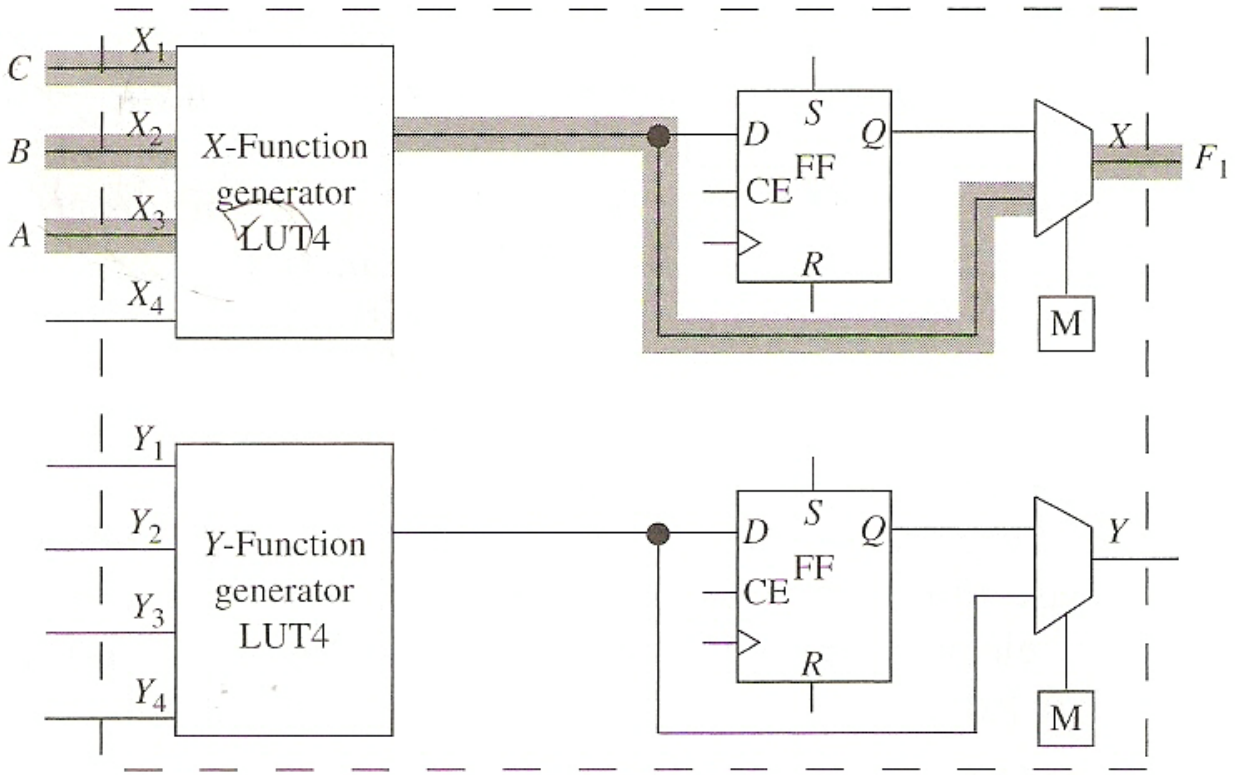
4 Input Lookup Table (LUT-4) Internal Configuration



Lookup Table Based FPGAs

$F_1 = A'B'C + A'BC' + AB$

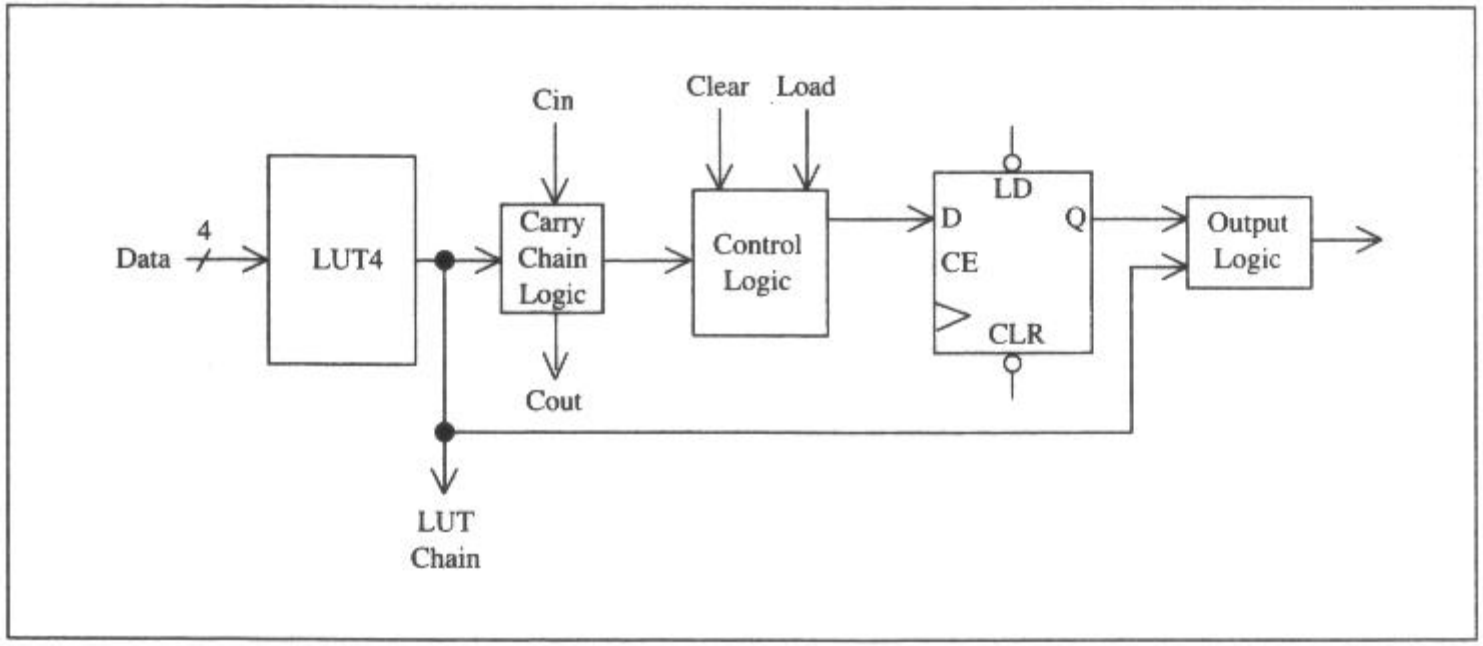
A	B	C	F_1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



X4	X3 A	X2 B	X1 C	X F_1
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	1

Contents of LUT4

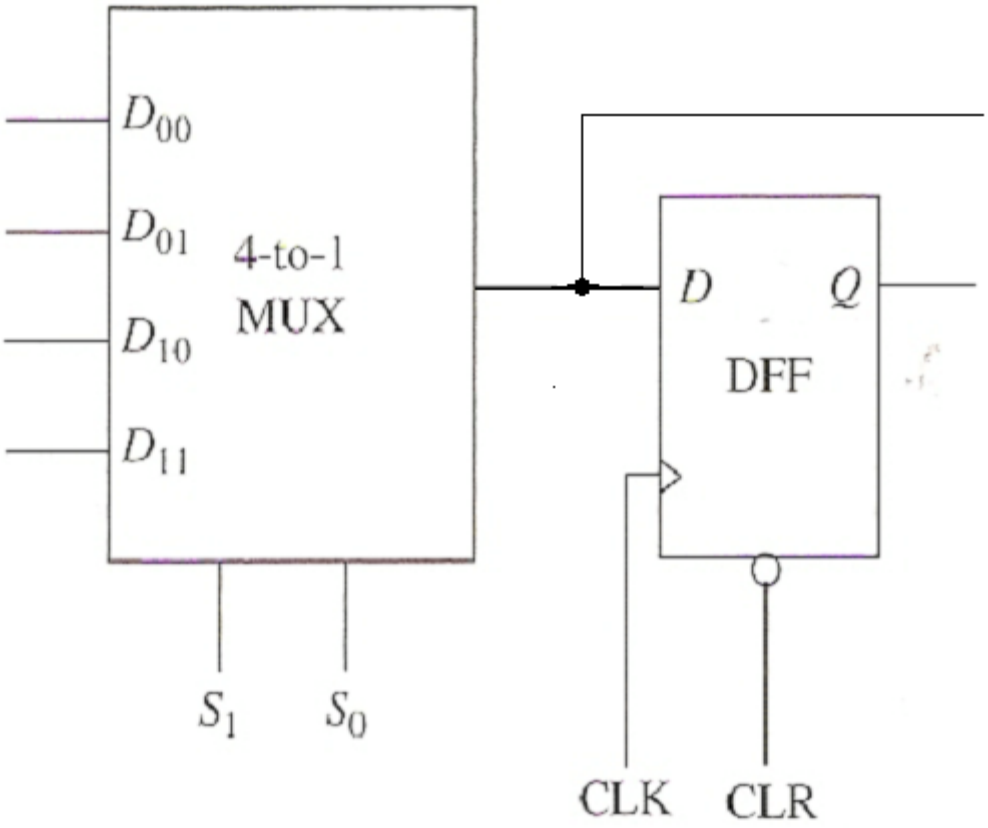
IntelFPGA Stratix Logic Element -- LE



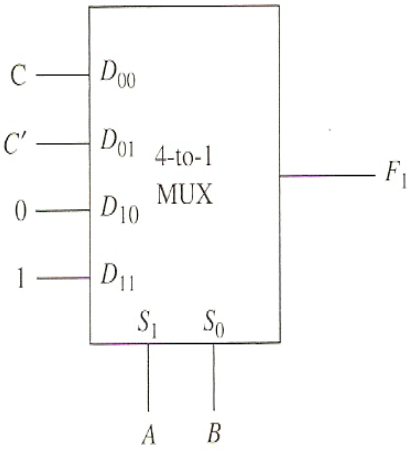
Multiplexer Based FPGAs

$F_1 = A'B'C + A'BC' + AB$

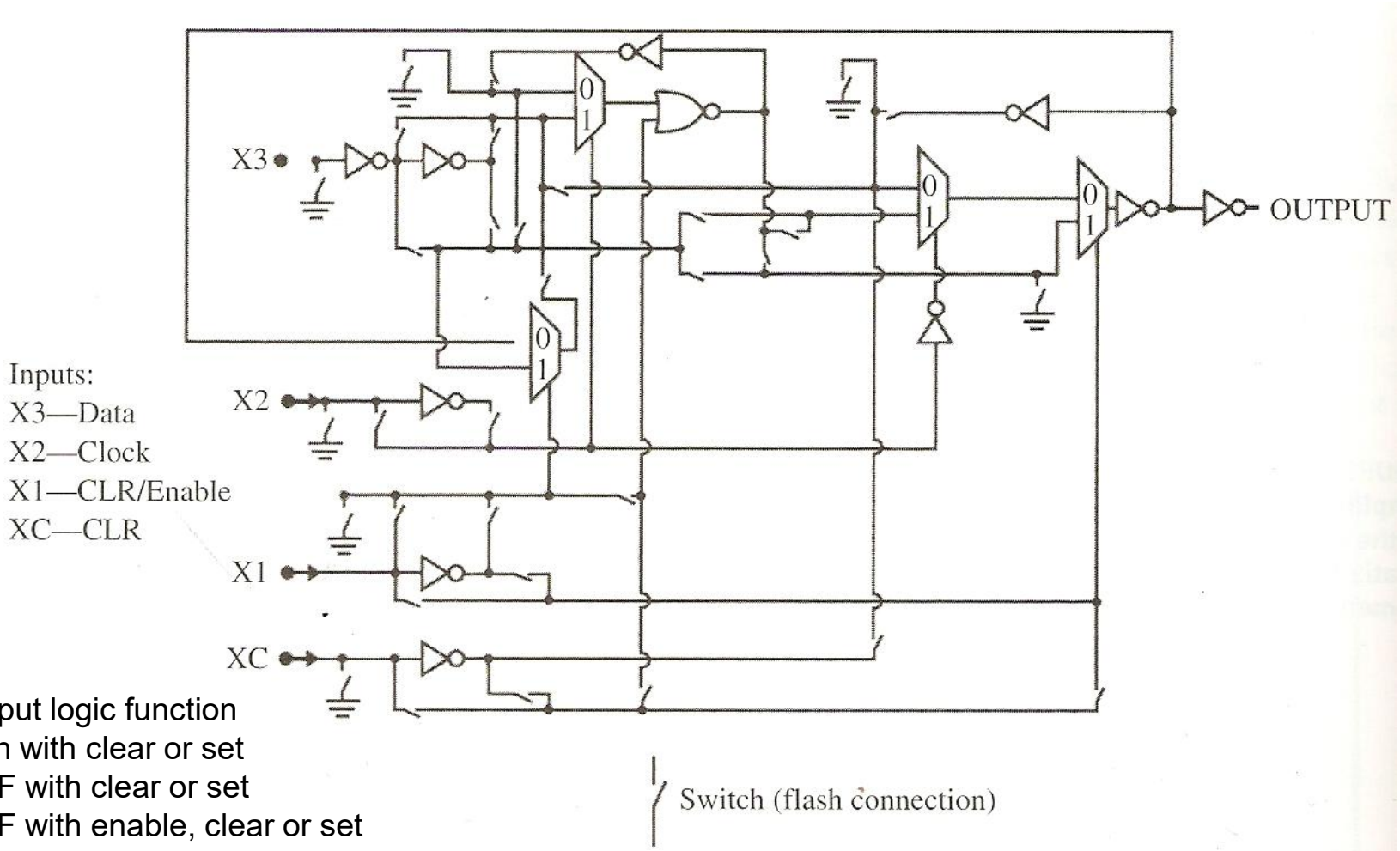
A	B	C	F_1
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1



A	B	C	F	Mux Input in Terms of {0, 1, C, C'}
0	0	0	0	} C
0	0	1	1	
0	1	0	1	} C'
0	1	1	0	
1	0	0	0	} 0
1	0	1	0	
1	1	0	1	} 1
1	1	1	1	



Microsemi Fusion & ProAS1C Logic Block



a 3-input logic function
a latch with clear or set
a D-FF with clear or set
a D-FF with enable, clear or set

Field Programmable Gate Array Capacities

Vendor	FPGA Product	Capacity (Approx) in Gates/LUTs
Xilinx	Kintex 7	41,000 to 298,600 LUTs
	Artix 7	63,400 to 134,600 LUTs
	Virtex-6	46,560 to 474,240 LUTs
	Spartan-3	50K to 5M
	Virtex-5	19,200 to 207,360 LUTs
Intel FPGA	Arria V	76,800 to 516,096 LUTs
(Altera)	Arria II	45,125 to 256,500 LUTs
	ACEX 1K	56K to 257K
	APEX II	1.9M to 5.25M
	FLEX 10K	10K to 50K
	Stratix/Stratix II	10,570 to 132,540 logic elements
Lattice	LatticeECP2	6K to 68K LUTs
	Lattice SC	15.2K to 115.2K LUTs
	ispXPGA	139K to 1.25M
	MachXO	256 to 2280 LUTs
	LatticeECP	6.1K to 32.8K LUTs
Microsemi	Fusion	90K to 1.5M system gates
	IGLOO	15K to 3M system gates
	Axcelerator	125K To 2M
	eX	3K to 12K
	ProASIC3	30K to 3M
	MX	3K to 54K
Quick Logic	Eclipse/EclipsePlus	248K to 662K
	Quick RAM	45K to 176K
	pASIC 3	5K to 75K
Atmel	AT40K	5K to 40K
	AT40KAL	5K to 50K

Architecture, Technology, and Logic Block Type

Company	Device Names	General Architecture	Logic Block Type	Programming Technology
Microsemi	IGLOO	Sea of Tiles	LUT	Flash
	ProASIC/ ProASIC3/ ProASIC^{plus}	Sea of Tiles	Multiplexers & Basic Gates	Flash, SRAM
	SX/SXA/eX/MX	Sea of Modules	Multiplexers & Basic Gates	Antifuse
	Axcelerator	Sea of Modules	Multiplexers & Basic Gates	SRAM
	Fusion	Sea of Tiles	Multiplexers & Basic Gates	Flash, SRAM
Xilinx	Kintex	Symmetrical Array	LUT	SRAM
	Virtex	Symmetrical Array	LUT	SRAM
	Spartan	Symmetrical Array	LUT	SRAM

Architecture, Technology, and Logic Block Type

Company	Device Names	General Architecture	Logic Block Type	Programming Technology
Atmel	AT40KAL	Cell-Based	Multiplexers & Basic Gates	SRAM
QuickLogic	Eclipse II	Flexible Clock	LUT	SRAM
	PolarPro	Cell-Based	LUT	SRAM
Intel FPGA (Altera)	Cyclone IVE	Two-Dimensional Row and Column Based	LUT	SRAM
	Stratix II	Two-Dimensional Row and Column Based	LUT	SRAM
	APEX II	Row and Column, But Hierarchical Interconnect	LUT	SRAM