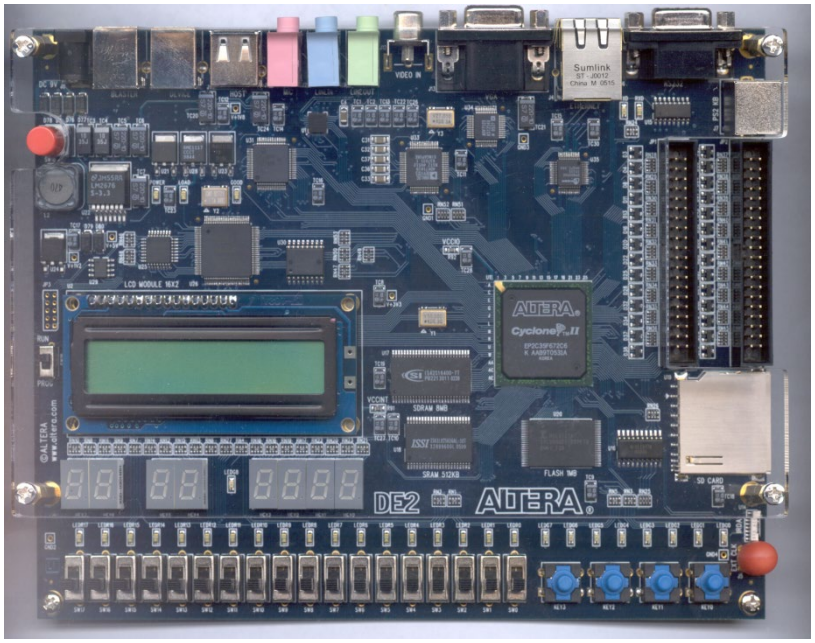
CPE 322
Digital Hardware Design Fundamentals

Electrical and Computer Engineering
UAH

Review of Basic Number Representation



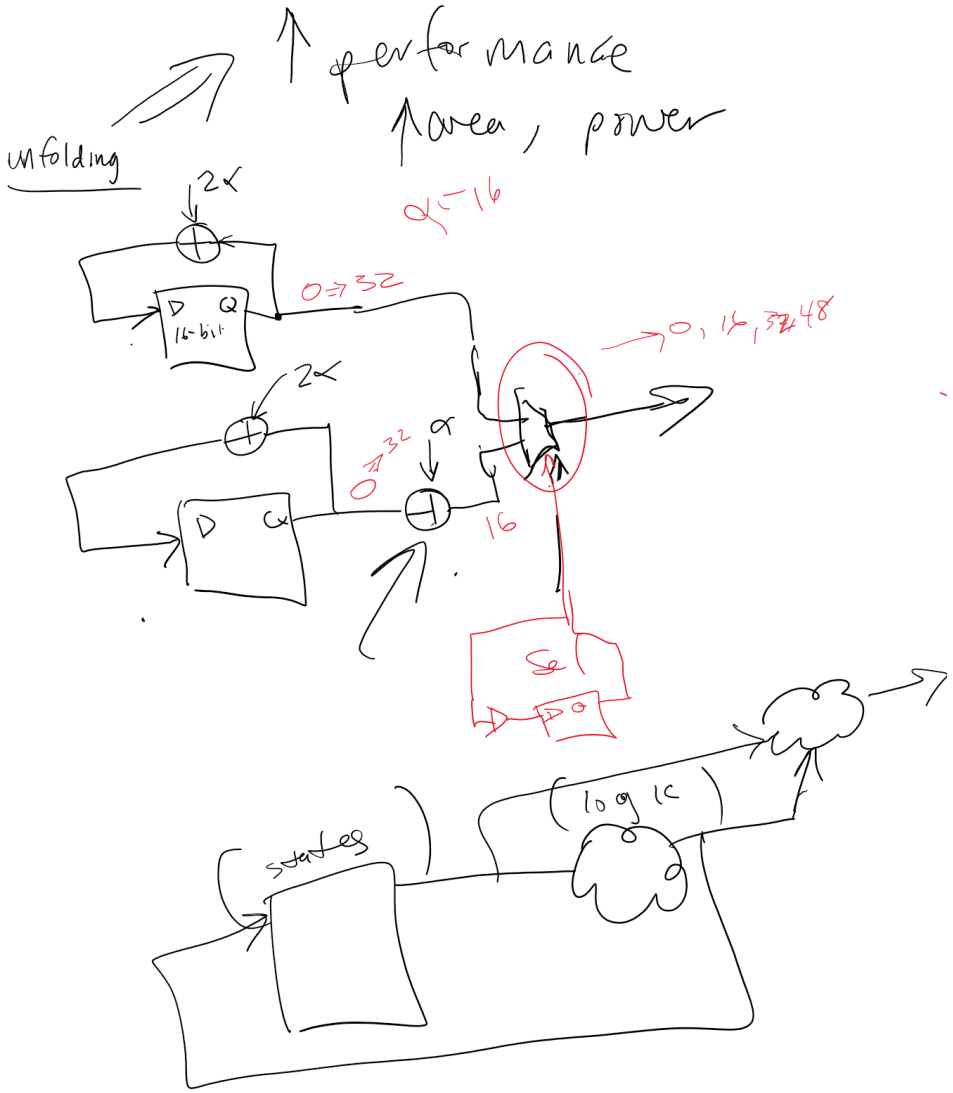
System Verilog

- Revised Verliog language with better support for verification and system integration
- Offers a few benefits over Verilog:
  - Convenience: can use “logic” type instead of “wire” or “reg” and have the tools decide which it is
  - Convenience: can use 2-dimensional vectors/arrays as types for passing data in or out of a module
  - Verification: can reach down into hierarchy and access signals without plumbing them all the way up to the toplevel/testbench
  - Verification: enables Universal Verification Methodology (UVM) suite of verification IP/tools/strategies

Optimization for Speed - Unfolding

- One useful technique is “Unfolding”
- Typically requires N copies of logic to go N times faster
- Limited by performance of multiplexer
- Must project intermediate state information, which can also limit usefulness
  - Projecting state information is also known as “lookahead”

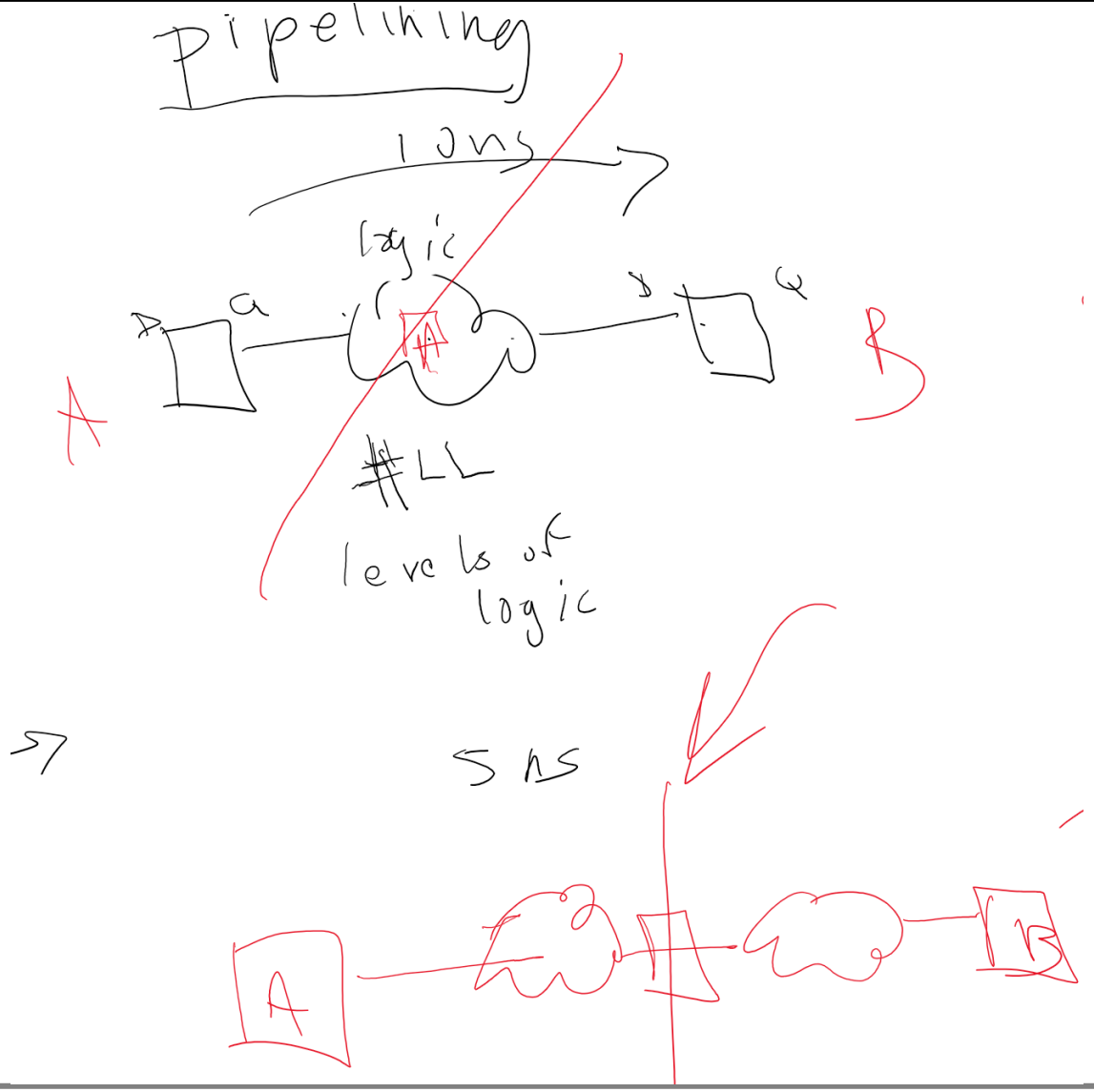
Unfolding (hand notes)



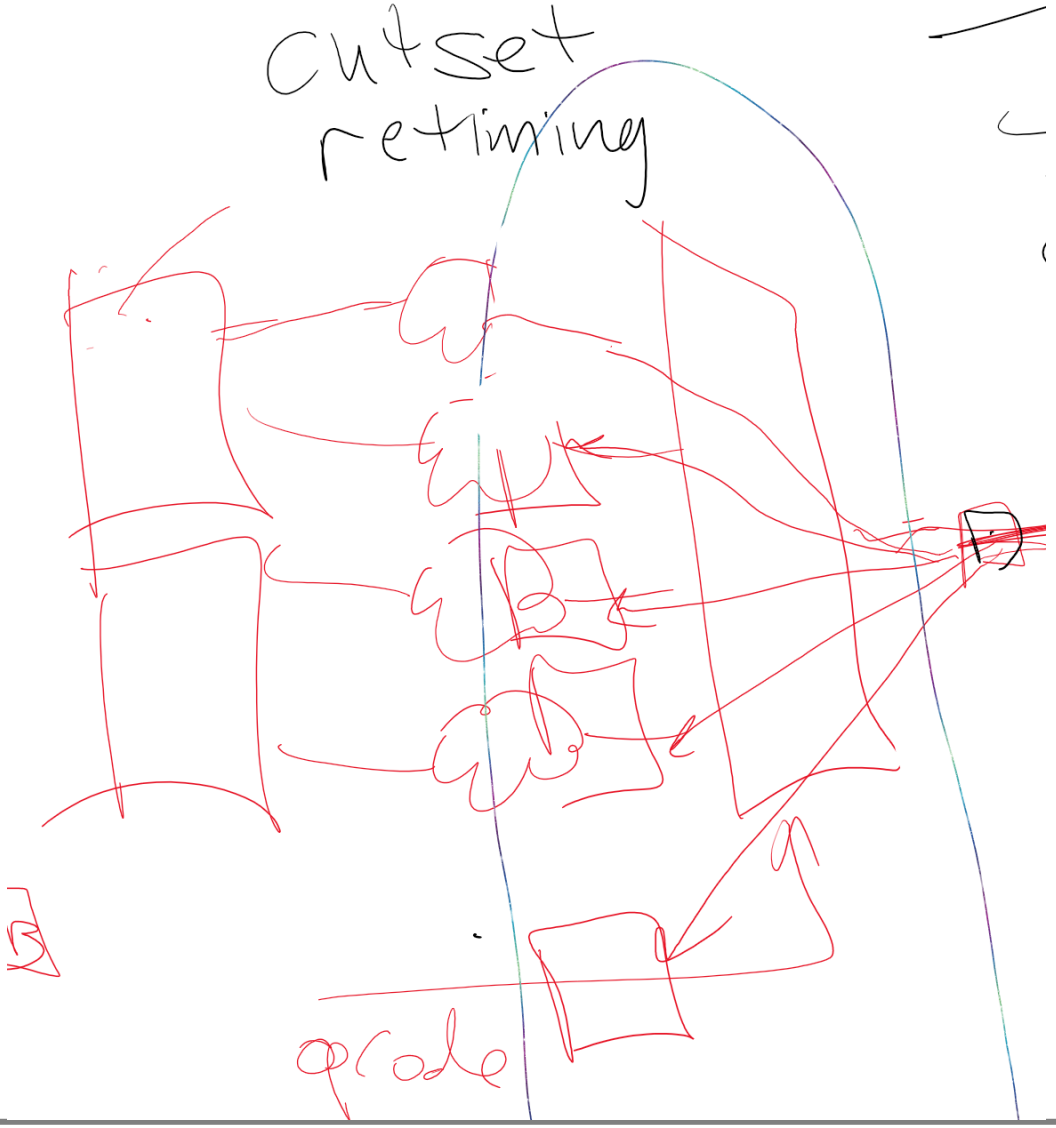
Optimization for Speed - Pipelining

- Another useful technique is “Pipelining”
- Adds registers within logic and/or routing paths to break up critical delays
  - Cannot generally place extra delays in feedback paths
- Can be guided by “cutset retiming” technique to maintain functionality while balancing delay along a path
  - Move registers along a path
  - Remember the 16-bit ALU for Lab 4?

Pipelining (hand notes)



Cutset Retiming (hand notes)



Optimization for Area - Folding

- A useful technique for trading off speed for area is "Folding"
- If one function can operate N times faster than required, then N instances can share the same logic as long as each instance has its own independent state
  - Clock must run at least N times as fast as a single instance
  - States are stored in shift regs or RAMs (to cover N instances) instead of FFs (to cover 1 instance)
  - Total number of LUTs is roughly equal to original single-instance circuit

Folding (hand notes)