Practice Quiz: Modules 09, 10: Clocks, Watchdog Timer, TimerB, UART

Due Nov 1 at 11:59pm **Points** 21 **Questions** 9 **Available** until Nov 1 at 11:59pm **Time Limit** 20 Minutes

Instructions

This quiz covers topics related to MSP430 clock subsystem, timer peripherals (watchdog timer, TimerB), and UART serial communication.

This quiz was locked Nov 1 at 11:59pm.

Attempt History

	Attempt	Time	Score
LATEST	Attempt 1	2 minutes	7.33 out of 21

Correct answers are hidden.

Submitted Nov 1 at 5:55pm

Partial

Question 1

2 / 3 pts

Match MSP430 clocks with their definitions.

MCLK	Master Clock ✔
SMCLK	Sub System - Master Clock ~~Substitute Clock~~
ACLK	Auxiliary Clock ✔

Question 2 ✓

1 / 1 pts

MSP430 Clock modules allow software developers to change frequencies of the clock signals used by the processor and peripherals.

- (●) True
- ( ) False

Unanswered

Question 3

0 / 2 pts

The ACLK clock frequency is 32,768 Hz. How many MCLK clock periods occur during one ACLK clock period if we know frequency of MCLK is 2^21 Hz. Note: enter positive decimal number.

2^{15}

$2^{21} / 2^{15} \rightarrow 2^{6}$

64

Partial

Question 4

1.33 / 2 pts

Select all operating modes of the MSP430 Watchdog Timer peripheral. Find more of these.

- [x] Watchdog mode
- [x] Interval timer mode
- [ ] UP/DOWN counting mode

- [ ] UP counting mode
- [ ] HOLD (not counting)

Incorrect

Question 5

0 / 2 pts

What action do you perform to "pat the dog" in case of the watchdog timer operating in the watchdog mode?

- [ ] Set all bits in the WDT control register
- [x] Set the WDTCTLCL bit to 1 in the WDT control register to clear the timer counter
- [ ] Send a bone to the dog by snail mail
- [ ] Clears all bits in the WDT control register

Partial

Question 6

1 / 2 pts

Pair TimerB counting modes with their definition.

STOP mode	The timer is halted.
UP mode	The timer repeatedly counts f → 0 → top
UP/DOWN mode	The timer repeatedly counts f → 0 → top, back down

CONTINOUS mode The timer repeatedly counts f

0 -> 2^{16}

Unanswered

Question 7

0 / 4 pts

TimerB configured in the UP counting mode uses SMCLK as the source clock. SMCLK clock frequency is 2,000,000 Hz.

What is the maximum resolution when timestamping an external event with frequency?

0.5 microseconds

1/2,000,000

What is duration of one period if TBCCR0=9,999?

5,000 microseconds

0 -> 9,999; counter to 10,000.

.5 microseconds each count, 5000mS

Answer 1:

(You left this blank)

Answer 2:

(You left this blank)

Unanswered

Question 8

0 / 3 pts

UART communication. You configure USCI for UART communication (8-bit data, 2 stop bits, odd parity).

-> If even, 0 parity bit added

1. How many bits is transferred when transmitting a single character (type in the number)?

12 bits

1 start bit
8 data bits
2 stop bits
1 parity
} 12 bits total.

2. What is the parity bit if you are sending ascii character 'a' (0x61)?

0 (enter 1 or 0) 0110 0001 0111 0001 → 1 odd. It need to be odd. If you have even, parity 1.

3. How long does it take to transmit this character if the UART is configured for 38,400 bps (bits per second)?

0.3125 ms (miliseconds) (enter 4 decimal places) 12 bits @ 38,400 bps 12/38400 = .3125

Answer 1:

(You left this blank)

Answer 2:

(You left this blank)

Answer 3:

(You left this blank)

Question 9

2 / 2 pts

UART communication. Device B always sends data to device A over a serial asynchronous link (UART). No data flows from A to B. How do you connect A and B? Symbol "---" means connects to,

- RxD pin of A -- RxD pin of B
- TxD pin of A -- RxD pin of A
- TxD pin of A -- TxD pin of B
- RxD pin of A -- TxD pin of B

ACLK Clock Frequency – 32,768

MCLK Clock Frequency – 2^{21} Hz

↳ How many MCLK clock periods occur?

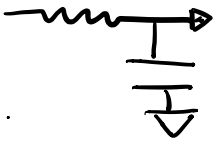
$\frac{2^{21}}{32768} = 64$ MCLK Clock ticks during 1 MCLK

Clocks:

Crystal Clocks

-> Accurate
-> High or low frequency
-> expensive, high current, extra capacitors leads to long start up time.

RC Clocks



-> cheap, quick to start
-> poor accuracy / stability
-> external or integrated into a chip.
-> DCO, SW ? HW controlled

- FLL+ : Frequency-Locked loop clock module
- Status Register control bits SCG0, SCG1, OSCOFF, and CPUOFF configure the msp430 operating modes and enable/disable components of the FLL+ clock module.

Watchdog Timer

-> Performs a controlled-system restart after a software problem occurs.
-> IF the selected time interval is expired, a system reset is generated.
-> can work as an interval timer.
-> WDT powers up active
  ↳ user must setup or halt WDT prior to exp. of initial reset interval.
-> expiration of selected time interval, set WDTIFG and triggers a PUC.
-> Interval mode: WDTTMSEL=1, periodic interrupts.

-> Interrupt flag is reset when interrupt is called.

Timer A

-> 16-bit counter w/ 4 operating modes

-> Selectable & configurable

UART

Communication

-> BIG FOUR

- sense, process, store, communicate

-> Integrated circuits on PCB

-> Dev platform and ws.

-> Between Es.

- Wired vs. wireless
- serial vs. parallel
- Synchronous vs. asynchronous.
- Unidirectional (simplex)
- Bidirectional (half/full duplex)

- UART -> Universal asynchronous receiver/transmitter
  - -> TxD transmit
  - -> RxD receive