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CPE221

Final Exam

1. True

2. MIPS

3. Embedded

4. True

5. Scope

6. r2 = -240 = **1111 0001**

7. -145 = 1111 1111 0110 1111

+379 = 0000 0001 0111 1011

= **1111 1110 0001 0100**

8. r2 = 0000 0100 0110 1000 0011 0001 1110 0110

r3 = 0101 1001 0011 0010 1100 1101 0000 0111

r2 = **1110 0000 1011 0011 0100 1100 1001 1010**

9.

Cycle	Concrete RTL	Signals
1	MAR <- R1	E_{IR_B} = 1, M_ALU = 1, C MAR
2	MBR <- MAR	M_MBR, C_{MBR}, READ = 1
3	R1 <- MBR	E_{MBR} = 1, M_ALU, C_{r1}
4	MAR <- r0	E_{R0_B} = 1, M_ALU = 1, C_{MAR}
5	MBR <- MAR	M_MBR, $C_{MBR,}$ Read = 1
6	MBR < MBR + r1	ALU(F1, F2) = 1, 0, E_{MBR_B} = 1, M_MBR = 1, C_{MBR}
7	MAR <- IR	E_{IR_B}, M_ALU = 1, C_{MAR}
8	M[MAR] <- MBR	Write
9		

10.

Address		Hit / Miss
0xFFa	1111 1111 1010	Miss
0x010	0000 0001 0000	Miss
0xFE8	1111 1110 1000	Hit
0x497	0100 1001 0111	Miss
0x 8E5	1000 1110 0101	Miss
0x483	0100 1000 0011	Hit
0x392	0011 1001 0010	Miss
0x027	0000 0010 0111	Miss
0x135	0001 0011 0101	Miss
0x592	0101 1001 0010	Miss

Index = log28 = 3 bits, block = log28 = 3 bits

Byte = 2 bits Tag = 12-(3+3+2) = 4 bits

Set	Tag	data
0	0000	M[000-01F]
1	0000 0001	M[020-03f], m[120-13f]
2		
3		
4	0100, 0101, 0011	M[480-49F], M[580-59F], M[380-39F]
5		
6		
7	1111, 1000	M[Fe0-FFF], M[8E0-8FF]

11.

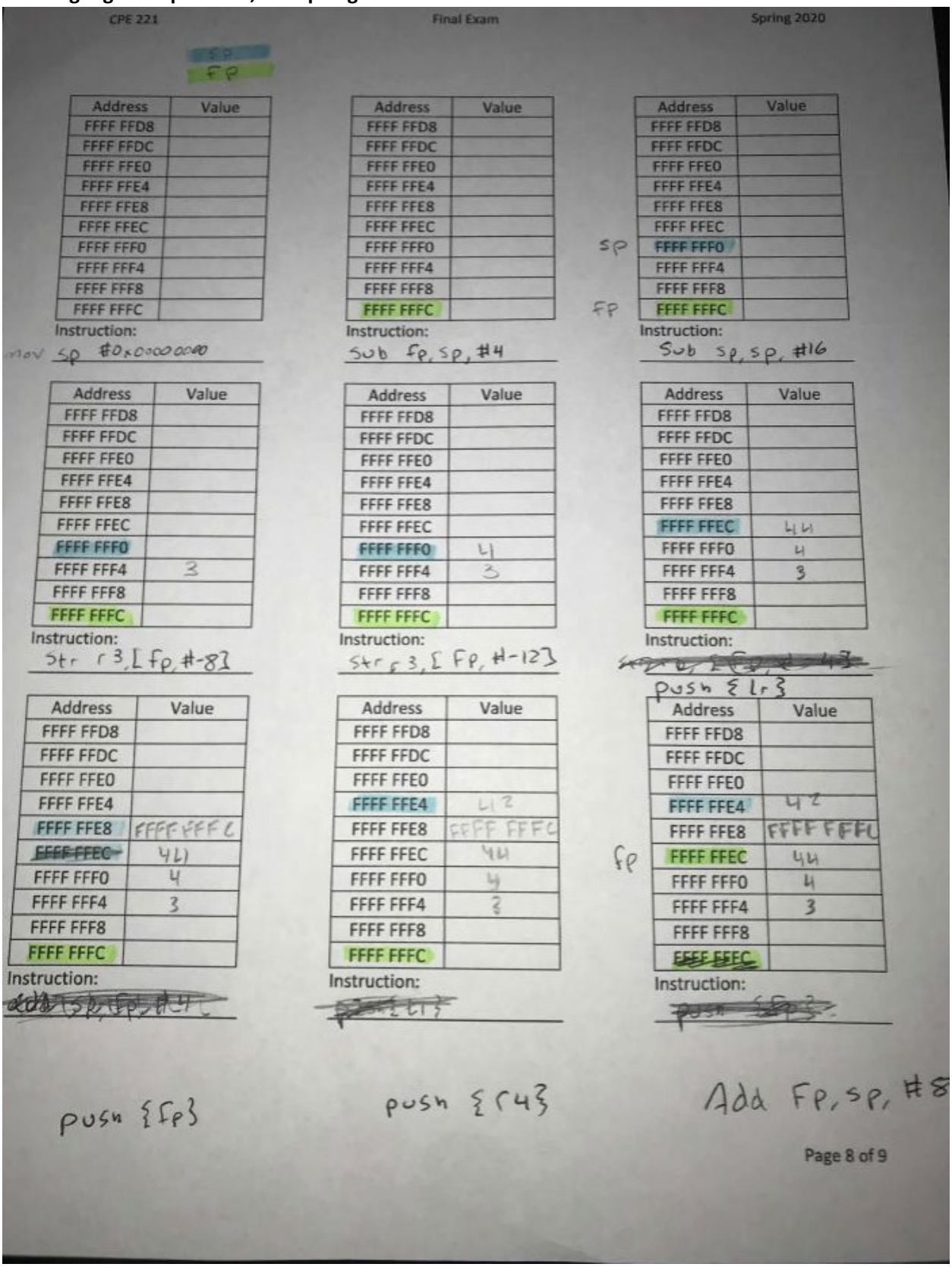
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			
STR R2, [r4]	IF	R	E	MR	MW	W												
ADD r6, r2, r5		IF	R	E	MR	MW	W											
LDR r7. [r3]			IF	R	E	MR	MW	W										
MOV r9, r6				IF	R	R	R	R	E	MR	MW	W						
EOR r7, r7, r6					IF	IF	IF	IF	R	E	MR	MW	W					

13 cycles

12.

```
        AREA PROB_12, CODE, READONLY
        ENTRY
        LDR     r3, size
        LDR     r4, i
loop    CMP     r4, r3              ; for(I = 0; I < 10; i++)
        BGE     done                ; if i is greater than 10, exit loop
        ADD     r5, r4, #1          ; j = i + 1
loop2   CMP     r5, r3              ; for(j = i+1; j < 10; j++)
        BGE     done2               ; if j is greater than 10, exit loop
        LDR     r6, [r5, LSL #2]    ; r6 <- x[j]
        LDR     r7, [r4, LSL #2]    ; r7 <- x[i]
        CMP     r6, r7              ;if(x[j] < x[i])
        BGE     done                ; if x[j] is greater than x[i] then end
        LDR     r8, r7              ; temp <- x [ i ]
        LDR     r7, r6              ; x[ i ] <- x[ j ]
        LDR     r6, r8              ; x[j] <- temp
        ADD     r4, r4, #1          ; i++
        ADD     r5, r5, #1          ; j++
        B       loop2
done2   B       loop
done    B       done
X       DCD     400, 2, -3, 285, 47, 11, -13, 17, 19, -95
temp    SPACE   4
i       DCD     0
size    DCD     10
        END
```

#13 I highlighted sp in blue, and fp in green.



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sp
fp

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction: mov sp #0x00000000

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	
FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
FFFF FFFC	

Instruction: sub fp, sp, #4

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	
sp FFFF FFF0	
FFFF FFF4	
FFFF FFF8	
fp FFFF FFFC	

Instruction: sub sp, sp, #16

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	
FFFF FFF0	
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: str r3, [fp, #-8]

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: str r3, [fp, #-12]

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: push {lr}

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: add sp, fp, #4

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: push {r4}

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
fp FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction: push {fp}

push {fp}

push {r4}

Add fp, sp, #8

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Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

~~push {r4}~~

sub sp, sp, #8

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

~~str r4, [sp, #4]~~

sub sp, fp, #18

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	9
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

pop {pc}

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	3
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

~~add fp, sp, #8~~

str r0, [fp, #-12]

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	9
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

~~sub sp, sp, #16~~

pop {r4, r5}

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	9
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	16

Instruction:

str r0, [fp, #-4]

Address	Value
FFFF FFD8	
FFFF FFDC	
FFFF FFE0	5
FFFF FFE4	42
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

sub sp, sp, #8

str r1, [fp, #-16]

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	9
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	

Instruction:

pop {fp}

Address	Value
FFFF FFD8	
FFFF FFDC	4
FFFF FFE0	3
FFFF FFE4	9
FFFF FFE8	FFFF FFFC
FFFF FFEC	44
FFFF FFF0	4
FFFF FFF4	3
FFFF FFF8	
FFFF FFFC	16

Instruction:

add sp, fp, #4