Module 1 Amplifier Fundamentals

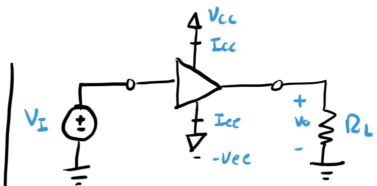
Amplifier types

- Voltage amps: $V_o = A_v \cdot V_I$ $A_v \equiv$ Voltage gain $A_v = v_o / v_I$ (V/V)
- Current amps: $i_o = A_i \cdot i_I$ $A_i \equiv$ current gain $A_i = i_o / i_I$ (A/A)
- Power amps: $P_o = A_p \cdot P_I$ $A_p \equiv$ Power gain $A_p = P_o / P_I$ (P/P) $= \dfrac{v_o\, i_o}{v_I\, i_I}$ (VA/VA)

Log Scale

↳ express gain in dB.

- $A_v = 20 \log |A_v|$
- $A_i = 20 \log |A_i|$
- $A_p = 10 \log |A_p|$



$$P_{dc} + P_I = P_L + P_{Loss}$$

Amplifier efficiency

$$\eta = \frac{P_L}{P_{dc}} \times 100$$ % efficiency.

$$P = \frac{V^2}{R}$$

Standard Amp

$$\frac{V_o}{V_i} = A_{vo}\left(\frac{R_L}{R_L + R_o}\right)\left(\frac{R_i}{R_s + R_i}\right)$$

Module 2A Operational Amplifiers

Ideal op-amps

1. Draws zero input current: $i_- = i_+ = 0\,A$
2. V_o is not a function of i_o: $R_o = 0$
3. Open loop gain is inf: $V_+ = V_-$
4. Inf common mode rejection: $V_o = 0$
5. Inf bandwidth: A is not a func of freq

Non-Ideal Op-Amps (Finite A)

- Inverting: $\dfrac{v_O}{v_I} = \dfrac{-R_2/R_1}{1 + 1/A\,(1 + R_2/R_1)}$
- Non-inverting: $\dfrac{v_O}{v_I} = \dfrac{(1 + R_2/R_1)}{1 + 1/A\,(1 + R_2/R_1)}$

Inverting Op-amps

closed loop gain

$$\frac{v_O}{v_I} = \frac{-R_2}{R_1} \rightarrow G = \frac{-R_2}{R_1}$$

$$R_i = \frac{v_I}{i_1} = R_1 \; ; \; R_o = 0$$

$$i_1 = \frac{v_I}{R_1}$$

$$i_2 = \frac{0 - v_O}{R_2}$$

Non-inverting op-amp

$$R_i = \frac{v_I}{i_I} = \infty \qquad R_o = 0$$

$$G = 1 + R_2/R_1$$

Non-inverting amp

Weighted Summer

$$v_O = v_{O1} + v_{O2} + v_{O3} =$$

$$v_o = -\frac{R_f}{R_1} v_1 - \frac{R_f}{R_2} v_2 + \frac{R_f}{R_3} v_3 \ldots$$

$$i_f = \frac{V_{o\,max}}{R_f}$$

Voltage Follower

$$R_1 = \infty$$

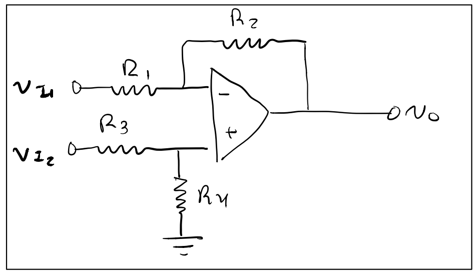
$$R_2 = 0$$

$$v_O = v_I$$

Module 2B Difference Amplifiers

Difference Amplifier

- $v_{I_1} = v_{ICM} - \frac{1}{2} v_{ID}$
- $v_{I_2} = v_{ICM} + \frac{1}{2} v_{ID}$



- $v_{O_1} = \left(-\frac{R_2}{R_1}\right) v_{I_1}$
- $v_{O_2} = \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right) v_{I_2}$
- $v_O = v_{O_1} + v_{O_2}$

- $A_{CM} = -\frac{R_2}{R_1} + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)$
- $A_d = \frac{1}{2}\left(\frac{R_2}{R_1} + \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_4}{R_3 + R_4}\right)\right)$
- $CMRR = 20 \log \left|\frac{A_d}{A_{CM}}\right| (dB)$ ★ If $A_{CM} = 0$ (ideal) then $CMRR = \infty$

When $A_{CM} = 0$...

- $A_d = \frac{R_2}{R_1}$; $R_{id} = 2R_1$; $R_1 = R_3$; $R_2 = R_4$

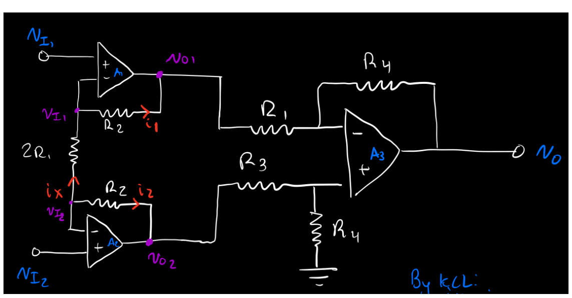
Instrumentation Amplifier

- $v_O = \frac{R_4}{R_3}\left(1 + \frac{R_2}{R_1}\right) v_{ID}$
- $v_{ID} = v_{I_2} - v_{I_1}$

↳ w/ R_2 mismatch:

- $v_O = \frac{R_4}{R_3}\left(1 + \frac{R_{2_1} + R_{2_2}}{R_1}\right) v_{ID}$

$i_1 = \frac{v_{I_1} - v_{O_1}}{R_1}$ $\quad i_2 = \frac{v_{I_2} - v_{O_2}}{R_2}$ $\quad i_x = \frac{v_{ID}}{2R_1}$



Ideal Diodes

OFF: Reverse Bias region: $v < 0$; $i = 0$
↳ Looks like an open circuit

ON: Forward bias region: $v > 0$; $i > 0$
↳ Looks like a short circuit

} Assume Diode state and Solve to check

Forward bias Diodes

$V_T = 25\,mV$
$k = 8.62\,E-5$ eV/K
$q = 1.6\,E-19\,C$

- $\frac{I_2}{I_1} = \exp\left(\frac{V_2 - V_1}{V_T}\right)$
- $i \cong I_S \exp\left(\frac{v}{nV_T}\right)$

- $V_T = \frac{kT}{q}$
- $V_2 - V_1 = V_T \ln\left(\frac{I_2}{I_1}\right)$

Modeling Diodes

Iterate: $I_D = \frac{V_{DD} - V_D}{R}$

Const Drop: use ↑ w/ $V_D = 0.7$ unless told otherwise.

Ideal: Solve w/ $V_D = 0$

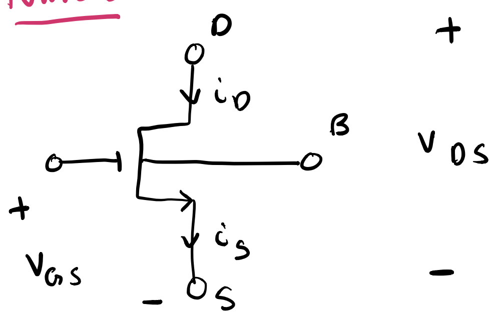
Zener Diodes

- $V_Z = V_{Z0} + I_Z r_Z$ or
- $V_{Z0} = V_Z - I_Z r_Z$

- $\Delta V_O = \frac{r_Z}{R + r_Z}(\Delta V_S)$

Module 4 MOSFET fundamentals

NMOS



Symmetric Device:

$i_D = i_S$; $i_G = 0$

$\mu_n C_{ox}$; $V_{tn} = V_t$

∘ Triode

① ∘ $V_{GS} > V_t$, V_{DS} is very small

∘ $i_D = k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)V_{DS}$

∘ $r_{ds} = \dfrac{1}{k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)}$

② ∘ $V_{GS} > V_t$, V_{DS} is small

∘ $V_{DS} < (V_{GS} - V_t)$

∘ $i_D = k'_n \left(\frac{W}{L}\right)\left[(V_{GS} - V_t)V_{ds} - \frac{1}{2} V_{ds}^2\right]$

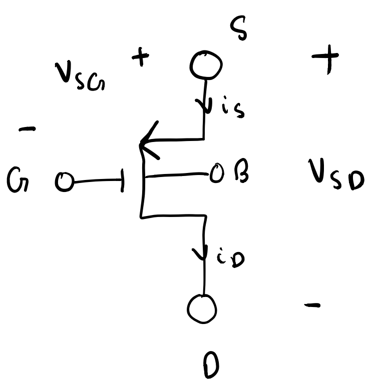
∘ Saturation region

∘ $V_{GS} > V_t$

∘ $V_{DS} > V_{GS} - V_t \longrightarrow V_{ds} = V_{GS} - V_t$ Edge of saturation:

∘ $i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

PMOS



Symmetric Device:

$i_D = i_S$; $i_G = 0$

$\mu_n C_{ox}$; $V_{tp} < 0$ so $|V_{tp}|$

∘ Triode

① $V_{SG} > |V_{tp}|$, V_{SD} very small

∘ $i_D = k'_n \left(\frac{W}{L}\right)(V_{SG} - |V_{tp}|)V_{SD}$

∘ $r_{ds} = \dfrac{1}{k' \,(W/L)(V_{SG} - |V_{tp}|)}$

② ∘ $V_{SG} > V_t$, V_D is small

∘ $V_{SD} < V_{SG} - |V_{tp}|$

∘ $i_D = k'_p \left(\frac{W}{L}\right)\left[(V_{SG} - |V_{tp}|)V_{SD} - \frac{1}{2} V_{SD}^2\right]$

∘ Saturation region

∘ $V_{GS} > V_t$

∘ $V_{DS} > V_{GS} - V_t \longrightarrow V_{ds} = V_{GS} - V_t$ Edge of saturation

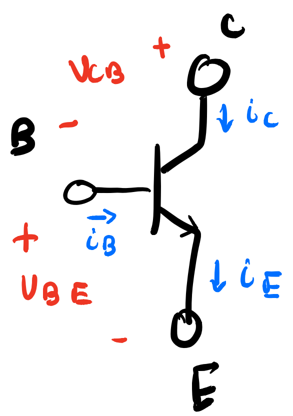
∘ $i_D = \frac{1}{2} k'_n \left(\frac{W}{L}\right)(V_{GS} - V_t)^2$

$\mu_p C_{ox}$
↑
mobility of holes in Silicon.
$V_{tp} < 0$; $|V_{tp}|$

Module 5: BJTs Fundamentals

BJT operation and DC biasing

npn



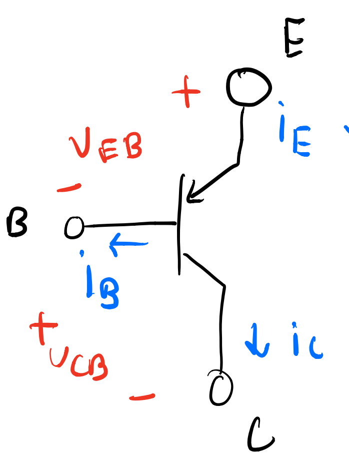
$$I_C = I_S \exp\left(V_{BE}/V_T\right)$$

$$i_B = \frac{i_C}{\beta} \qquad \beta = \frac{\alpha}{\alpha - 1} \qquad \alpha = \frac{\beta}{\beta + 1}$$

$$i_E = i_B + i_C$$

active: $V_{BE} > 0$ $\quad V_{CB} > -0.4v$

pnp



- $I_C = I_S \exp\left(V_{EB}/V_T\right)$
- $i_B = \frac{i_C}{\beta}$
- $\beta = \frac{\alpha}{\alpha - 1}$
- $\alpha = \frac{\beta}{\beta + 1}$
- $i_E = i_C + i_B$
- $i_C = \alpha i_E$

active mode $V_{EB} > 0$ $\quad V_{BC} > -0.4v$

• Forward Bias equation

↳ used in the diode and BJT forward bias lectures

✳ know how and when to use them.

General Forms

○ $\frac{I_2}{I_1} = \exp\left(\frac{V_2 - V_1}{V_T}\right)$ ○ $V_2 - V_1 = V_T \ln\left(\frac{I_2}{I_1}\right)$

Example for BJT to find VBE2

$$V_{BE2} - V_{BE1} = V_T \ln\left(\frac{I_{C2}}{I_{C1}}\right)$$

• Transition equations

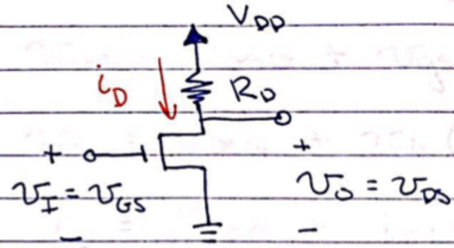
A: $V_{GS} = V_t$ $V_{DS} = V_{DD}$

B: $V_{GS} = V_t + \frac{\sqrt{1 + 2R_D k'_n (W/L) V_{DD}} - 1}{R_D k'_n (W/L)}$

$V_{DS} = V_{GS} - V_t$

C: $V_{GS} = V_{DD}$ $V_{DS} = \frac{V_{DD}}{(1 + R_D k'_n (\frac{W}{L})(V_{DD} - V_t))}$

- MOSFETs + Amplifiers ★ know how we are using prev. MOSFET Eq.



Always true: (Ohm's Law)

$$i_D = \frac{V_{DD} - v_{DS}}{R_D}$$

combine w/ MOSFET eqs.

- Cutoff: $v_{GS} < V_t$, $i_D = 0$, $v_{DS} = V_{DD}$

$$0 = \frac{V_{DD} - V_{DS}}{R_D} \Rightarrow v_{DS} = V_{DD}$$

- Saturation: $(v_{DS} \geq v_{GS} - V_t)$

$$v_{DS} = V_{DD} - \underbrace{\tfrac{1}{2} R_D k'_n \left(\tfrac{W}{L}\right)(v_{GS} - V_t)^2}_{R_D i_D}$$

- Triode: $(v_{DS} < v_{GS} - V_t)$

$$v_{DS} = \frac{v_{GS}}{1 + R_D k'_n \left(\frac{W}{L}\right)(v_{GS} - V_t)}$$

max $v_{GS} = V_{DD}$

$$v_{DS} = \frac{V_{DD}}{1 + R_D k'_n \left(\frac{W}{L}\right)(V_{DD} - V_t)}$$

- Edge of Saturation:

$$v_{GS} = V_t + \frac{\sqrt{1 + 2\left(R_D k'_n \left(\frac{W}{L}\right) V_{DD}\right)} - 1}{R_D k'_n \left(\frac{W}{L}\right)}$$

- MOS Amplifier Voltage Gain + the Q-Point:

$v_{GS} = V_{GSQ} + v_{gs}(t)$

$v_{DS} = V_{DSQ} + v_{ds}(t)$

$i_D = \underbrace{I_{DQ}}_{\text{DC-bias point (Q-point)}} + \underbrace{i_d(t)}_{\text{small signal}}$

Finding Max v_i:

$V_{DSQ} - |A_v| v_i = V_{GSQ} + v_i - V_t$

→ solve for v_i

comes from:

$v_{DS_{min}} = v_{GS_{max}} - V_t$

$v_{ds} = A_v v_{gs}$

↳ small signal volt. gain

$A_v = -R_D \, k'_n \left(\frac{W}{L}\right)(V_{GSQ} - V_t)$

* can pick resistors, transistors, and Q-point to get desired gain when designing.

- Small Signal Eq.:

$i_d = k'_n \left(\frac{W}{L}\right)\left[v_{gs}(V_{GSQ} - V_t)\right]$

$g_m = \frac{i_d}{v_{gs}} = k'_n \left(\frac{W}{L}\right)(V_{GSQ} - V_t)$ units $\left[\frac{A}{V}\right]$

$A_v = -g_m R_D$

reminder: $r_o = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$

* coupling capacitors act as open circuits for DC and as short circuits for AC.

n

- MOS Amplifier Voltage Gain + the Q-Point:

$v_{GS} = V_{GSQ} + v_{gs}(t)$

$v_{DS} = V_{DSQ} + v_{ds}(t)$

$i_D = \underbrace{I_{DQ}}_{\text{DC-bias point (Q-point)}} + \underbrace{i_d(t)}_{\text{small signal}}$

Finding Max v_i:

$V_{DSQ} - |A_v| v_i = V_{GSQ} + v_i - V_t$

→ solve for v_i

comes from:

$v_{DS_{min}} = v_{GS_{max}} - V_t$

$v_{ds} = A_v v_{gs}$

small signal volt. gain

$A_v = -R_D \, k'_n \left(\frac{W}{L}\right)(V_{GSQ} - V_t)$

* can pick resistors, transistors, and Q-point to get desired gain when designing.

- Small Signal Eq.:

$i_d = k'_n \left(\frac{W}{L}\right)\left[v_{gs}(V_{GSQ} - V_t)\right]$

$g_m = \frac{i_d}{v_{gs}} = k'_n \left(\frac{W}{L}\right)(V_{GSQ} - V_t)$ units $\left[\frac{A}{V}\right]$

$A_v = -g_m R_D$

reminder: $r_o = \frac{1}{\lambda I_{DQ}} = \frac{V_A}{I_{DQ}}$

* coupling capacitors act as open circuits for DC and as short circuits for AC.

- MOS Amps: * Combined w/ the Small sig. eqs.

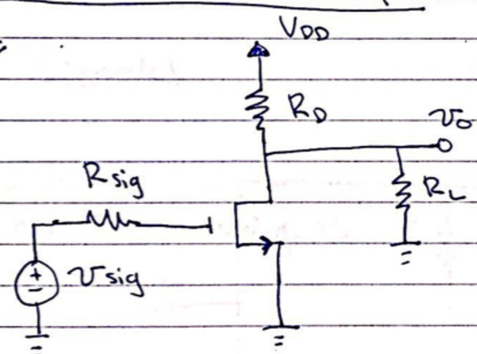
$$R_{in} = \frac{v_i}{i_i} \qquad v_i = \frac{R_{in}}{R_{in}+R_{sig}} \cdot v_{sig}$$

$$A_{vo} = \left.\frac{v_o}{v_i}\right|_{R_L \to \infty} \qquad A_v = \frac{v_o}{v_i}$$

$$G_v = \frac{v_o}{v_{sig}}$$

- Common Source Amp: ("Source Grounded")

Given



so $v_i = v_{sig}$

$R_{in} = \infty \qquad i_i = 0$

$$R_o = R_D \parallel r_o$$

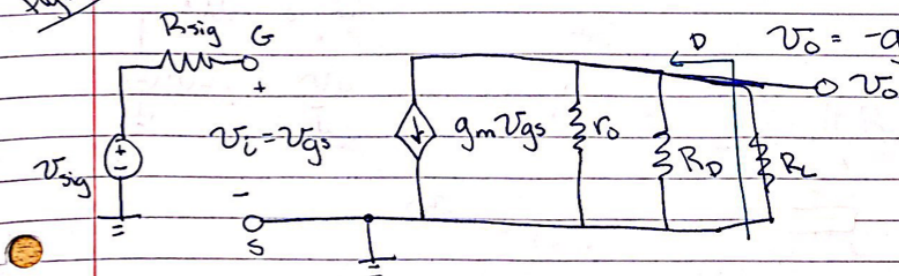
$$A_{vo} = -g_m (r_o \parallel R_D)$$

$$A_v = -g_m (r_o \parallel R_D \parallel R_L)$$

$$G_v = -g_m (r_o \parallel R_D \parallel R_L)$$

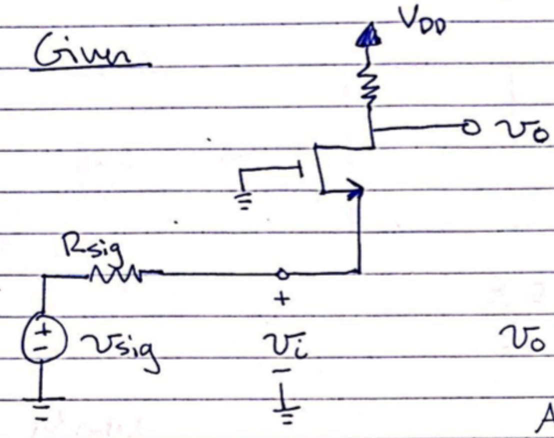
$$v_o = -g_m (v_i)(r_o \parallel R_D)$$

Hybrid-π



- Common Gate Amp: (gate grounded, v_i is @ source)

Given



$R_{in} = 1/g_m$

$R_o = R_D$

$v_{gs} = -v_i$

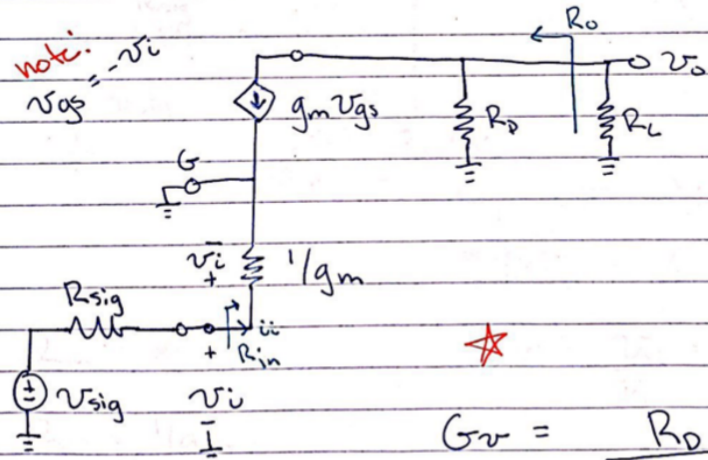
$v_o = -g_m(R_D)(-v_i) = g_m R_D v_i$

$A_{vo} = g_m R_D$

$A_v = g_m(R_D \| R_L)$

T-model

note: $v_{gs} = -v_i$



☆

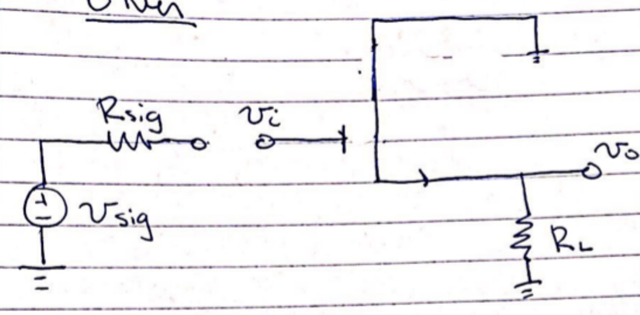
$$G_v = \frac{R_D \| R_L}{R_{sig} + 1/g_m}$$

or

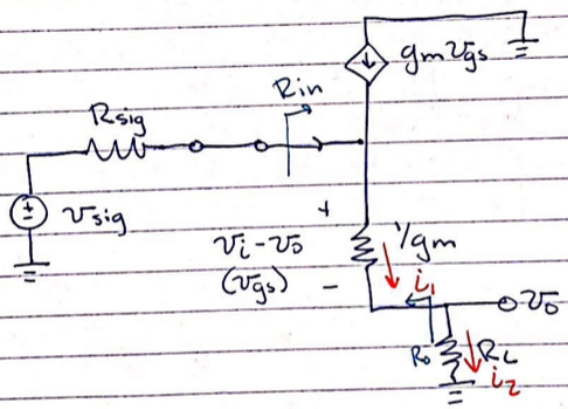
$$G_v = \frac{R_D \| R_L}{R_{sig} + R_{in}}$$

Common Drain Amp: (voltage follower, v_i at gate)

Given



Model



$$i_1 = \frac{v_i - v_o}{1/g_m}$$

$$i_2 = \frac{v_o}{R_L}$$

$$i_1 = i_2$$

$R_{in} = \infty$

$R_o = 1/g_m$

$A_{vo} = \left.\frac{v_o}{v_i}\right|_{R_L \to \infty} = 1$

$$A_v = \frac{v_o}{v_i} = \frac{R_L}{R_L + 1/g_m}$$

$$G_v = \frac{v_o}{v_{sig}} = \frac{R_L}{R_L + 1/g_m}$$

if R_L is $\gg 1/g_m$ then $G_v \cong 1$