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CPE348

HW #2 (10 pts)

Due Fri Feb 26, 2021

a) $2 \times 10^8 \text{ m/s}$ 40km

$$40 \text{ km} / (2 \times 10^8 \text{ m/s}) = 200 \text{ ns}$$

1) (2 pts) Chapter 2 Text Book Problem 23

23. Consider an ARQ algorithm running over a 40-km point-to-point fiber link.

(a) Compute the one-way propagation delay for this link, assuming that the speed of light is 2×10^8 m/s in the fiber.

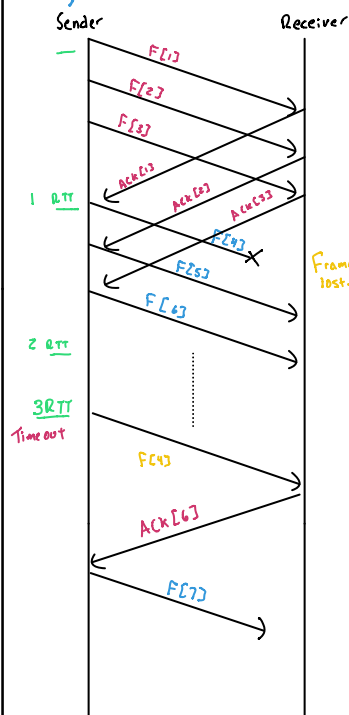
(b) Suggest a suitable timeout value for the ARQ algorithm to use.

(c) Why might it still be possible for the ARQ algorithm to time out and retransmit a frame, given this timeout value?

b) $\text{RTT} = 400 \text{ ns}$, double this would be good for a timeout value. 0.8 ms .

c) The sender does not know the delay on the receiving node. It may not answer immediately.

a)



2) (2 pts) Chapter 2 Text Book Problem 31

31. Draw a timeline diagram for the sliding window algorithm with $\text{SWS} = \text{RWS} = 3$ frames, for the following two situations. Use a timeout interval of about $2 \times \text{RTT}$.

(a) Frame 4 is lost.

(b) Frames 4 to 6 are lost.

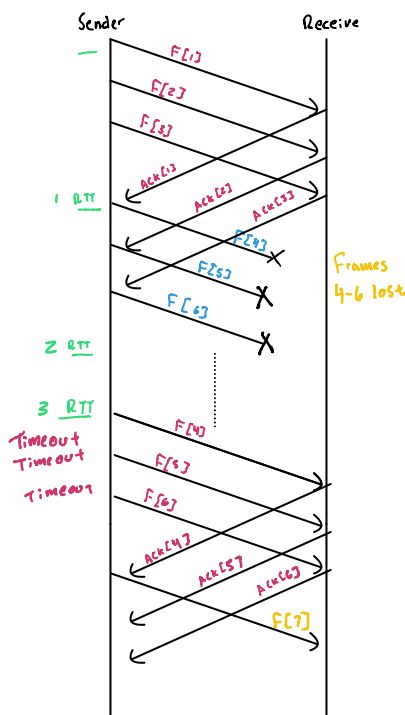
Hints/Help: Look at extra problem #32 for a timeline example. In this problem, assume that it takes $\frac{1}{4}$ RTT to transmit a frame. Use a timeout of 2 RTT .

a) When frames 5 and 6 are received no ack is sent. An ack is sent for frames 4, 5 and 6 once the retransmitted frame 4 is received.

Something to keep in mind (but not part of this problem) is when a frame is received (but not 4), protocol could have the receiver send an ack for frame 3 again which indicates a frame received but not 4.

b) When frames 4-6 are sent, the transmitter needs to wait for an ack or for timeout before sending another frame.

b)



$$RT - PD = 46.4 \text{ NS}$$

> 512 bits

a) $4640 + 48 = 586 \text{ bytes}$

b) You would waste a lot of bandwidth. If you sent smaller packet sizes, you could send more different data points. If your message is only 2 bytes, you would have to send way too much data.

3) (2 pts) Chapter 2 Text Book Problem 42 a,b (answer b to the best of your ability)

42. Suppose the round-trip propagation delay for Ethernet is $46.4 \mu\text{s}$. This yields a minimum packet size of 512 bits (464 bits corresponding to propagation delay + 48 bits of jam signal).

- (a) What happens to the minimum packet size if the delay time is held constant, and the signalling rate rises to 100 Mbps?
(b) What are the drawbacks to so large a minimum packet size?

4) (2 pts) short answer problems:

53. How can a wireless node interfere with the communications of another node when the two nodes are separated by a distance greater than the transmission range of either node?

This is called the hidden node problem. Essentially the 2 nodes' data collides at the third.



54. Why is collision detection more complex in wireless networks than in wired networks such as Ethernet?

As shown in #53, there is the hidden node problem. The biggest issue is that A and B do not know each other exist. Also, two nodes cannot send data @ the same time

55. How can hidden terminals be detected in 802.11 networks?

RTS-CTS

Sender \rightarrow CTS, CTS \rightarrow all other nodes it can access. Essentially, the other nodes are aware that the original sender exists.

5) (2 pts) Chapter 3 Text Book Problem 1.

1. Using the example network given in Figure 3.44, give the virtual circuit tables for all the switches after each of the following connections is established. Assume that the sequence of connections is cumulative; that is, the first connection is still up when the second connection is established, and so on. Also assume that the VCI assignment always picks the lowest unused

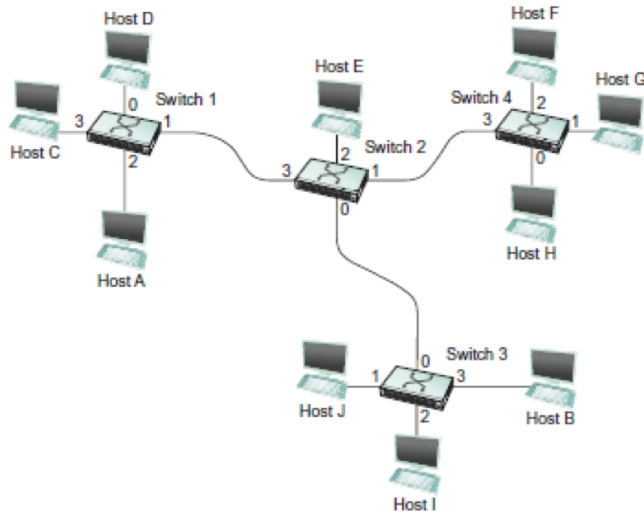


FIGURE 3.44 Example network for Exercises 1 and 2.

VCI on each link, starting with 0, and that a VCI is consumed for both directions of a virtual circuit.

- (a) Host A connects to host C.
- (b) Host D connects to host B.
- (c) Host D connects to host I.
- (d) Host A connects to host B.
- (e) Host F connects to host J.
- (f) Host H connects to host A.

Part	Switch	Input Port	Input VCI	Output Port	Output VCI
a	1	2	0	3	0
b	1 2 3	0 3 0	0 0 0	1 0 3	0 0 0
c	1 2 3	0 3 0	1 1 1	1 0 2	1 1 0
d	1 2 3	2 3 0	1 2 2	1 0 3	2 2 1
e	2 3 4	1 0 2	0 3 0	0 1 3	3 0 0
f	1 2 4	1 1 0	3 1 0	2 3 3	2 3 1

The switches we go to

Input port for each switch

Output port for each switch