EE 315 – Module #1 Practice Problems

1. For a given amplifier, you are given the following information.

    - The source is a microphone that produces a sine wave with a peak input signal of 0.2 V and 1mA.
    - The output drives a 100 Ω resistor that absorbs 48.4 mW of average power.
    - The DC supplies are ±3V with dc currents of 20mA (assume average quantities).

    Find the following:

    a. Voltage gain, Current gain, and Power gain in ratio units and dB units
    b. Amplifier efficiency
    c. Power dissipated by the amplifier

2. An amplifier provides linear operation at a gain of 200 V/V. You are given the following information about the clipping levels for given DC supplies.

DC supplies	**Input at which Clipping occurs**
± 2V	± 0.00850 V
± 5V	± 0.02150 V
± 10V	± 0.0.4250 V

    Find the output voltage range for each power supply level and at what the percentage of the DC supplies does the output clips.

3. An amplifier with a gain of 1 V/V has an input resistance of 1MΩ and an output resistance of 40 Ω. A source with a peak 2 volt signal and a 200kΩ resistance is utilized as an input to drive a 150 Ω load. Draw the circuit and find the voltage, current and power gains in ratio units and dB.

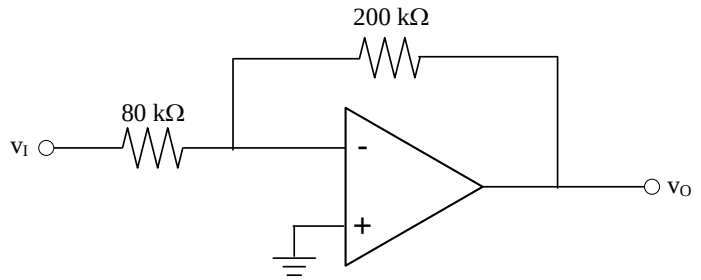
4. You have a 10mV, 100kΩ source that will drive a 50 Ω load. You are given the following amplifiers to cascade between the source and load. What combination works best? Why?

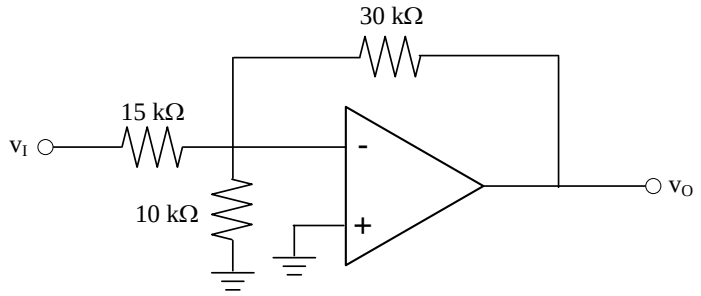
	Voltage Gain (dB)	Ri (Ω)	Ro(Ω)
Amplifier I	40	10k	10k
Amplifier II	6	100k	20

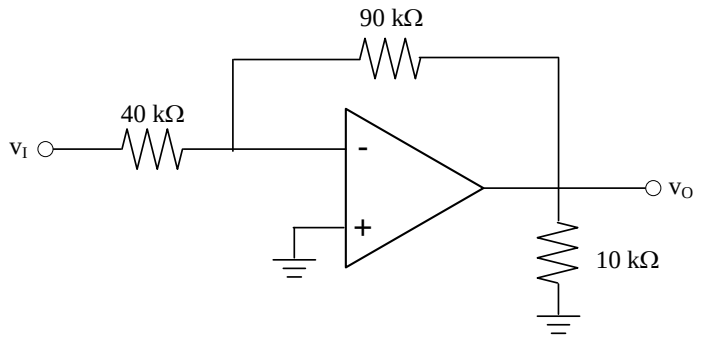
EE 315

Module 2 ! π tℕl·ŎűλŎŜ tℕ2ōfŜYă

1. For the following circuits, find the closed loop voltage gain and the input resistance. Assume ideal op-amps.







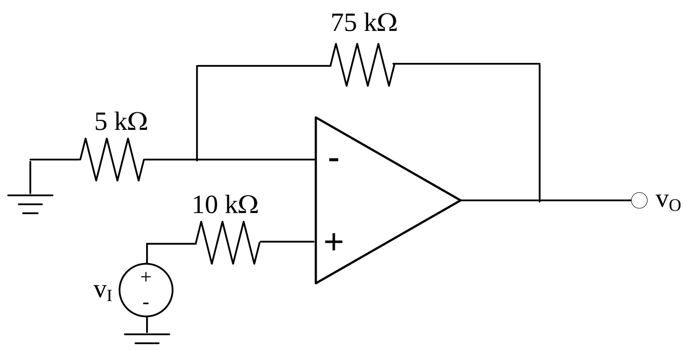
2. Design an ideal inverting amplifier with a closed loop gain of -5V/V. The output voltage is limited to –10 V≤ v_O≤ 10V, and the maximum current in any resistor is limited to 50μA.

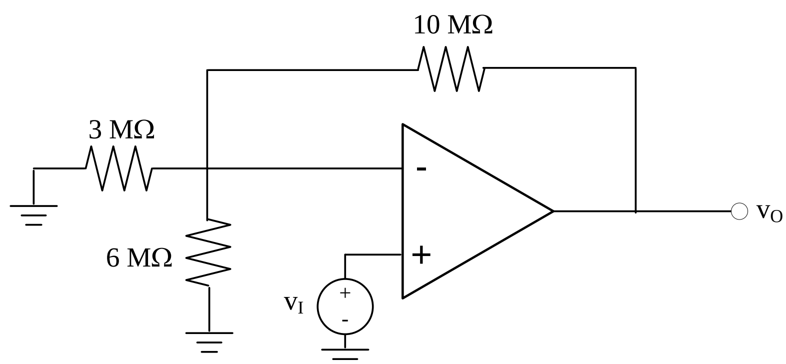
3. Using the standard inverting configuration with an ideal op-amp, design for a closed loop gain of -1000 V/V. The maximum resistor value allowed in 100 kΩ. What is the input resistance? Use the circuit with the T resistor feedback and the same maximum resistor value, design the circuit for the same closed-loop gain of -1000 V/V. What is the input resistance for this circuit?

4. Design a weighted summer circuit for the following equations:
   a. $v_O = -2v_1 - 8v_2$
   b. $v_O = -12v_1 - 3v_2 + 2v_3$

   Resistors should range between 10kΩ and 1MΩ

5. For the following circuits, find the closed loop voltage gain and the input resistance. Assume ideal op-amps.





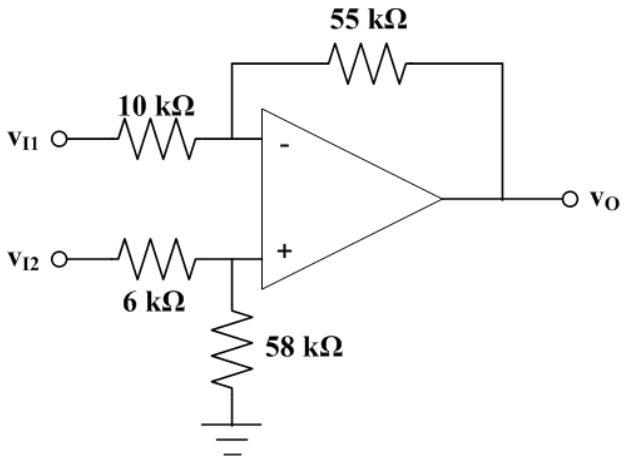
6. We worked an example where a potentiometer was used to divide the resistance between R1 and R2 for a typical non-inverting amplifier configuration. We found that the range of gain was 1 to infinity. For this problem, consider how you might add a fixed resistor to the circuit to prevent the gain from increasing above 11 V/V. Draw the circuit and show how you calculated the new range of closed loop gain from 1 to 11 V/V.

7. [illegible]

EE 315
Module 2B – Practice Problems

1. Design a difference amplifier such that the differential gain is 50 V/V, the minimum differential input resistance is 50kΩ, and the common mode gain is zero.

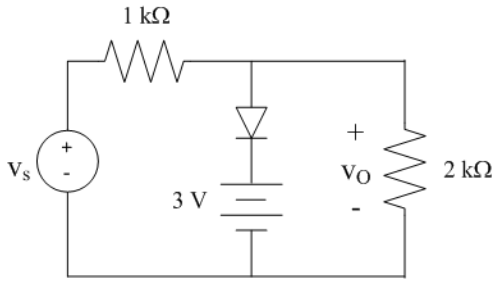
2. For the following circuit, derive and solve for the differential and common mode gain and the CMRR.



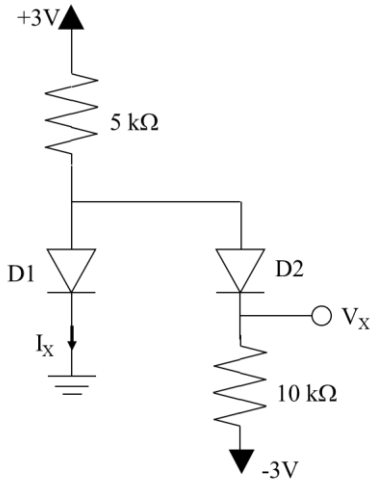
3. Design an instrumentation amplifier for a differential gain that is adjustable between 5 and 500 V/V. Assume that the gain of the second stage is 2 V/V.

EE 315 – Module 3 Practice Problems

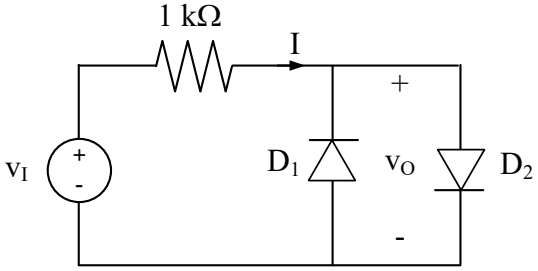
1. For the following circuit assume that the source voltage is a square wave with a peak voltage of 6 volts and has a zero average value. For the following circuit, sketch the voltage, $v_O(t)$ and find the average value. Assume ideal diode.



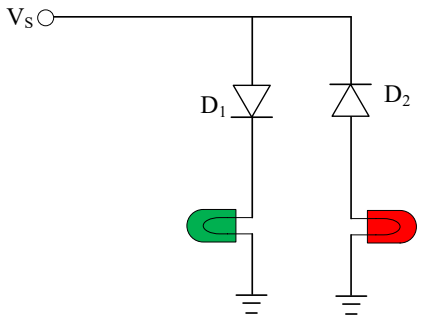
2. For the following circuit, find the voltage, V_x and the current, I_x. Assume ideal diodes



3. For the following circuit, $v_I = 10\cos(t)$ volts. Assume ideal diodes.
   a. For what values of v_I is diode 1 on?
   b. For what values of v_I is diode 2 on?
   c. What is the peak current value, I (magnitude only required).
   d. Plot the voltages, v_I and v_O.

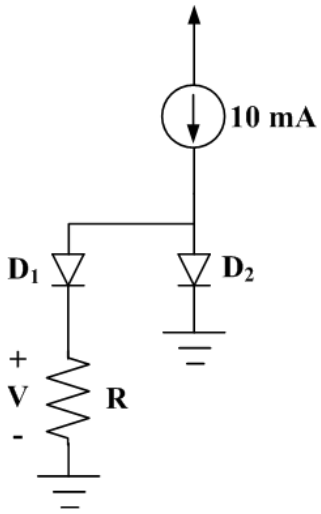


4. Consider the following circuit. The voltage, V_S, can be either +3V, 0V, or -3V. The LED lights require +3 volts dropped across them in order to light up. Assume ideal diodes.

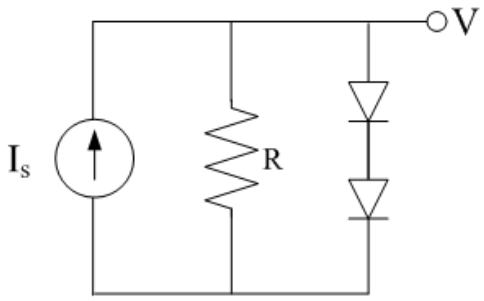


   a. What does V_S need to be for the green light (only) to be on?
   b. What does V_S need to be for the red light (only) to be on?
   c. Can both lights be on simultaneously?

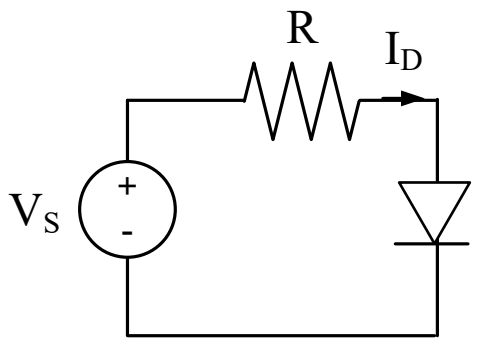
5. Consider the following circuit. The diodes are identical and operate in the forward bias region at room temperature. Find the value of the resistor, R, such that the voltage drop, V is 80mV.



6. Consider the following circuit. The diodes are identical and have a current of 1mA for a voltage of 0.7V. The source current is 100mA. Design the resistor, R, such that the voltage, V is 1.6V.

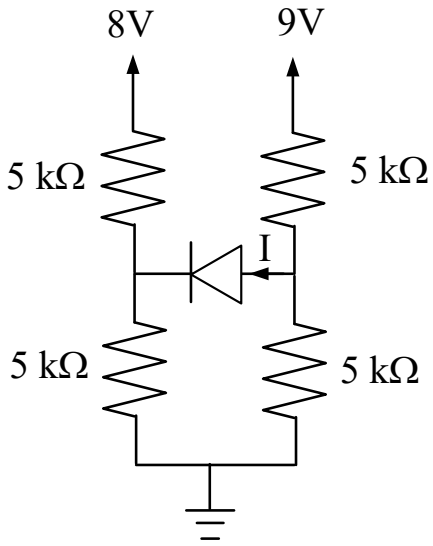


7. Consider the following circuit where the voltage source is 1V and the resistor is 200 ohms. The diode is known to have 1mA at 0.7V.

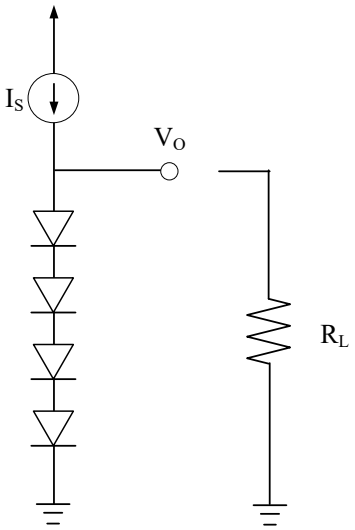


   a. What is the current, I_D assuming an ideal diode?
   b. What is the current, I_D assuming a 0.75 constant drop model?
   c. What is the current, I_D using the iterative process using the exponential model?

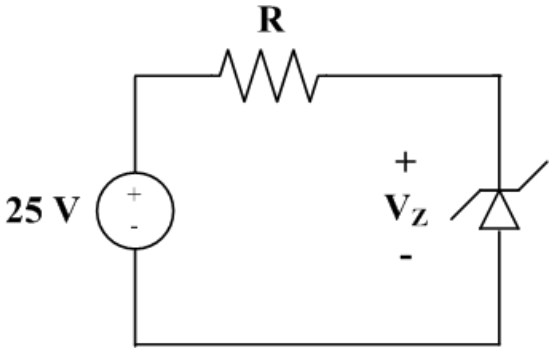
8. Consider the following circuit. Find the current I using (a) the ideal model and (b) using a 0.7V constant drop model of the diode. Hint! Use Thevenin equivalent circuits to simplify the circuit.



9. Consider the following circuit. The diodes are identical with a saturation current of $1X10^{-16}$ A. What should the current I_S be to obtain an output voltage of 2.8V? Suppose a load resistor is connected at the output and draws 0.1mA of current from the diodes. What is the change in the output voltage?



10. Consider the following circuit, which contains a 9.1 V zener diode. It is know that when the zener voltage is 9.1V, the zener current is 3mA. The incremental zener resistance is 25Ω. Find the resistor R, if the zener current is 5mA.



EE 315 Module 4 Practice Problems

1. An NMOS transistor is characterized as follows: V_{DS}=0.1V, V_t=1.5V, k'_n= 25 µA/V^2, and W/L = 10. Find the drain current for V_{GS}=0V, 1V, 2V, and 3V.

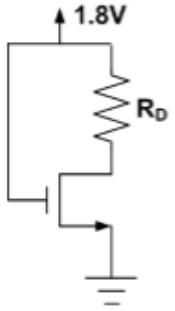
2. An NMOS transistor is characterized as follows: V_{DS}=3.3V, V_t=1.V, k'_n= 37.5 µA/V^2, and W/L = 10. Find the drain current for V_{GS}=0V, 1V, 2V, and 3V.

3. Identify the region of operation and the drain current for an NMOS transistor where the k'_n= 25 µA/V2, V_t=1Vand W/L = 10.
   a. V_{GS}=5V and V_{DS}=6V
   b. V_{GS}=0V and V_{DS}=6V
   c. V_{GS}=2V and V_{DS}=-0.5V

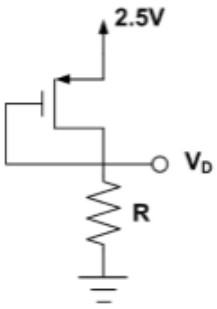
4. An NMOS transistor has V_t=0.8V, k'^n= 0.05 mA/V^2, and W/L = 2. The device is biased at V^{GS}=2.5 V. Calculate the drain current and the resistance r_O for V_{DS}=2V and 10V for
   a. λ=0
   b. λ=0.02
   c. V_A=35V

5. A PMOS transistor has k'_p= 0.1 mA/V^2, W/L = 2, V_t= -2V and V_{SG}= 3V. Find the region of operation and the drain current for:
   a. V_{SD}=0.5V
   b. V_{SD}=2V
   c. V_{SD}=5V

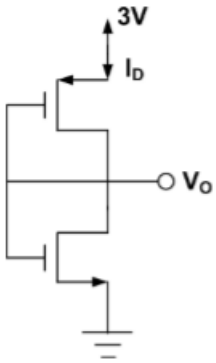
6. Consider the following NMOS circuit where V_t=0.5V, k'_n= 0.4 mA/V2, and W/L = 5. If the circuit operates at the edge of saturation with a drain current of 1mA, find the resistor, R_D.



7. Consider the following PMOS circuit where V_t=-0.6V, k'_p= 250 µA/V^2, and L = 0.25µm. find the values required for W and R such that the drain current is 0.8mA and the drain voltage is 1.5V.



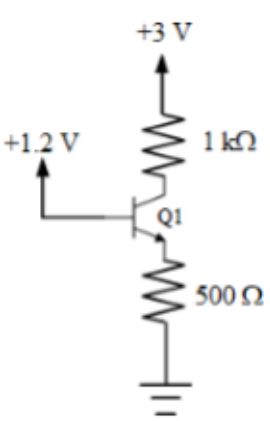
8. Find the labeled voltages and currents in the following circuit where V_{tn} =+1V, V_{tp} = -1V, k'_n= 20 µA/V^2, k'_p= 8 µA/V^2 and W/L = 3 (for both n and p-type transistors).

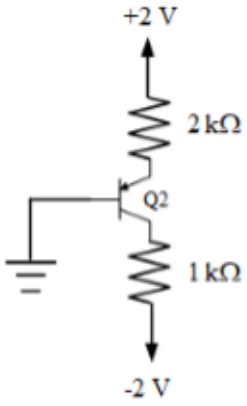


EE 315

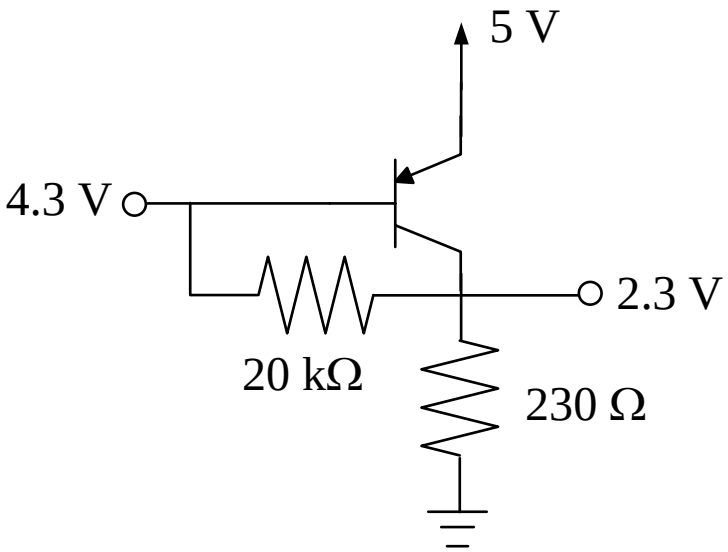
Practice Problems Module 5

1. For an npn BJT, the voltage v_{BE}=0.74 V for i_C=9.5mA. What i_C for v_{BE}=0.714 V?
2. For a given BJT, i_B=0.010mA and i_C=0.6mA. What are I_S, β, α, and i_E?
3. A BJT has $I_S=5x10^{-15}$ A and β fall in the range of 50 to 500. If the BJT operates in the active mode with v_{BE} = 0.64V, find the expected range of the collector, base, and emitter currents.
4. For Q_1 and Q_2 below, find the collector, base, and emitter currents for β=50 and $|V_{BE}|$=0.8V. What is the mode of operation for each circuit?

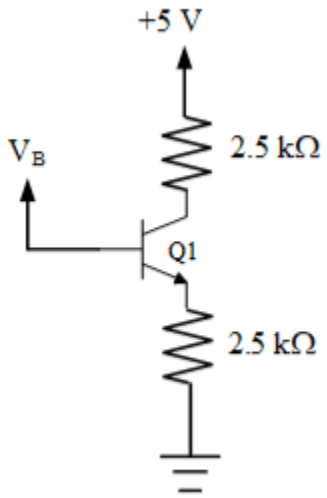




5. For the pnp transistor circuit below, find I_C and β.



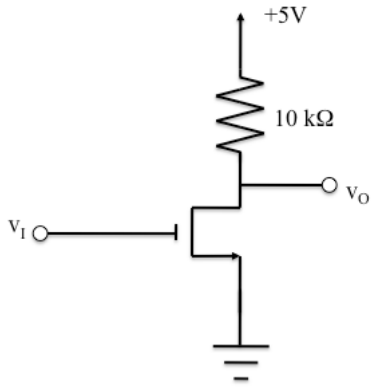
6. For the following transistor, find the collector, base, and emitter currents and the collector and emitter voltages for the case where $\beta=100$ and β being very large. Assume $V_{BE}=0.7$ V. Do this for each of the following base voltages: $V_B=0$ V, $V_B=1$ V, and $V_B=2$ V.



Module 6: Homework

EE 315

1. Consider the following common source amplifier, where V_t= 1.5V, k'_nW/L = .2 mA/V^2.



a. Sketch the voltage transfer characteristic, clearly labeling the transition points, A, B and C.
b. The device is biased for a 0.15 mA drain current. Find the Q-point.
c. Find the voltage gain at this bias point.

2. A common source amplifier uses an NMOS transistor with k'_n=0.4mA/V^2, W/L = 10, V_t=0.4V, V_{DD}=2.5 Vand V_A=10V. The amplifier Q-point is at I_{DQ}=0.2mA and uses a drain resistor of 6.2kohms.

a. Find V_{GSQ} and V_{DSQ}.
b. Draw the small signal model and find g_m, R_{in}, A_{vo}, and R_o.
c. If a load resistor is connected to the drain where R_L = 15kohms, what is the gain, A_v. Update your small signal model.
d. If a source signal, v_{sig} in series with a resistance of R_{sig} = 300kohms is connected to the gate, what is the gain, G_v.

3. A common gate amplifier uses an NMOS transistor with g_m=4mA/V and a drain resistor of 5kohms and a load resistor of 7.5 kohms. The amplifier is driven by a source, v_{sig}, that has R_{sig} = 500 ohms.

a. Find the input resistance (R_{in}) and the overall voltage gain, G_v. Draw the small signal model.
b. Suppose we want the input resistance to equal the signal resistance at the Q-point, I_{DQ}. What would the drain current Q-point need to change to for this to happen?

4. A common drain amplifier has the following characteristics: $k'_n=0.1mA/V^2$ and V_t = 0.6V. The operating point is $V_{GSQ}=0.85$ V.
   a. What is the W/L ratio for an output resistance of 300 ohms?
   b. What is the drain current at the operating point?
   c. This amplifier is connected to a 10kohm potentiometer as the load. What is the range of possible overall voltage gain?

Practice Problems Module 7

EE 315

1. A CE amplifier uses an npn BJT with β=100 and I_{CQ}=0.5 mA. The collector resistor, R_C is 12 kΩ and R_L=12 kΩ. The amplifier is connected to a signal source with a signal resistance of 10 kΩ. Find the input resistance, R_{in}, output resistance R_o, and the gain, G_v. Assume that V_A = 50V. Draw and clearly label the small signal model.

2. A CB amplifier uses an npn BJT with R_C is 10 kΩ and R_L=10 kΩ. The signal resistance is 50 Ω. If α is approximated to 1, what should the collector current q-point be such that the input resistance, R_{in}, is equal to the signal resistance? What is G_v?

3. A CC amplifier uses an npn BJT biased at a collector q-point of 2mA. The signal resistamce, R_{sig} is 10 kΩ and R_L= 500 Ω. β is 100. Find R_{in} and G_v.