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CPE221
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EXAM 2 Answers

1.Byte Addressable

2. STR

3. Link Register

4. False

5. True

6.

a)

6*MAX((170,120,250,230,270,120)+20) = 6*290 = 1740ps, 1.740ns

b)

1*(170+120+250+230+270+120) = 1160ps

7.)

3-Address	2-Address	1-Address	0-Address

MPY A,B,D
SUB A,A,C
SUB T, F, G
ADD A, A, T
DIV A, E, A
	LOAD A, B
	MPY A, D
	SUB A,C
	LOAD T,F
	ADD T,G
	DIV A, T
	LOAD Z, E
	LOAD Z, A
		LDA B
		MPY D
		SUB C
		STA T
		LDA F
		ADD G
		STA Z
		LDA T
		DIV Z
		STA Y
		LDA E
		SUB Y
		STA A
			PUSH E
			PUSH B
			PUSH D
			MPY
			PUSH C
			SUB
			PUSH F
			PUSH G
			ADD
			DIV
			SUB
			POP A

```
29          AREA PROB_8, CODE, READ
30          ENTRY
31          ADR     r0, x
32          ADR     r2, z
33          LDR     r3, size
34          LDR     r4, i
35 loope    CMP     r4,r3
36          BGE     done
37          LDR     r8, [r0, r4, LSL #2]
38          BL      times4
39          STR     r9, [r2, r4, LSL #2]
40          ADD     r4, r4, #1
41          B       loope
42 done     B       done
43 times4   MOV     r9, #0
44          MOV     r1, #0
45 loopf    CMP     r1, #4
46          BGE     back
47          ADD     r9, r8, r9
48          ADD     r1, r1, #1
49          B       loopf
50 back     MOV     pc, lr
51 done     B   done
52 x        DCD     100, 3, -1, 2, 4, 4, 2, -1, 3, 100
53 z        SPACE   40
54 i        DCD     0
55 size     DCD     10
56          END
```

8.
Wrote in arm and then transferred over.

9.

Cycle	Concrete RTL	Signals
1	P <- PC	EPC = 1, C_{L1}
2	MAR <- P	ALU(F2,F1,F0) = 0,0,1 C_{MAR}
3	PC < P+1	ALU(F2,F1,F0) = 0,1,1 C_{PC}
4	P <- MAR	Read = 1, E_{MSR} = 1, C_{L1}
5	IR <- P	ALU(F2,F1,F0) = 0,0,1, C_{IR}
6		

10.

Cycle	Concrete RTL	Signals
1	B <- R0, C<-R1	ERO_D = 1, ER1_C = 1
2	T <- B or C	ALU(0110), M_ALU_B, M_T
3	R0 <- B’	ALU(0111), M_ALU_B, CR1
4	R1 <- C’	ALU(0110), M_ALU_B, CR1
5	R0 <- B’ or C’	ALU(0110), M_ALU_B, CR0
6	R1 <- T and R0	ALU(0101), M_ALU_B, CR1

11.)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
MUL r0, r1, r2	F	O	E	W										
ADD r2, r1, r8		F	O	E	W									
LDR r1, [r0]			F	O	E	W								
ADD r7, r6, r6				F	O	O	E	W						
ADD r3, r0, r7						F	O	O	E	W				
STR r3, [r1]								F	O	O	E	W		

12 Cycles

12.)

	1	2	3	4	5	6	7	8	9	10	11
LDR r1, [r2]	F	O	E	M	W						
ADD r3, r1, r6		F	O	O	O	E	M	W			

8 Cycles