## Practice Quiz: Modules 09, 10: Clocks, Watchdog Timer, TimerB, UART

Due Nov 1 at 11:59pm Points 21 Questions 9 Available until Nov 1 at 11:59pm Time Limit 20 Minutes

## **Instructions**

This quiz covers topics related to MSP430 clock subsystem, timer peripherals (watchdog timer, TimerB), and UART serial communication.

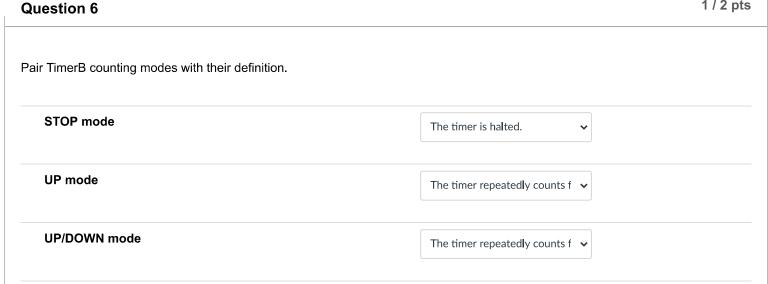
This quiz was locked Nov 1 at 11:59pm.

## **Attempt History**

|               | Attempt                                  | Time Score         |           |
|---------------|--|--------------------|-----------|
| TEST          | Attempt 1                                | 2 minutes 7.33 o   | ut of 21  |
|               |  |                    |           |
| ① Correct ans | swers are hidden.                        |                    |           |
| submitted Nov | 1 at 5:55pm                              |                    |           |
| Partial       | Question 1                               |                    | 2 / 3 pts |
|               |  |                    |           |
|               | Match MSP430 clocks with their definitio | ons.               |           |
|               | Match MSP430 clocks with their definitio | ons.  Master Clock |           |
|               |  |                    |           |

|            | Question 2  | 1 / 1 pts    |
|------------|---|--------------|
|            | MSP430 Clock modules allow software developers to change frequencies of the clock signals used by the processor and peripherals.  | i            |
|            | True  |              |
|            | ○ False   |              |
| L          |   |              |
| Unanswered | Question 3  | 0 / 2 pts    |
|            | The ACLK clock frequency is 32,768 Hz. How many MCLK clock periods occur during one ACLK clock period if we know of MCLK is 2^21 Hz. Note: enter positive decimal number. | r frequency  |
| Partial    | Question 4  | 1.33 / 2 pts |
|            | Select all operating modes of the MSP430 Watchdog Timer peripheral.   |              |
|            | ✓ Watchdog mode   |              |
|            | Interval timer mode   |              |
|            | ☐ UP/DOWN counting mode   |              |

| )         | Practice Quiz: Modules 09, 10: Clocks, Watchdog Timer, TimerB, UART: (CPE 323-01) (FA20) INTRO TO EMBEDDED CO | OMPUTER SYS |
|-----------|---|-------------|
|           | ☐ UP counting mode  |             |
|           | HOLD (not counting)   |             |
|           |   |             |
| Incorrect | Question 5  | 0 / 2 pts   |
|           | What action do you perform to "pat the dog" in case of the watchdog timer operating in the watchdog mode?     |             |
|           | Set all bits in the WDT control register  |             |
|           | Set the WDTCTLCL bit to 1 in the WDT control register to clear the timer counter                              |             |
|           | Send a bone to the dog by snail mail  |             |
|           | Clears all bits in the WDT control register   |             |
|           |   |             |
| Partial   | Question 6  | 1 / 2 pts   |
|           |   |             |



| CONTINOUS mode | The timer repeatedly counts f 🐱 |
|----------------|---------------------------------|
|                |                                 |

| Jnanswered | Question 7   | 0 / 4 pts |
|------------|--|-----------|
|            | TimerB configured in the UP counting mode uses SMCLK as the source clock. SMCLK clock frequency is 2,000,000 Hz.  What is the maximum resolution when timestamping an external event with frequency?  microseconds |           |
|            | What is duration of one period if TBCCR0=9,999?  microseconds  |           |
|            | Answer 1:  (You left this blank)   |           |
|            | Answer 2:  (You left this blank)   |           |
| ,          |  |           |
| Jnanswered | Question 8   | 0 / 3 pts |

UART communication. You configure USCI for UART communication (8-bit data, 2 stop bits, odd parity).

1. How many bits is transferred when transmitting a single character (type in the number)?

bits

| 2. What is the parity bit if y | you are sending ascii character 'a' (0x61)?   |
|--------------------------------|---|
| (enter                         | 1 or 0)   |
| 3. How long does it take to    | o transmit this character if the UART is configured for 38,400 bps (bits per second)? |
| ms (m                          | niliseconds) (enter 4 decimal places)   |
|                                |   |
| Answer 1:                      |   |
| (You left this blank)          |   |
| Answer 2:                      |   |
| (You left this blank)          |   |
| Answer 3:                      |   |
| (You left this blank)          |   |
|                                |   |

| Question 9   | 2 / 2 pts  |
|--|------------|
| UART communication. Device B always sends data to device A over a serial asynchronous link (UART). No data flows from How do you connect A and B? Symbol "" means connects to, | om A to B. |
| RxD pin of A RxD pin of B  |            |
| TxD pin of A RxD pin of A  |            |
| ○ TxD pin of A TxD pin of B  |            |
| RxD pin of A TxD pin of B  |            |