CPE 323
Intro to Embedded Computer Systems
Interrupts (Exceptions)

Aleksandar Milenkovic

milenka@uah.edu

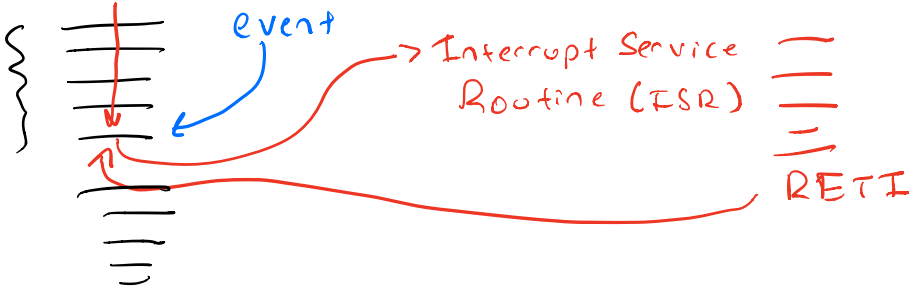
Admin

Instruction Execution Stages

- 1. Instruction Fetch
- 2. Decode
- 3. Operand Fetch
- 4. Execute
- 5. Store results
- 6. Exception process

What are Interrupts?

-> Events (asynchronous) triggered in hardware.



Interrupts are in hardware, not software!

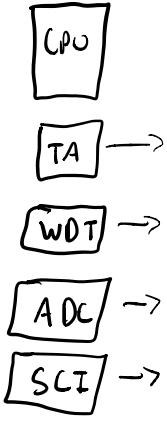
Asynchronous events!

Internally & externally.

You can trigger them by setting bits...

Sources of Interrupts

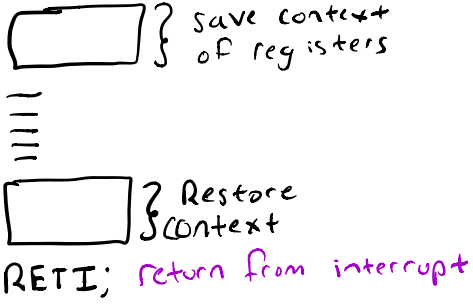
- Internal to CPU
- External (peripherals) → Polling
  → Interrupt



Interrupt Service Routine (ISRs)

→piece of code that handles event

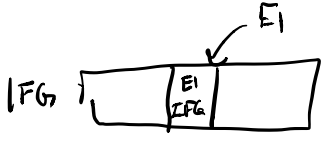
P1_ISR



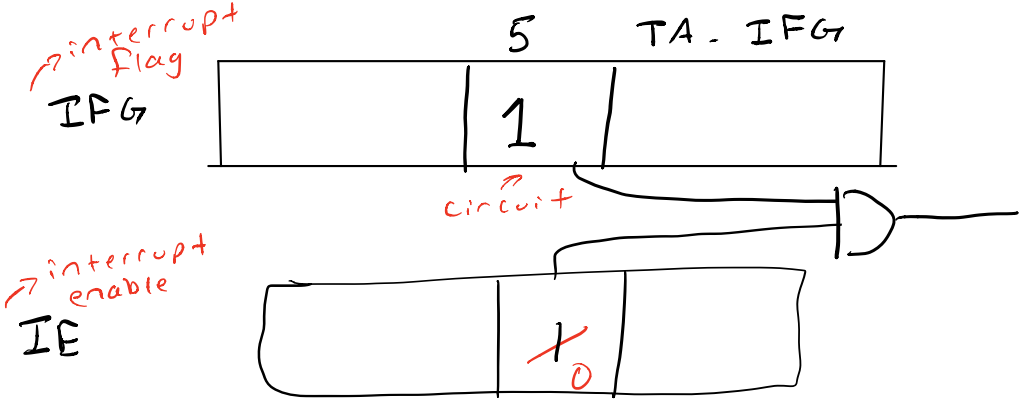
Different operating modes

What does MSP430 do as a response? (Exception Processing)

- 1. Finish instruction execution
- 2. Push PC and SR onto stack
- 3. Clear SR →
- 4. Select highest priority interrupt
- 5. Clear IFG bit for single source interrupts
- 6. Read the starting address of the corresponding ISR from the IVT (Interrupt Vector Table)
- 7. Move into PC.



Tracking Interrupts? (IFG bits)

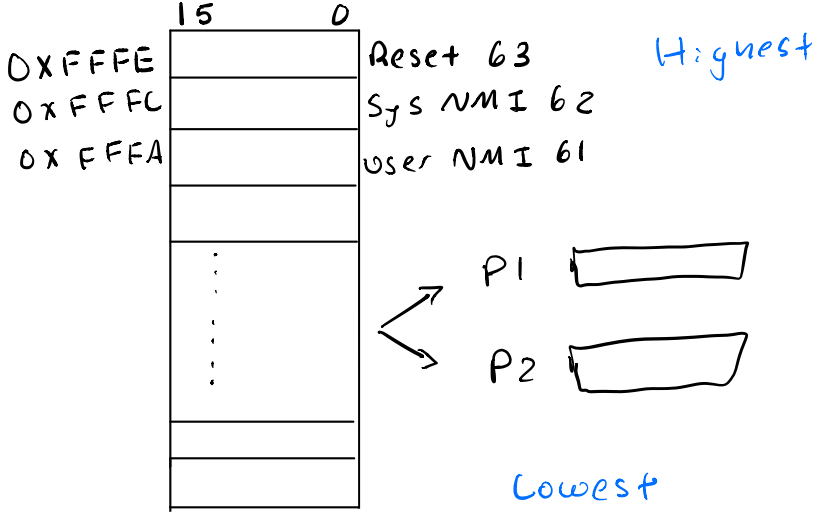


GIE- Global Interrupt Enable (SR)

Masking Interrupts (IE Bits)

- Selective masking
- Global masking (GIE)
- NMI - Non-maskable interrupt

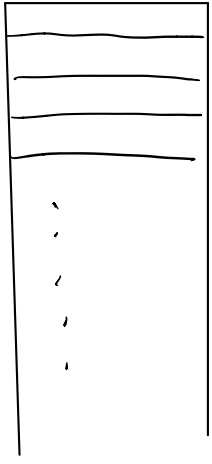
Interrupt Vector Table



Interrupt Priorities

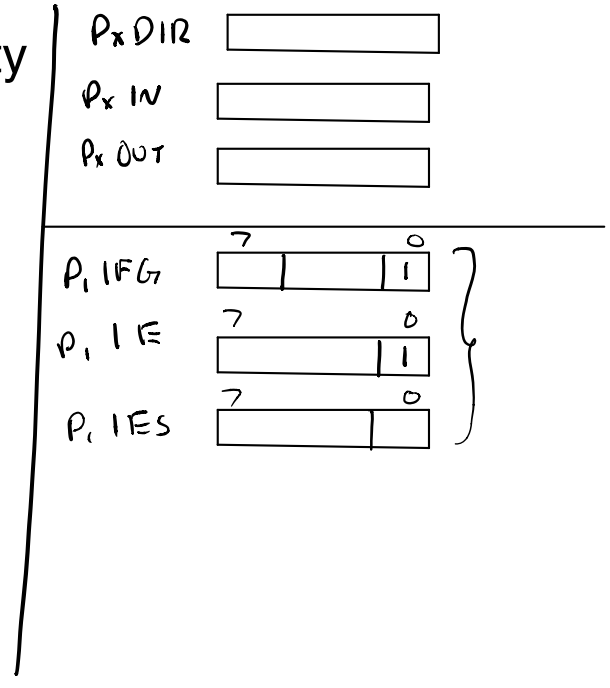
→ Vectored

→ Fixed priorities (cannot change them)



Parallel Ports and Interrupts

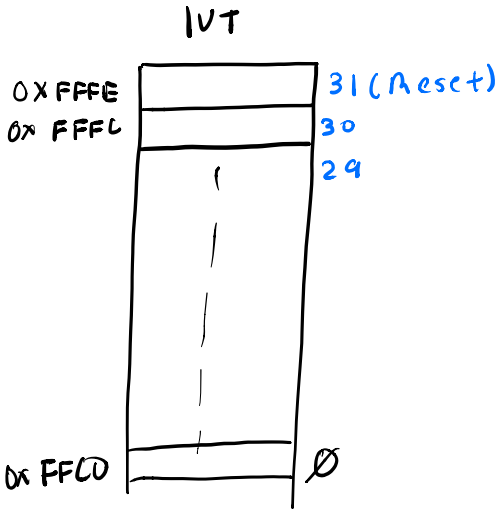
- P1 and P2 have interrupt capability
- P1IFG
- P1IE
- P1IES
- P2IFG
- P2IE
- P2IES



- Interrupts Review

1) Instruction fetch
2) " " Decode
3) Operand fetch
4) Instruction exe
5) Store results
6) Exception processing

1. Finish instruction execution
2. Push PC
3. Push SR
4. Clear SR except SCG0
5. Pick highest priority interrupt.
6. Clear corresponding IFG bit. (single source)
7. Read the corresponding entry from IVT



length = 1 word, 2 bytes.

Total size = 32 x 2 = 64 bytes.