Department of Electrical and Computer Engineering
University of Alabama in Huntsville

CPE 323 – Introduction to Embedded Computer Systems
Final Exam

Instructor: Dr. Aleksandar Milenkovic

Date: December 10, 2012

Place: EB 207

Time: 3:00 PM – 5:15 PM

Note: Work should be performed systematically and neatly. This exam is closed books and closed neighbor(s). Allowable items include exam, pencils, straight edge, calculator, and materials distributed by the instructor. Best wishes.

Question	Points	Score
1	20	
2	20	
3	20	
4	20	
5	20	
6(bonus)	7	
Sum	100+7	

Please print in capitals:

Last name:_____

First name: _____

1. (20 points) MSP430 System Architecture/Miscellaneous

Answer the questions or circle the correct answers when appropriate.

A. (6 points) The MSP430552x is a 16-bit microcontroller with 64KB of address space divided between code memory (flash), RAM memory, and input/output peripherals. It has 32 KB of flash memory placed at the top of the address space, 4KB of RAM memory starting at the address 0x2400, and 4KB of address space reserved for input/output peripherals starting at the address 0x0000. Determine the address map by filling in the following table.

Address	*Address [hexadecimal]*	*What?*
Last Flash address	0xFFFF	Flash Memory
First Flash address	0x8000	32768
Last RAM address	0x33FF	RAM Memory
First RAM address	0x2400	
Last I/O address	0x0FFF	I/O address space
First I/O address	0x0000	

B. (2 points) What is the maximum number of long words that can be allocated in the RAM memory from above?

C. (2 points) (True | False) The MOV.W #40, &0x2800 will actually write the constant 0x28 into a memory location at the address 0x2800.

D. (2 points) (True | False) The program downloaded into the flash memory through a JTAG port will remain in the flash memory only until the power is turned on (i.e., will be lost when the device is turned off).

E. (2 points) (True | False) The content of the RAM memory remains intact if a MSP430 goes into a low-power mode.

F. (2 points) (True | False) To exit a low-power mode we can execute an instruction in an ISR to clear a copy of the status register on the stack.

G. (2 point) (True | False) MSP430 instruction set includes a multiply instruction that finds a product two unsigned operands.

H. (2 point) (True | False) The MSP430 devices can read/write a byte from memory only if is placed at an even address in the address space.

2. (20 points) Interrupts

Answer the questions or circle the correct answers when appropriate.

A. (2 points) (True | False) Interrupt service routines must end with a RET (MOV @SP+, PC) instruction that retrieves the return address from the top of the stack.

B. (2 points) (True | False) The GIE bit in the status register can be set or cleared by the programmer at any point of time.

C. (2 points) (True | False) If multiple interrupt requests are pending at the time of exception processing, the MSP430 selects the one with the highest priority.

D. (2 points) (True | False) The interrupt vector table is filled with the starting addresses of the ISRs at the time of manufacturing of the microcontroller and its content cannot be changed.

E. (2 points) (True | False) The MSP430 automatically resets (in hardware) the relevant interrupt flags that record pending requests for both single-sourced and multi-sourced interrupt service routines.

An MSP430-based system interfaces 3 external devices (ED1, ED2, ED3), each capable of generating an interrupt request. The external devices place a request by setting the request line (a transition from a logic zero to a logic one). The request lines are connected on port 2 pins P2.4, P2.5, P2.6, respectively. A request line is kept active as long as the interrupt request is pending, until the request is serviced. Answer the following questions.

F (3 points) Outline the main steps that need to be taken in the main program to initialize the system for accepting the interrupts from the devices ED1-ED3.

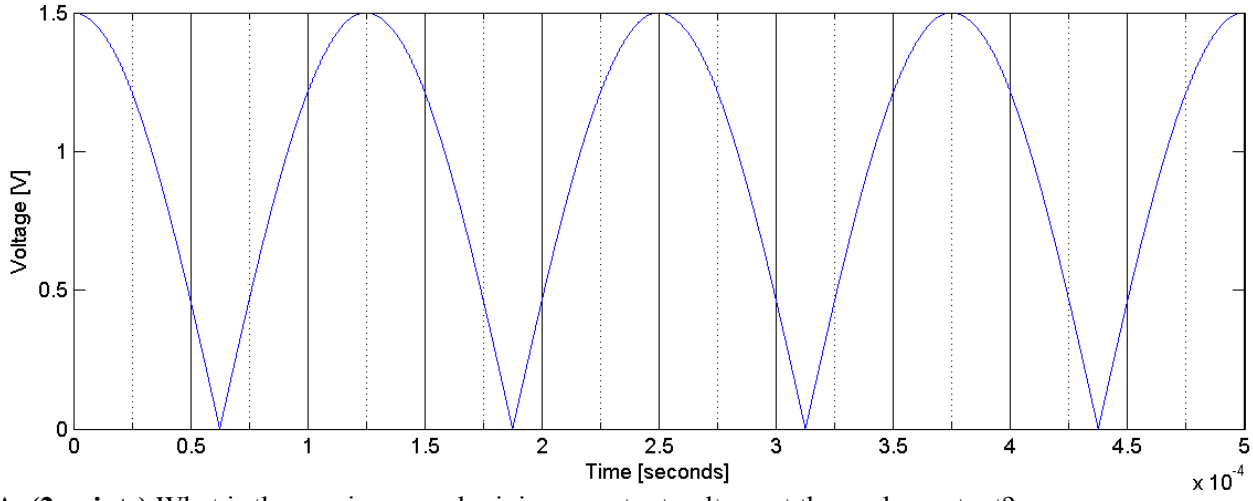
G. (3 points) If multiple requests occur at the same time, ED1 should have the highest priority and ED3 the lowest priority. Only one request should be serviced at a time. Outline the main steps taken in the interrupt service routine.

H (4 points) Assume that the ISR from part G takes 5 ms to execute. The processor is in a low-power mode when not executing the ISR. The following table describes a sequence of events in time. Fill in the table by answering what happens with the MSP430 in chronological order on each relevant event if we know the following: ED3 raises an interrupt request at 35 ms, ED2 at 37 ms, and ED1 at 48 ms. Note: add more rows in the table if needed.

Time	**Event**	**MSP430 status**
0 ms	*SW initialization*	*Active (run initialization software)*
10 ms	*Go to a low-power mode*	*Sleep*
35 ms	*Request from ED3 is received*	*P2_ISR (ED3 portion executed)*

3. (20 points) Embedded Software Design (Digital to Analog Conversion).

To drive an external actuator we need to provide an analog periodic signal y, defined as follows, y = 1.5*|cos (2*pi*f*t)| (see below), f=4,000 Hz. Your task is to generate this signal using the MSP430's digital-to-analog converter peripheral (DAC12). Answer the following questions.



A. (2 points) What is the maximum and minimum output voltage at the analog output?

$V_{R+} = 1.5V$

$V_{R-} = 0V$

B. (2 points) What is duration of one period of the signal y in milliseconds?

1.25 E-4 S .000125 S .125ms

C. (2 points) What is frequency of the signal y?

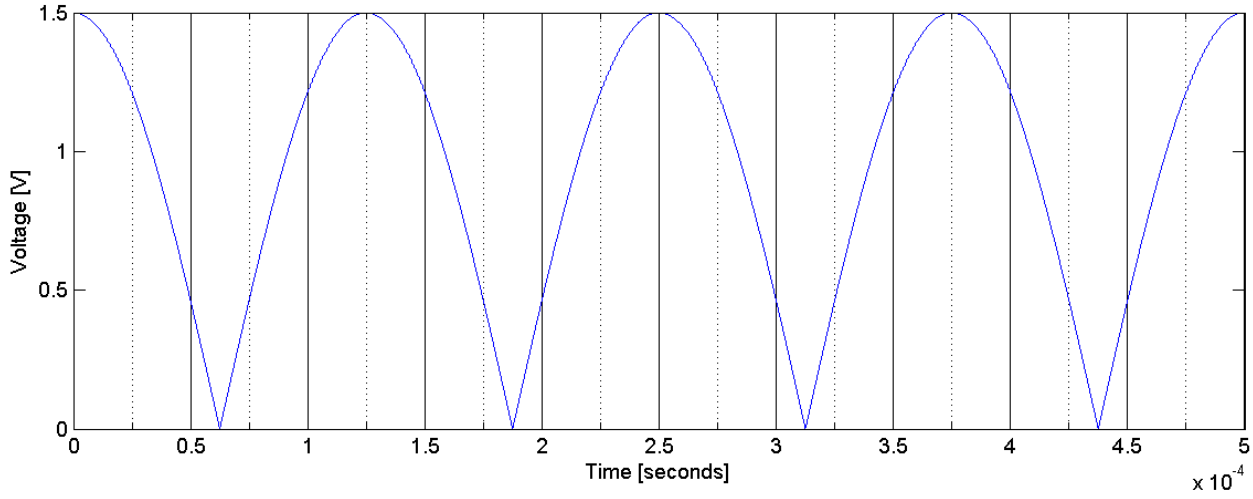
1/period = 8000

D. (6 points) Let us assume that we provide a lookup table with only 5 samples for a single period of the signal y? Fill in the following table (assume the first sample starts at t=0).

Sample	t=? [ms]	cos(2*pi*f*t)	y=1.5*|cos(2*pi*f*t)|	Lookup table [12-bit unsigned value]
1	.0	1	1.5	4045
2	.025	0.809	1.214	3312.9
3	.075	-.309	0.464	1265.4
4	.1	-.809	1.214	3312.9
5	.125	.309	0.464	1265.4

$2^{12}-1\left(\frac{1.5-0}{1.5}\right)$

E. (4 points) Sketch the output analog signal as you would see it on the oscilloscope. Use the lookup table from part C.



F. (2 points) If we use a TimerA ISR to control sending the next value to the DAC, how many interrupts per second TimerA should generate? IPS 8,000 x 5 samps = 40,000

G. (2 points) If $f_{MCLK}=f_{SMCLK}=4{,}194{,}304$ Hz, how would you configure TimerA?

4194304 = 105 - 1 = TACCR0.

4. (20 points) Time, Timers, Operating time

Answer the questions or circle the correct answers when appropriate.

A. (2 points) (True | False) The MSP430's clock module produces multiple clock signals that can be configured in software independently from each other.

B. (2 points) (True | False) The MSP430 clock signals are active all time regardless of the operating mode.

C. (2 points) (True | False) The watchdog timer (WDT) can be configured in such a way to timestamp an external hardware event (e.g., rising edge of a signal) without intervention in software.

D. (2 points) (True | False) The watchdog timer supports only several predefined time intervals.

E. (2 points) An MSP430 FLL+ is configured as follows: MCLK = 2,097,152 Hz and ACLK = 32,768 Hz. How many MCLK clocks occur in one ACLK clock?

Let us consider a program that samples a data from a 3-dimensional accelerometer. The ADC12 samples acceleration with frequency of 40 samples per second. When all 3 samples are ready, the MSP430 reads the samples from the ADC12 in the ISR and then sends the samples over a UART to a workstation in the main program. The processor is active when executing ADC12_ISR (40 processor clock cycles) and while sending samples in the main program (3,960 processor clock cycles for one triplet x, y, and z). After sending one triplet, the processor goes into a low-power mode (TimerA and ADC12 remain active). The MCLK in the active mode is 1 MHz. The platform draws 1.2 mA when the MSP430 is in the active mode and 0.2 mA when in the low-power mode.

F. (3 points) What is the total active and sleep time during one application cycle?

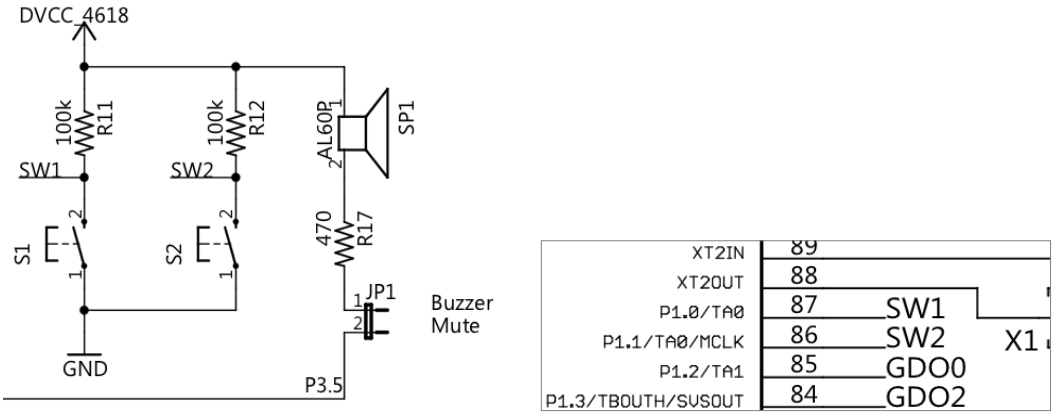
G. (3 points) Calculate the average current drawn by the MSP430.

H. (2 points) Calculate the total power P consumed (in milliWatts) if we power the platform by two AA batteries (V=3 V). Determine the system operating time in days if we know that the battery capacity is 2500 mAh.

I. (2 points) Determine the system operating time in days if we know that the battery capacity is 2500 mAh.

5. (20 points) Misc. peripherals

Consider the following schematic that describes switches (S1 and S2) and a buzzer interface to an MSP430.



A. (2 points) S1 is pressed and S2 is released. What register will reflect the status of these switches? What is the value observed in that register?

B. (4 points) Write a C code segment that detects when a switch is pressed (including debouncing) and sets a flag named sw1p to 1. The code segment should end by detecting that a switch is released.

The buzzer SP1 is connected to P3.5 of the MSP430. To sound the buzzer a pulse-width modulated signal (a square wave) with frequency of 2,500 Hz must be provided. The port P3.5 is multiplexed with TB4 – an output coming from the TimerB4 (capture and compare module 4 of TimerB).

C. (4 points) Describe how TimerB should be configured to drive the buzzer as described above. Outline steps taken in software during initialization and in steady-state operation. Assume SMCLK = 1MHz.

An MSP430 development platform is connected to a workstation over a RS232 serial interface. Assume that MSP430 uses the following UART configuration: baud rate 38,400; 8-bit characters; 1 stop bit, parity bit is included (even parity). Note: ignore multiprocessing bit.

D. (2 points) What is the maximum number of characters you can send in 1 second from the MSP430 to the workstation?

E. (2 points) (True | False) The number of characters your program can send to the workstation will dramatically decrease if the workstation starts sending characters to the MSP430 at the same time.

F. (2 points) (True | False) When sending ascii character for '0' (ascii('0')=48), the parity bit P = 1.

G. (2 points) Two devices C and D are communicating using a serial peripheral interface link. How many signals need to be routed between the devices excluding the common ground? Sketch the connection between the devices, including signal names.

H (2 points) Two devices E and F are communicating using a parallel bidirectional link with 8 data lines (half-duplex link, i.e., E and F cannot send data at the same time). In addition to data lines, what other control signals are needed to implement proper data communication? Sketch the connections.

6. (7 points) BONUS QUESTION, DMA, LCD

Answer the questions or circle the correct answers when appropriate.

A. (1 point) (True | False) DMA controller can be initialized to perform a transfer of a block of data from a memory buffer to a serial communication interface (USCI peripheral).

B. (2 points) List DMA controller registers that enable transfer of a block of the data in part A and explain how they should be initialized.

C. (2 points) Could you use a DMA controller to transfer 128 samples coming from the ADC12 controller to a buffer in RAM memory? If yes, explain what steps would you take to configure the DMA properly? How do you know when the transfer has been completed?

D. (2 points, bonus) LCD_A controller is configure in the 2-MUX mode. How many common signals are provided by the controller in this mode? Sketch the waveform(s) for the common signal(s).