The University of Alabama in Huntsville
ECE Department
CPE 221 01
Spring 2020
Homework #5

Due March 11, 2020
7.91(10), 7.92(10), 7.95(15), 7.96(15), 7.97(15), 7.98(15), 7.99(20)

F1	F0	Action
0	0	B + 1
0	1	B – 1
1	0	B + C
1	1	B - C

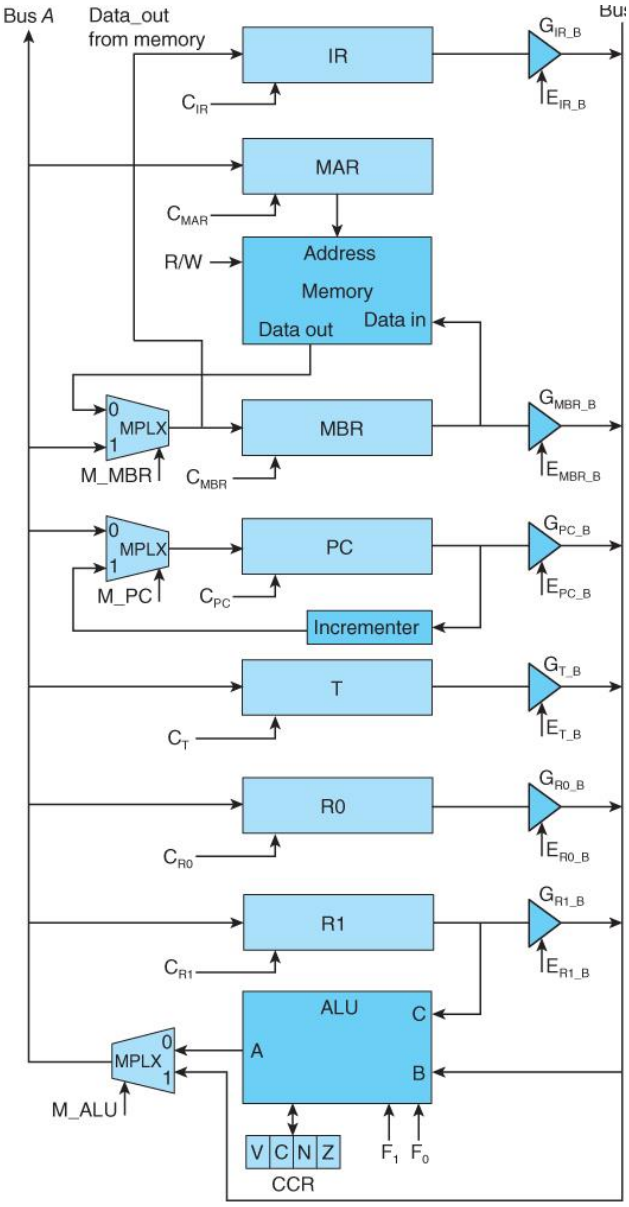
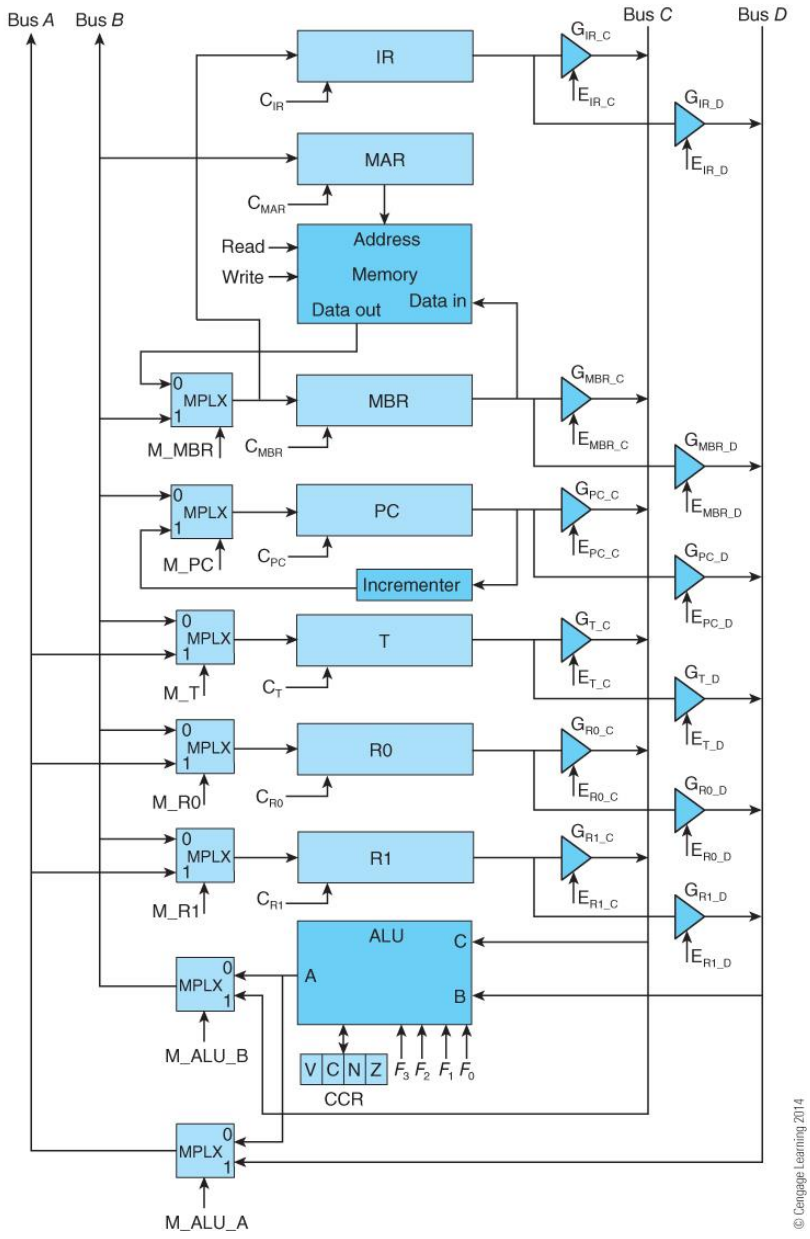


Figure 7.2



F3	F2	F1	F0	Action
0	0	0	0	B + 1
0	0	0	1	B – 1
0	0	1	0	B + C
0	0	1	1	B - C
0	1	0	0	C – B
0	1	0	1	C and B
0	1	1	0	C or B
0	1	1	1	B’
1	0	0	0	C’
1	0	0	1	C – 1
1	0	1	0	C + 1
1	0	1	1	C * B
1	1	0	0	C/B
1	1	0	1	Unused
1	1	1	0	Unused
1	1	1	1	Unused

Figure 7.3

7.91 For the microprogrammed architecture of Figure 7.3, give the sequence of actions required to implement the instruction ADD D0, D1 which is defined in RTL as D1 ← D1 + D0. You should describe the actions that occur in plain English (e.g., “Put data from this register on that bus”) and as a sequence of events (e.g., Read = 1, E_{MSR}).

7.92 For the architecture of Figure 7.3 write the sequence of signals and control actions necessary to implement the fetch cycle.

7.95 For the architecture of Figure 7.3, write the sequence of signals and control actions necessary to execute the instruction ADD M, D0 that adds the contents of memory location M to data register D0 and deposits the result in D0. Assume that the address M is in the instruction register IR. This instruction is defined in RTL form as D0 ← M[M] + D0

7.96 This question asks you to implement *register indirect addressing*. For the architecture of Figure 7.3, write the sequence of signals and control actions necessary to execute the instruction ADS [D1], D0 that adds the contents of the memory location pointed to by the contents of register D1 to register D0 and deposits the result in D0. This instruction is defined in RTL form as D0 ← M[D1] + D0

7.97 This question asks you to implement *memory indirect addressing*. For the architecture of Figure 7.2, write the sequence of signals and control actions necessary to execute the instruction ADD [M], D0 that adds the contents of the memory location pointed to by the contents of memory location M to register D0 and deposits the result in D0. This instruction is defined in RTL form as D0 ← M[M[M]] + D0

7.98 This question asks you to implement *memory indirect addressing with index*. For the architecture of Figure 7.2, write the sequence of signals and control actions necessary to execute the instruction ADD [M, D1], D0 that adds the contents of the memory location pointed at by the contents of the memory location M plus the contents of register D1 to register D0 and deposits the result in D0. This instruction is defined in RTL form as D0 ← M[M + D1] + D0

7.99 Write the code to implement the expression A = ((B * (C – D))/E + F) * G on 3-, 2-, 1-, and 0-address machines. Do not rearrange the expression. In accordance with programming language practice, computing the expression should not change the values of its operands. When working with 0-address instructions, assume that the operation is TOS ← SOS OP TOS.