Solution

- $\begin{array}{c|c}
 1. & a) & 11000 | 0 \\
 \hline
 1011 | 1101 | 0.000 \\
 \hline
 1011 | 1 | 1 \\
 \hline
 1011 | 1 | 1 \\
 \hline
 1000 \\
 \hline
 1011 \\
 \hline
 110
 \end{array}$ $\begin{array}{c}
 CRC = 110 \\
 \hline
 1000 \\
 \hline
 1011 \\
 \hline
 110
 \end{array}$
 - b) 01111110,1001111100110110,01111110
 stuffed bit
- 2. a) Network layer
 - b) baseline wander & clock recovery
 - C) hidden / exposed node problem
 - d) 1;0;0;0;1
 - e) Yes, no problem.
 - 3. a) $t_{tx} = \frac{2400}{40 \times 106} = 60 \, \mu \text{S}$
 - b) tprop= 5000 = 20 US
 - C) t = tex+tprop = 80 US
 - d) tex > 2 tprop (or 60 > 40, us), so Yes!

4.

1	Msg	Incoming Interface	Incoming VC	Outgoing Interface	Outgoing uc
1	A>2	3	4	2	71_
	2=A	2	5	3	2_

Switch 2 (52)

Msg	Incoming Interface	Incoming VCI	Outgoing Interface	Ortgory UCI
A-> 2	4	12	2	28
Z>A	2	2 1	4	5

Switch 3 (53)

	Incoming Interface	lacomy UCI	Outgoing Interface	Ougoing uc
	Incoming Interface	8 4	A land	3
A-> Z	0	7	0	12
224				

