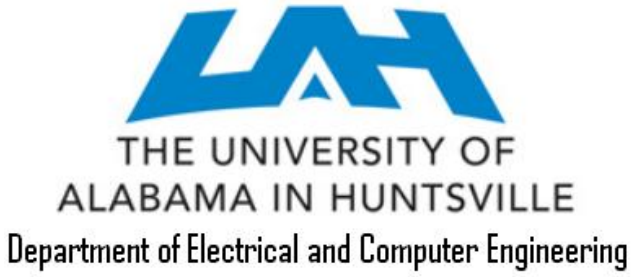

CPE 322 Digital Hardware Design Fundamentals

Simulation Assignment #1

Simulation of Finite State Machine Designs

The goal of this assignment is to give students the opportunity to gain some practical experience using Verilog HDL to simulate Finite State Machines based designs using functional RTL techniques.

Reference

In this assignment students are required to use the ModelSim® Simulator to verify that three of the implementations of the two's complement serial adder works in a manner that implements the rules of multi-bit addition. To accomplish this students are also to create a testbench module that incorporates the appropriate verilog implementation A short guide for this is presented on the CPE 322 Canvas site and is entitled "Simulating a Verilog HDL Design using the ModelSim® Compiler and Simulator in Stand-Alone Mode". Also see negator testbench example worked out in class under Homework & Simulations folder (negator.v and tb_negator.v)

Assignment

Part 1: Behavioral Simulation of Mealy FSM using ModelSim®

In this part of the assignment students are to simulate behaviorally the functionality of the STG of the Mealy FSM developed in Part 1 of Homework Assignment 1. They are to demonstrate the correct functionality of the simulation using the same input stimulus sequence that was also developed in Part 1 of Homework Assignment 1. They are to use simple RTL type behavioral simulation (zero delay).

In the final report students are to

- Include a copy of their behavioral Verilog Model of their design

- Include their simulation testbench file
- Include a screen shot of the waveform and the textual listing output that illustrates their results. Students must clearly indicate where they are reading the output relative to the clock in determining the functionality of their design.

Part 2: Structural Simulation of Mealy FSM using ModelSim®

In this part of the assignment students are to construct a structural model in Verilog of Part 2 of the Mealy FSM developed in Part 2 of Homework Assignment 1. They are to demonstrate the correct functionality of the simulation using the same input stimulus sequence that was also developed in Part 1 of Homework Assignment 1. They are to assume that all gate and flip-flop delays are 0ns.

In the final report students are to

- Include a copy of their behavioral Verilog Model of their design
- Include their simulation testbench file
- Include a screen shot of the waveform and the textual listing output that illustrates their results. Students must clearly indicate where they are reading the output relative to the clock in determining the functionality of their design.

Part 3: Behavioral Simulation of Moore FSM using ModelSim®

In this part of the assignment students are to simulate behaviorally the functionality of the STG of the Moore FSM developed in Part 5 of Homework Assignment 1. They are to demonstrate the correct functionality of the simulation using the same input stimulus sequence that was also developed in Part 5 of Homework Assignment 1. They are to use simple RTL type behavioral simulation (zero delay) and enter their design using ModelSim® .

In the final report students are to

- Include a copy of their behavioral Verilog Model of their design
- Include their simulation testbench file
- Include a a screen shot of the waveform and the textual listing output that illustrates their results. Students must indicate where they are reading the output relative to the clock in determining the functionality of their design.

Simulation Assignment Turn in Procedure

This is to be an electronic submission -- no hardcopy needs to be turned in to the instructor. You are to upload to via the course Canvas site a copy of the simulation assignment on or before its due date. Acceptable file formats include pdf, doc, and docx. This simulation assignment will be graded based on correctness, completeness and clarity of presentation.