**CPU课程设计报告**

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# 一、课程目的

# 二、设计方案

|  |  |  |
| --- | --- | --- |
| Bit in Control Memory | Micro-operation | Meaning |
| C0 | Memory<=MAR |  |
| C1 | MBR<=PC |  |
| C2 | MAR<=PC | Copy PC value to MAR for next address |
| C3 | PC<=MBR | MBR to PC |
| C4 | IR<=MBR | Copy MBR [15..8] to IR for OPCODE |
| C5 | MBR<=memory | Read from memory to MBR |
| C6 | BR<=MBR | Copy MBR data to BR for buffer to ALU |
| C7 | ALU<=ACC |  |
| C8 | MAR<=MBR | Copy MBR[7..0] to MAR for address |
| C9 |  |  |
| C10 | ACC<=MBR |  |
| C11 | MBR<=ACC | ACC to MBR |
| C12 | Memory<=MBR | Write MBR to memory |
| C13 | Control Unit<=IR |  |
| C14 | ALU<=BR |  |
| C15 | MBR<=MR |  |
| C16 |  |  |
| C17 | CAR<=CAR+1 | Increase CAR |
| C18 | CAR<=\*\*\* | Control Address Redirection, depends on the position of microinstruction |
| C19 | CAR<=0 | Reset Control Address to zero position |
| C20 | PC<=PC+1 | Increase PC |
| C21 | ACC<=0 | Reset ACC register to zero |
| C22 | ACC<=ACC+BR | Add BR to ACC |
| C23 | ACC<=ACC-BR | Sub BR to ACC |
| C24 | ACC<=ACC and BR | And |
| C25 | ACC<=ACC or BR | Or |
| C26 | ACC<=NOT ACC | Not |
| C27 | ACC<=SLL ACC 1 bit |  |
| C28 | ACC<=SRL ACC 1 bit |  |
| C29 | ACC<=ACC\*BR(L) MR<=ACC\*BR(H) | MPY and send results |
| C30 | ACC<=SLA ACC 1 bit |  |
| C31 | ACC<=SRA ACC 1 bit |  |

Auto fetch

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory,CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8],CAR<=CAR+1 | C4,C17 | 00020010 |
| CU<= IR, CAR<=CAR+1 | Control Unit<=IR,C17 |  |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |

STORE

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=ACC, CAR<=CAR+1 | C11,C17 | 00020800 |
| memory<=MBR, CAR<=CAR+1 | C12,C17 | 00021000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

LOAD

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, ACC<=0, CAR<=CAR+1 | C6,C21,C17 | 00220040 |
| ACC<=ACC+BR, CAR<=CAR+1 | C22,C17 | 00420000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

ADD

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=ACC+BR, CAR<=CAR+1 | C22,C17 | 00420000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

SUB

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=ACC-BR, CAR<=CAR+1 | C23,C17 | 00820000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

MPY

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=ACC\*BR(L), MR<=ACC\*BR(H), CAR<=CAR+1 | C29,C17 | 40020000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

AND

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=ACC&&BR, CAR<=CAR+1 | C24,C17 | 01020000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

OR

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=ACC||BR, CAR<=CAR+1 | C25,C17 | 02020000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

NOT

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| MAR<=MBR[7..0], PC<=PC+1,  CAR<=CAR+1 | C8,C20,C17 | 00120100 |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| BR<=MBR, CAR<=CAR+1 | C6,C17 | 00020040 |
| ACC<=!ACC, CAR<=CAR+1 | C26,C17 | 04020000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

SLL

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| ACC<=SLL(ACC), PC<=PC+1, CAR<=CAR+1 | C27,C20,C17 | 08120000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

SRL

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| ACC<=SRL(ACC), PC<=PC+1, CAR<=CAR+1 | C28,C20,C17 | 10120000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

SLA

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| ACC<=SLA(ACC), PC<=PC+1, CAR<=CAR+1 | C30,C20,C17 | 40120000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

SRA

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| ACC<=SRA(ACC), PC<=PC+1, CAR<=CAR+1 | C31,C20,C17 | 80120000 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |

JMPGEZ

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| IF(FLAG=0)PC<=MBR[7..0], CAR<=CAR+1 | C3,C17 | 00020008 |
| MAR<=PC, CAR<=0 | C2,C19 | 00080004 |
| IF(FLAG=1)PC<=PC+1,  CAR<=CAR+1 | C20,C17 | 00120000 |
| MAR<=PC,CAR<=0 | C2,C19 | 00080004 |

JMP

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| MBR<=memory, CAR<=CAR+1 | C5,C17 | 00020020 |
| IR<=MBR[15..8], CAR<=CAR+1 | C4,C17 | 00020010 |
| CAR<=\*\*\* (\*\*\* is determined by OPCODE) | C18 | 00040000 |
| PC<=MBR[7..0],CAR<=CAR+1 | C3,C17 | 00020008 |
| MAR<=PC,CAR<=0 | C2,C19 | 00080004 |

HALT

|  |  |  |
| --- | --- | --- |
| Microprogram | Control signals | Microinstruction |
| CAR<=0 | C19 | 00080000 |

# 三、结果仿真

# 四、总结和讨论