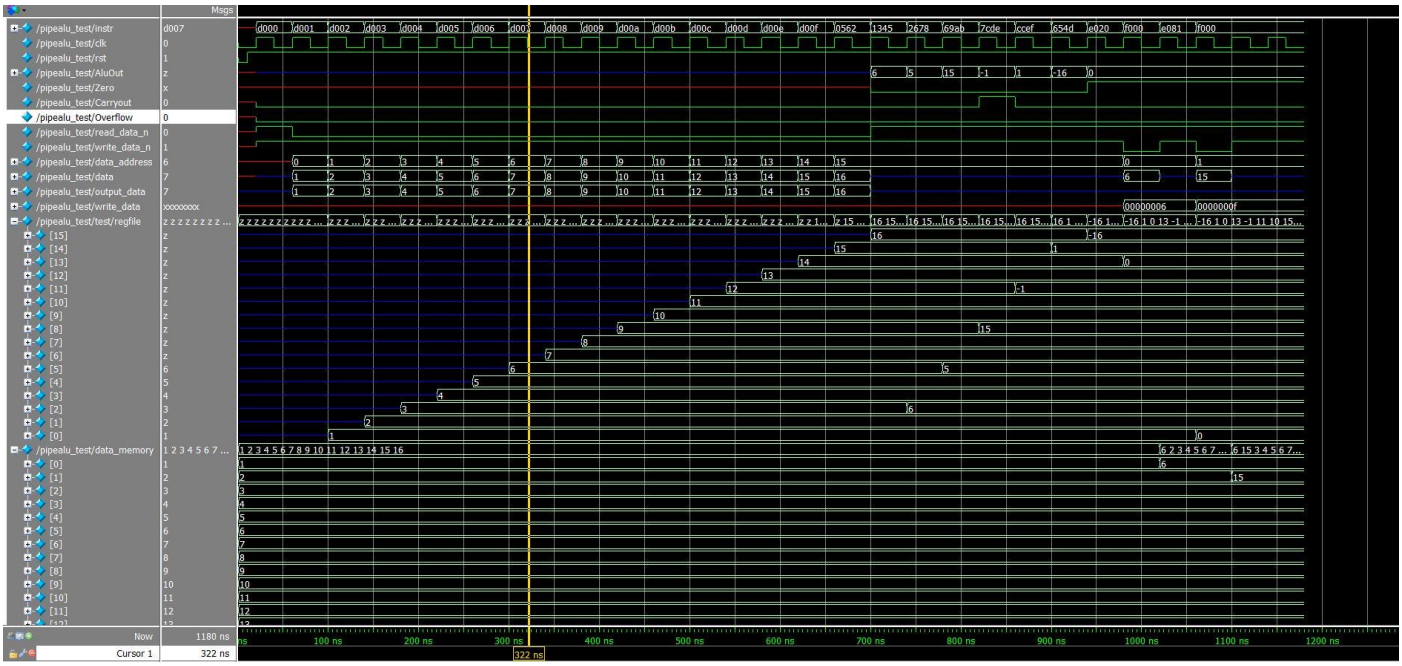

加分規定：實作出有 load/store 功能的 pipeline ALU

我將原本 HW2 改寫為 3-stage pipeline

(1)IF/ID

(2)EX

(3)WB

參考 HW3 thumb.v 加入 load store 功能

詳情見 pipealu.v 測試指令：

```
instr = 16'hd000;//ldr reg[0]<-data_memory[0]

instr = 16'hd001;//ldr reg[1]<-data_memory[1]

instr = 16'hd002;//ldr

instr = 16'hd003;//ldr

instr = 16'hd004;//ldr

instr = 16'hd005;//ldr
```

```
instr = 16'hd006;//ldr

instr = 16'hd007;//ldr

instr = 16'hd008;//ldr

instr = 16'hd009;//ldr

instr = 16'hd00a;//ldr

instr = 16'hd00b;//ldr

instr = 16'hd00c;//ldr

instr = 16'hd00d;//ldr

instr = 16'hd00e;//ldr

instr = 16'hd00f;//ldr

instr = 16'h0562;//R2 = R5 & R6

instr = 16'h1345;//R5 = R4 | R3

instr = 16'h2678;//R8 = R6 + R7

instr = 16'h69ab;//R11 = R10 -R9

instr = 16'h7cde;//R14 = a(R12)<b(R13) ? 1 : 0

instr = 16'hccef;//R15 = R12 nor R14

instr = 16'h654d;//R13 = R4 - R5 = 0

instr = 16'he020;//str reg[2]->data_memory[0]

instr = 16'hf000;//nop

instr = 16'he081;//str reg[8]->data_memory[1]

instr = 16'hf000;//nop
```