程式碼檔案：pipealu.v　　Testbench：pipealu_test.v

程式碼分兩個 always，分別代表 pipeline 的兩個階段：

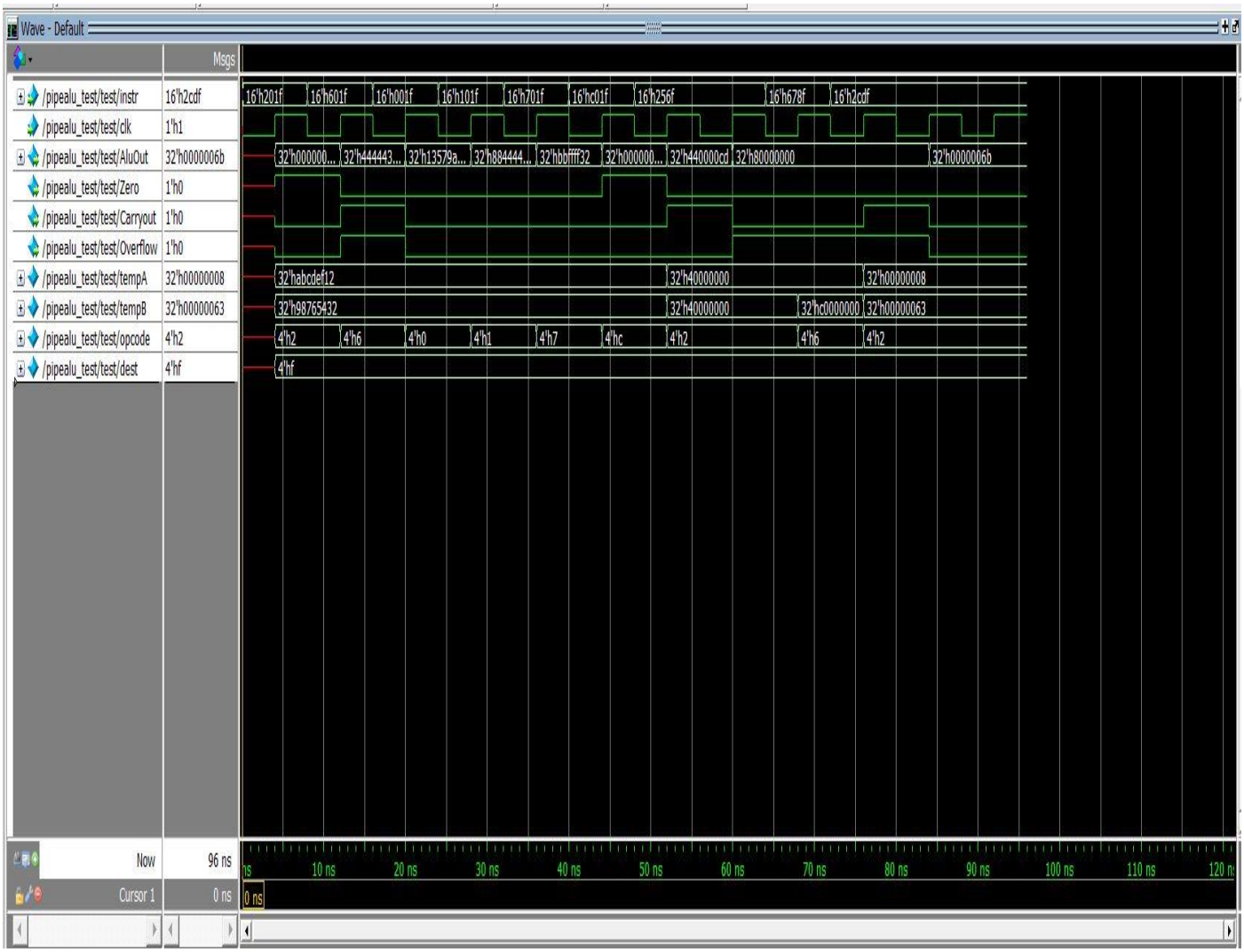
第一階段：(1)設定記憶體的值(值為固定)，(2)instruction fetch。

第二階段：(1)邏輯運算(2)計算 Carryout(3)計算 overflow

途中遇到的問題：

原本是將記憶體初始化寫在一個 initial-begin~end 內來做初始化，在 modelsim 模擬實沒有問題，但是用 Desgin Complier 合成完的 module 再度放回 modesim 模擬時就出現問題：initial 無法合成，導致結果錯誤。

Modelsim 模擬結果(modelsim_behave_result.JPG)：



Critical path delay：

```
sub_59/U2_20/CO (FADDX1)                          0.10       2.14 r
sub_59/U2_21/CO (FADDX1)                          0.10       2.24 r
sub_59/U2_22/CO (FADDX1)                          0.10       2.34 r
sub_59/U2_23/CO (FADDX1)                          0.10       2.43 r
sub_59/U2_24/CO (FADDX1)                          0.10       2.53 r
sub_59/U2_25/CO (FADDX1)                          0.10       2.63 r
sub_59/U2_27/CO (FADDX1)                          0.10       2.73 r
sub_59/U2_28/CO (FADDX1)                          0.10       2.83 r
sub_59/U2_29/CO (FADDX1)                          0.10       2.92 r
sub_59/U2_30/CO (FADDX1)                          0.10       3.02 r
sub_59/U2_31/S (FADDX1)                           0.11       3.13 f
sub_59/DIFF[31] (pipealu_DW01_sub_0)              0.00       3.13 f
U108/Q (AO221X1)                                  0.11       3.23 f
U97/Q (OR4X1)                                     0.10       3.33 f
U93/QN (NOR4X0)                                   0.03       3.37 r
U92/Q (AND2X1)                                    0.06       3.43 r
Zero_reg/D (DFFX1)                                0.00       3.43 r
data arrival time                                            3.43

clock CLK_0 (rise edge)                          10.00      10.00
clock network delay (ideal)                       0.00      10.00
Zero_reg/CLK (DFFX1)                              0.00      10.00 r
library setup time                               -0.06       9.94
data required time                                           9.94
-----------------------------------------------------------------------------
data required time                                           9.94
data arrival time                                           -3.43
-----------------------------------------------------------------------------
slack (MET)                                                  6.51
```

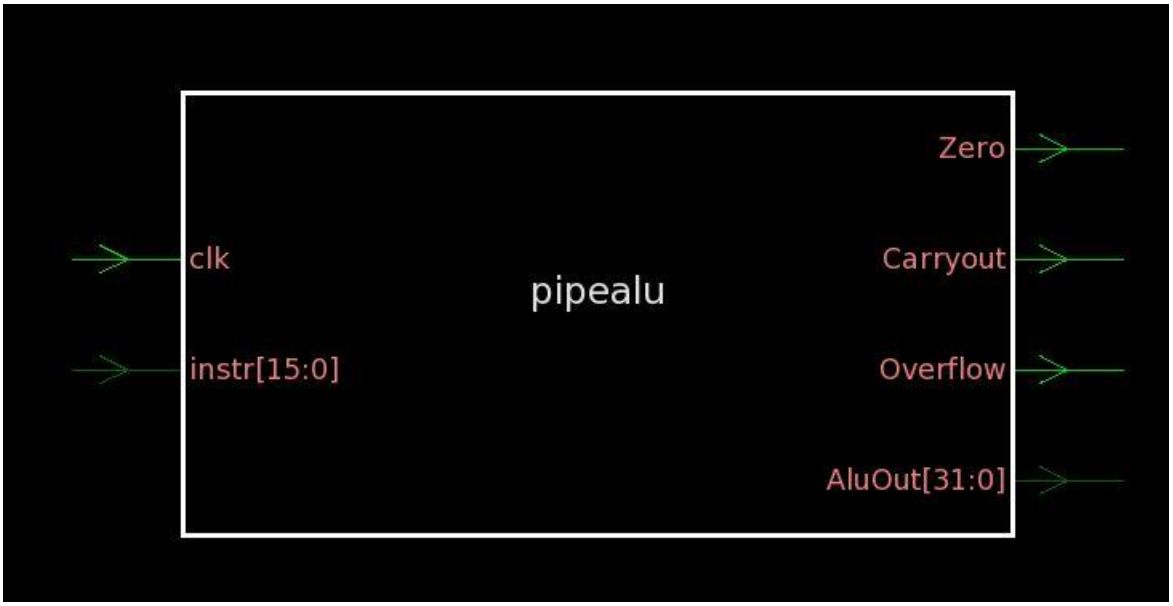
詳細資訊在：DC_timing.txt

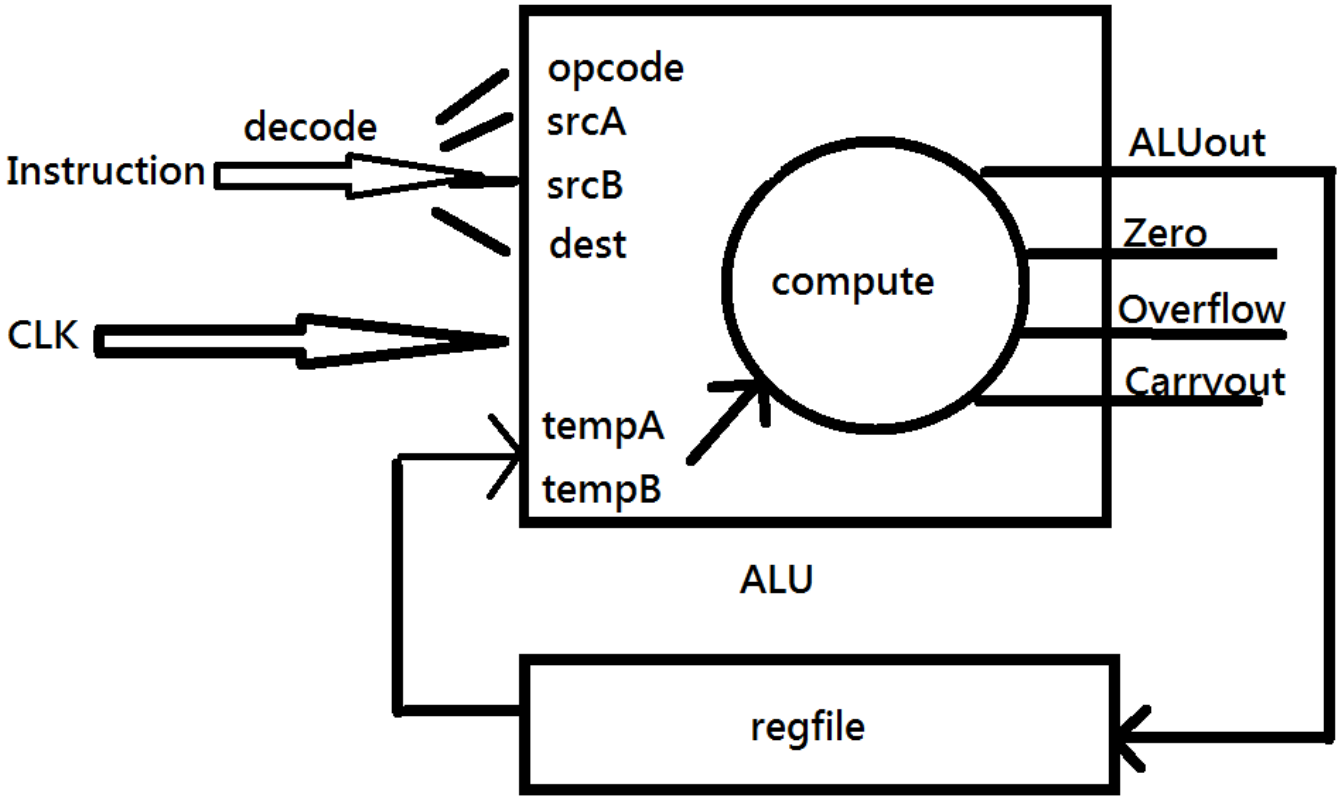
Total area cost：

```
****************************************
Report : area
Design : pipealu
Version: H-2013.03-SP5
Date   : Tue Oct 27 20:18:39 2015
****************************************

Library(s) Used:

    saed90nm_typ (File: /CBDK/SAED90_EDK/SAED_EL

Number of ports:                           52
Number of nets:                           424
Number of cells:                          333
Number of combinational cells:            231
Number of sequential cells:                99
Number of macros/black boxes:               0
Number of buf/inv:                         29
Number of references:                      24

Combinational area:               4930.559980
Buf/Inv area:                      575.078415
Noncombinational area:            2463.436769
Macro/Black Box area:                0.000000
Net Interconnect area:           23243.713499

Total cell area:                  7393.996750
Total area:                      30637.710249
```

詳細資訊在：DC_area.txt

結構圖：

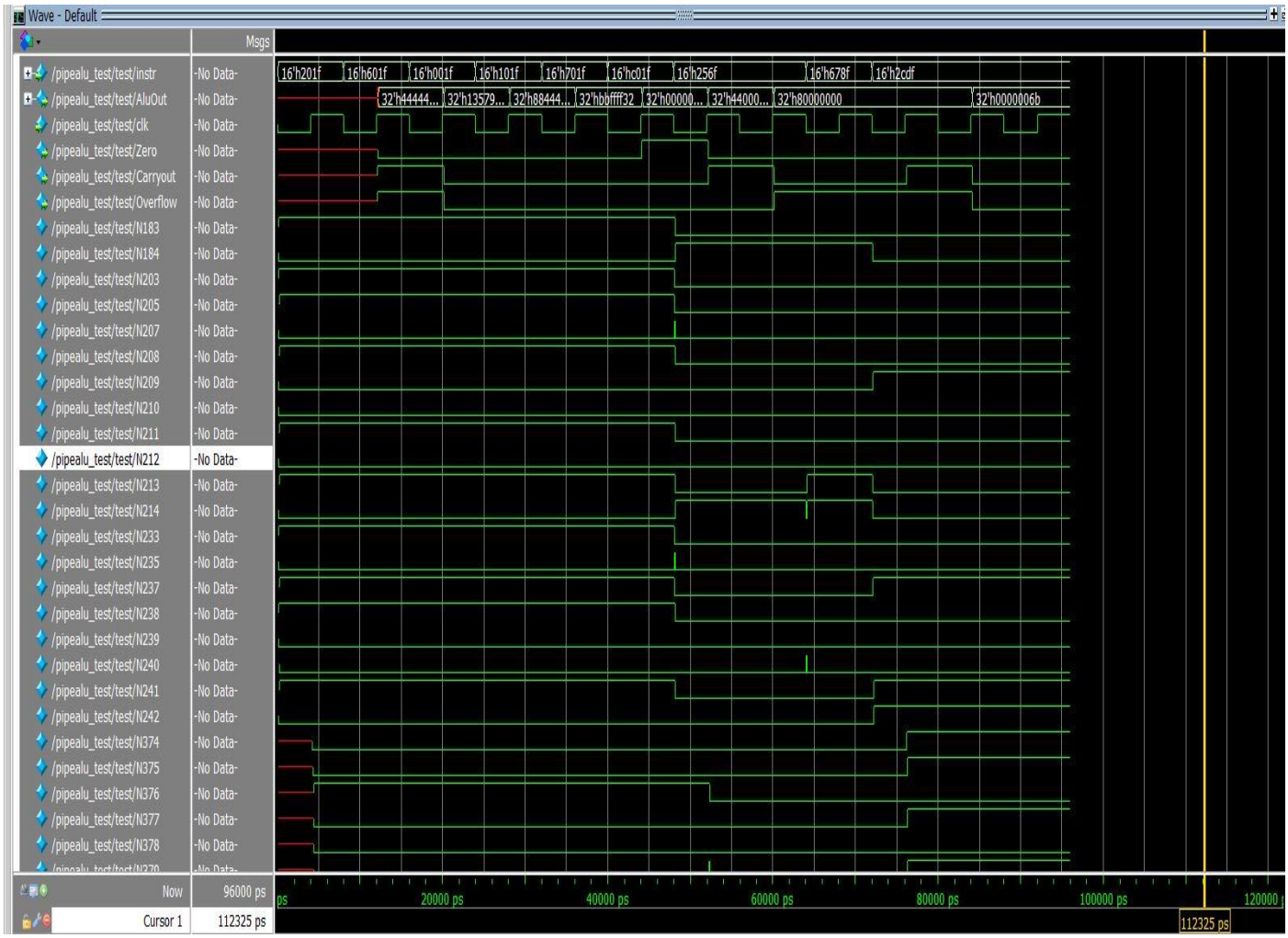


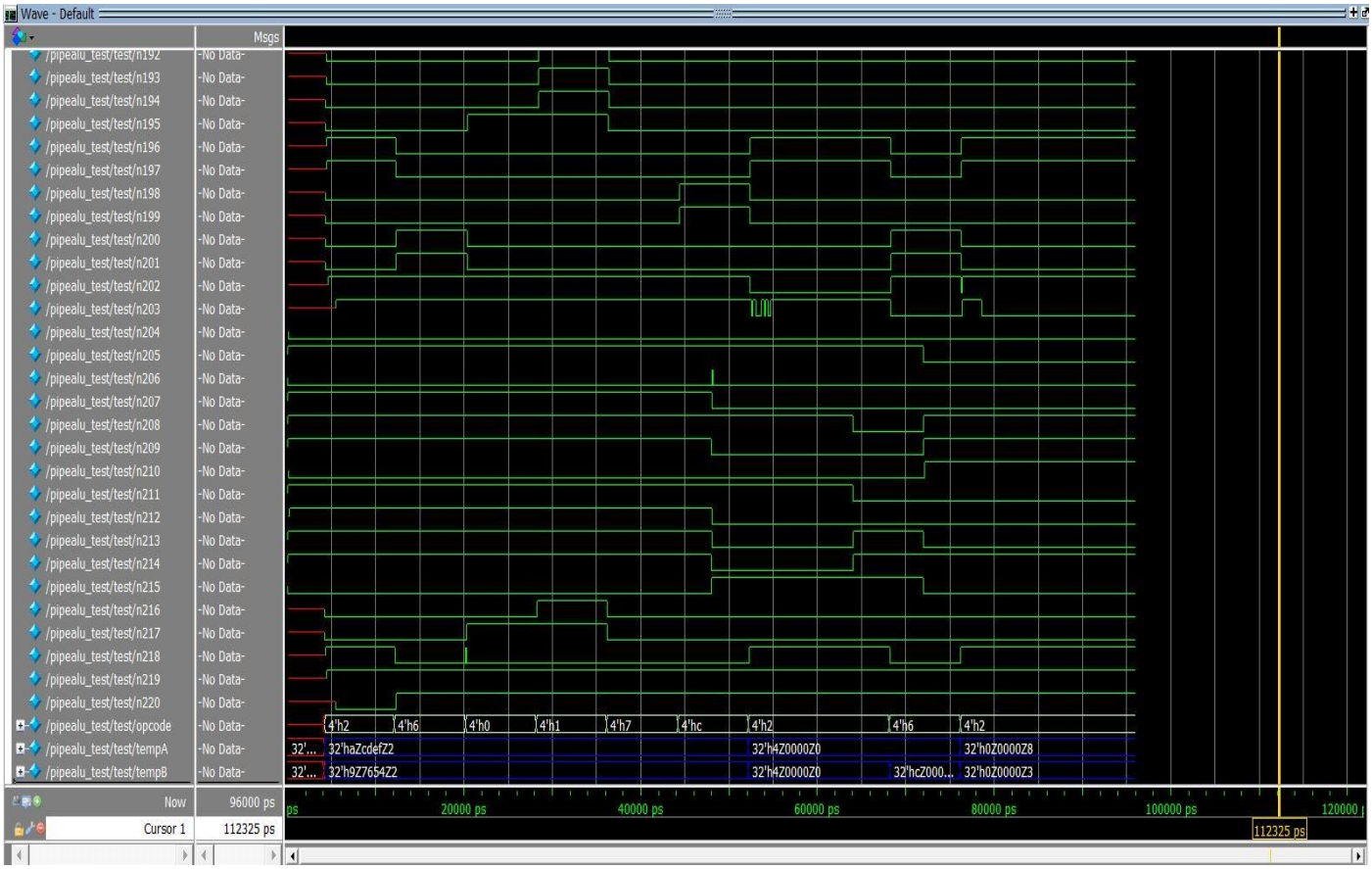


程式碼合成之後之大略結構圖如上面兩個圖片 。

用 Design Compiler 合成出來的模組(檔案 after_dv.v)用原本的 testbench 模擬：

模擬結果與原本 behavior 的寫法模擬結果相同，但是 regfile 的初始化出現問題，可能是程式寫法不嚴謹，導致合成出來的 gatelevel 模組有漏洞。


Wave - Default
Msgs
/pipealu_test/test/instr
/pipealu_test/test/AluOut
/pipealu_test/test/clk
/pipealu_test/test/Zero
/pipealu_test/test/Carryout
/pipealu_test/test/Overflow
/pipealu_test/test/N183
/pipealu_test/test/N184
/pipealu_test/test/N203
/pipealu_test/test/N205
/pipealu_test/test/N207
/pipealu_test/test/N208
/pipealu_test/test/N209
/pipealu_test/test/N210
/pipealu_test/test/N211
/pipealu_test/test/N212
/pipealu_test/test/N213
/pipealu_test/test/N214
/pipealu_test/test/N233
/pipealu_test/test/N235
/pipealu_test/test/N237
/pipealu_test/test/N238
/pipealu_test/test/N239
/pipealu_test/test/N240
/pipealu_test/test/N241
/pipealu_test/test/N242
/pipealu_test/test/N374
/pipealu_test/test/N375
/pipealu_test/test/N376
/pipealu_test/test/N377
/pipealu_test/test/N378
-No Data-
16'h201f
16'h601f
16'h001f
16'h101f
16'h701f
16'hc01f
16'h256f
16'h678f
16'h2cdf
32'h44444...
32'h13579...
32'h88444...
32'hbbffff32
32'h00000...
32'h44000...
32'h80000000
32'h0000006b
Now
96000 ps
Cursor 1
112325 ps
20000 ps
40000 ps
60000 ps
80000 ps
100000 ps
120000 ps


Wave - Default
Msgs
/pipealu_test/test/n193
/pipealu_test/test/n194
/pipealu_test/test/n195
/pipealu_test/test/n196
/pipealu_test/test/n197
/pipealu_test/test/n198
/pipealu_test/test/n199
/pipealu_test/test/n200
/pipealu_test/test/n201
/pipealu_test/test/n202
/pipealu_test/test/n203
/pipealu_test/test/n204
/pipealu_test/test/n205
/pipealu_test/test/n206
/pipealu_test/test/n207
/pipealu_test/test/n208
/pipealu_test/test/n209
/pipealu_test/test/n210
/pipealu_test/test/n211
/pipealu_test/test/n212
/pipealu_test/test/n213
/pipealu_test/test/n214
/pipealu_test/test/n215
/pipealu_test/test/n216
/pipealu_test/test/n217
/pipealu_test/test/n218
/pipealu_test/test/n219
/pipealu_test/test/n220
/pipealu_test/test/opcode
/pipealu_test/test/tempA
/pipealu_test/test/tempB
-No Data-
4'h2
4'h6
4'h0
4'h1
4'h7
4'hc
4'h2
4'h6
4'h2
32'haZcdefZ2
32'h4Z0000Z0
32'h0Z0000Z8
32'h9Z765ZZ2
32'h4Z0000Z0
32'hcZ000...
32'h0Z0000Z3
Now
96000 ps
Cursor 1
112325 ps
20000 ps
40000 ps
60000 ps
80000 ps
100000 ps
120000 ps

用 FPGA 合成 gatelevel ：

因 Xlinx 授權問題的關係，經由助教同意改用：

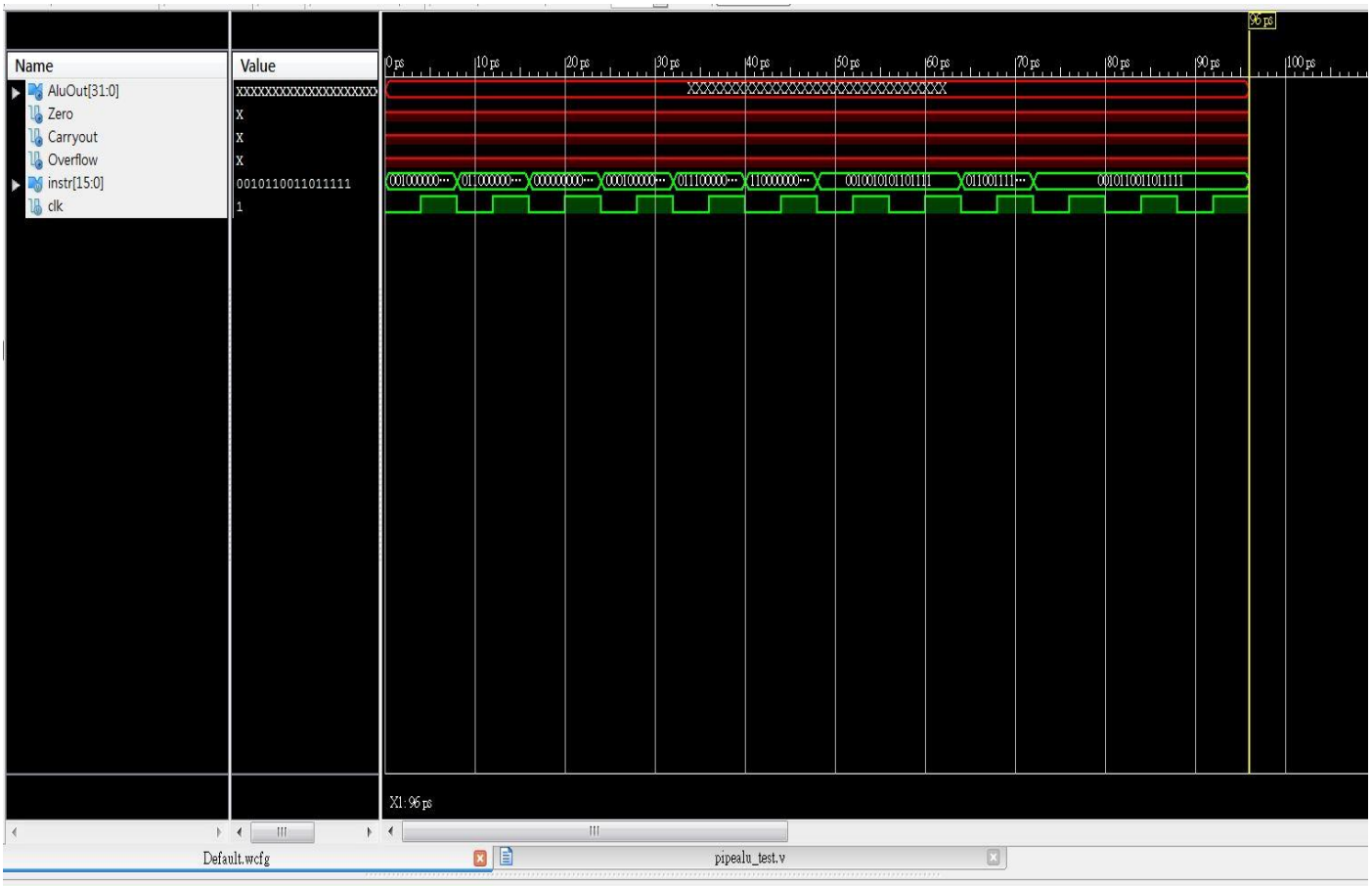
Device： XC3S400 Package：FG456

FPGA 合成 Area：(fpga_area.txt)

```
Device utilization summary:
---------------------------

Selected Device : 3s400fg456-5

 Number of Slices:                      119  out of   3584     3%
 Number of Slice Flip Flops:             65  out of   7168     0%
 Number of 4 input LUTs:                223  out of   7168     3%
 Number of IOs:                          52
 Number of bonded IOBs:                  48  out of    264    18%
 Number of GCLKs:                         1  out of      8    12%

---------------------------
Partition Resource Summary:
---------------------------

  No Partitions were found in this design.

---------------------------


================================================================================
TIMING REPORT
```

Timing(fpga_timing.txt)：

```
================================================================================
Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'
  Total number of paths / destination ports: 106 / 42
--------------------------------------------------------------------------------
Offset:              2.660ns (Levels of Logic = 2)
  Source:            instr<6> (PAD)
  Destination:       tempB_1 (FF)
  Destination Clock: clk rising

  Data Path: instr<6> to tempB_1
                                Gate     Net
    Cell:in->out      fanout   Delay   Delay  Logical Name (Net Name)
    ----------------------------------------  ------------
     IBUF:I->O             13   0.715   1.289  instr_6_IBUF (instr_6_IBUF)
     LUT4:I0->O             1   0.479   0.000  Mrom__COND_421 (Mrom__COND_42)
     FD:D                       0.176          tempB_2
    ----------------------------------------
    Total                       2.660ns (1.370ns logic, 1.289ns route)
                                        (51.5% logic, 48.5% route)

================================================================================
Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'
  Total number of paths / destination ports: 35 / 35
--------------------------------------------------------------------------------
```



將 FPGA 合成出來的 gatelevel 用 testbench 跑模擬時失敗，原因可能是記憶體初始化錯誤。