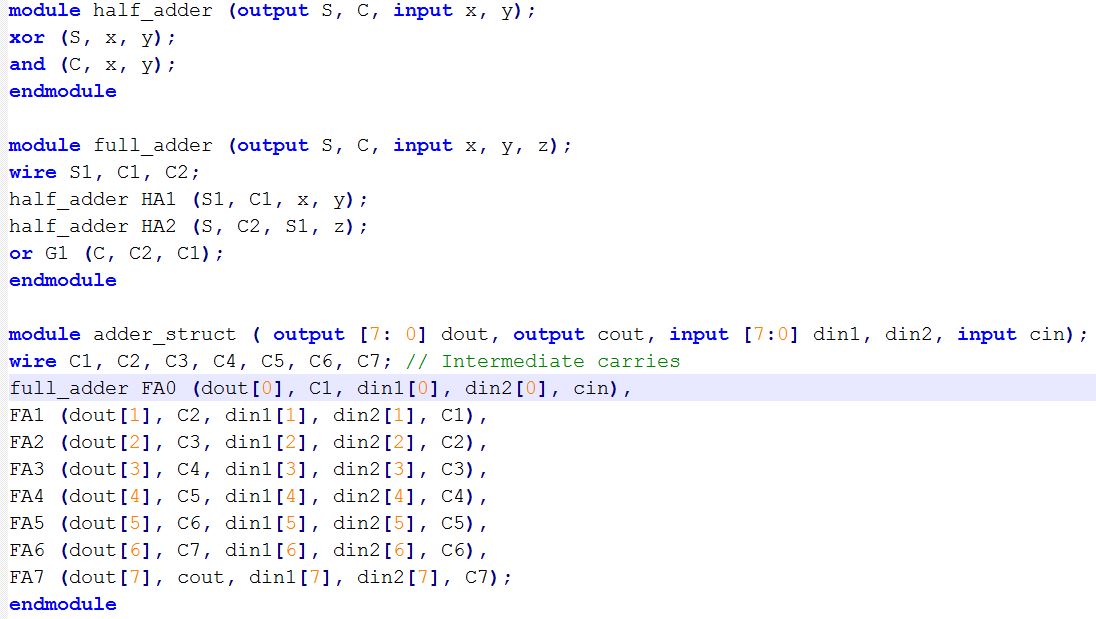
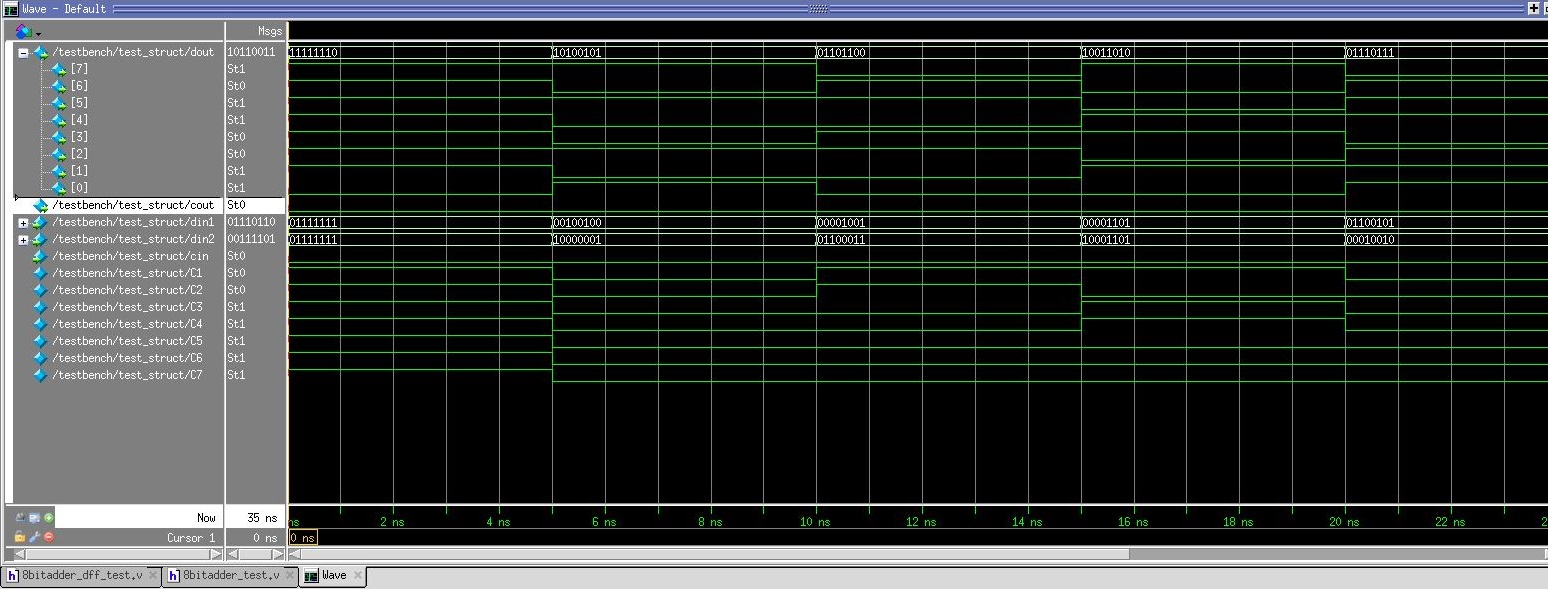
B023040050 顏義洋

Homework 1: 8-bit Adders Using Verilog in Structural, Dataflow, and Behavioral Levels

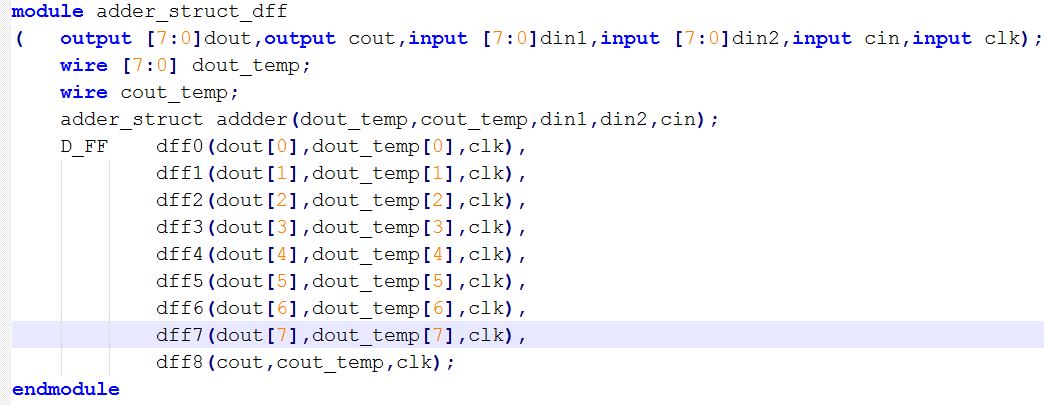
第一部分：Structure-Level Modeling



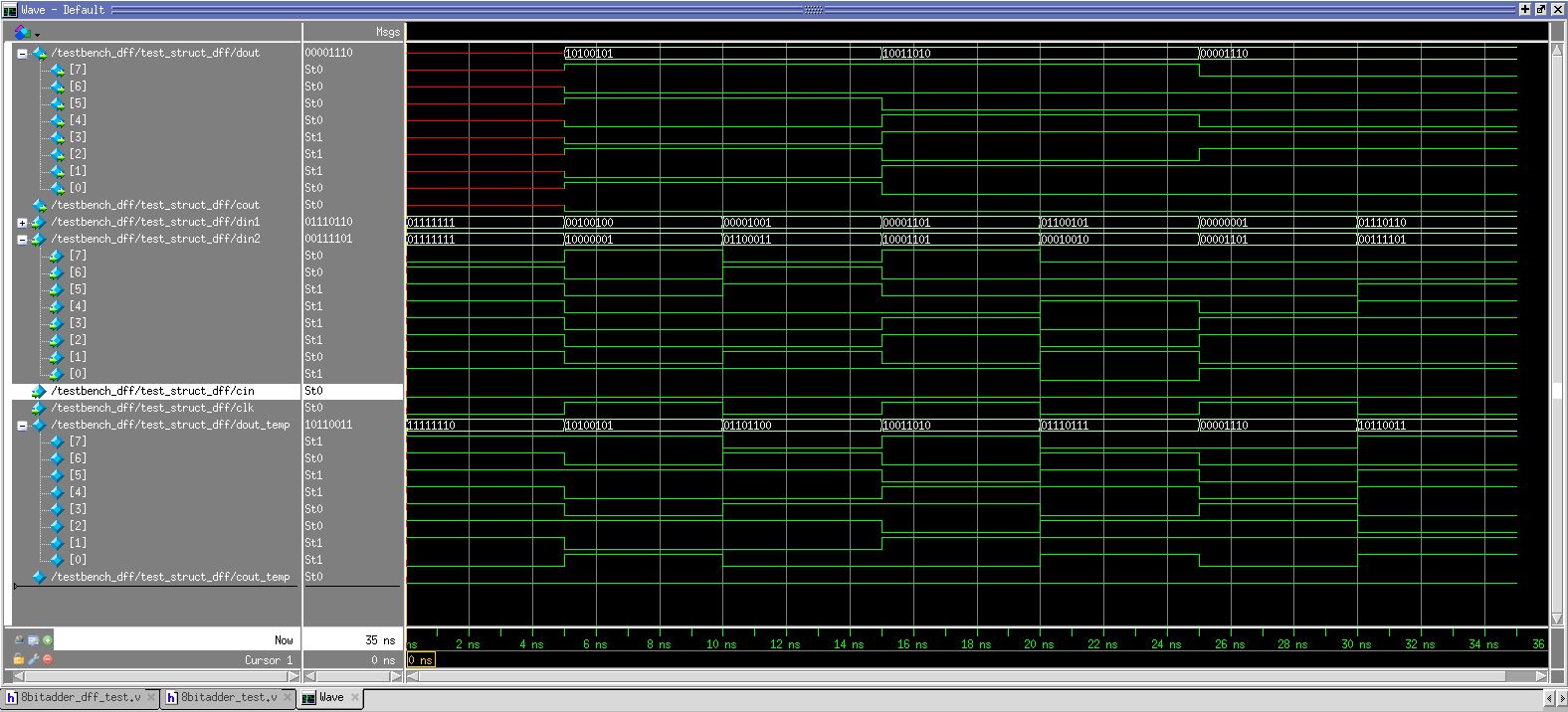
利用以前數位系統實驗課的寫的half adder跟full adder，用八個full adder拼成8-bit ripple carry adder。

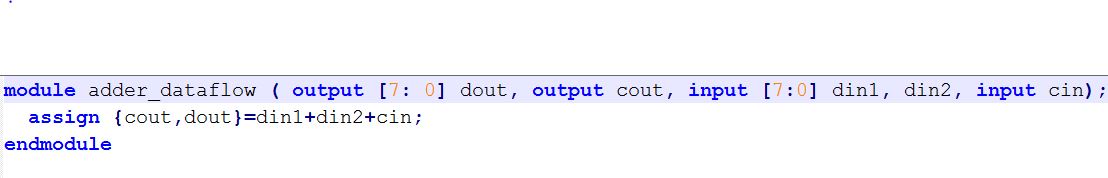


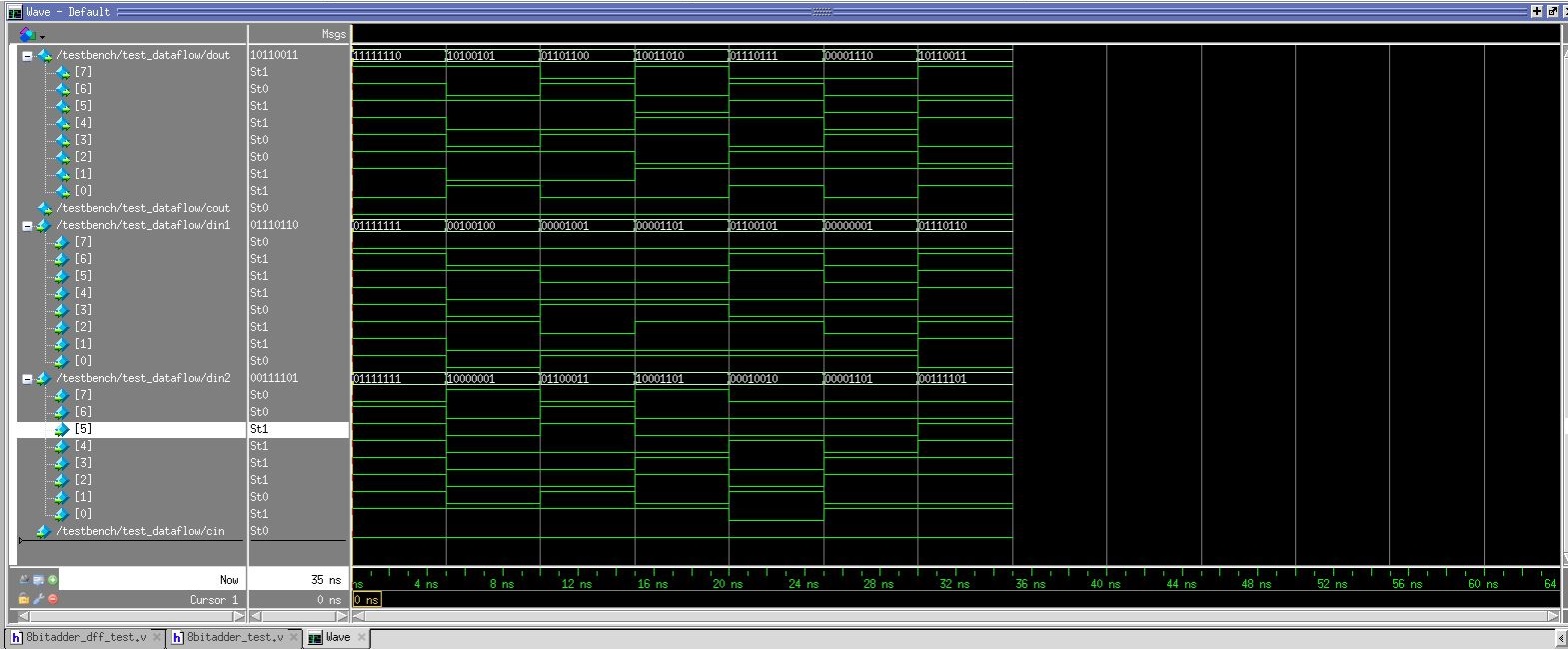
配上D-Flip-Flop：



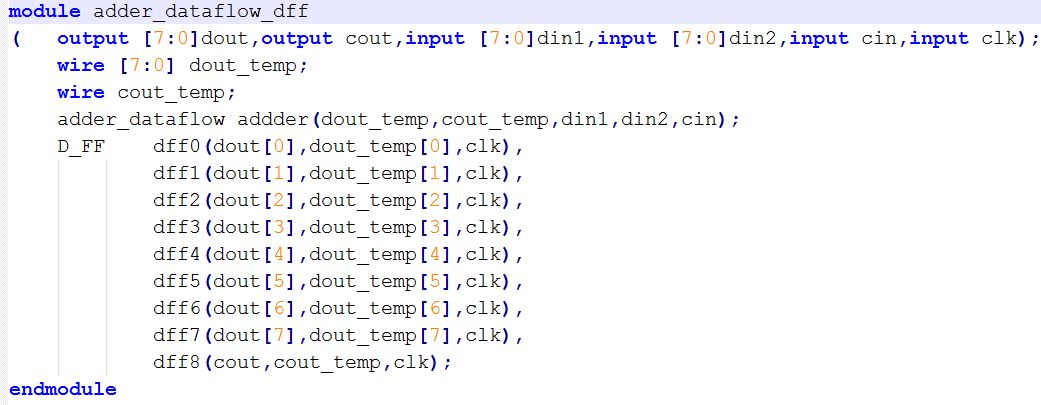
將相加的結果暫時存在DFF內，等clock正緣時讓ouput出現。

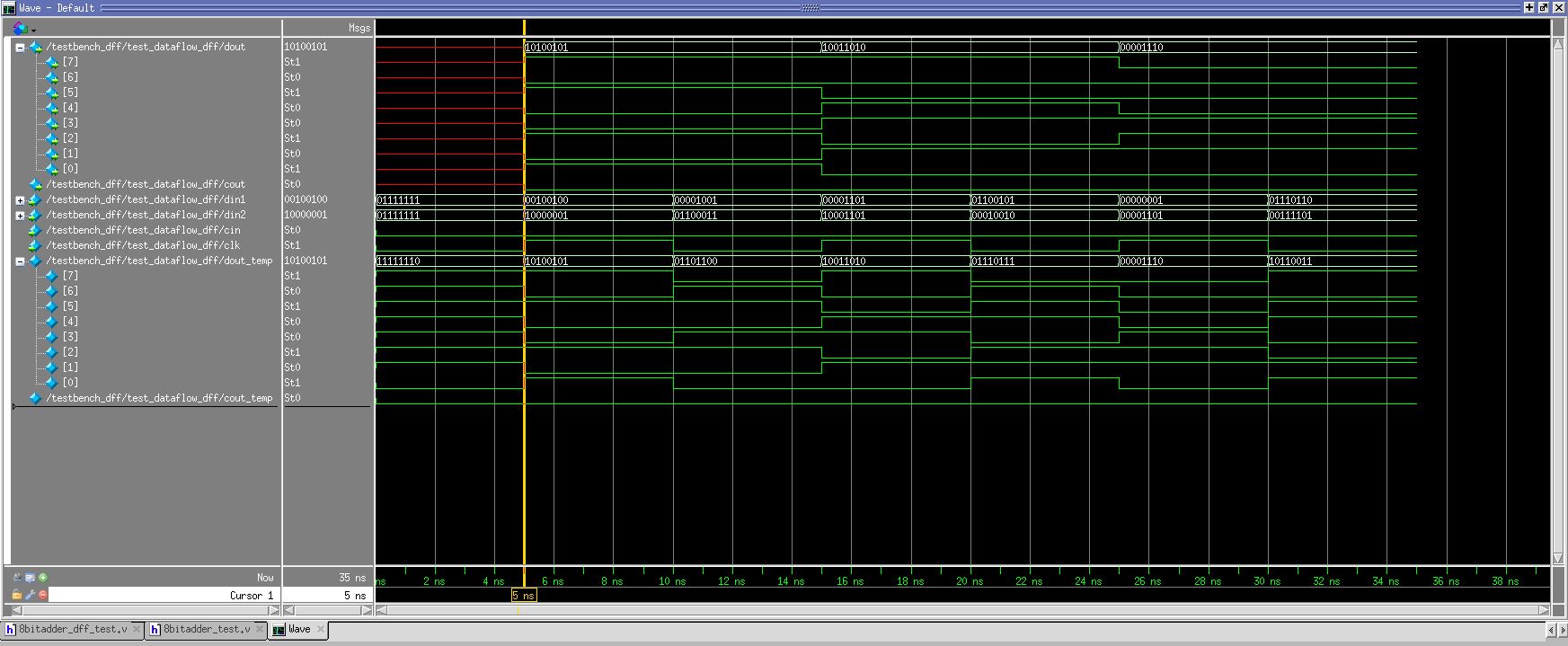


第二部分：Data Flow Modeling

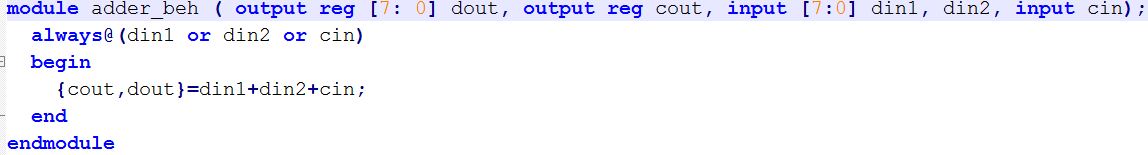


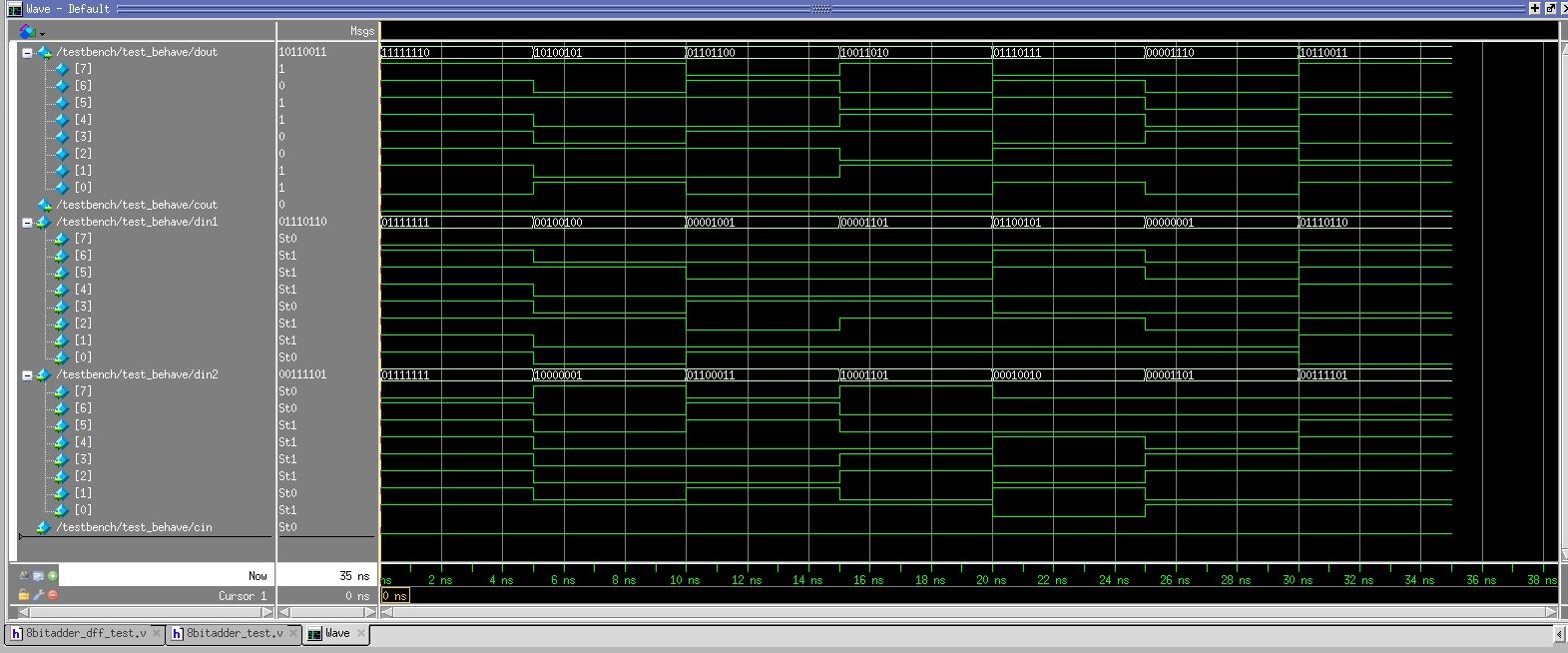
配上D-Flip-Flop：





第三分：Behavioral Modeling





配上D-Flip-Flop：

