Points Grade

# Team: -

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# Digital Integrated Circuits Lab (LDIS) 384.088, Summer Term 2019

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Task 1: Digital Thermometer

# 1 Problem statement

The goal was to design a digital thermometer with the Nexys 4 DDR FPGA Board. To use was one of the two temperature sensors on the board. One sensor is especially for measuring the temperature and to read out via i2c, while the other one is part of the accelerometer sensor and is to read out with SPI. The samling rate of the sensor should be defined pre-synthesis. The data then should go to an DSP part which was to be implemented as an moving average filter. The filter width should be able to be changed during runtime. The output of the DSP should be displayed on the 8 BCD segments on the board.



Figure 1: Block diagram of the system. Source: Original Task Description

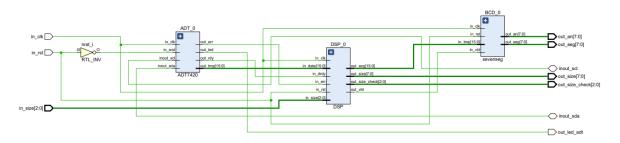


Figure 2: Schematic of the system. Source: Vivado

# 2 Implementation

In this section I explain how i implemented a possible solution to the proposed problem. I choose to use an active low reset for this task, which is the onboard switch with the name SW15.

# 2.1 Sampling

For the reading of the temperature i choose the onboard I2C-sensor. To get the values I used the IP-core from the Nexys 4 DDR Demo which includes an readout of this sensor. The sensor itself is an ADT7420 I2C temperature sensor. The output of the sampling part consists of the out\_data and the out\_vld ports. The out\_vld ports is high for the time of once clock cycle. It also has one LED, which toggles everytime valid data was retrieved.

# 2.1.1 Changes of the IP

The TWI Controller file was changed only in the way to use the ieee.numeric\_std.all; library. Other than that this file is original.

To the original readoutfiles were made some changes to get the wished functionality. To get 16 bit readouts I added another init vector:

```
constant NO_OF_INIT_VECTORS : natural := 4; -- number of init vectors in TempSensInitMap
                                := 1 + 8 + 8;
                                                 RD/WR bit
                      : integer
120
   constant ADDR_WIDTH : natural := natural(ceil(log(real(NO_OF_INIT_VECTORS), 2.0)));
121
   122
123
   signal TempSensInitMap: TempSensInitMap_type IRD & x"OB" & x"CB", -- Read ID R[0x0B]=0xCB
124
   IWR & x"2F" & x"00",
                                R[0x2F] = don't ca
126
         x"OB" & x"CB",
127
   IRD &
                          Read ID R[0x0B] = 0xCB
128
   TWR.
       & x"03" & x"80"
                          configure it for 16bit
129
```

To get the sampling timing right i added an extra state in which the I2C waits.

```
type state_type is (
105
             stIdle, -- Idle State
106
             stInitReg,
                          -- Send register address from the init vector
                          -- Send data byte from the init vector
107
             stInitData,
             stRetry, -- Retry state reached when there is a bus error, will retry RETRY_COUNT times stReadTempR, -- Send temperature register address
108
109
             stReadTempD1, -- Read temperature MSB
110
             stReadTempD2, -- Read temperature LSB
             stError,
112
                        -- Error state when reached when there is a bus error after a successful init; stays
                  here until reset
113
             stWait -- State to wait for the next sample
114
    signal state, nstate : state_type;
```

The new state was also added to the ReadyFlag process:

```
253
    -- Ready Flag
254
255
    ReadyFlag: process (in_clk)
256
    begin
             if Rising_Edge(in_clk) then
257
258
                      if (state = stIdle or state = stError) or state = stWait then
                      fReady <= false;
elsif (state = stReadTempD2 and twiDone = '1' and twiErr = '0') then
259
260
261
                               fReady <= true;
                      end if;
262
             end if:
263
    end process;
```

In the OUTPUT DECODE process another when statement got added.

```
349 when stWait => null;
```

In the NEXT\_STATE\_DECODE process the stReadTempD2 state got changed and another state got added:

```
when stReadTempD2 =>
             if (twiDone = '1') then
412
                      if (twiErr = '1') then
413
                               nstate <= stError;</pre>
414
                               nstate <= stWait;
415
416
                           nstate <= stReadTempR; -- old version
417
                      end if;
418
             end if;
419
420
    when stWait =>
             if waitSample = SAMPLECNT then
421
422
                     nstate <= stReadTempR;</pre>
             end if;
423
```

And a whole new process got added in which the counting happens for the sampling rate:

```
266
    -- Sample counter wait
267
    SAMPLEWAIT : process(in_clk)
268
269
    begin
              if rising_edge(in_clk) then
                       if state = stWait then
271
272
                                 \mbox{if $\mbox{waitSample}$ = $SAMPLECNT$ then } 
                                          out_led <= led_helper;
273
274
                                         led_helper <= not led_helper;</pre>
275
                                 else
276
                                         waitSample <= waitSample +1;
277
                                 end if;
278
279
                       else
280
                                waitSample <= 0;
                       end if;
281
              end if;
282
    end process;
```

#### 2.2 DSP

The moving average is implemented as a state machine. The size of the filter window is determined by the 3 switches SW2, SW1 and SW0. Each switch equals a number to the power of 2. SW0 = 1, SW1=2 and SW2=4. For example if SW2 is switched on and the others off then the size equals  $2^4 = 16$ . or if SW1 and SW2 are on then the size equals  $2^{2+1} = 8$ . It is done this way to make the divison for the mean value easier, since divison by a number which is a power of two equals a bitshift to the right.

The formula of the mean averge is dependent on the size which gets choosen by the switches.

$$y = \sum_{i=0}^{n} x[i] \tag{1}$$

Where i represents the last value in the buffer. This way the mean average is causal but the mean value is shifted if you print it against the original values.

I choose to implement it with a state machine. I also tried it with for loops but it took very long to synthesize. The synthesizing time shrunk from greater than 25 minutes down to less than 7 minutes.

When the size gets changed the buffer gets set to zero. It then gets slowly refilled and the temperature which gets sent to the BCD slowly increases, because it uses the fixed size for the division. It is done this way to show the working of the filter on the FPGA.

## 2.3 Output

The output part gets the averaged temperature. The hard part is to get from the binary value to a representation which fits on the BCD. One cannot just take the usual 4 bit approach for a segment because in the decimal system values only range from 0 to 9. So if the value would be an B in hex one needs to subtract from the current position and add to the next position. This problem is solved by using the double dabble algorithm (explanation on Wikipedia or Youtube).

Since the BCD share the an anode contact there is also the need to multiplex the data which gets to the corresponding outputs. This is done with the out\_an outputs. It is also important to notice that the active select anode is active low.

This is solved in two processes. The first process takes the data in if the valid flag is high. Contrary to DSP part it calculates the double dabble with for loops instead of a state machine. It then saves its solutions to variables. The second process takes these solutions, converts it to an integer format and uses these as indices for a predefined map of outputs. Furthermore the second process does this about 800 times per second to get a refresh rate of 100Hz per BCD. This is done with a simple counter signal.

# 3 Reports

### 3.1 Timing

After the first implementation

```
report timing | INFO: Timing | 38-91 | UpdateTimingParams: Speed grade: -3, Delay Type: max. | INFO: Timing | 38-191 | Multithreading enabled for timing update using a maximum of 4 CPUs | INFO: Timing | 38-35 | Done setting XDC timing constraints. | INFO: Timing | 38-78 | ReportTimingParams: -max | paths | 1 -nworst | 1 -delay_type | max -sort_by | slack | Copyright | 1986-2017 | Xilinx | Inc. | All | Rights | Reserved | Times | Times
                                                                                      Vivado v.2017.4 (lin64) Build 2086221 Fri Dec 15 20:54:30 MST 2017
Mon Apr 8 20:52:07 2019
ldis running 64-bit Debian GNU/Linux 9.3 (stretch)
                     Host
                     Design
Device
12
13
14
15
16
17
                                                                                                     Ot - csg324
PRODUCTION 1.20 2017-11-01
                     Speed File
             Timing Report
                                                                                                                           3.570 ns (required time - arrival time)

BCD_0/out_an_reg[1]/C (rising edge-triggered cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.0000 period=20.000ns})

out_an[1] (output port clocked by sys_clk_pin {rise@0.000ns fall@10.000ns period=20.000ns})

sys_clk_pin
            Slack (MET) :
                                                                                                                                                                                                                                       cell FDRE clocked by sys_clk_pin {rise@0.000ns fall@10.000ns
                     Destination :
\frac{22}{23}
                   (output po-
sys_clk_pin
Max at Slow Process Corner
20.000ns (sys_clk_pin rise@20.000ns -
7.160ns (logic 3.481ns (48.618%) rou
\frac{24}{25}
                                                                                                                             Max at Slow Pr
20.000ns (sys
7.160ns (logi
1 (OBUF=1)
5.000ns
-4.235ns (DCD
                                                                                                                                                                                                                                                                                   ns - sys_clk_pin rise@0.000ns)
route 3.679ns (51.382%))
26
27
28
29
30
                                                                                                                                                                                {
m CD - SCD + CPR} \\ {
m 0.000ns} = (20) \\ {
m 4.235ns}
                                                                                                                                                                                                                                 20.000 - 20.000 )
\begin{array}{c} 31\\ 32\\ 33\\ 34\\ 35\\ 36\\ 37\\ 38\\ 40\\ 41\\ 42\\ 43\\ 44\\ 45\\ 46\\ 47\\ 48\\ 49\\ 50\\ 51\\ 52\\ \end{array}
                    Source Clock Delay
Clock Pessimism Removal
Clock Uncertainty: 0.
Total System Jitter
Total Input Jitter
Discrete Jitter
                                                                                                                                                                                      .2000 ns
.0000 ns
J^2 + TIJ^2)^1/2 + DJ) / 2 + PE
                              Discrete Ji
Phase Error
                                                                                                                                          (PE)
                                                                                                                                                                                 0.000ns
                                                                                                                                                                                                                                                                                   Path (ns)
                             Location
                                                                                                                         Delay type
                                                                                                                                                                                                                                                                                                                                         Netlist Resource(s)
                                                                                                                         (\ \mathtt{clock} \ \ \mathtt{sys} \_ \mathtt{clk} \_ \mathtt{pin} \ \ \mathtt{rise} \ \ \mathtt{edge})
                             E_3
                                                                                                                                                                                                                                                                                                 \begin{smallmatrix} 0 & . & 0 & 0 & 0 \\ 0 & . & 0 & 0 & 0 \end{smallmatrix}
                                                                                                                                                                                                                                                                                                                                         in clk (IN)
                                                                                                                                                                                                                                                       0.000
                                                                                                                                                                                                                                                                                                                                     in_clk (IIV)
in_clk_IBUF_inst/O
in_clk_IBUF BUFG inst/O
BCD_0/in_clk_IBUF BUFG
BCD_0/out_an_reg[1]/C
                                                                                                                       net (fo=0)
IBUF (Prop_ibuf_I_O)
net (fo=1, routed)
                             E_3
                                                                                                                                                                                                                                                       1.330
                                                                                                                                                                                                                                                                                                  1.330
                                                                                                                                                                                                                                                       1.525
                                                                                                                                                                                                                                                                                                  2.855
                                                                                                                                           (Prop_bufg_I_O)
(fo=2366, routed)
                             BUFGCTRL_X0Y16
                                                                                                                        BUFG
                                                                                                                                                                                                                                                       0.076
                                                                                                                                                                                                                                                                                                  2.931
4.235
                             {\tt SLICE\_X1Y74}
                                                                                                                        FDRE
                             SLICE X1Y74
                                                                                                                        FDRE (Prop fdre C Q)
                                                                                                                                                                                                                                                       0.341
                                                                                                                                                                                                                                                                                                 4.576
                                                                                                                                                                                                                                                                                                                                      BCD 0/out an reg[1]/Q
```

```
\begin{array}{ccc} n \; et & (\; f \, o \, = \, 1 \,, & rou \, t \, ed \;) \\ OBUF & (\; Prop\_obuf\_I\_O \;) \\ n \; et & (\; f \, o \, = \, 0 \,) \end{array}
                                                                                                                                                                                                                       out_an_OBUF [1]
out_an_OBUF [1] _inst/O
out_an [1]
out_an [1] (OUT)
53
54
55
56
57
58
59
60
61
62
63
64
65
66
67
68
                    К2
                                                                                                                                                                                            11.394 r
11.394
                                                                                                                                                                   3.140
                                                                                                                                                                  0.000
                    К2
                                                                                (clock sys_clk_pin rise edge)
                                                                                                                                                                                            20.000 r
20.000
19.965
                                                                                clock pessimism
clock uncertainty
output delay
                                                                                                                                                                  0.000
-0.035
                                                                                                                                                                -5.000
                                                                                                                                                                                            14.965
                                                                                required time
arrival time
                                                                                                                                                                                           14.965
-11.394
                                                                                 slack
                                                                                                                                                                                               3.570
```

### 3.2 Utilization

#### 3.2.1 Summary

I have the whole report further down. Here is the condensed information in a picture.

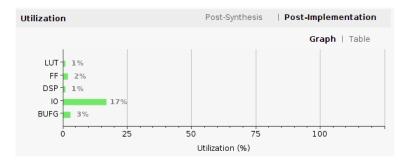


Figure 3: Utilization graph

tilization		Post-Synthesis   P	ost-Implementation
			Graph   Table
Resource	Utilization	Available	Utilization %
LUT	902	63400	1.42
FF	2366	126800	1.87
DSP	1	240	0.42
10	35	210	16.67
BUFG	1	32	3.13

Figure 4: Utilization table

I use more ports than needed because i output extra information with the LEDs and also use the whole BCD. The IO could be reduced this way, because who needs 4 digits after the comma. Something thats very interesting is the fact that my design uses an DSP. This is contrary to the other design i saw to compare. The DSP is the DSP48E1 and it is used in the BCD part of my design. It is needed in the part where the number gets calculated for the fractional part of the output temperature.

## 3.2.2 Whole Report

# Slice Logic

1. Slice						
ļ	Site <b>Type</b>	Used	Fixed	A v	ailable	Ut:
Slice L		902	0	1	63400	
	s Logic s Memory	902	0	}	63400 19000	
Slice R	legisters	2366	0	į	126800	1.
	ter as Flip Fl ter as Latch	op   2366   0	0	ł	126800 126800	
F7 Muxe	S	259	0	ļ	31700	0.
F8 Muxe	· S	128		-	15850	- <del>/</del> 0.
1.1 Summa	ry of Register	s by Type				
+		<del> </del>				+
Total	Clock Enable	Synchro	nous   As	ynch	ronous	+
0	_		_		Set	
0	_	İ	- Set		Reset	İ
0	_	R	eset		_	
0	Yes Yes	-	_		Set	
0	Yes	ì	_		Reset	
					iteset	
27 2339	Yes Yes	R	Set   eset			 +
2339	Yes	1				+
2339	Yes Logic Distribu	tion				Fired
2339   - / 2. Slice	Yes	tion		— <i> </i> -	Used	
2. Slice	Yes Logic Distribu Site	tion				0
2. Slice  Slice SLICE SLICE	Yes  Logic Distribu  Site  L	tion			Used   644   440   204	0
2. Slice  Slice SLICE SLICE LUT as	Yes  Logic Distribu  Site  L  M  Logic	tion			Used / 644   440	0
2. Slice  2. Slice  Slice  SLICE  SLICE  LUT as  using  using	Yes  Logic Distribu  Site  L  M  Logic  O5 output onl  O6 output onl	tion			Used	0
2. Slice  Slice SLICE SLICE LUT as using using using LUT as	Yes  Logic Distribu  Site  L M Logic O5 output onl O6 output onl O5 and O6 Memory	tion Type			Used	( ( ( (
2. Slice  Slice SLICE SLICE LUT as using using using LUT as LUT as	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6  Memory S Distributed	tion Type y y			Used / / 644   440   204   902   0   830   72   0   0   0	( ( ( ( (
2. Slice  Slice SLICE: SLICE: LUT as using using LUT as LUT a LUT a	Yes  Logic Distribu  Site  L  M  Logic  O5 output onl  O6 output onl  O5 and O6  Memory  s Distributed is  s Shift Regist p Flop Pairs	tion Type  y y RAM er			Used	( ( ( ( ( ( ( (
2. Slice  Slice SLICE SLICE SLICE LUT as using using LUT as LUT a LUT a	Yes  Logic Distribu  Site  M Logic 05 output onl 06 output onl 075 and 06  Memory 5 Distributed 5 5 Shift Regist	tion Type  y y x RAM er	eset		Used / 440   440   204   902   0   830   72   0   0   0   0   0	0 0
2. Slice  SLICE SLICE SLICE SLICE LUT as using using using LUT as LUT a LUT a LUT a	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6 Memory s Distributed: s Shift Regist p Flop Pairs used LUT-FF p pairs with o F pairs with o	tion Type  y y x RAM er	LUT outp		Used	0 0 0 0 0
2. Slice  SLICE SLICE SLICE SLICE SLICE LUT as using using LUT a LUT a LUT a LUT a LUT a LUT a LUT a LUT a LUT a	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6  Memory S Distributed S Shift Regist p Flop Pairs used LUT-FF p F pairs with o F pairs with o Control Sets	tion  Type  y y  RAM er  airs ne unused ne unused	LUT outp	P	Used 4440 204 902 0 830 0 0 0 198 24 159 25	0 0 0 0
2. Slice  SLICE SLICE SLICE SLICE SLICE LUT as using using LUT a LUT a LUT a LUT a LUT a LUT a LUT a LUT a	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6 Memory s Distributed: s Shift Regist p Flop Pairs used LUT-FF p pairs with o F pairs with o	tion  Type  y y  RAM er  airs ne unused ne unused	LUT outp	P	Used 4440 204 902 0 830 0 0 0 198 24 159 25	C C C C C C C C C C C C C C C C C C C
2. Slice  SLICE SLICE SLICE SLICE SLICE LUT as using using LUT a LUT a LUT a LUT a LUT a LUT a LUT a LUT a	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6  Memory S Distributed S Shift Regist p Flop Pairs used LUT-FF p F pairs with o F pairs with o Control Sets	tion  Type  y y  RAM er  airs ne unused ne unused	LUT outp	P	Used 4440 204 902 0 830 0 0 0 198 24 159 25	C C C C C C C C C C C C C C C C C C C
2. Slice  SLICE SLICE SLICE LUT as using using using LUT as LUT a LUT a LUT bli fully LUT-F LUT-F LUT-F Unique	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6  Memory S Distributed S Shift Regist p Flop Pairs used LUT-FF p F pairs with o F pairs with o Control Sets	tion  Type  y y  RAM er  airs ne unused ne unused	LUT outp	P	Used 4440 204 902 0 830 0 0 0 198 24 159 25	C C C C C C C C C C C C C C C C C C C
2. Slice  SLICE: SLICE: SLICE: SLICE: LUT as using using using LUT as LUT a LUT a LUT a LUT a LUT a LUT a SLICE: S	Yes  Logic Distribu  Site  Logic O5 output onl O6 output onl O5 and O6  Memory S Distributed S Shift Regist p Flop Pairs used LUT-FF p F pairs with o F pairs with o Control Sets	tion Type  y y RAM er airs ne unused ne unused	LUT outp	p   r mo	Used 4440 204 902 0 830 0 0 0 198 24 159 25	0 0 0 0
2. Slice  SLICE SLICE SLICE SLICE LUT as using using using LUT as LUT a LUT a LUT Bli fully LUT-F Unique  * Note: R	Logic Distribu  Site  L M Logic O5 output onl O6 output onl O5 and O6 Memory s Distributed: s Shift Regist p Flop Pairs used LUT-FF p pairs with o Control Sets eview the Cont	tion  Type  y y  RAM er airs ne unused ne unused trol Sets	LUT outp Flip Flo Report fo	p   r mo	Used 4440 204 902 0 830 72 0 0 198 24 159 25 re info	Fixed 00 00 00 00 00 00 00 00 00 00 00 00 00

Total	Clock Enable	Synchronous	Asynchronous
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0	Yes Yes Yes Yes Yes	Set Reset - - Set Reset	Set Reset - Set Reset

#### 2. Slice Logic Distribution

Site <b>Type</b>	Used	Fixed	Available	Util%
Slice	644	I 0	15850	4.06
SLICEL	440	0		İ
SLICEM	204	0		İ
LUT as Logic	902	0	63400	1.42
using O5 output only	0	ĺ		İ
using O6 output only	830	j		İ
using O5 and O6	72	j		İ
LUT as Memory	0	0	19000	0.00
LUT as Distributed RAM	0	0		İ
LUT as Shift Register	0	0		İ
LUT Flip Flop Pairs	198	0	63400	0.31
fully used LUT-FF pairs	24	ĺ		İ
LUT-FF pairs with one unused LUT output	159	ĺ		İ
LUT-FF pairs with one unused Flip Flop	159	ĺ		İ
Unique Control Sets	2.5	ĺ	İ	İ

\* Note: Review the Control Sets Report for more information regarding control sets.

#### 3. Memory

Site Type	Used	Fixed	A vailable	Util%
Block RAM Tile	0	0	135	0.00
RAMB36/FIFO *	0	0	135	0.00
RAMB18	0	0	270	0.00

\* Note: Each Block RAM Tile only has one FIFO logic available and therefore can accommodate only one FIFO36E1 or one FIFO18E1. However, if a FIFO18E1 occupies a Block RAM Tile, that tile can still accommodate a RAMB18E1

Site Type	Used	Fixed	A vailable	Util%
DSPs DSP48E1 only	1 1	0	240	0.42

#### 5. IO and GT Specific

Site Type	Used	Fixed	Available	Util%
Bonded IOB	35	35	210	16.67
IOB Master Pads	16			İ
IOB Slave Pads	17			i
Bonded IPADs	0	0	2	0.00
PHY CONTROL	0	0	6	0.00
PHASER REF	0	0	6	0.00
OUT FIFO	0	0	24	0.00
IN FIFO	0	0	24	0.00
IDELAYCTRL	0	0	6	0.00
IBUFDS	0	0	202	0.00
PHASER OUT/PHASER OUT PHY	0	0	24	0.00
PHASER IN/PHASER IN PHY	0	0	24	0.00
IDELAYE2/IDELAYE2 FINEDELAY	0	0	300	0.00
ILOGIC	0	0	210	0.00
OLOGIC	0	0	210	0.00

#### 6. Clocking

Site Type	Used	Fixed	Ava	ilable
DSPs DSP48E1 only	1 1	0	<u> </u>	240
5. IO <b>and</b> GT Spec	ific	,		
Site T	ype		Used	Fixed
Bonded IOB			35	35
IOB Master Pac		j	16	ļ
IOB Slave Pads	3	ļ	17	
Bonded IPADs PHY CONTROL		ļ	0	0   0
PHASER REF		ł	0	i
OUT FIFO		ł	ō	ő
IN FIFO		i	0	0
IDELAYCTRL		ĺ	0	0
		ļ	_	0
			_	0
			_	0   0
	INEL	ALLEN I	_	0
OLOGIC		ł	0	ŏ
IDĒLAYCTRL IBUFDS PHASER_OUT/PHASE PHASER_IN/PHASER IDELAYĒ2/IDELAYF ILOGIC	IN PH	7	0 0 0 0 0	

LEZ   ADV   0   0   6   0.00	Market   M	Lie	MMCME2 AD	ov	0   0	0	24 6	0.00				
Fire	Specific Feature	Specific Feature   Site Type	PLLE2 ADV		0	0		0.00				
Specific Feature	Specific Feature	Specific Feature   Specific Feature	BUFMRCE	ĺ								
Specific Feature	Site Type	Site Type										
Site Type	Site Type	Site Type	BUFR	_/	/		24					
Site Type	Site Type	Site Type										
SCANE2   0   0   4   0.00   APTUREE2   0   0   1   0.00   NA PORT   0   0   1   0.00   NA PORT   0   0   1   0.00   NA PORT   0   0   1   0.00   NAME ECCE2   0   0   1   0.00   APEZ   0   0   2   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   0	SSCANE2	SCANE2	Specific	Featu	re							
SCANE2   0   0   4   0.00   APTUREE2   0   0   1   0.00   NA PORT   0   0   1   0.00   NA PORT   0   0   1   0.00   NA PORT   0   0   1   0.00   NAME ECCE2   0   0   1   0.00   APEZ   0   0   2   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   0   1   0.00   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   0   NAPEZ   0   0   0   0   0   0   0   0   0	SSCANE2	SCANE2										
APTUREE2	APTURE2	APTUREE2	Site <b>Typ</b>	oe   U	sed	Fixed	Available	Util%				
NA PORT   0   0   1   0.00	NA PORT   0   0   1   0.00   FUSE USR   0   0   1   0.00   RAME ECCE2   0   0   1   0.00   CAPET   0   0   1   0.00   CAPET   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   0   1   0.00   TARTUPE2   0   0   0   1   0.00   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   0   0   TARTUPE2   0   0   0   0   TARTUPE2   0   0   0   0   0   TARTUPE2   0   0   0   0   0   TART	NA PORT	BSCANE2	1	0	0	4	0.00				
Name   Used   Functional Category	Public   Section   Secti	FUSE USR	CAPTUREE2									
AAME ECCE   0   0   1   0.00   AAPE2   0   0   0   2   0.00   CIE 2 1   0   0   1   0.00   CARTUPE2   0   0   1   0.00   CARTUPE2   0   0   1   0.00   COLUMN   0   0   1   0.00   COLUMN   0   0   1   0.00   COLUMN   0   0   1   0.00   COLUMN   0   0   0   1   0.00   COLUMN   0   0   0   1   0.00   COLUMN   0   0   0   0   0   COLUMN   0   0   0   0   0   COLUMN   0   0   0   0   COLUMN   0   0   0   0   0   COLUMN   0   0   0   0   COLUMN   0   0   0   0   COLUMN   0   0   0   0   COLUMN   0   0   0   COLUMN   0   0   0   COLUMN   0   0   0   COLUMN   0   0   0   COLUMN   0   COLUMN   0   COL	RAMÉ ECCE   0   0   1   0.00   CAPEZ   0   0   0   2   0.00   CAPEZ   0   0   0   1   0.00   TARTUPE2   0   0   1   0.00   AACC   0   0   1   0.00    Primitives  Primitives    DRE	RAME   ECCE2	DNA_PORT	j								
APE2	CAPEZ   0   0   2   0.00   TARTUPEZ   0   0   1   0.000   TARTUPEZ   0   0   1   0.000   TARTUPEZ   0   0   1   0.000   TARTUPEZ   0   0   0   1   0.000   TARTUPEZ   0   0   0   1   0.000   TARTUPEZ   0   0   0   1   0.000   TARTUPEZ   0   0   0   1   0.000   TARTUPEZ   TART	CAPE2	EFUSE_USR	.								
DIE   2	Primitives	Name		CE2								
Primitives    Primitives	Primitives	TARTUPE2		ļ								
Primitives    Primitives	Primitives    Ref Name   Used   Functional Category	Primitives   Ref Name										
Primitives    Section 2	Primitives	Primitives										
ef Name	Used	DRE	ADC	ļ	0	U	1	0.00				
ef Name	Used	DRE		7	7		,	7				
ef Name	DRE	DRE										
DRE 2339 Flop & Latch  TT6 700 LUT  UXF7 259 MuxFx  UXF8 128 MuxFx  UT2 68 LUT  TT5 56 LUT  TT3 52 LUT  TT4 50 LUT  JT1 48 LUT  JT1 48 LUT  HRRY4 44 CarryLogic  BUF 28 IO  SDE 27 Flop & Latch  UUF 7 IO  SDE 27 Flop & Latch  SDF 2 SP48E1 1 Block Arithmetic	DRE 2339 Flop & Latch UT6 700 LUT UXF7 259 MuxFx UXF8 128 MuxFx UT2 68 LUT UT5 56 LUT UT3 52 LUT UT4 50 LUT UT4 4 50 LUT UT4 4 50 LUT UT4 4 50 LUT UT9 48 LUT9 UT9 48 LUT9	DRE   2339	Primitiv	es								
DRE 2339 Flop & Latch  TT6 700 LUT  UXF7 259 MuxFx  UXF8 128 MuxFx  UT2 68 LUT  TT5 56 LUT  TT3 52 LUT  TT4 50 LUT  JT1 48 LUT  JT1 48 LUT  HRRY4 44 CarryLogic  BUF 28 IO  SDE 27 Flop & Latch  UUF 7 IO  SDE 27 Flop & Latch  SDF 2 SP48E1 1 Block Arithmetic	DRE	DRE										
DRE 2339 Flop & Latch  TT6 700 LUT  UXF7 259 MuxFx  UXF8 128 MuxFx  UT2 68 LUT  TT5 56 LUT  TT3 52 LUT  TT4 50 LUT  JT1 48 LUT  JT1 48 LUT  HRRY4 44 CarryLogic  BUF 28 IO  SDE 27 Flop & Latch  UUF 7 IO  SDE 27 Flop & Latch  SDF 2 SP48E1 1 Block Arithmetic	DRE   2339	DRE   2339		1								
Triangle   Triangle	UT6 700 LUT	UT6	Ref Name	Used	Fu	nctiona	l Category	_				
Triangle   Triangle	UT6	MuxFr	FDRE	2339	í	Flo	op & Latch					
UXPS 128 MuXFX   127	IUXF8         128         MuxFx           UUT2         68         LUT           UUT5         56         LUT           UUT3         52         LUT           UUT4         50         LUT           UUT1         48         LUT           VARRY4         44         CarryLogic           BUF         28         IO           DSE         27         Flop & Latch           BUF         7         IO           BUFT         2         IO           SP48E1         1         Block Arithmetic	MuxFx	LUT6		İ							
JT	UT2 68 LUT	UT2	MUXF7	259	İ		MuxFx					
TT	UT5	UT5	MUXF8	128	i		MuxFx					
T13	UT3	UT3	LUT2		ĺ							
TT4	UT	LUT 4 50 LUT 148 LUT 148 LUT 150 160 160 160 160 160 160 160 160 160 16	LUT5									
T1	LUT	ARRY4	LUT3									
ARRY4     44     CarryLogic       SUF     28     IO       SSE     27     Flop & Latch       IUF     7     IO       SUFT     2     IO       SSP48E1     1     Block Arithmetic	ARRY4	ARRY4 44   CarryLogic BUF 28   10   DDSE 27   Flop & Latch BUF 7   10   DSP48E1 1   Block Arithmetic BUF 1   Clock    Black Boxes	LUT4									
BUF 28 IO     SEE   27   Flop & Latch     UF   7   Flop & Lotch     UF   7   IO     SUFT   2   IO     SP48E1   1   Block Arithmetic	BUF	DBUF 28 IO DDSE 27 Flop & Latch BUF 7 IO BUFT 2 IO SDSP48E1 1 Block Arithmetic BUFG 1 Clock  Black Boxes  Ref Name Used    Instantiated Netlists			ļ							
OSE 27 Flop & Latch   UF 7 IO   SUFT 2 IO   SP48E1 1   Block Arithmetic	DSE 27 Flop & Latch BUF 7 IO BUFT 2 IO SP48E1 1 Block Arithmetic	DSE 27   Flop & Latch BUF 7   10   BUFT 2   10   SP48E1 1   Block Arithmetic   UFG 1   Clock    Black Boxes  Instantiated Netlists			ļ							
IUF 7 IO   SUFT 2 IO   SP48E1 1 <b>Block</b> Arithmetic	BUF 7 IO DBUFT 2 IO DSP48E1 1 Block Arithmetic	BUF 7 10 BUFT 2 10 DSP48E1 1 Block Arithmetic UFG 1 Clock  Black Boxes  Ref Name Used    Instantiated Netlists										
3UFT 2 IO SP48E1 1 <b>Block</b> Arithmetic	DBUFT 2 IO DSP48E1 1 <b>Block</b> Arithmetic	BUFT 2   Block Arithmetic   DOSP48E1 1   Block Arithmetic   Clock    Black Boxes   Tef Name   Used   Tef Name   Used   Tef Name   Te				F 1 c						
SP48E1 1 Block Arithmetic	OSP48E1 1 Block Arithmetic	Black Boxes  Black Boxes  Ref Name   Used										
		Black Boxes  Ref Name Used   The stantiated Netlists			1	D10-1-						
TG   T   Glock	1   Clock	Black Boxes  Ref Name   Used    Instantiated Netlists			1	ьюск						
		Instantiated Netlists					Clock	_				
		Instantiated Netlists	Black Bo	xes								
Black Boxes	Black Boxes	Instantiated Netlists										
Black Boxes	Black Boxes	Instantiated Netlists		/	-+							
				Used	-L							
			lef Name	/	-+							
	<del></del>		tef Name									
			Ref Name									
ef Name Used	Ref Name   Used   +	Ref Name Used   + + + + + + + + + + + + + + + + + +		iated	Netlis	t s						
ef Name Used   + + + + + + + + + + + + + + + + + +	Ref Name   Used   +	Ref Name Used		iated	Netlis	ts						
ef Name Used t	Ref Name   Used   +	<del></del>		iated	Netlis	t s						
ef Name   Used	Ref Name Used    Instantiated Netlists			1	-+	ts						
ef Name   Used	Ref Name Used    Instantiated Netlists			1	-+	ts						