EE517: ANALOG VLSI LAB
COURSE PROJECT

Design and analysis of a 2-stage op-amp with high gain bandwidth product

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EEE - VLSI & Nanoelectronics

Contents

1 Objective:

Design a 2-stage Op-amp in 180 nm technology targeting the folowing application.

1. High Gain Band Width (GBW)

1.1 Problem 2: High Gain Band Width (GBW)

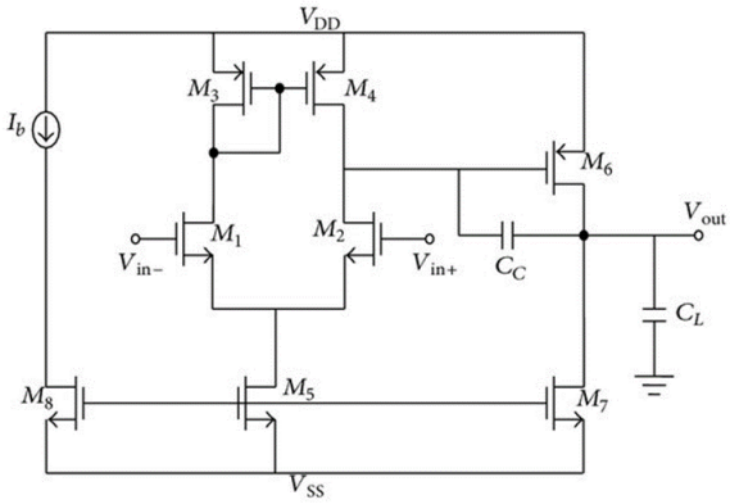
1. $Gain \geq 40dB$
2. $GBW \geq 70MHz$
3. $P_{diss} \leq 1mW$
4. $L_{max} \leq 2\mu m$

1.2 General Specifications:

- **A Reference current source = 20µA.**
- **Supply voltage = 1.8V.**
- **Slew Rate $\geq$ 1 V/µs**
- **ICMR = 0.6-1.4 V**
- **Load Capacitance C_L = 10 pF**
- **Phase Margin $\geq$ 60 degrees**

1.3 Analysis:

1. DC Analysis
   (a) Report the schematic of the diff pair with DC OP point annotated: $I_d, V_{gs}, V_{ds}, V_{th}, V_{dsat}, g_m, g_{ds}, g_{mb}$, region.
   (b) Check that all transistors operate in saturation.
2. AC Analysis
   (a) Observe pole-zero analysis of your circuit
   (b) Frequency response of your circuit
   (c) Find A_v, PM, Bandwidth, CMRR, PSRR
   (d) Give a proper reason for selecting any value of any parameter
3. Transient Analysis
   (a) slew rate
   (b) ICMR, OCMR



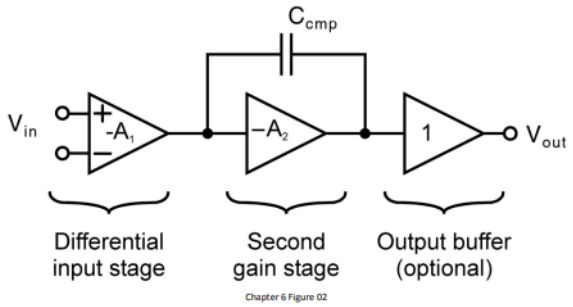
1.4 Circuit Diagram:

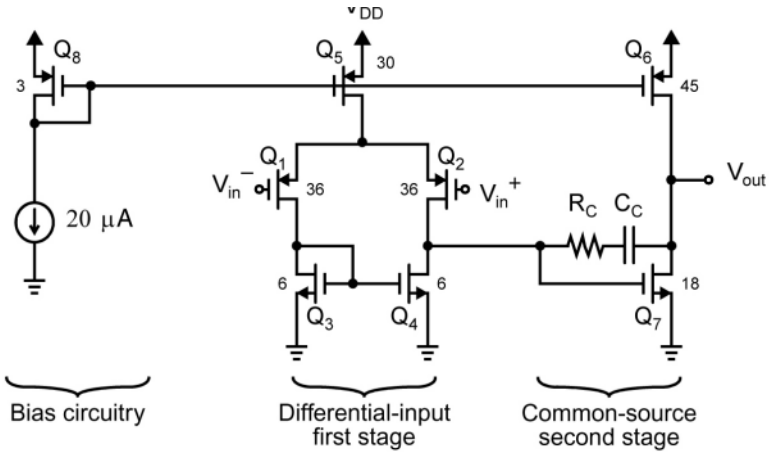
2 Theory

The two-stage circuit architecture has historically been the most popular approach to OpAmp design.
It can provide high gain and high output swing.
It is an excellent example to illustrate many important design concepts that area also directly applicable to other designs.
Typical applications of OpAmps in analog integrated circuits:

1. Amplification and filtering
2. Biasing and reguation
3. Switched-capacitor circuits

The two-stage refers to the number of gain stages in the OpAmp. The output buffer is normally present only when resistive loads needs to be driver. If the load is purely capacitive, it is not needed.
The load is assumed capacitive.
The first stage is a pMOS differential pair with nMOS current mirrors. Second stage is a common-source amplifier.
Shown in the diagram are reasonable widths in 0.18um technology (length all made 0.3um). Reasonable sizes for the lengths are usually 1.5 to 10 times of the minimum length (while digital circuits usually use the minimum).





2.1 OpAmp gain

For low-frequency applications, the gain is one of the most critical parameters. Note that compensation capacitor Cc can be treated open at low frequency. gain of 1st stage

$$A_{V1} = -g_{m1}(r_{ds2}||r_{ds4}) \tag{1}$$

The second gain stage is simply a common stage gain stage with a pchannel active load Q6s .Its gain is given by

$$A_{V2} = -g_{m7}(r_{d6}||r_{ds7}) \tag{2}$$

$$Overallgain(A_V) = A_{V1} * A_{V2} \tag{3}$$

2.2 Gain Band Width(GBW)

The gain-bandwidth product (GBW) of an operational amplifier (op amp) is a crucial parameter that characterizes its behavior. Let's delve into its definition and significance:

1. Definition:
   (a) The GBW represents the product of the open-loop gain of an op amp and the frequency at which the open-loop gain equals one (unity gain).
   (b) It is also referred to as (f_{unity}).
   (c) Manufacturers often specify this parameter on op amp datasheets.
2. Explanation:
   (a) The open-loop frequency response of a general-purpose op amp exhibits a characteristic shape with a 20 dB per decade rolloff slope
   (b) The lag break frequency (fc) is determined by a compensation capacitor (usually in the Miller position).
   (c) Due to the Miller effect, this capacitor's apparent value increases significantly, resulting in a very low critical frequency (often in the range of 10 to 100 Hz).
   (d) Other lag networks caused by stray or load capacitances operate at much higher frequencies (usually over 1 MHz).
   (e) The remaining lag networks do not affect the open-loop response until the gain has already dropped below zero dB.
   (f) This frequency response curve allows you to set almost any desired gain with stability, maintaining satisfactory gain and phase margins.
3. Practical Implications
   (a) The GBW is crucial when designing closed-loop amplifier circuits.
   (b) It helps determine the maximum usable bandwidth for a given gain configuration.
   (c) As the frequency increases beyond the GBW, the gain starts declining steadily.
   (d) Engineers must consider the GBW when selecting op amps for specific applications.

3 THEORETICAL ANALYSIS

For MOSFET we have several basic parameters including

$$I_D = \frac{1}{2} * Kn\frac{W}{L}(V_{gs} - V_{tn})^2 \tag{4}$$

3.1 Gain, Pole and zeros

We define the input Vin, the output voltage of the first stage i.e. the input voltage of the second stage V1, and the output voltage of the whole circuit Vout, so we can get that for two stage operational amplifier we have

$$V_{out}/V_{in} = (V_{out}/V_1) * (V_1/V_{in}) \tag{5}$$

so we can calculate the voltage gain of two stage separately and then combine together We set the output resistance of the first stage Ro2 k Ro4 as R1 and the output resistance of the second stage Ro6 k Ro7 as R2. We also se the output capacitance of the first stage as C1 and C2 CL for the second stage. So we finally get that

$$V_{out}/V_{in} = \frac{(gm1 * R1)(gm2 * R2)(1 - sCc/gm2)}{as^2 + bs + c} \tag{6}$$

$$a = R_1R_2(C_1C_2 + C_1C_L + C_2C_L) \tag{7}$$

$$b = R_2(C_c + C_2) + R_1(C_c + C_1) + Cc * gm2 * R1R2 \tag{8}$$

to find the poles and zeros, we must transform the equation into form like

$$\frac{V_{out}}{V_{in}} = \frac{A_{dc}(1 - \frac{s}{z1})}{(1 + \frac{s}{p1})(1 + \frac{s}{p2})} \tag{9}$$

here for this two stage amplifier we have the DC gain of the amplifier

$$A_{dc} = gm1R1gm2R2 \tag{10}$$

the zero point of the circuit

$$z1 = \frac{gm2}{Cc} \tag{11}$$

When it comes to the poles of the circiut, approximately we have

$$p1 = \frac{1}{b} \tag{12}$$

we can simply it to

$$p_1 = \frac{1}{C_c g_{m2} R_1 R_2} \tag{13}$$

for another pole p2 we have

$$p_2 = \frac{g_{m2}}{C_1 + C_2} \tag{14}$$

3.2 Phase Margin

The gain band with GBW is equal to $DCgainp_1 = (g_{m1}/C_c)$ For phase margin, we have

$$z = 10 * GBW \tag{15}$$

then we need

$$p_2 \geq 2.2GBW \tag{16}$$

and finally

$$C_c \geq 0.22C_L \tag{17}$$

to get more than 60∘ phase margin. Thus we also have

$$\frac{gm1}{gm2} \leq 0.22 \tag{18}$$

3.3 Slew Rate

In our design, the slew rate is just equal to

$$slewrate = \frac{I_5}{C_c} \tag{19}$$

we already have I5 = 40µA so Cc must be under 10C, with is certain to full-fill. Here we need to obtain 10MV /s slew rate under 100MHZ, so we need the voltage change more than 0.05V in one pulse, which is 5ns in width.

4 2 stage OPAMP design

here i am considering the below circuit to calculate the theoreitical values

4.1 Design procedure

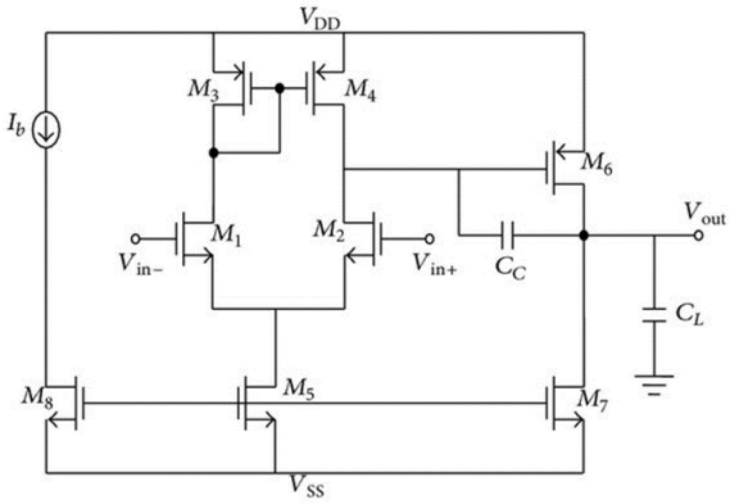
Step 1

Assuming that for a stable system, the phase margin is 60 degrees and zero frequency at greater than 5 times Gain Bandwidth product. So, by solving the equation of one zero and two pole system, with the above Assumptions we got the equation,

$$C_c \geq 0.23C_L \tag{20}$$

They given C_L is 10 pF.so we got miller capacitance is

$$C_c > 2.3pF \tag{21}$$



Step 2

This design focuses on the high gain bandwidth of a two-stage opamp. One of the provided design parameters specified that the power *leq* 1mW and reference current source is 20µA.

$$power \leq 1 * 10^{-3}W$$
$$1.8 * (I_{ref} + I_5 + I_7) \leq 10^{-3}$$
$$I_5 + I_7 \leq 535.55mW$$

Fixing I_5 is 80µA and I_7 is 440µA.

Step 3

$$slew_rate = \frac{I_5}{C_c} \tag{22}$$

Given slew rate minimum 1V/μm. Assumed the slew rate to be 20V/μm.

$$C_c = 4pF \tag{23}$$

Step 4

The gain bandwidth product is the voltage unit gain frequency. Because there is a dominant pole, there will be a 20dB decay at unit gain frequency.

$$gm_1 = 2\pi * GBW * C_c \tag{24}$$

then gm_1 is

$$gm_1 = 1759.291\mu A \tag{25}$$

with

$$gm_1 = \sqrt{2I_d \mu_n C_{ox} \frac{W}{L}_1} \tag{26}$$

substituting the values in the above equation then

$$\frac{W}{L}_1 = 113.066 = \frac{W}{L}_2 \tag{27}$$

Step 5

maximum ICMR is 1.4V. In the above circuit, for M1 to be in saturation

$$V_{d1} > V_g - V_{th1} \tag{28}$$

$$V_g < (V_{dd} - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L} 3}}) + Vth1 \tag{29}$$

here gate voltage is the maximum ICMR voltage. Substituting all the values

$$ICMRmax > (Vdd - (V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} \frac{W}{L} 3}}) + Vth1 \tag{30}$$

$$\frac{W}{L}_3 = \frac{W}{L}_4 > 3.6448 \tag{31}$$

Step 6

ICMR minimum is 0.4V. For all transistors to be in saturation.

$$V_{dsat} = ICMR_{min} - \sqrt{\frac{2I_D}{\mu_n C_{ox} \frac{W}{L} 1}} - Vthn \tag{32}$$

substituting all the values,

$$V_{dast} = 0.0045V \tag{33}$$

But the minimum overdrive voltage should be 0.1V, V_{dsat} is assumed as 0.1V, then substituting the value in the current equation

$$\frac{W}{L}_5 = 46.76 \tag{34}$$

Step 7

M6 and M4 are in the current mirror.

$$\frac{(W/L)_6}{(W/l)_4} = \frac{I_6}{I_4} \tag{35}$$

this gives

$$\frac{W}{L}_6 = 40.095 \tag{36}$$

Step 8

$$\frac{(W/L)_7}{(W/L)_5} = \frac{I_7}{I_5} \tag{37}$$

M6 and M7 are in series so both currents are equal.

$$(w/l)_7 = 257.175 \tag{38}$$

Now that all the (W/L) ratios have been found, individual transistor lengths are to be calculated. Since the optimization to be done on obtaining high bandwidth implies that the circuit is a high-frequency circuit. For high-frequency circuits, the design is done on minimum lengths so the length of transistors is considered as 360nm. Gain of two two-stage opamp is

$$gain = gm_1 gm_2 (r01||r04)(ro6||ro7) \tag{39}$$

5 Simulation Results

5.1 DC ANALYSIS

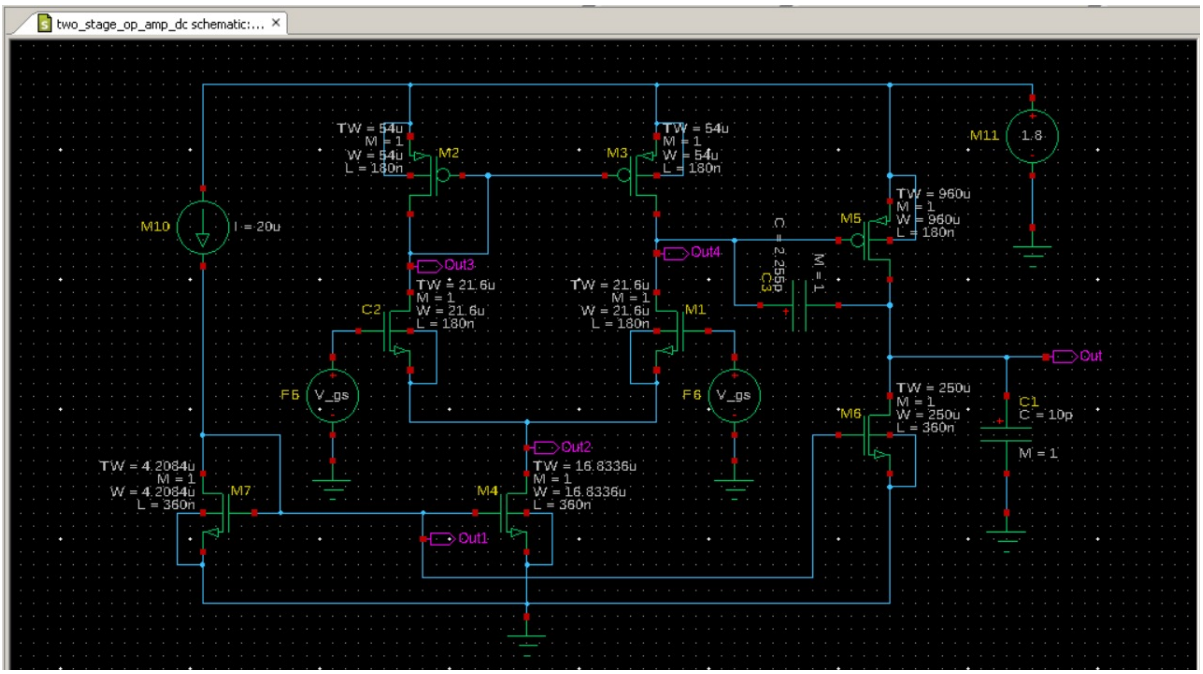


Figure 1: schematic of DC analysis

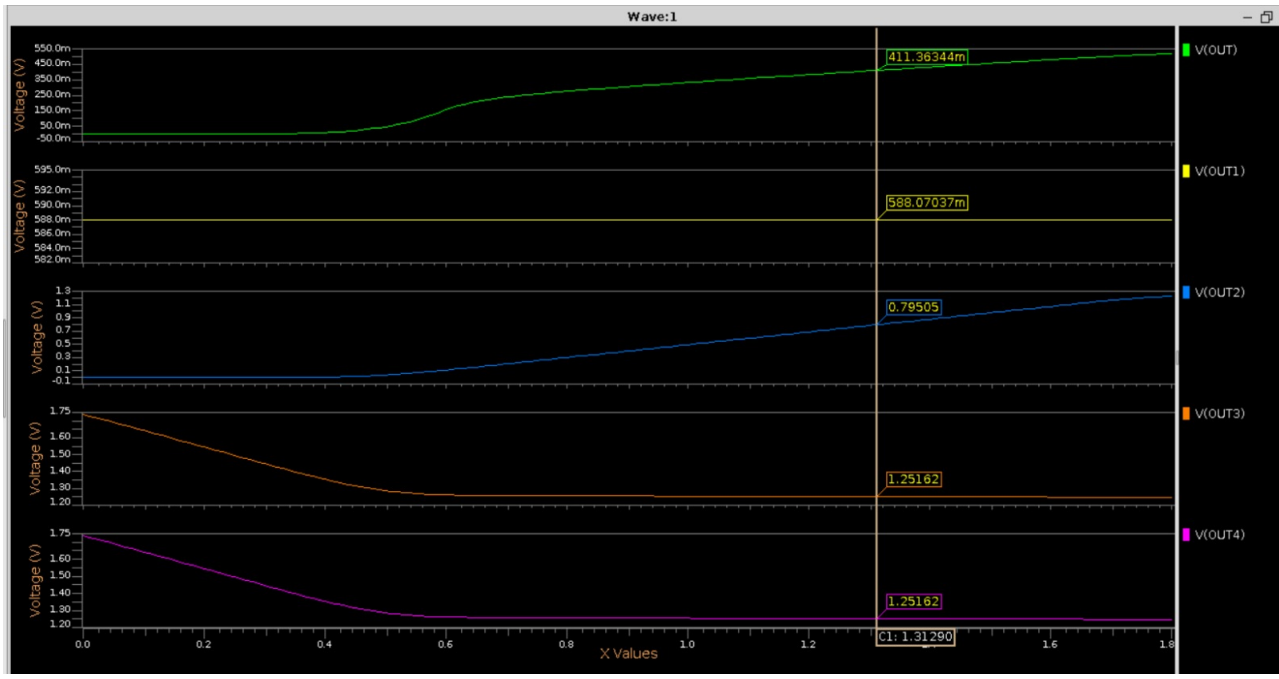


Figure 2: Operating Point for transistors in saturation

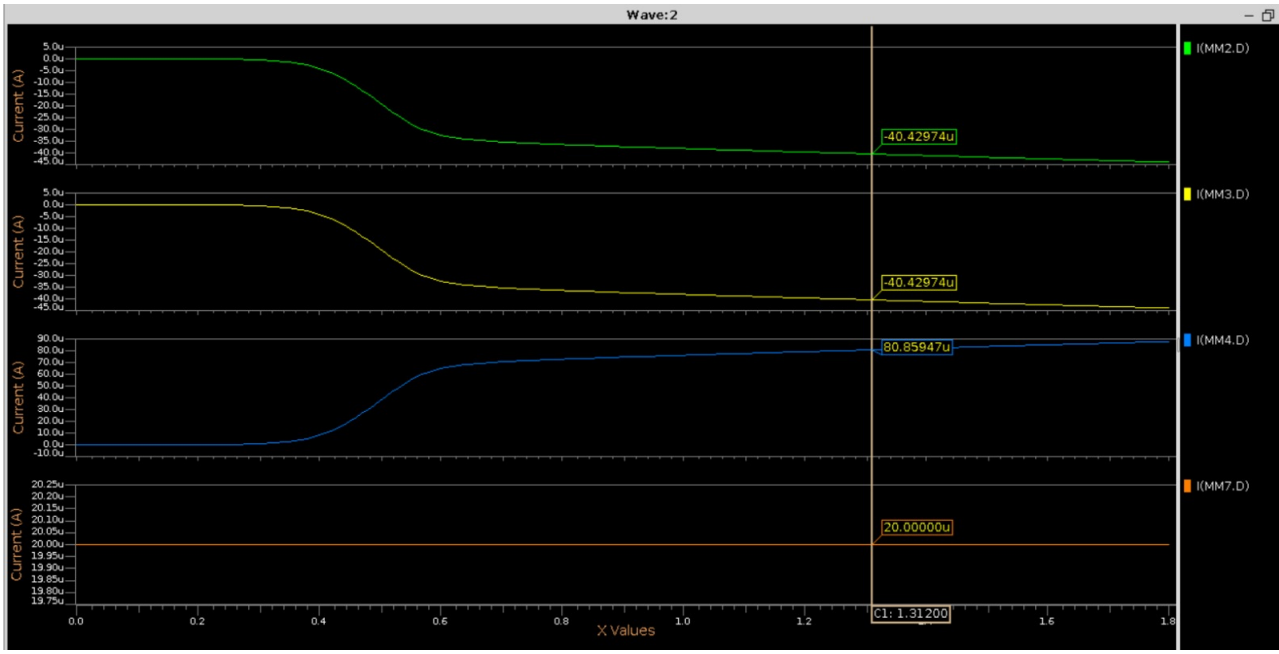


Figure 3: Operating Point for transistors in saturation

5.2 AC ANALYSIS

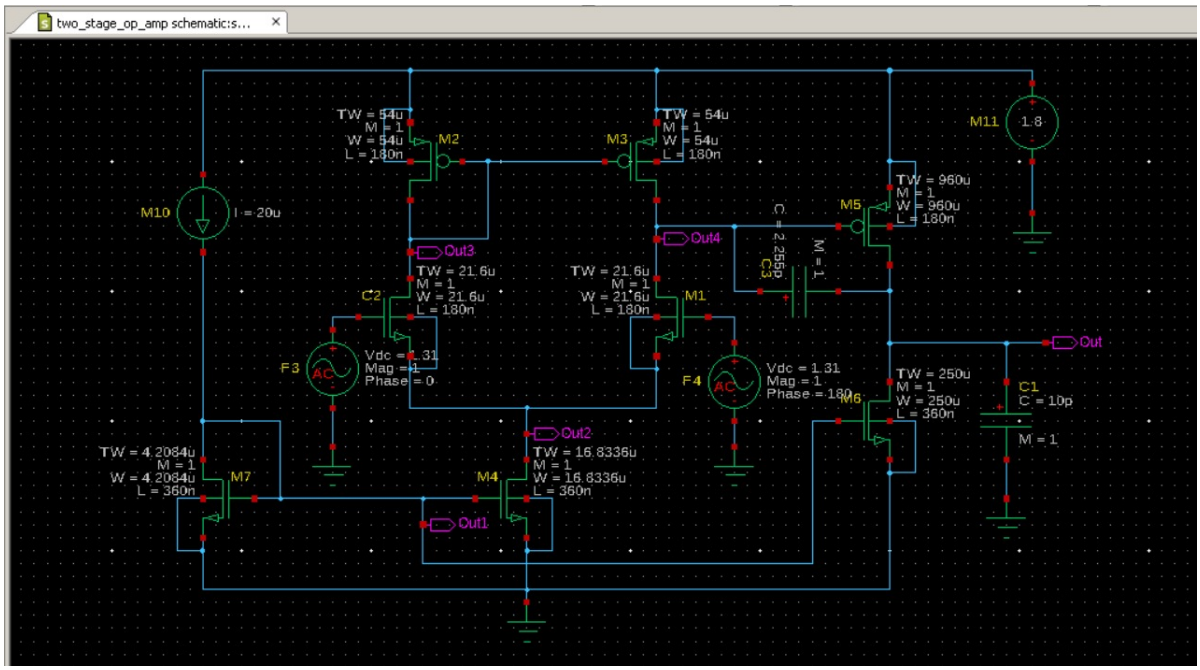


Figure 4: schematic of AC analysis

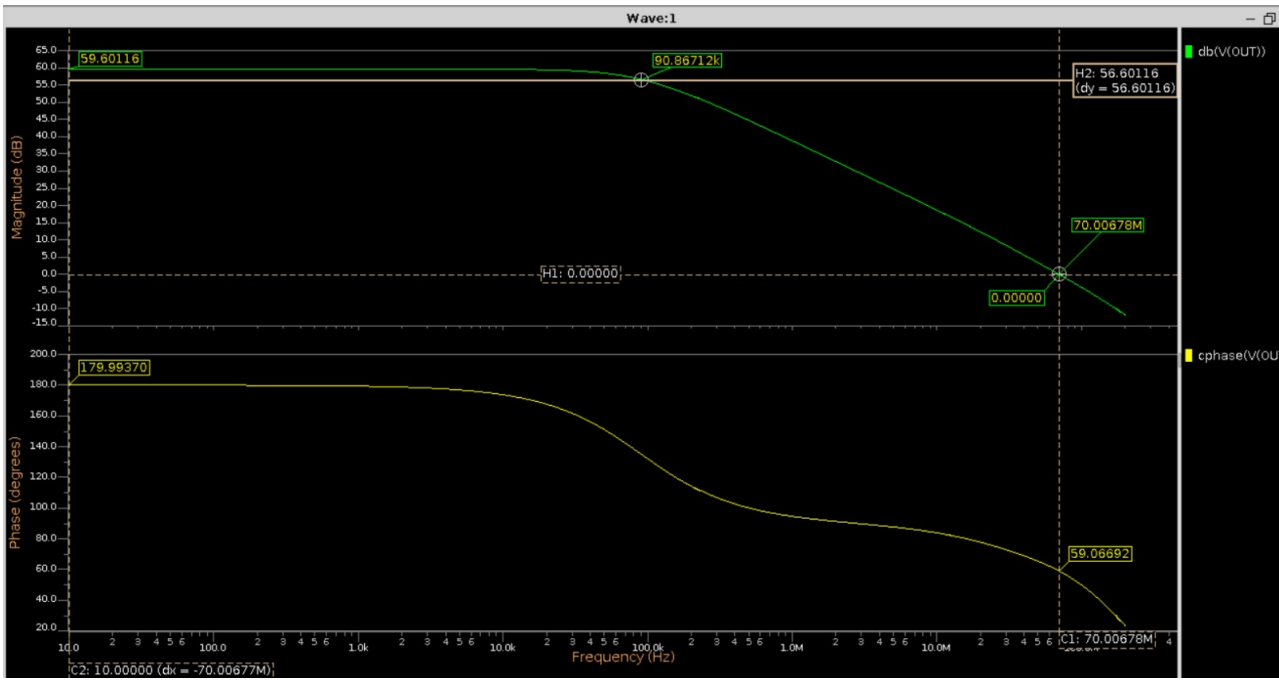


Figure 5: Gain, Bandwidth, Unity gain frequency and phase margin

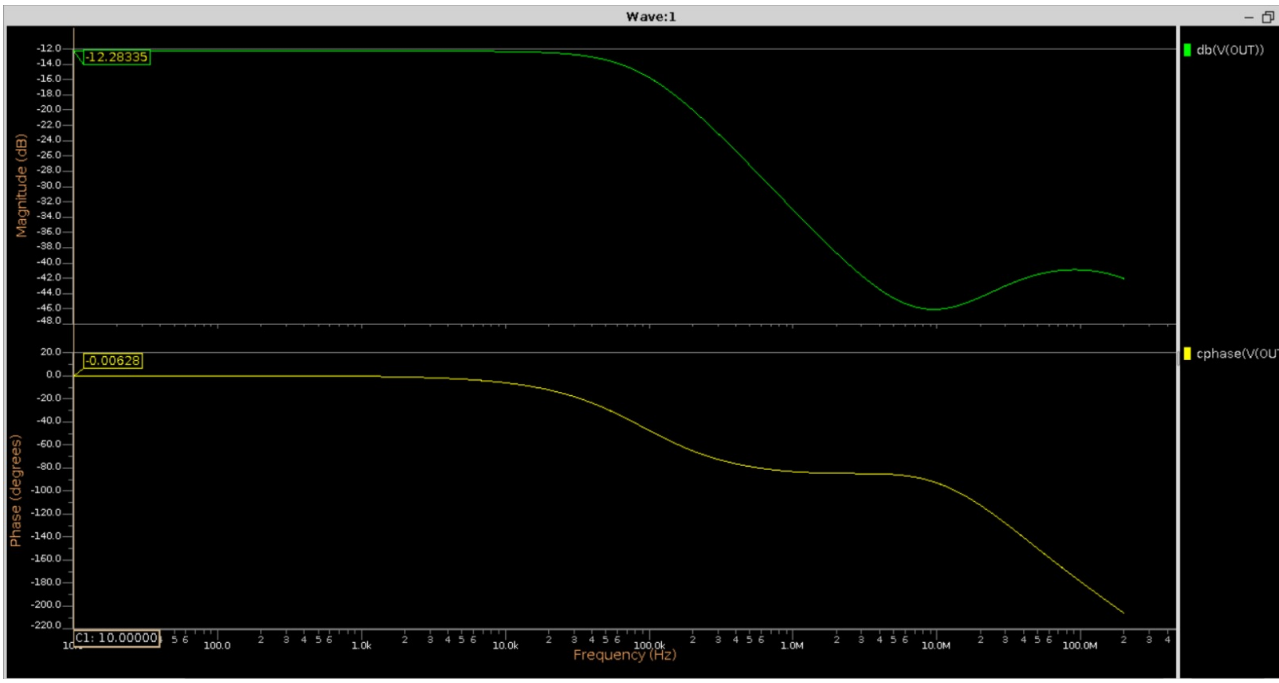


Figure 6: Common Mode Gain

- **To find the common mode gain, the same input is applied at both ends of the input. Then AC analysis is done to find the gain.**
- **To find PSRR the AC input is applied in place of Vdd, dc bias is applied at the input gate of the transistors and one branch input is connected to the output. AC analysis is then done and gain is found out.**

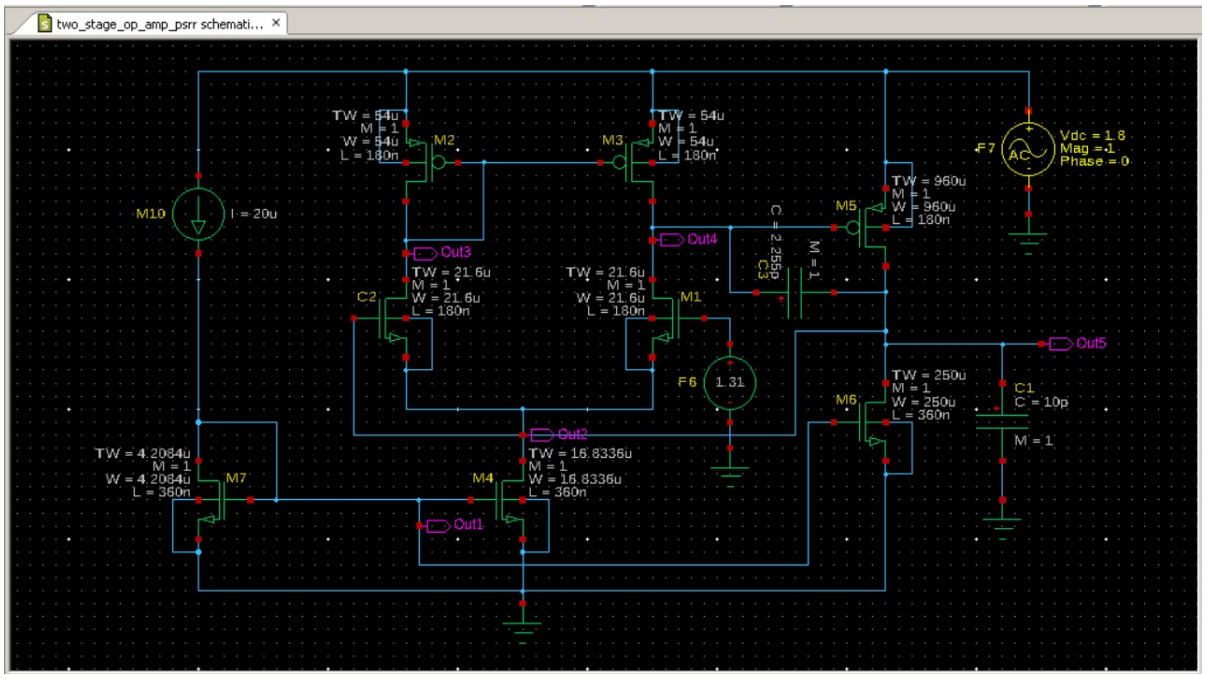


Figure 7: schematic of PSRR in AC analysis

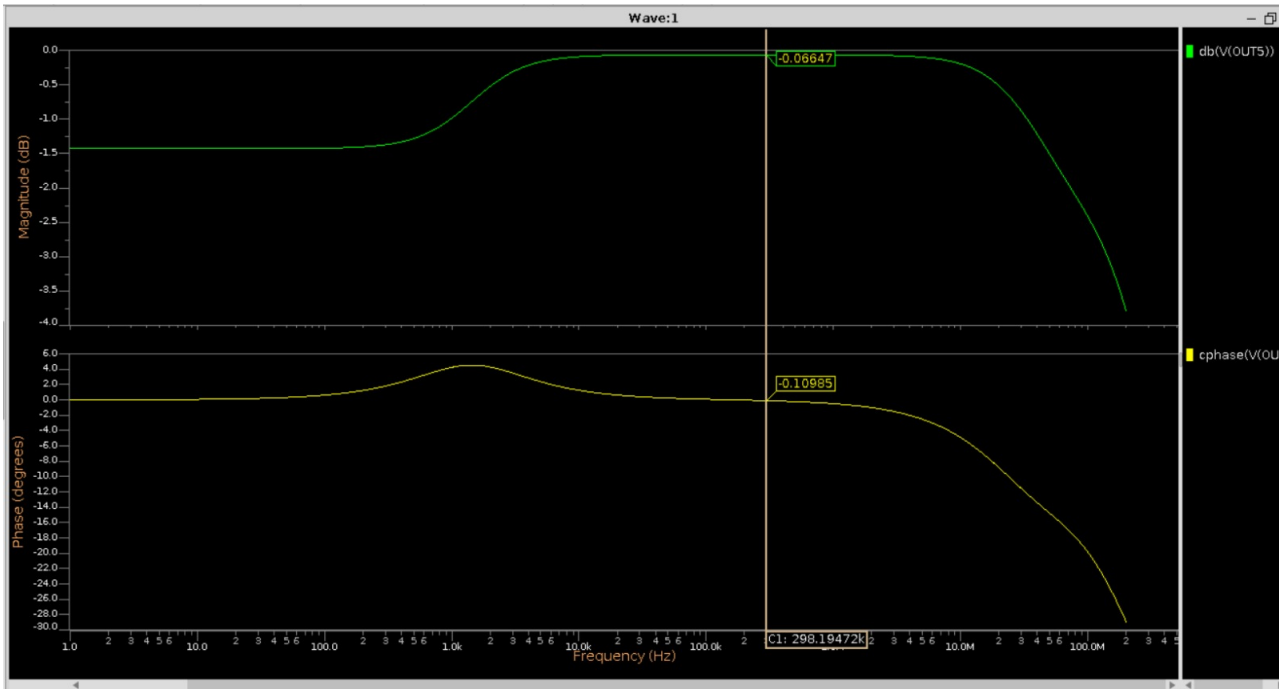


Figure 8: Plot to measure PSRR

5.3 TRANSIENT ANALYSIS

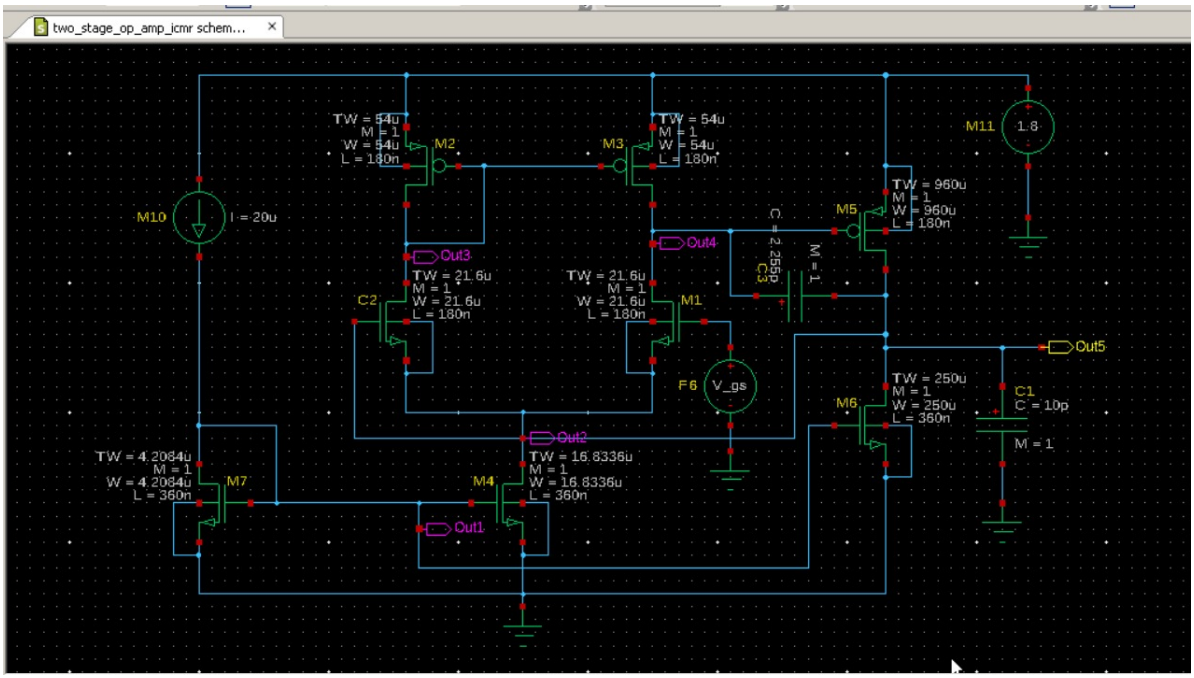


Figure 9: schematic of ICMR/OCMR analysis

- **For ICMR and OCMR, The branch in which the output is sensed will be connected to the output and a DC sweep is done to find the minimum to maximum input and minimum to maximum output.**
- **For Slew Rate, for a maximum slew rate the entire current should flow through only a single branch.; For that, a square pulse is input at one end and the other is grounded. Transient analysis is done then the max difference in output in a period gives the slew rate of the design im[plemented]**

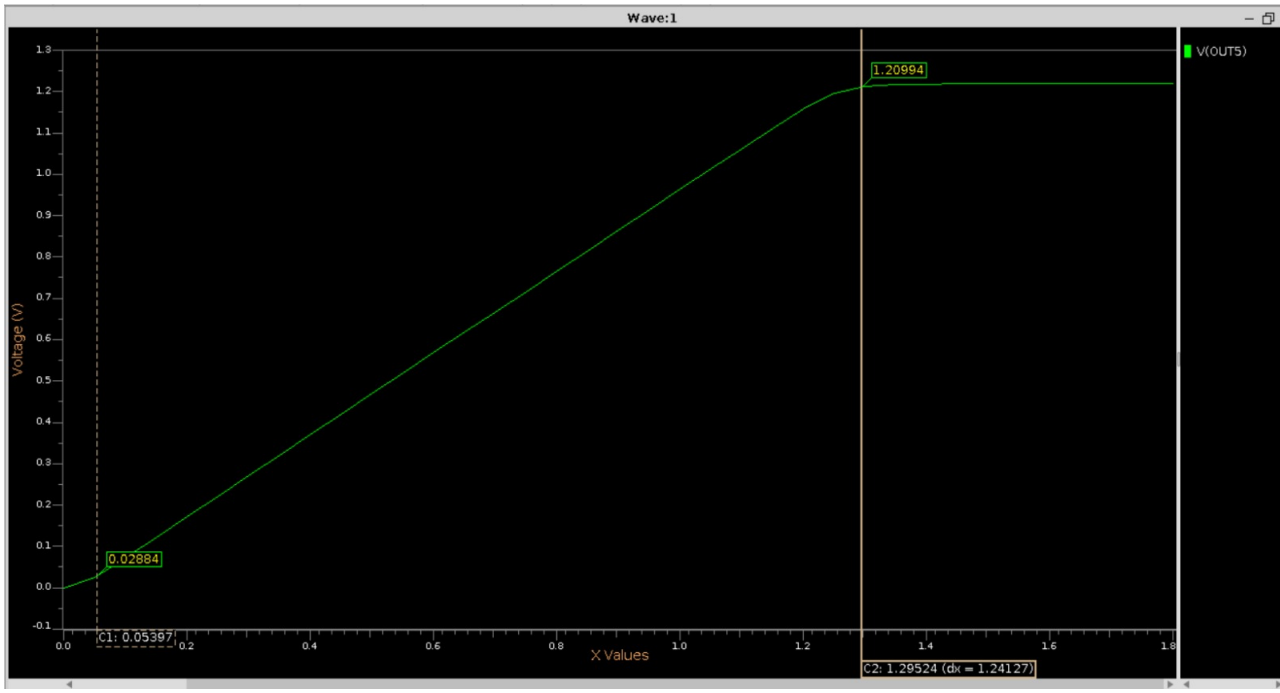


Figure 10: Plot for ICMR and OCMR

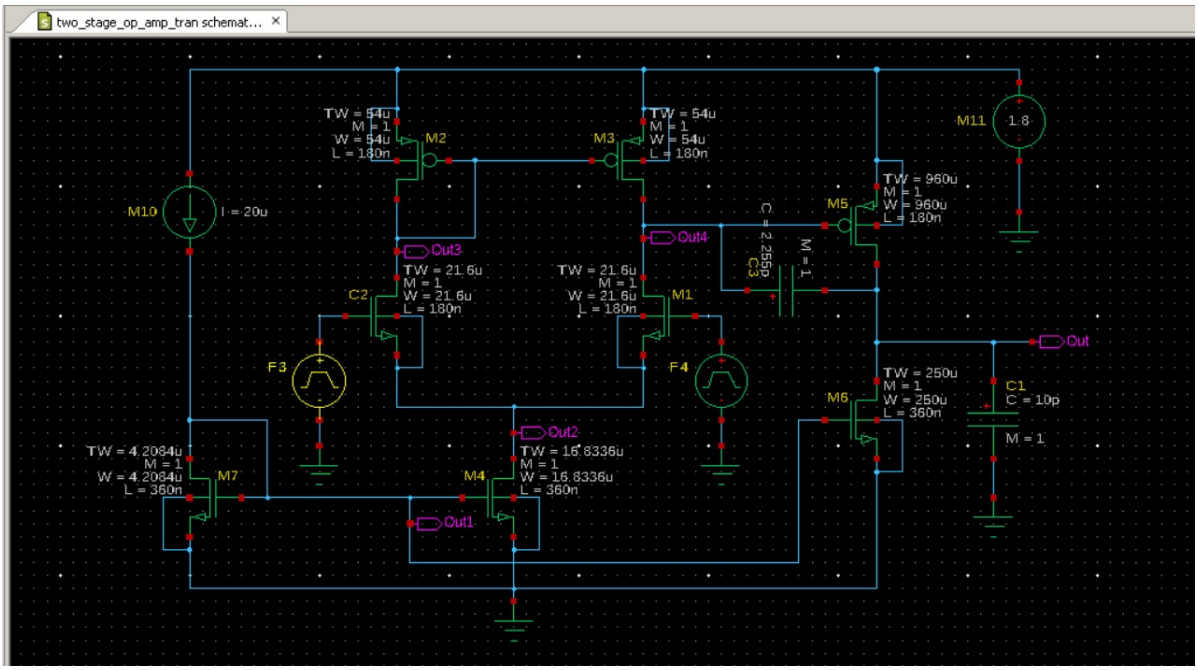


Figure 11: Schematic for Slew Rate

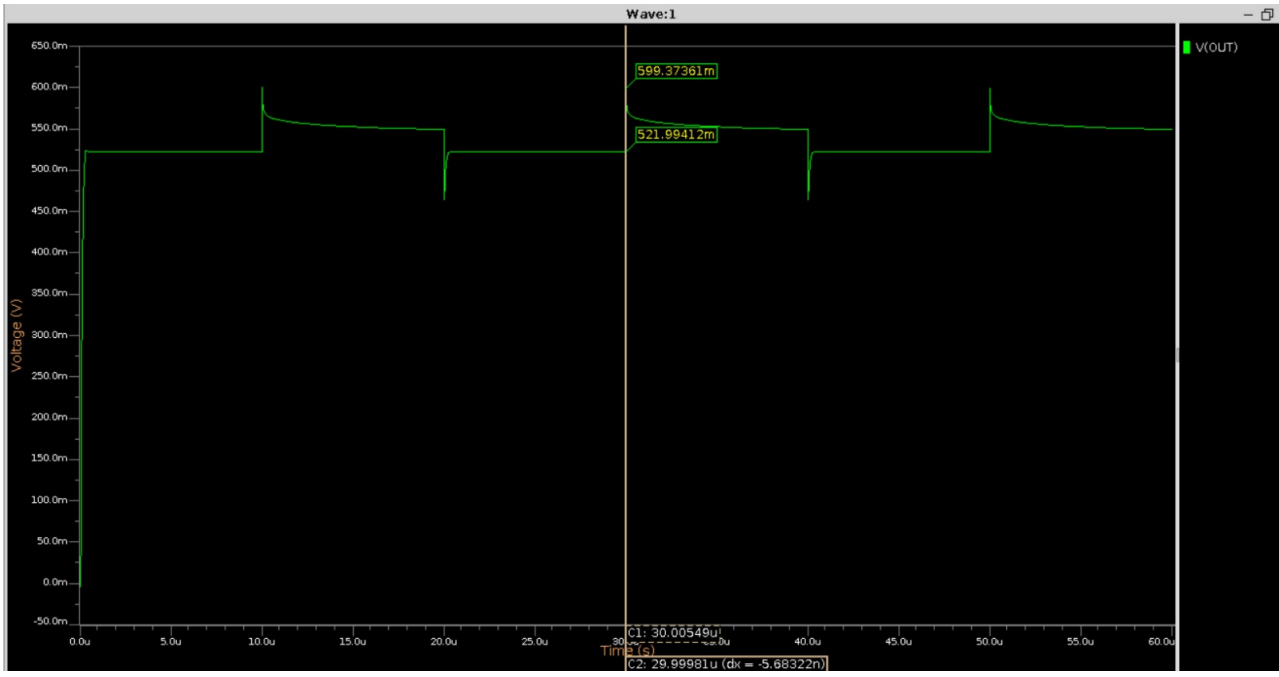


Figure 12: Plot for Slew Rate

6 RESULTS

6.1 TRANSISTOR SIZES

transistor	width (um)	length (nm)
M5	16.8336	360
M6	960	180
M1	21.6	180
M2	21.6	180
M3	54	180
M4	54	180
M7	250	360
M8	4.2084	360

6.2 CAPACITOR VALUE

capacitor	value (pf)
C_c	2.255
c_L	10

6.3 AC analysis

parameter	theoretical value	practical value
GAIN	$\geq 40db$	59.60db
bandwidth	70Mhz	70.006Mhz
PM	≥ 60	59.066
Power	$\leq 1mW$	0.94mW
CMRR	–	-12.28db
PSRR	–	-0.06647db

6.4 Transient analysis

Parameter	practical value
SLEW RATE	13.623 V/μs
ICMR	0.05397-1.29524
OCMR	0.02884-1.20994

7 Conclusions:

- The analysis for the given design specification GAIN BAND WIDTH PRODUCT of 2-stage CMOS opamp including simulation results has done in this work.
- Since the GBW is dependend on the bandwidth of the circuit so for the slew rate one we are getting he GBW as the 3MHz so and we need to increase the GBW we taken the slew rate as 14 and we got the GBW as the 70Mhz.
- Here the idths are also taken larger so that to satisfy the phase margin of the circuit and also to change the gain.
- The mentioned results and graphs also depicted in the which estimates the limits of scaling for sevaral applications and devices.
- Designed op amp has high gain circuit for the application like comparators.