Analog IC Design Lab
Experiment 8

Design a fully differential folded cascode single-stage opamp

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EEE - VLSI & Nanoelectronics

Contents

1 Experiment

Design a fully differential folded cascode single-stage opamp.

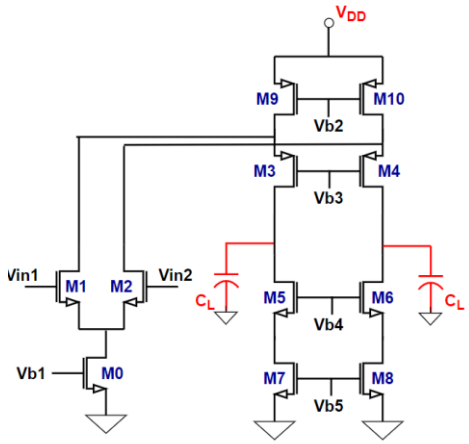
2 Objective

To find W/L, gain bandwidth product, output swing, ICMR, and compare the practical and theoretical results.

2.1 Specifications:

- VDD= 1.8V
- Differential output swing= 1.8V
- Power dissipation $\leq$ 0.12mW
- Voltage Gain=2000 V/V
- Technology=180 nm
- CL=10pF

2.2 Circuit Schematic:



3 Analysis:

3.1 DC Analysis

- Report the schematic of the diff pair with DC OP point annotated: Id, Vgs, Vds, Vth, Vdsat, gm, gds, gmb, region.
- Check that all transistors operate in saturation

3.2 AC Analysis.

- Observe pole-zero analysis of your circuit
- Frequency response of your circuit.
- Find Av, PM, Bandwidth, CMRR, PSRR.
- Give a proper reason for selecting any value of any parameter

3.3 Transient Analysis

- slew rate.
- ICMR, OCMR

4 Theory:

Certainly! Let's delve into the theory behind a differential cascode op-amp.

4.1 Basic Concepts:

1. Differential Amplifier Basics
    - A differential amplifier is a fundamental building block in analog circuit design. It amplifies the difference between two input voltages while rejecting common-mode signals (signals that appear equally on both inputs).

- The basic differential amplifier consists of two transistors (usually BJTs or MOSFETs) with their emitters/sources connected together. The collector/drain currents are combined to form the output voltage.

2. Cascaded Differential Amplifier

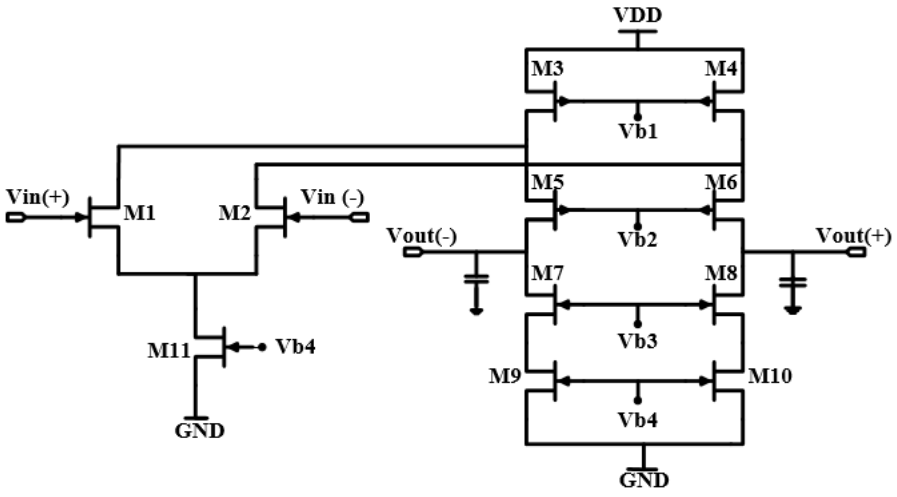
   - A cascaded differential amplifier involves connecting multiple differential amplifier stages in series to create an operational amplifier (op-amp).
   - Here's how it works:
     (a) The output of the first differential amplifier stage feeds into the input of the second stage, which is again a differential amplifier.
     (b) This cascading provides several benefits:
         – **Common-Mode Rejection Ratio (CMRR):** By cascading, we enhance CMRR, making the op-amp less sensitive to common-mode signals.
         – **Differential Voltage Gain:** The cascaded structure allows us to achieve higher differential voltage gain.
         – **Output Impedance:** The third section (often a common collector or common emitter follower stage) ensures low output impedance.
   - The output is single-ended, meaning it provides only one phase with respect to ground. The inverting input is 180° out of phase with the output, while the noninverting input is in phase with the output.

The below diagram shows the general Schematic that we are designing in this report,
So the over all gain will Be cascoded which is given by the equation as

$$A_v = A_{v1} * A_{v2} \tag{1}$$

so by considering the transconductance and the small signal resistance the Overall gain will be given by the

$$A_v = g_{m1}(g_{m5}(r_{05} * r_{03})||gm_7 r_{07}(r_{09}||r_{01}) \tag{2}$$



4.2 Applications and Advantages

- Proper functioning of differential stages often requires matching transistors and resistor values.
- To simplify this, consider using transistor arrays like the CA3086, which offer inherent advantages unique to IC circuits (compactness, ease of handling, and electrical/thermal matching).
- Remember, the differential cascode op-amp is a powerful tool in analog design, providing improved performance and versatility.

4.3 Basic Definations:

1. **CMRR(Common Mode Rejection Ratio)**
   - It is the most important specification and it indicates how much of the common mode signals will present to measure. The value of the CMMR frequently depends on the signal frequency and the function should be specified. The function of the CMMR is specifically used to reduce the noise on the transmission lines.
   - When the same input voltage is applied to both input terminals of an op-amp, the op-amp is said to be operating in a common mode configuration.

- A common-mode voltage v_{cm} can be ac, dc, or a combination of ac and dc.

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2. **Power supply rejection ratio (PSRR)**

   - It describes the ability of a circuit to suppress any power supply variations from passing to its output signal and is typically measured in dB. It's most often used with operational amplifiers (op amps), dc/dc converters, linear regulators, and low drop out regulators (LDOs). For op amps, the PSRR describes the ability of the amplifier to maintain its output voltage as its DC power supply voltage is varied. PSRR quantifies the ability to block ripple voltage from an input source in power conversion applications.
   - An ideal op amp would have zero PSRR. However, the PSRR of a real op amp is frequency-dependent; the higher the signal frequency, the lower the PSRR. PSRR is commonly measured in terms of the input, but there is no industry standard

3. **ICMR**

   - It refers to the range of common-mode voltages over which a differential amplifier continues to function optimally. Specifically, it's the region where the differential pair operates properly.
   - The Input Common Mode Range (ICMR) significantly influences the performance of an analog circuit.
     (a) **Signal Linearity:**If the common-mode voltage exceeds the ICMR, the circuit may become nonlinear, leading to distortion in the output signal.
     (b) **Biasing and Stability:**If the common-mode voltage is outside the ICMR, biasing conditions may be compromised, affecting stability and causing unexpected behavior.
     (c) **Differential Amplifier:** Performance:If the common-mode voltage exceeds the ICMR, the differential amplifier may saturate or operate in an undesirable region.
     (d) **CMRR (Common-Mode Rejection Ratio):**A wider ICMR improves CMRR, enhancing the circuit's ability to reject unwanted common-mode noise.

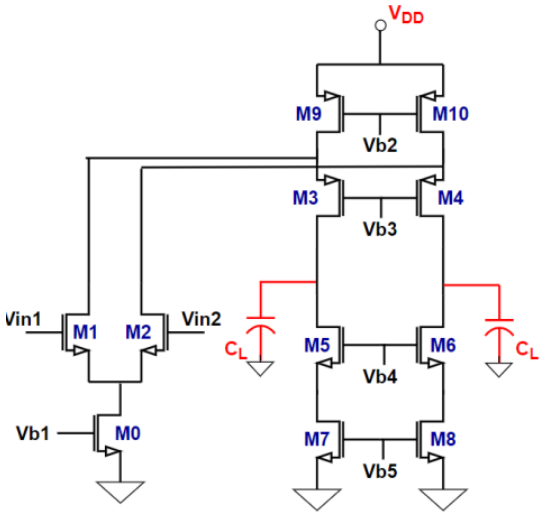
(e) **Protection Circuits:**The ICMR helps design these protection circuits by defining safe voltage limits.

4. **OCMR(Output common mode rejection Ratio):**

- The OCMR refers to the range of output voltages within which an analog circuit, such as an operational amplifier (op-amp), can provide a valid output signal.
- It specifies the allowable common-mode voltage range for the output signal.
- If the output voltage exceeds the OCMR, the op-amp may saturate or clip the signal, leading to distortion.

5 Design Approach:

For designing i am considering this circuit to calculate the values of the ovr drive voltages and current



5.1 Current Calculation:

From the given power budget and the supply voltage we can calculate current by

$$1.8 * I_{total} = 0.12\mu W \tag{3}$$

$$I_{total} = I_{M9} + I_{M10} = 66.66\mu Amp \tag{4}$$

so the current that i will consider is 60μAmp
The current will be divided equally in both ides that is given by the 30μAmp

$$I_{M9} = 30\mu amp \tag{5}$$

$$I_{M10} = 30\mu amp \tag{6}$$

$$I_{M3,M4,M5,M6,M7,M8} = 30\mu amp \tag{7}$$

$$I_{M9,M10} = 30\mu amp \tag{8}$$

$$I_{M1,M2} = 30\mu amp \tag{9}$$

$$I_{M0} = 30\mu amp \tag{10}$$

5.2 Calculation oF Overdrive Voltages:

In this experiment they wanted us to design the for higher swing.So according that we need to design the ratios and also the Overdrive Voltages

$$2(V_{DD}(V_{OD9} + V_{OD5} + V_{OD3} + V_{OD7} + V_{OD9})) = 1.8 \tag{11}$$

$$(V_{OD9} + V_{OD5} + V_{OD3} + V_{OD7}) = 0.9 \tag{12}$$

Based on the above values we need to design the Over drive voltages for the transistors
Here we have 2 Nmos and 2 Pmos so according to the mobility Nmos has more mobility than the Pmos so to have the same current to flow we need to have the pmos hould have the high overdrive voltage than the Nmos aand according to that i designed the over drive voltages as follows

$$V_{0D9} = 0.3; V_{0D7} = 0.2; V_{0D5} = 0.2; V_{0D3} = 0.1; \tag{13}$$

5.3 Calculation Of W/L ratios

we know the current equation

$$I_D = \frac{1}{2} Kn \frac{W}{L} (V_{gs} - V_{tn})^2 \tag{14}$$

From the above equation the ratio is given by the

$$\frac{W}{L} = \frac{2I_D}{Kn(V_{gs} - V_{tn})^2} \tag{15}$$

we know the overdrive voltages and the also the kn so we can calculate the $\frac{W}{L}$ ratios as given by the

$$\frac{W}{L}_{M9.M10} = 4.72 \tag{16}$$

$$\frac{W}{L}_1 = \frac{W}{L}_2 = \frac{W}{L}_3 = \frac{W}{L}_4 = 3.65 \tag{17}$$

$$\frac{W}{L}_5 = \frac{W}{L}_6 = \frac{W}{L}_7 = \frac{W}{L}_8 = 1.5 \tag{18}$$

$$\frac{W}{L}_1 = \frac{W}{L}_2 = 11.7 \tag{19}$$

$$\frac{W}{L}_0 = 5.9 \tag{20}$$

5.4 Bias Voltage Calculation

we generally have the condition for the saturation

$$VDS \geq VGS - Vth \tag{21}$$

for **M1,M2**
we have the over drive voltage of 0.1 and also the souurce voltage of both these trx is overdrive voltage of M9 so that from the above equation we have the gate voltage which is equal to

$$VG_1 = VG_2 = 0.85V \tag{22}$$

For M3,M4 we now source voltage of M3 ,is nothing but drain voltage of M1 which is 0.4 and we know overdrive voltage of 0.1.

$$VG_3 = VG_4 = 0.75V \tag{23}$$

For M7,M8 we now source voltage of M7 ,is nothing but Vdd. and we know overdrive voltage of 0.2.

$$VG_7 = VG_8 = 0.75V \tag{24}$$

For **M5 and M6** we now source voltage of M5 ,source voltage of M5 nothing but drain voltage of M7 which is 1.6. and we know overdrive voltage of 0.2.

$$VG_5 = VG_6 = 0.95V \tag{25}$$

For **M9 and M10**

$$VG_9 = VG_{10} = 0.95V \tag{26}$$

For **M0**

$$VG_0 = 0.75V \tag{27}$$

5.5 Capacitor Calculation

Slew rate is given in the design specification is given as 50 volt per micro sec.

$$slewrate = \frac{I_9}{C_L} \tag{28}$$

we already have the current that is flowing throgh the M9 is 15mAmp.
So,From the above slew rate equation we can calulate capacitor which is given by the

$$C_L \leq 10pF \tag{29}$$

5.6 Calculation Of Gain:

for the 180nm length mosfet we have the channel length modulation is given by the 0.9

$$r_{ds} = \frac{V_A}{I_D} \tag{30}$$

$$r_{ds} = 360 \tag{31}$$

transconductance g_m which is given by

$$g_{mN} = \frac{2I_D}{V_{GS} - V_{TH}}$$

$$g_{m1} = 400\mu mho$$

$$gm_5 = 100\mu mhos$$

$$g_{m3} = 100\mu mho$$

if u substitute these values in the gain formula u will gget nearly equal to

$$A_V = 54$$

to increase the gain wehave the two options namely chnging overdrive voltage and the changing lenghth..
we cannot change the overdrve voltage because the overdrive voltage that we are taken is very less so we will consider the changing length so we willtake the length to be maximum of $2.0420m$ and then accordingly we will calculate the aspect ratios

$$A_v = 4145$$

5.7 Calculation of GBW

Given we have the gain band width is 200 mega hertz

$$GBW = \frac{g_m}{2 * \pi * C_L} \tag{32}$$

$$C_L < 30.1pF \tag{33}$$

6 DC Analysis:

6.1 Schematic

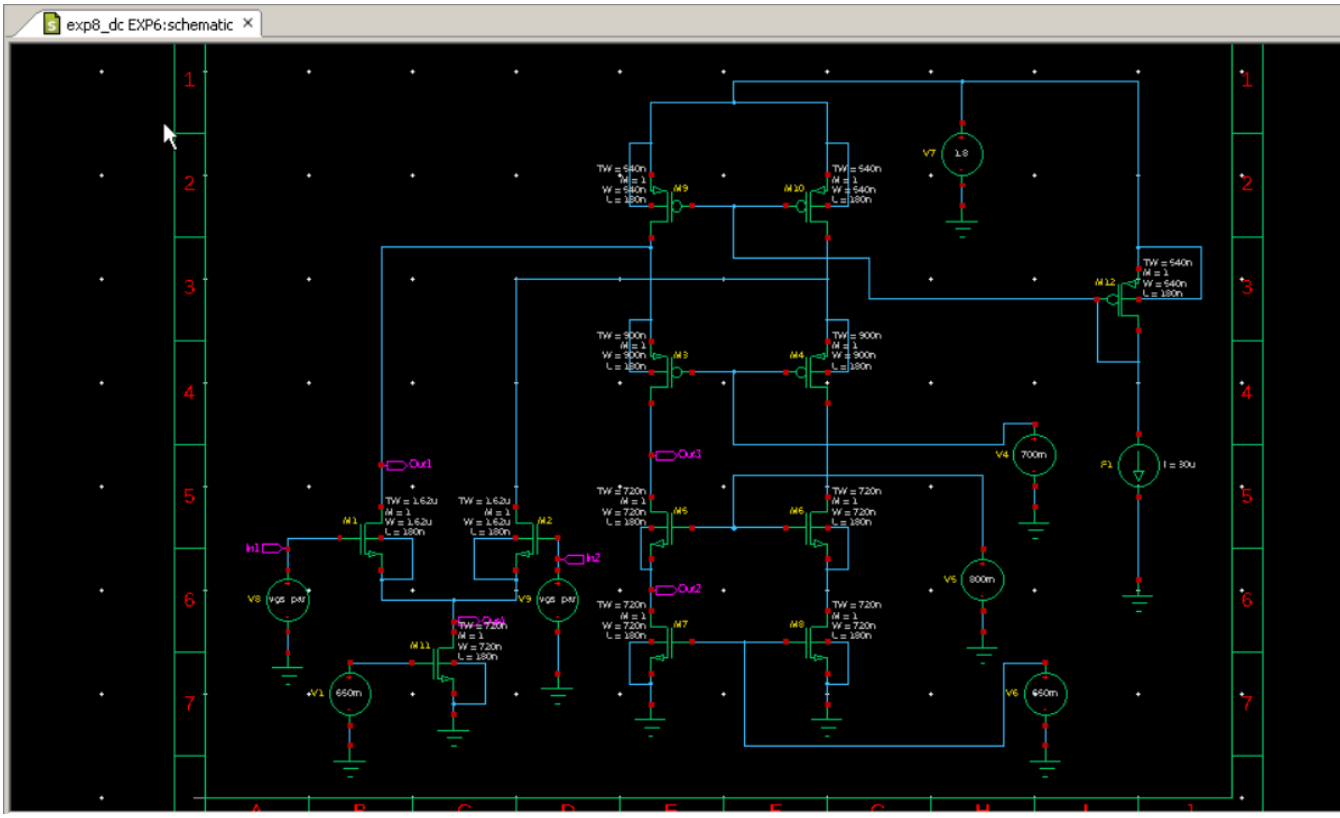


Figure 1: Schematic for DC analysis

6.2 Output Wave Forms for DC

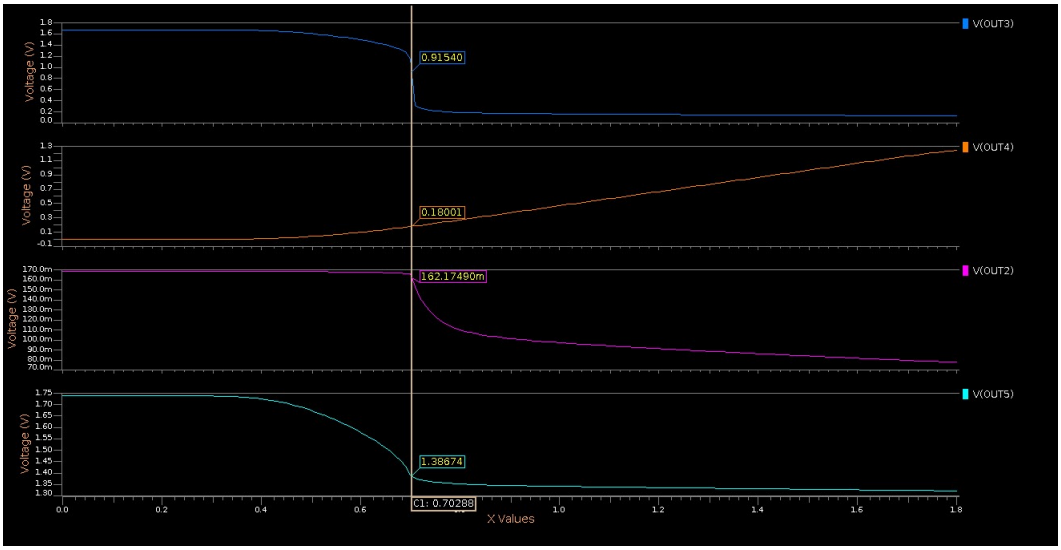


Figure 2: Output wave forms for Dcanalysis

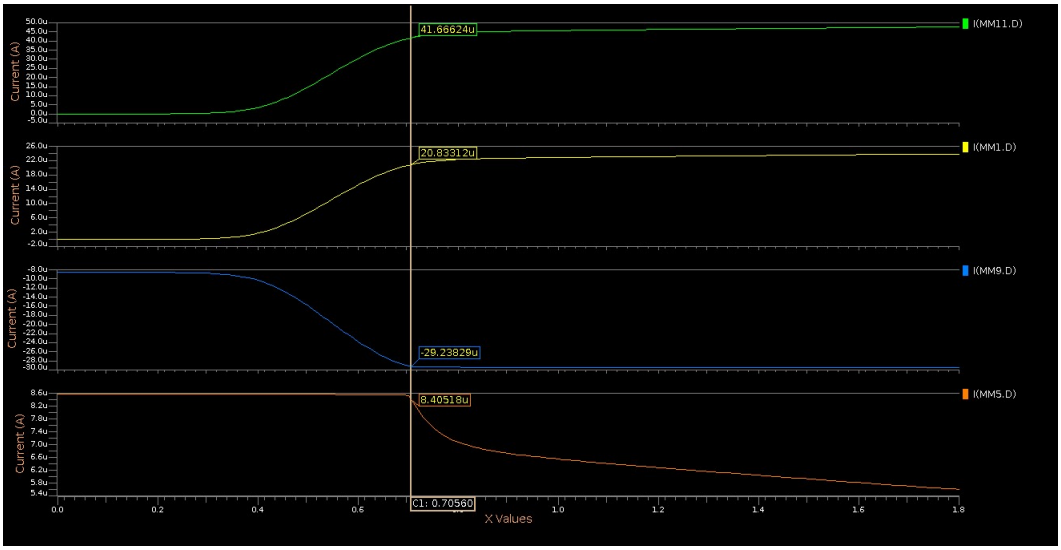


Figure 3: Output wave forms for Dcanalysis

From the dc analysis we got that all the transistors are in the saturation region..so that the current is constant.

7 AC analysis:

7.1 Schematic:

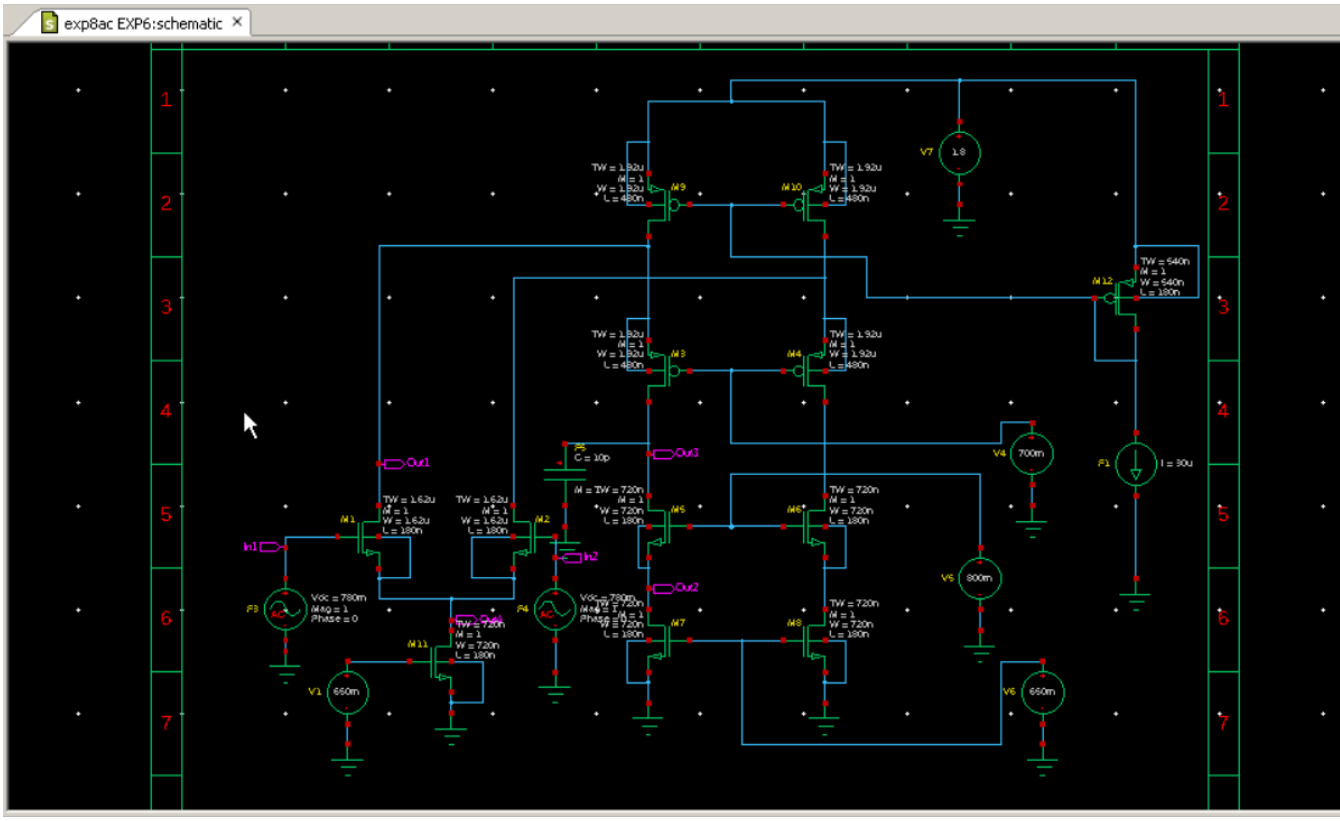


Figure 4: Schematic for AC analysis

7.2 Output waves for AC

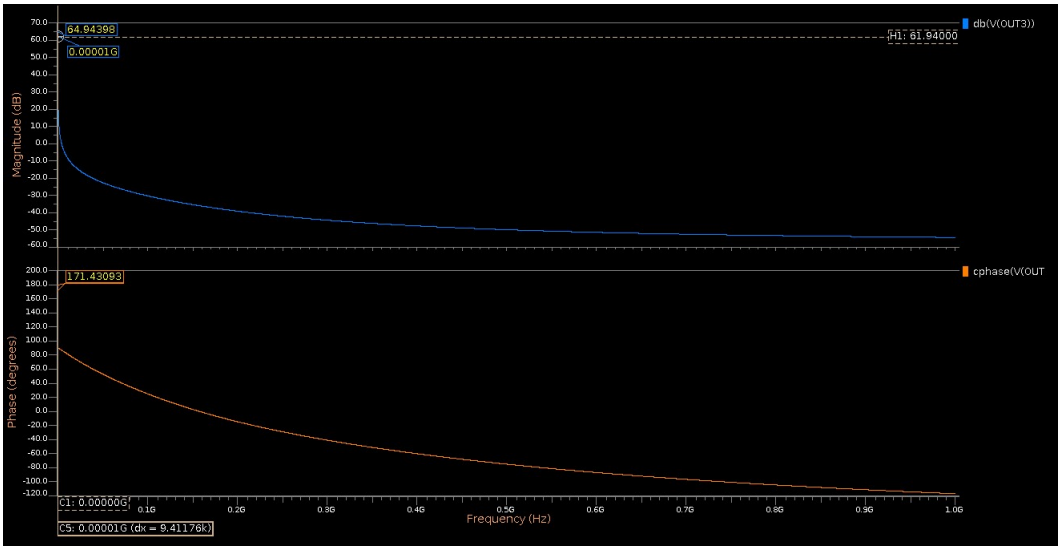


Figure 5: Output wave forms for AC analysis

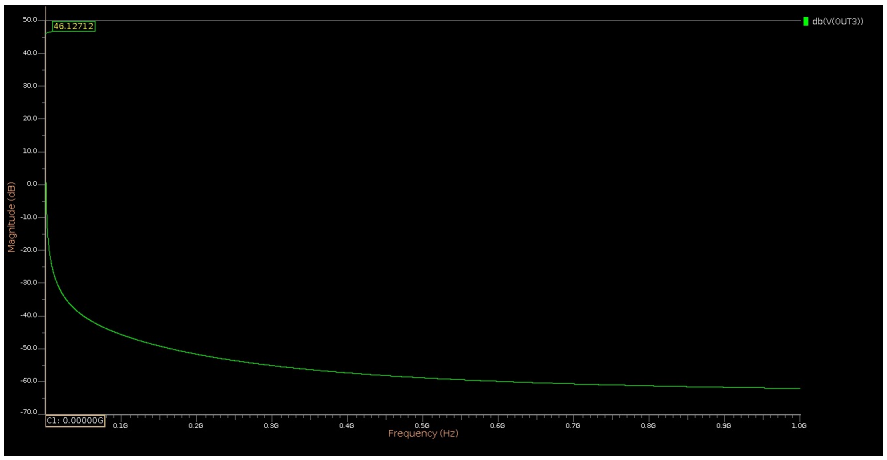


Figure 6: common mode gain

7.3 PSRR:

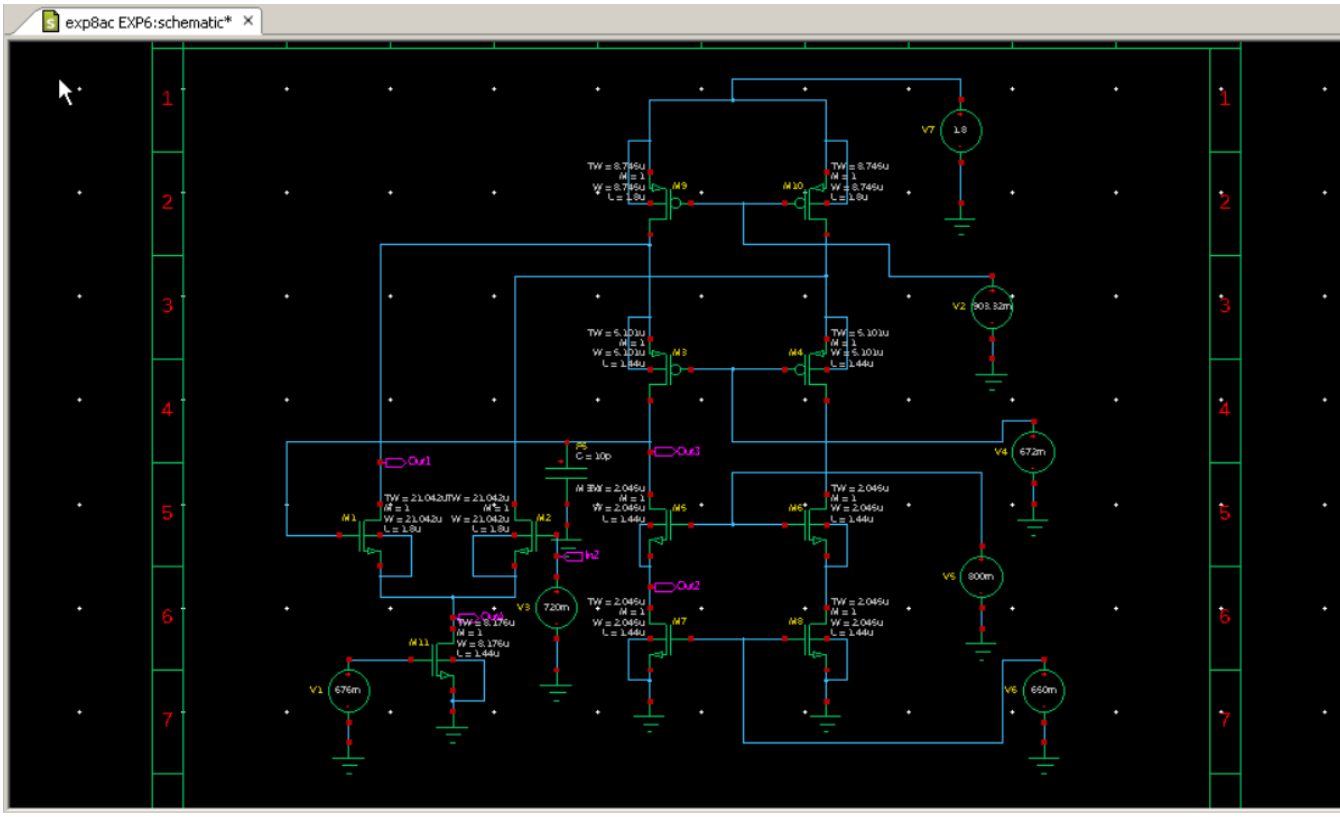


Figure 7: Schematic

We used the inverted terminal and the unity feed back to compute the PSRR.At the non-inverting terminal, we added the dc bias voltage.which result in NMOS.Next, we must use the AC source at the VDD and take the PSRR will be obtained from the output.

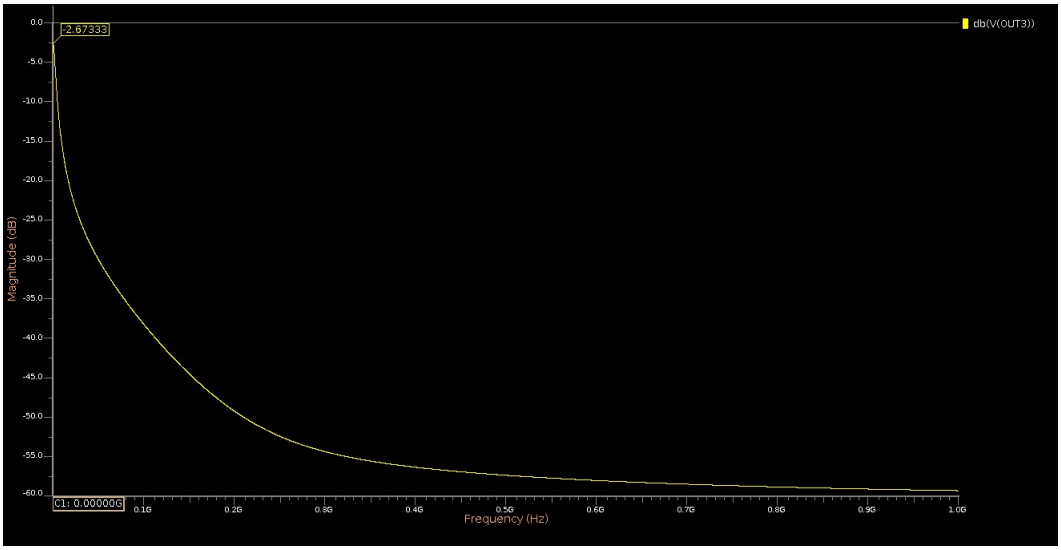


Figure 8: Output waves for the PSRR

7.4 AC Observations:

From the graph we got gain of the designed telescope amplifier is

$$A_v = 64.94dB \tag{34}$$

at the 3dB freq we got

$$bandwidth = 0.001MHz \tag{35}$$

then the gain band width product is given by the

$$GBW = 2.48Mhz$$

and the phase magin is given as

$$Phasemargin = 86.6$$

and the common mode gain is little higher than what we expected as this is because of the technology that we are using

$$ACM = 46.12dB \tag{36}$$

and the PSRR value is given as

$$PSRR = -2.67dB$$

8 Tranient Analysis:

8.1 ICMR and OCMR

Since we are using the unit gain amplifier concept, ICMR A and OCMR are the same.Thus, at the non-inverting terminal, we have applied the DC sweep and provided the negative feed back.after which the output must be examined.It is linear within the ICMR and OCMR input ranges up to a certain point.

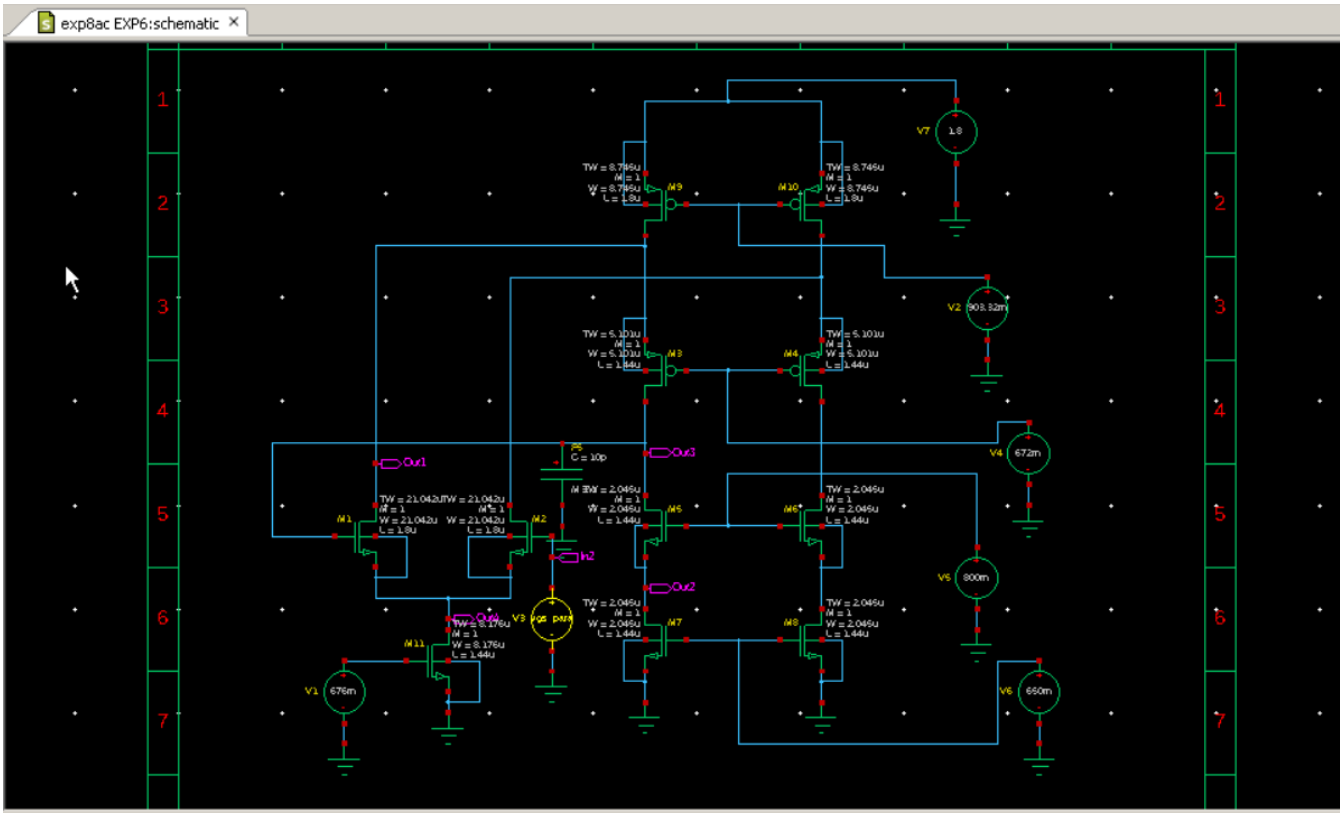


Figure 9: schemtic for ICMR

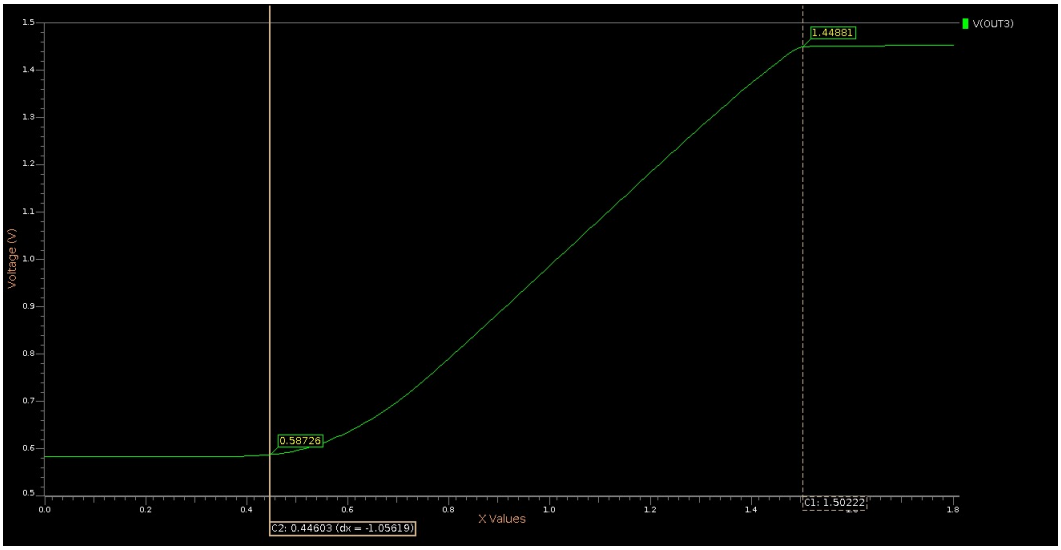


Figure 10: output wave for for ICMR

From the above

$$ICMR_{min} = 0.44 \tag{37}$$

$$ICMR_{max} = 1.50 \tag{38}$$

$$OCMR_{max} = 1.44 \tag{39}$$

$$ICMR_{min} = 0.58 \tag{40}$$

8.2 SLEW rate:

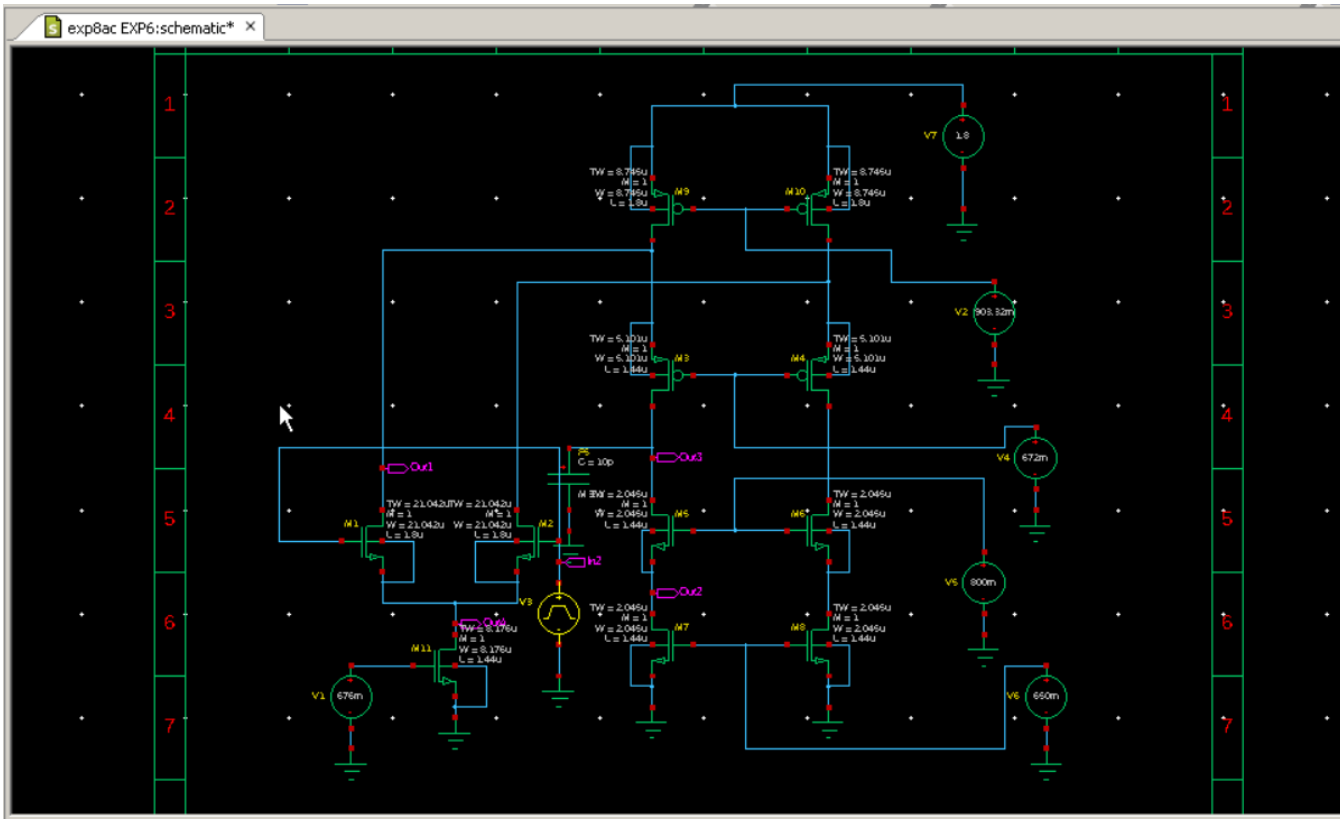


Figure 11: Schematic for slew rate

we realize slew rate will be ,when entire current going through one side.so I have given one side information zero volts .so presently entire current going through one side .we got greatest current.

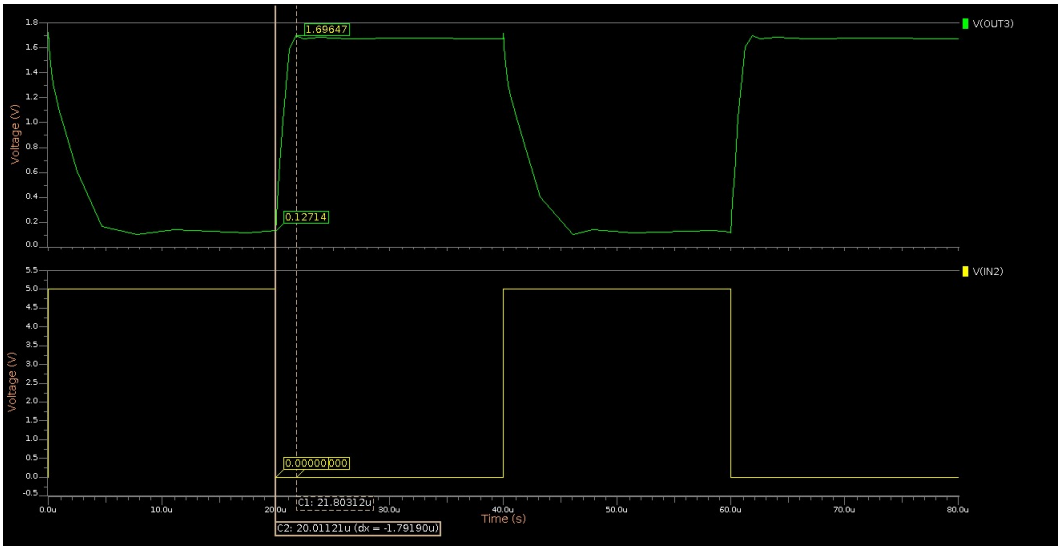


Figure 12: outputwave for for slew rate

$$Slewrate = 0.868\frac{V}{\mu s} \tag{41}$$

9 Results

9.1 W/L Ratios:

transistor	Aspect ratios	Width(meters)	Length
M11	5.8	1440 nm	8176nm
M1	11.7	1800 nm	21040nm
M2	11.7	1800 nm	21040nm
M3	3.7	1440 nm	5240nm
M4	3.7	1440 nm	5240nm
M5	1.5	1440 um	2103nm
M6	1.5	1440 um	2103nm
M7	1.5	1440 um	2103nm
M8	1.5	1440 um	2103nm
M9	4.9	1800 nm	8745nm
M10	4.9	1800 nm	8745nm

9.2 Bias voltages and Currents of transistors:

transistor	V_G	V_{GS}	V_{DS}	I_D
M11	0.67v	0.67v	0.18v	41.5μ A
M1	0.7v	0.52v	1.2v	20.7μA
M2	0.7v	0.52v	1.2v	20.7μA
M3	0.6v	-0.71v	-0.488v	8.5 μA
M4	0.6v	-0.71v	-0.488v	8.5 μA
M5	0.8v	0.63v	0.712v	8.5 μA
M6	0.8	0.63v	0.712v	8.5 μA
M7	0.65v	0.65v	0.162v	8.5 μA
M8	0.65v	0.65v	0.162v	8.5 μA
M9	0.9v	-0.89 v	-0.414v	-29.1μA
M10	0.9v	-0.89v	-0.414v	-29.1μA

9.3 AC analysis Results

Variable	practicalvalue
gain	64.94dB
bandwidth	0.001Mhz
GBW	2.48MHz
PM	82.79
CMRR	18.82dB
PSRR	-2.67dB

9.4 Transient results:

Variable	theoretical value	practicalvalue
slew rate	≥ 1	0.868 $\frac{V}{\mu s}$

Variable	max value	min value
ICMR	1.5	0.44
OCMR	1.44	0.58

10 CONCLUSION:

- Here in this report we designed and implemented DIFFERENTIAL folded cascode amplifier for high swing and high gain.
- Here we are generally taking high length and width because for the given voltage 1.8 we need to design the circuit by only changing length if we have the voltage above 2.5 then we can change the over drive voltage and we can design the circuit accordinglyy.
- We will get good CMRR and High OCMR because ,due to high current we have the very less resistance at the tail current MOSFET.
- Here in this case the pwer consumption is more becauese the number of transiors are more in Differntial cascode..

- All the above results obtained are measured theoretically and are matched with the practical values.