CS 226: Course Project

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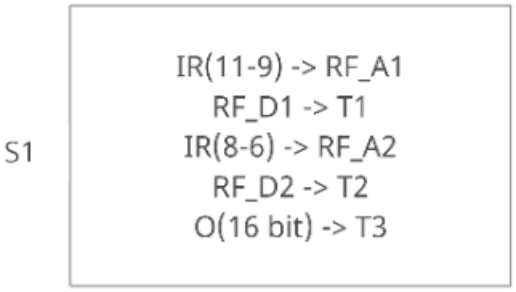
Contents

Data Paths

S0

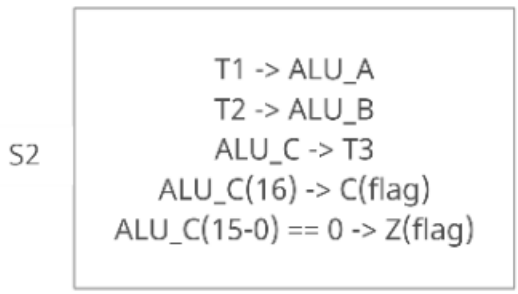
Control pins:
Register 3 write (IR)
MUX 2 select 01

S1



Control pins:
Register 5 write (T1)
Register 6 write (T2)
Register 7 write (T3)
MUX 6 select 01
MUX 7 select 01
MUX 8 select 0

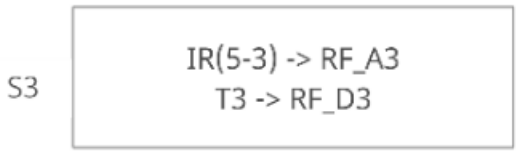
S2



Control pins:
Register 5 write (T1)

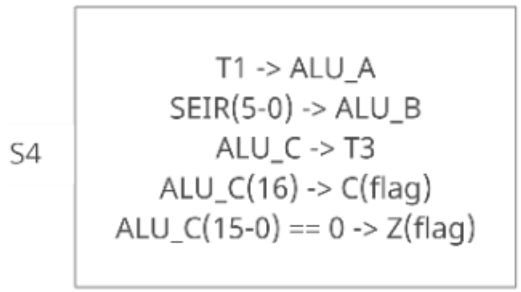
MUX 6 select 10
MUX 9 select 10
MUX 10 select 10
if (op_code is "0000") then alu_control is 0, carry write, zero write
else alu_control is 1, zero write

S3



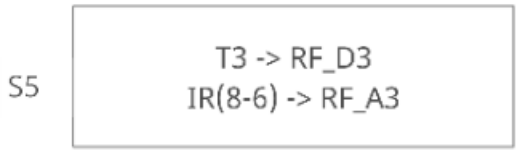
Control pins:
Register 4 write (RF)
MUX 3 select 10
MUX 5 select 11

S4



Control pins:
Register 5 write (T1)
MUX 6 select 10
MUX 9 select 01
MUX 10 select 10
carry write, zero write

S5

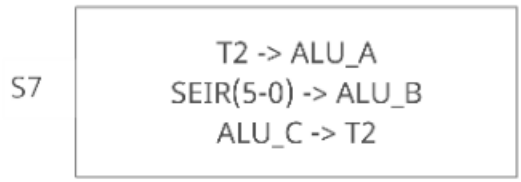


Control pins:
Register 4 write (RF)
MUX 3 select 10
MUX 5 select 11

S6

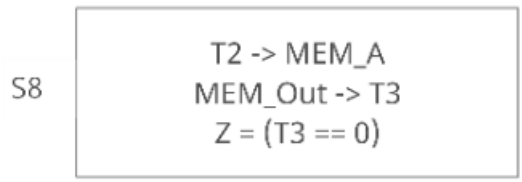
Control pins:
Register 4 write (RF)
MUX 3 select 00
MUX 5 select 01

S7



Control pins:
Register 6 write (T2)
MUX 7 select 10
MUX 9 select 01
MUX 10 select 11

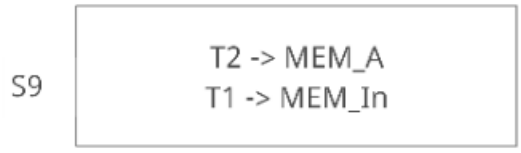
S8



Control pins:
Register 5 write (T1)
MUX 2 select 00
MUX 6 select 00

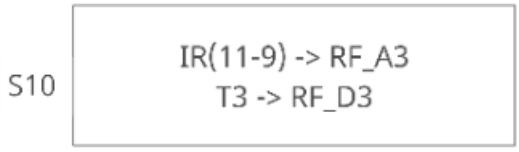
MUX 11 select 1
zero write

S9



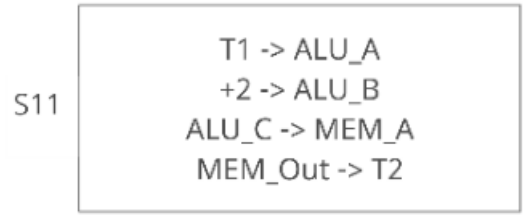
Control pins:
Register 2 write (MEM)
MUX 2 select 00

S10



Control pins:
Register 4 write (RF)
MUX 3 select 00
MUX 5 select 11

S11

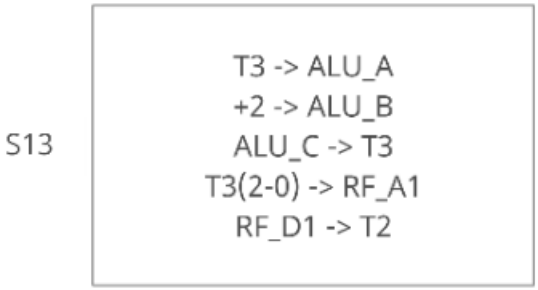


Control pins:
Register 6 write (T2)
Register 7 write (T3)
MUX 2 select 11
MUX 7 select 11
MUX 8 select 1
MUX 9 select 11
MUX 10 select 01

S12

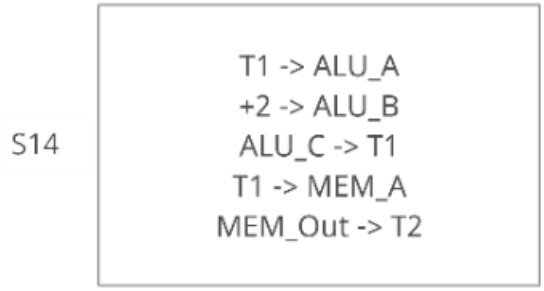
Control pins:
Register 4 write (RF)
Register 5 write (T1)
MUX 3 select 11
MUX 5 select 10
MUX 6 select 10
MUX 9 select 11
MUX 10 select 00

S13



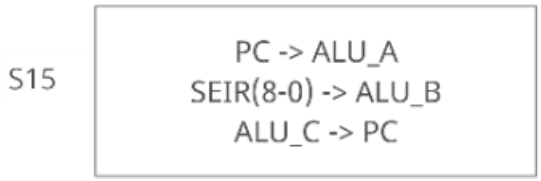
Control pins:
Register 5 write (T1)
Register 6 write (T2)
MUX 4 select 1
MUX 6 select 10
MUX 7 select 00
MUX 9 select 11
MUX 10 select 00

S14



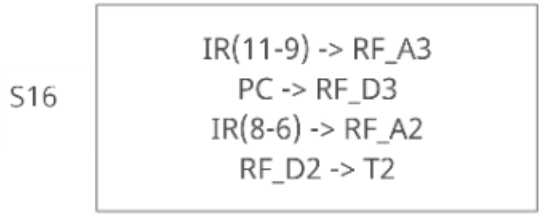
Control pins:
Register 2 write (MEM)
Register 7 write (T3)
MUX 2 select 11
MUX 8 select 1
MUX 9 select 11
MUX 10 select 10
MUX 12 select 1

S15



Control pins:
Register 1 write (PC)
MUX 1 select 0
MUX 9 select 00
MUX 10 select 01

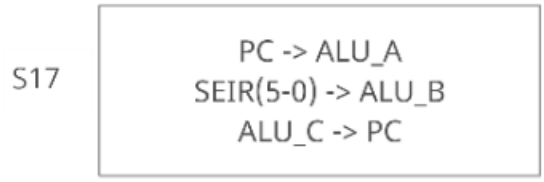
S16



Control pins:
Register 4 write (RF)

Register 6 write (T2)
MUX 3 select 00
MUX 5 select 00
MUX 7 select 01

S17

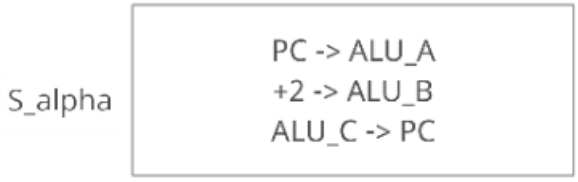


Control pins:
Register 1 write (PC)
MUX 1 select 0
MUX 9 select 01
MUX 10 select 01

S18

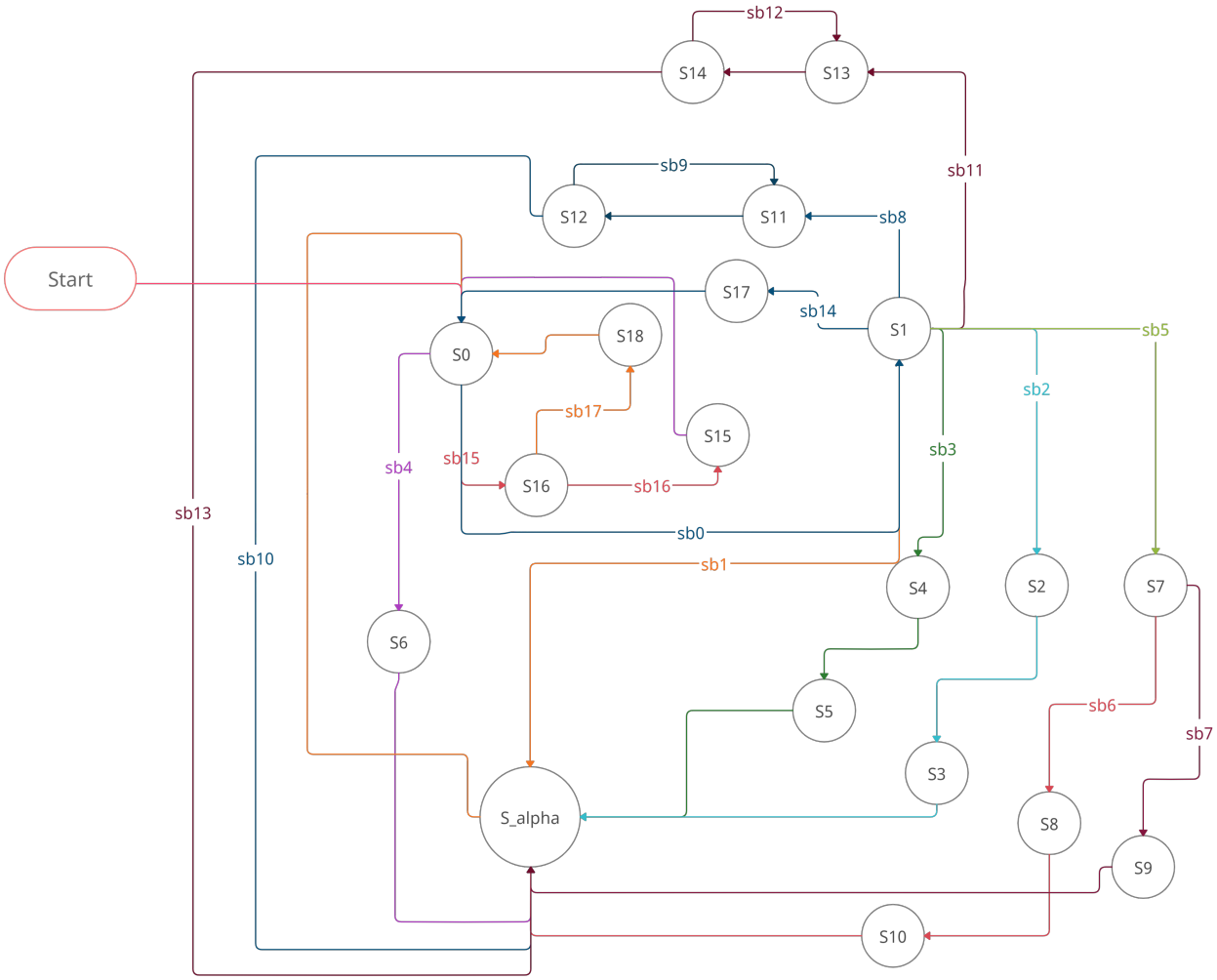
Control pins:
Register 1 write (PC)
MUX 1 select 1

S_α



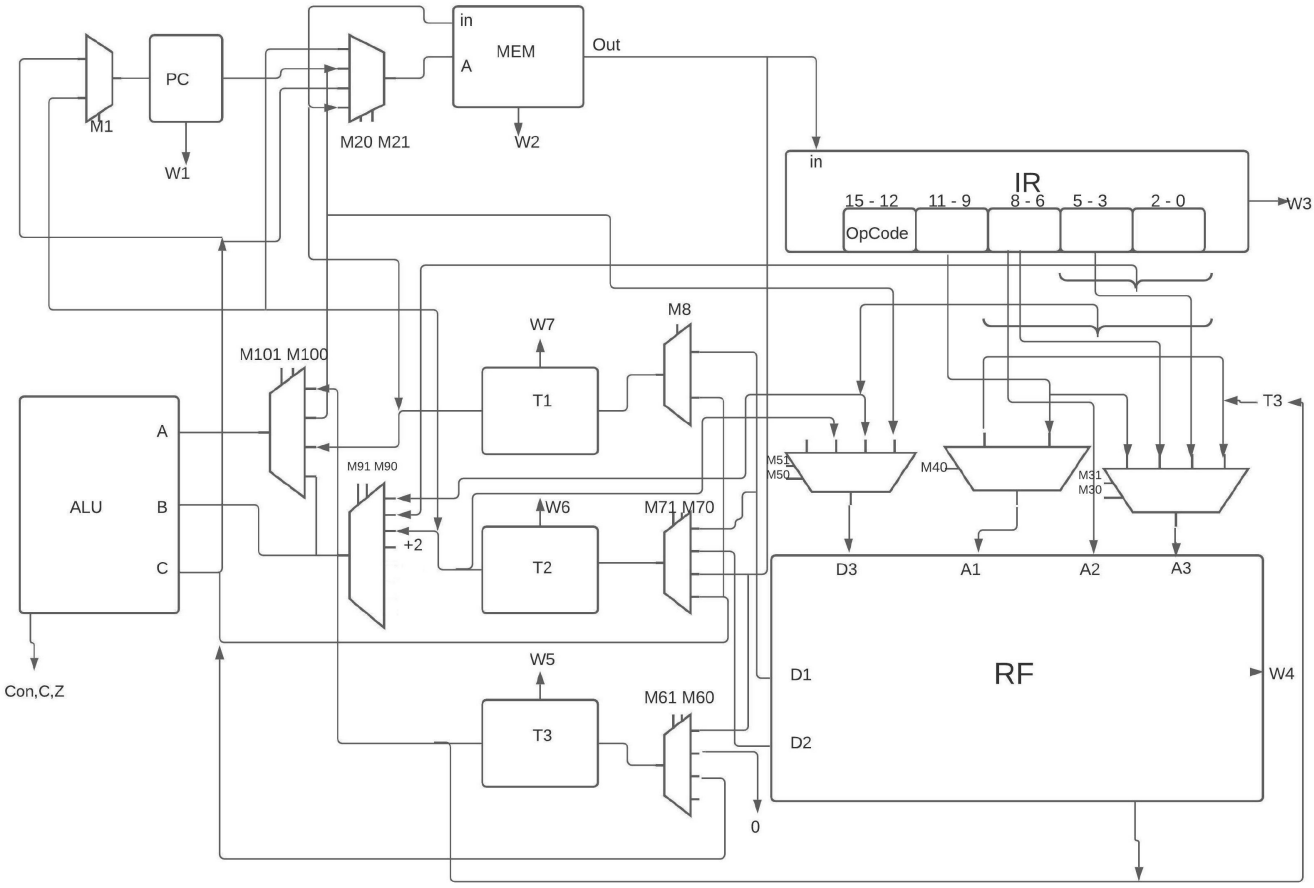
Control pins:
Register 1 write (PC)
MUX 1 select 0
MUX 9 select 11
MUX 10 select 01

State Transition Diagram

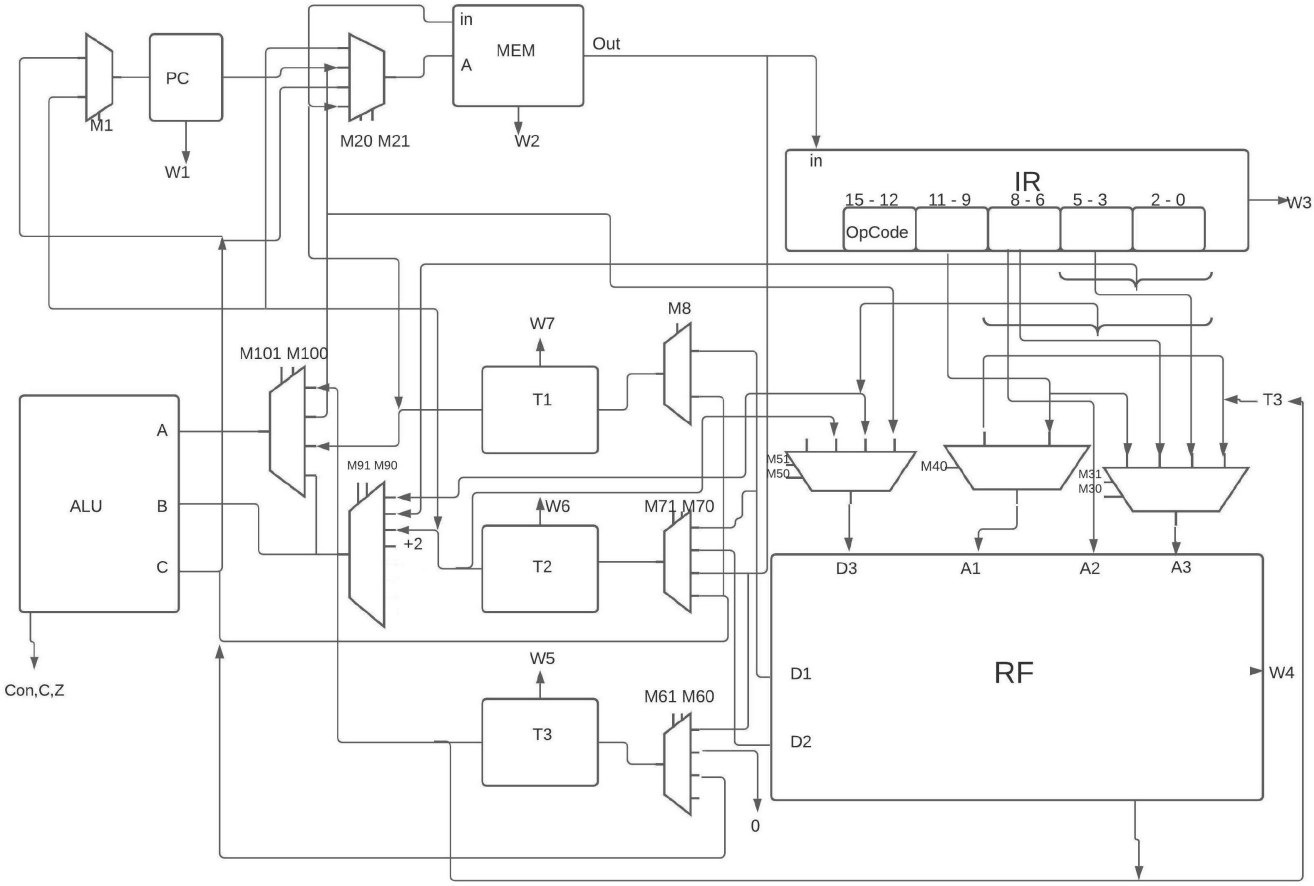


Edge labels:
`sb0`: OpCode is not (0011 or 1000 or 1001);
`sb1`: [OpCode is (0000 or 0010) with (last two bits are 01 and carry flag unset) or (last two bits are 10 and zero flag unset)] or [OpCode is 1100 with RF_D1 != RF_D2];
`sb2`: [OpCode is (0000 or 0010) with (last two bits are 01 and carry flag set) or (last two bits are 10 and zero flag set) or (last two bits are 00)];
`sb3`: OpCode is 0001;
`sb4`: OpCode is 0011;
`sb5`: OpCode is (0100 or 0101);
`sb6`: OpCode is 0100; `sb7`: OpCode is 0101;
`sb8`: OpCode is 0110;
`sb9`: T3(2-0) is not 111; `sb10`: T3(2-0) is 111;
`sb11`: OpCode is 0111;
`sb12`: T3(2-0) is not 111; `sb13`: T3(2-0) is 111;
`sb14`: OpCode is 1100 with RF_D1 == RF_D2;
`sb15`: OpCode is (1000 or 1001);
`sb16`: OpCode is 1000; `sb17`: OpCode is 1001;

Circuit Diagram



RTL Viewer


in
MEM
A
Out
PC
M1
W1
M20 M21
W2
in
IR
15 - 12
11 - 9
8 - 6
5 - 3
2 - 0
OpCode
W3
W7
M8
M101 M100
T1
T3
A
ALU
B
C
M91 M90
+2
W6
M71 M70
T2
M51
M50
M40
M31
M30
D3
A1
A2
A3
W5
M61 M60
T3
D1
RF
W4
D2
Con,C,Z
0

State Machine Viewer