CS 226: Course Project

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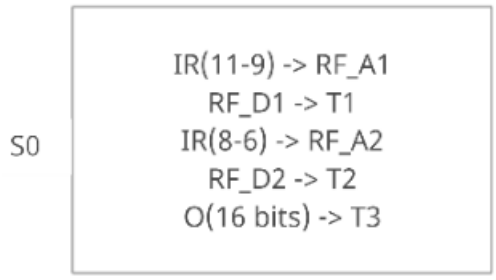
Contents

Data Paths

Si

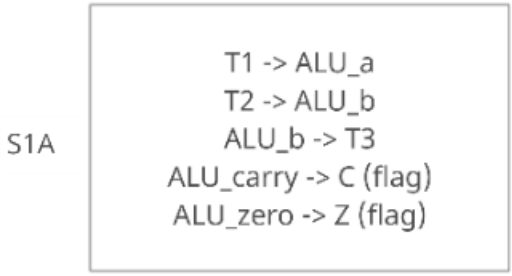
Control pins:
Register IR write
MUX 2 select 01

S0



Control pins:
Register T1 write
Register T2 write
Register T3 write
MUX 6 select 0
MUX 7 select 01
MUX 8 select 01

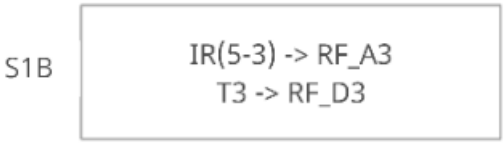
S1A



Control pins:

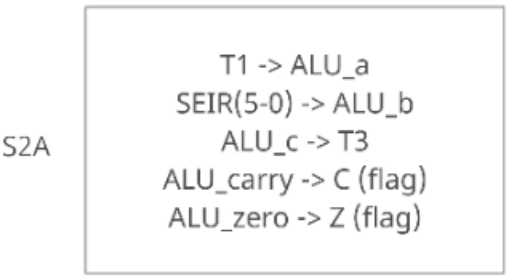
Register T3 write
MUX 8 select 10
MUX 9 select 10
MUX 10 select 10
if (op_code is "0000") then alu_control is 0, carry write, zero write
else alu_control is 1, zero write

S1B



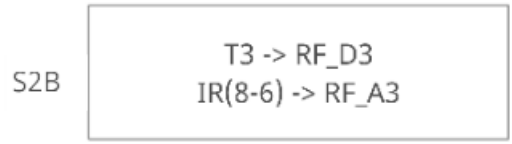
Control pins:
Register RF write
MUX 4 select 10
MUX 5 select 11

S2A



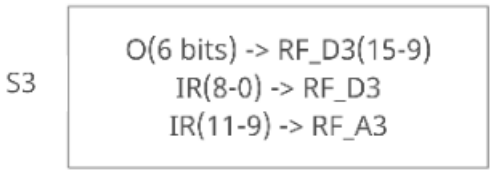
Control pins:
Register T3 write
MUX 6 select 10
MUX 9 select 01
MUX 10 select 10
carry write, zero write

S2B



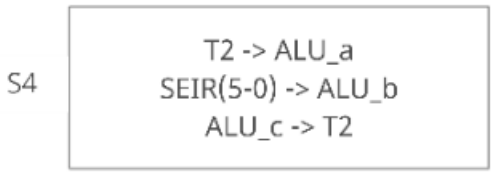
Control pins:
Register RF write
MUX 4 select 10
MUX 5 select 11

S3



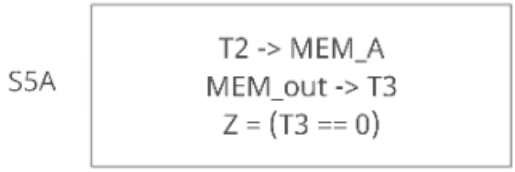
Control pins:
Register RF write
MUX 4 select 00
MUX 5 select 01

S4



Control pins:
Register T2 write
MUX 7 select 10
MUX 9 select 01
MUX 10 select 11

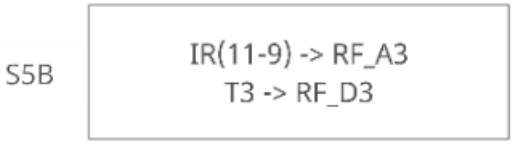
S5A



Control pins:
Register T3 write

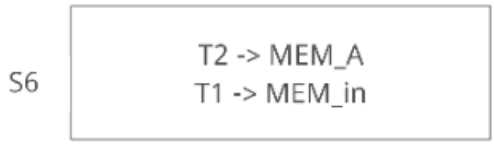
MUX 2 select 00
MUX 8 select 00
MUX 11 select 1
zero write

S5B



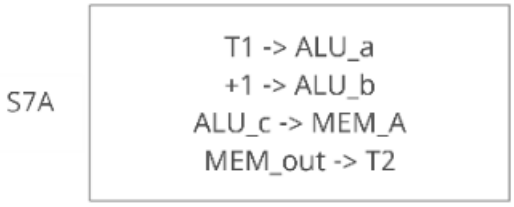
Control pins:
Register RF write
MUX 4 select 00
MUX 5 select 11

S6



Control pins:
Register MEM write
MUX 2 select 00

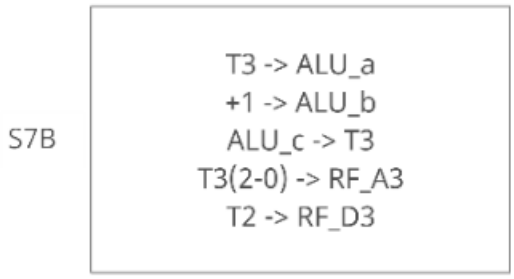
S7A



Control pins:
Register T1 write
Register T2 write
MUX 2 select 11

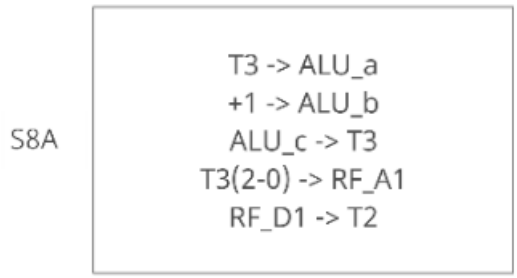
MUX 6 select 1
MUX 7 select 11
MUX 9 select 11
MUX 10 select 01

S7B



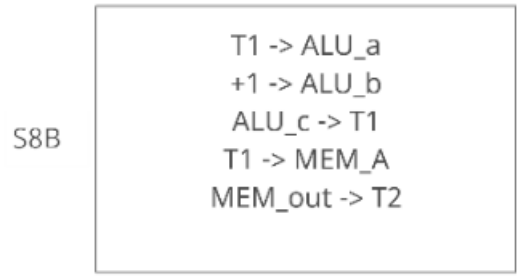
Control pins:
Register RF write
Register T3 write
MUX 4 select 11
MUX 5 select 10
MUX 8 select 10
MUX 9 select 11
MUX 10 select 00

S8A



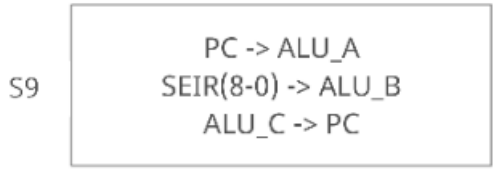
Control pins:
Register T2 write
Register T3 write
MUX 3 select 1
MUX 7 select 00
MUX 8 select 10
MUX 9 select 11
MUX 10 select 00

S8B



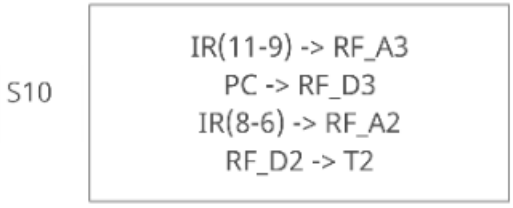
Control pins:
Register MEM write
Register T1 write
MUX 2 select 11
MUX 6 select 1
MUX 9 select 11
MUX 10 select 10
MUX 12 select 1

S9



Control pins:
Register PC write
MUX 1 select 0
MUX 9 select 01
MUX 10 select 01

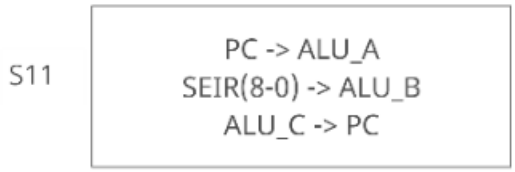
S10



Control pins:

Register RF write
Register T2 write
MUX 4 select 00
MUX 5 select 00
MUX 7 select 01

S11

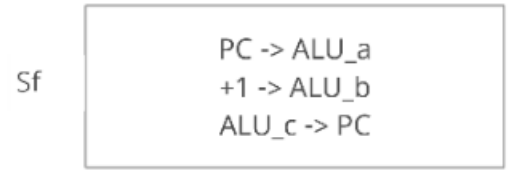


Control pins:
Register PC write
MUX 1 select 0
MUX 9 select 00
MUX 10 select 01

S12

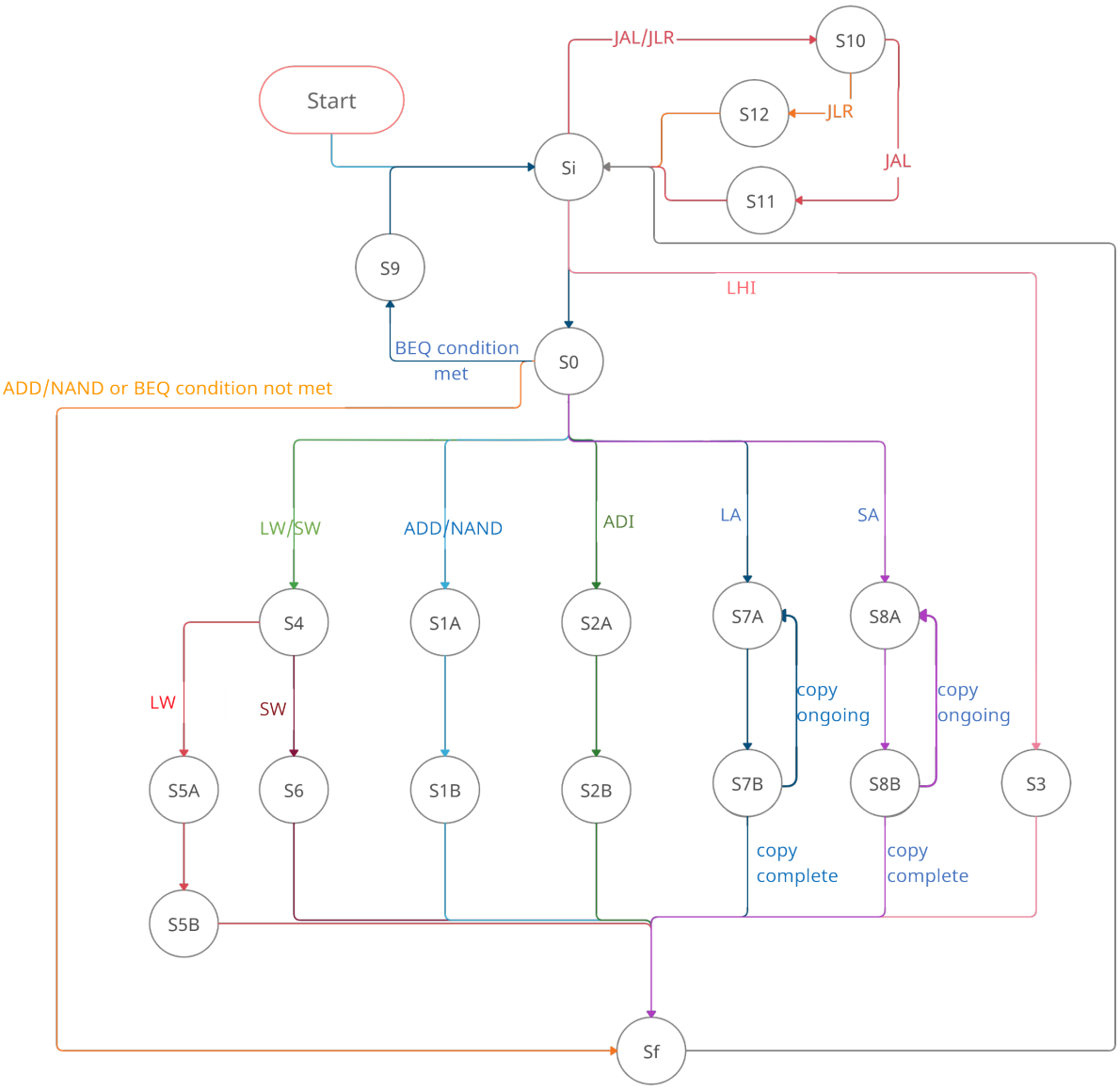
Control pins:
Register PC write
MUX 1 select 1

Sf

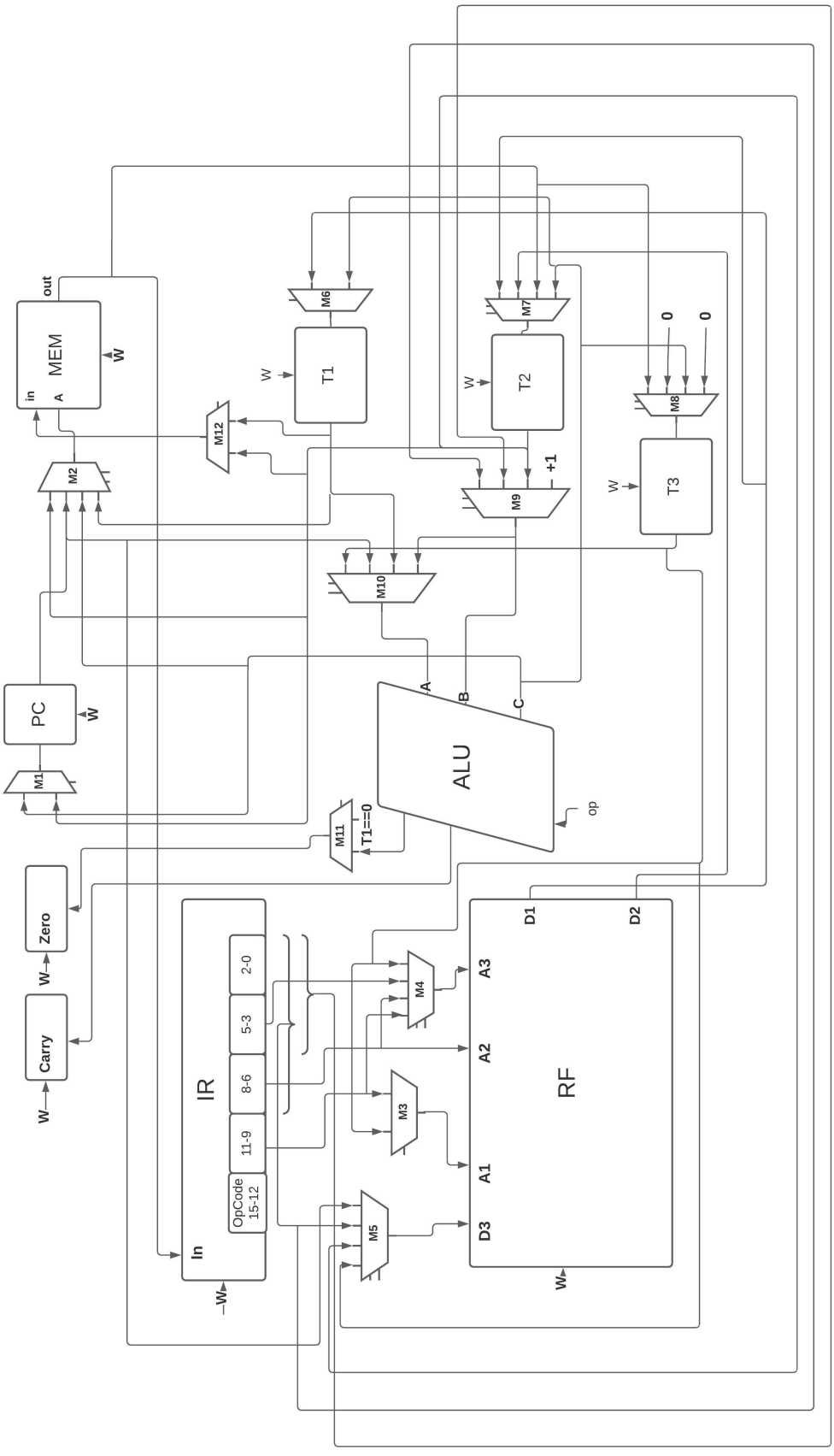


Control pins:
Register PC write
MUX 1 select 0
MUX 9 select 11
MUX 10 select 01

State Transition Diagram



Circuit Diagram



State Machine Viewer