

CS 226: Course Project

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Data Paths

Si

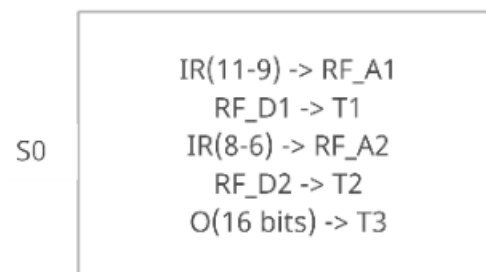


Control pins:

Register IR write

MUX 2 select 01

S0



Control pins:

Register T1 write

Register T2 write

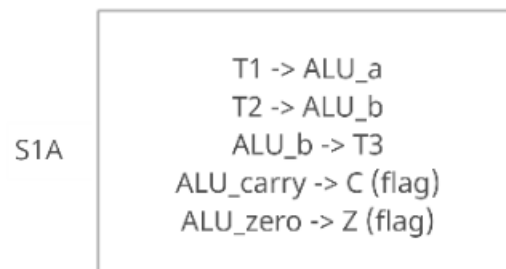
Register T3 write

MUX 6 select 0

MUX 7 select 01

MUX 8 select 01

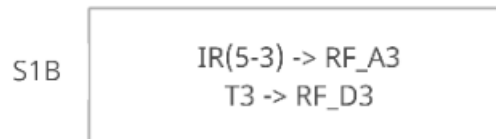
S1A



Control pins:

Register T3 write
 MUX 8 select 10
 MUX 9 select 10
 MUX 10 select 10
 if (op_code is "0000") then alu_control is 0, carry write, zero write
 else alu_control is 1, zero write

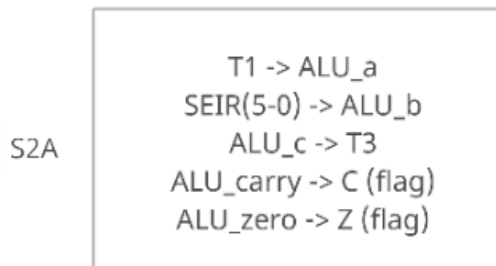
S1B



Control pins:

Register RF write
 MUX 4 select 10
 MUX 5 select 11

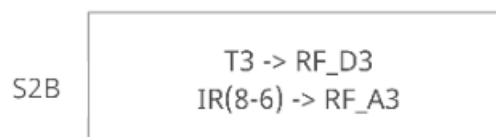
S2A



Control pins:

Register T3 write
 MUX 6 select 10
 MUX 9 select 01
 MUX 10 select 10
 carry write, zero write

S2B



Control pins:

Register RF write

MUX 4 select 10

MUX 5 select 11

S3

S3

O(6 bits) -> RF_D3(15-9)

IR(8-0) -> RF_D3

IR(11-9) -> RF_A3

Control pins:

Register RF write

MUX 4 select 00

MUX 5 select 01

S4

S4

T2 -> ALU_a

SEIR(5-0) -> ALU_b

ALU_c -> T2

Control pins:

Register T2 write

MUX 7 select 10

MUX 9 select 01

MUX 10 select 11

S5A

S5A

T2 -> MEM_A

MEM_out -> T3

 $Z = (T3 == 0)$ **Control pins:**

Register T3 write

MUX 2 select 00
MUX 8 select 00
MUX 11 select 1
zero write

S5B

S5B

IR(11-9) -> RF_A3
T3 -> RF_D3

Control pins:

Register RF write
MUX 4 select 00
MUX 5 select 11

S6

S6

T2 -> MEM_A
T1 -> MEM_in

Control pins:

Register MEM write
MUX 2 select 00

S7A

S7A

T1 -> ALU_a
+1 -> ALU_b
ALU_c -> MEM_A
MEM_out -> T2

Control pins:

Register T1 write
Register T2 write
MUX 2 select 11

MUX 6 select 1
 MUX 7 select 11
 MUX 9 select 11
 MUX 10 select 01

S7B

S7B

T3 -> ALU_a
 +1 -> ALU_b
 ALU_c -> T3
 T3(2-0) -> RF_A3
 T2 -> RF_D3

Control pins:

Register RF write
 Register T3 write
 MUX 4 select 11
 MUX 5 select 10
 MUX 8 select 10
 MUX 9 select 11
 MUX 10 select 00

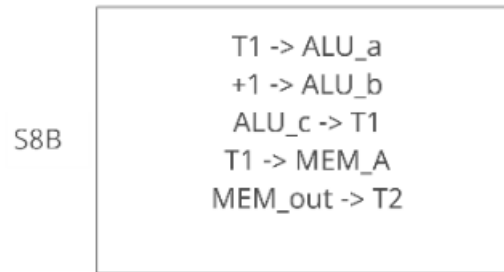
S8A

S8A

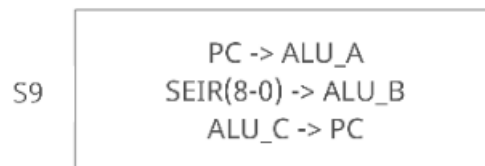
T3 -> ALU_a
 +1 -> ALU_b
 ALU_c -> T3
 T3(2-0) -> RF_A1
 RF_D1 -> T2

Control pins:

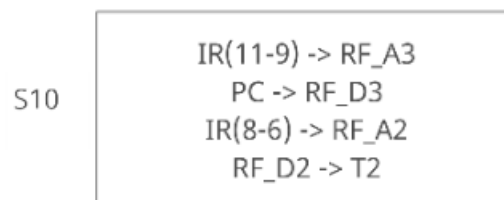
Register T2 write
 Register T3 write
 MUX 3 select 1
 MUX 7 select 00
 MUX 8 select 10
 MUX 9 select 11
 MUX 10 select 00

S8B**Control pins:**

Register MEM write
 Register T1 write
 MUX 2 select 11
 MUX 6 select 1
 MUX 9 select 11
 MUX 10 select 10
 MUX 12 select 1

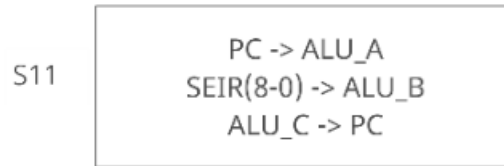
S9**Control pins:**

Register PC write
 MUX 1 select 0
 MUX 9 select 01
 MUX 10 select 01

S10**Control pins:**

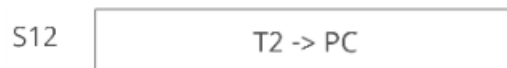
Register RF write
 Register T2 write
 MUX 4 select 00
 MUX 5 select 00
 MUX 7 select 01

S11



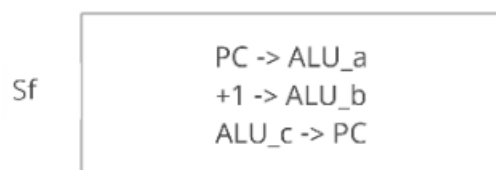
Control pins:
 Register PC write
 MUX 1 select 0
 MUX 9 select 00
 MUX 10 select 01

S12



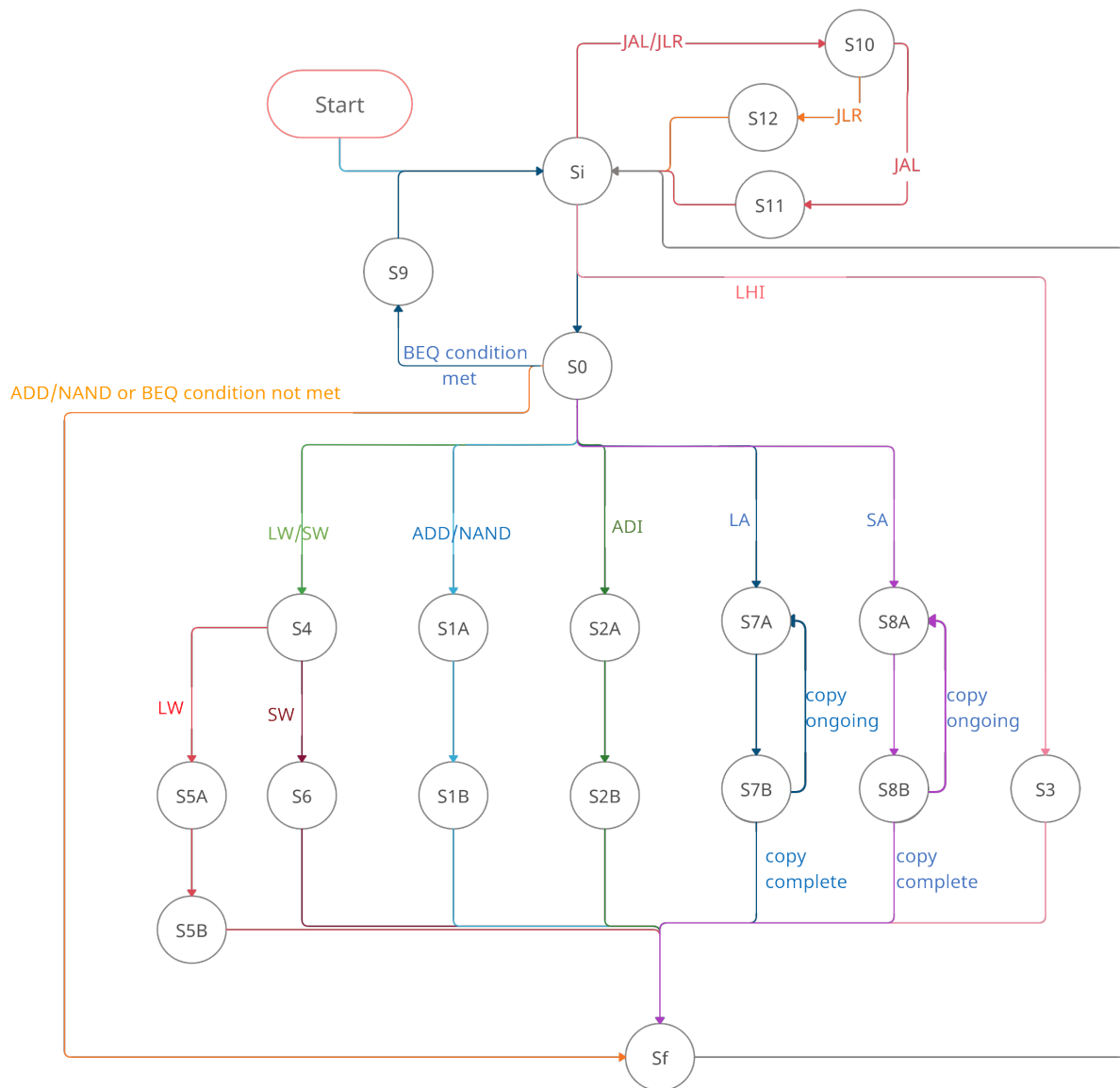
Control pins:
 Register PC write
 MUX 1 select 1

Sf

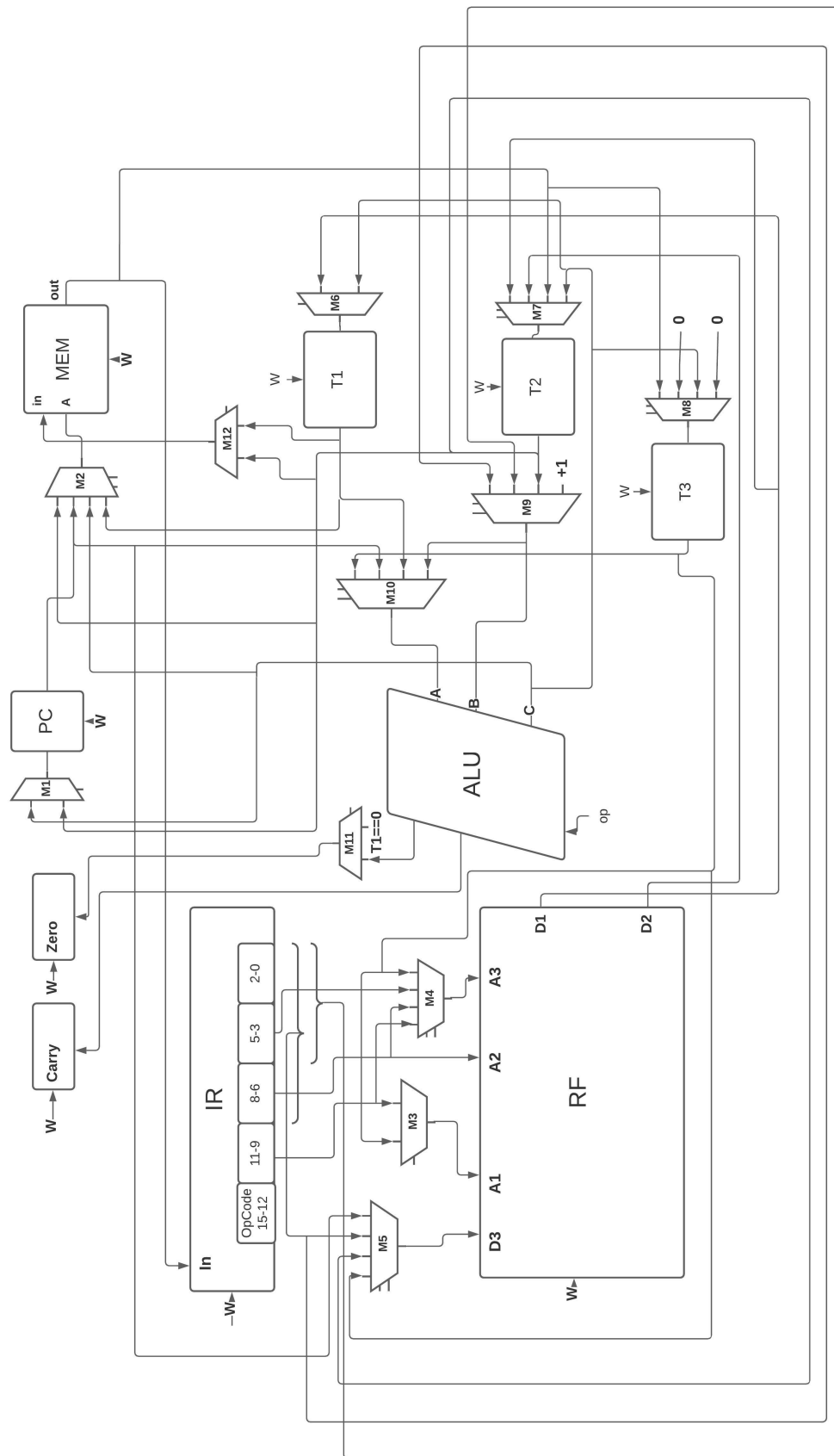


Control pins:
 Register PC write
 MUX 1 select 0
 MUX 9 select 11
 MUX 10 select 01

State Transition Diagram



Circuit Diagram



State Machine Viewer

