

# CS 226: Course Project

Ankit Kumar Misra	Devansh Jain	Harshit Varma	Richeek Das
190050020	190100044	190100055	190260036

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## Contents

<b>Data Paths</b>	<b>1</b>
<b>State Transition Diagram</b>	<b>8</b>
<b>Circuit Diagram</b>	<b>9</b>
<b>State Machine Viewer</b>	<b>10</b>

## Data Paths

Si

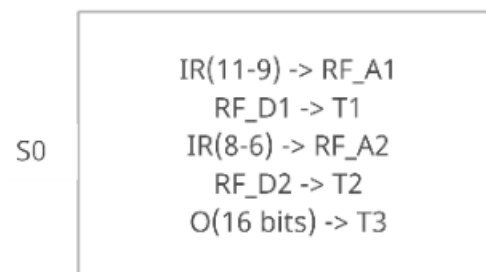


### Control pins:

Register IR write

MUX 2 select 01

S0



### Control pins:

Register T1 write

Register T2 write

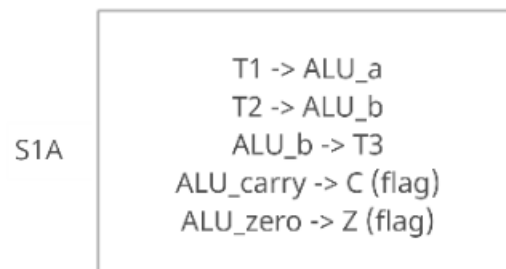
Register T3 write

MUX 6 select 0

MUX 7 select 01

MUX 8 select 01

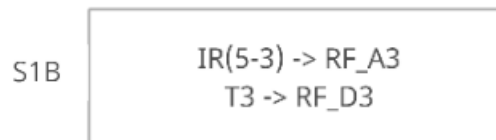
S1A



### Control pins:

Register T3 write  
 MUX 8 select 10  
 MUX 9 select 10  
 MUX 10 select 10  
 if (op\_code is "0000") then alu\_control is 0, carry write, zero write  
 else alu\_control is 1, zero write

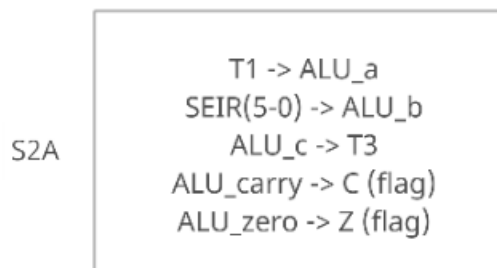
### S1B



#### Control pins:

Register RF write  
 MUX 4 select 10  
 MUX 5 select 11

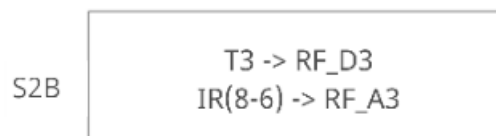
### S2A



#### Control pins:

Register T3 write  
 MUX 6 select 10  
 MUX 9 select 01  
 MUX 10 select 10  
 carry write, zero write

### S2B



**Control pins:**

Register RF write  
MUX 4 select 10  
MUX 5 select 11

**S3**

S3

O(6 bits) -> RF\_D3(15-9)  
IR(8-0) -> RF\_D3  
IR(11-9) -> RF\_A3

**Control pins:**

Register RF write  
MUX 4 select 00  
MUX 5 select 01

**S4**

S4

T2 -> ALU\_a  
SEIR(5-0) -> ALU\_b  
ALU\_c -> T2

**Control pins:**

Register T2 write  
MUX 7 select 10  
MUX 9 select 01  
MUX 10 select 11

**S5A**

S5A

T2 -> MEM\_A  
MEM\_out -> T3  
Z = (T3 == 0)

**Control pins:**

Register T3 write

MUX 2 select 00  
MUX 8 select 00  
MUX 11 select 1  
zero write

### S5B

S5B

IR(11-9) -> RF\_A3  
T3 -> RF\_D3

#### Control pins:

Register RF write  
MUX 4 select 00  
MUX 5 select 11

### S6

S6

T2 -> MEM\_A  
T1 -> MEM\_in

#### Control pins:

Register MEM write  
MUX 2 select 00

### S7A

S7A

T1 -> ALU\_a  
+1 -> ALU\_b  
ALU\_c -> MEM\_A  
MEM\_out -> T2

#### Control pins:

Register T1 write  
Register T2 write  
MUX 2 select 11

MUX 6 select 1  
 MUX 7 select 11  
 MUX 9 select 11  
 MUX 10 select 01

### S7B

S7B

T3 -> ALU\_a  
 +1 -> ALU\_b  
 ALU\_c -> T3  
 T3(2-0) -> RF\_A3  
 T2 -> RF\_D3

#### Control pins:

Register RF write  
 Register T3 write  
 MUX 4 select 11  
 MUX 5 select 10  
 MUX 8 select 10  
 MUX 9 select 11  
 MUX 10 select 00

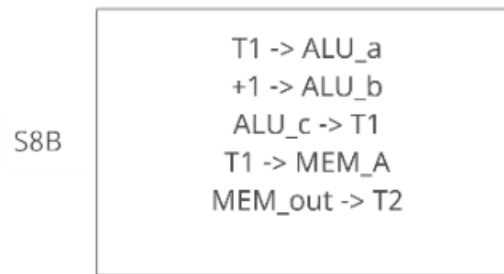
### S8A

S8A

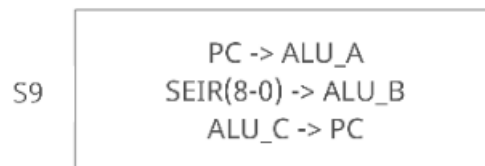
T3 -> ALU\_a  
 +1 -> ALU\_b  
 ALU\_c -> T3  
 T3(2-0) -> RF\_A1  
 RF\_D1 -> T2

#### Control pins:

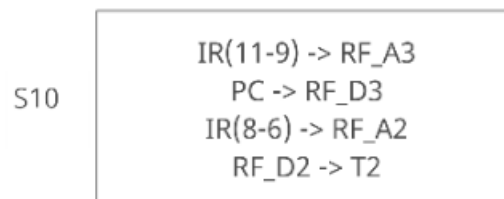
Register T2 write  
 Register T3 write  
 MUX 3 select 1  
 MUX 7 select 00  
 MUX 8 select 10  
 MUX 9 select 11  
 MUX 10 select 00

**S8B****Control pins:**

Register MEM write  
Register T1 write  
MUX 2 select 11  
MUX 6 select 1  
MUX 9 select 11  
MUX 10 select 10  
MUX 12 select 1

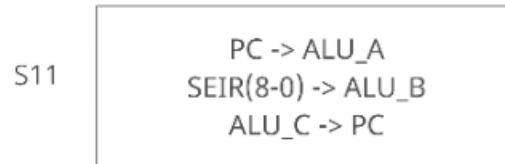
**S9****Control pins:**

Register PC write  
MUX 1 select 0  
MUX 9 select 01  
MUX 10 select 01

**S10****Control pins:**

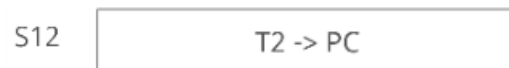
Register RF write  
Register T2 write  
MUX 4 select 00  
MUX 5 select 00  
MUX 7 select 01

### S11



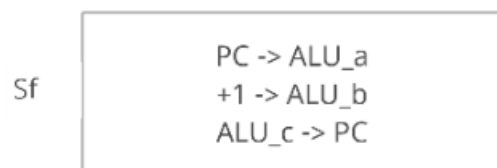
**Control pins:**  
Register PC write  
MUX 1 select 0  
MUX 9 select 00  
MUX 10 select 01

### S12



**Control pins:**  
Register PC write  
MUX 1 select 1

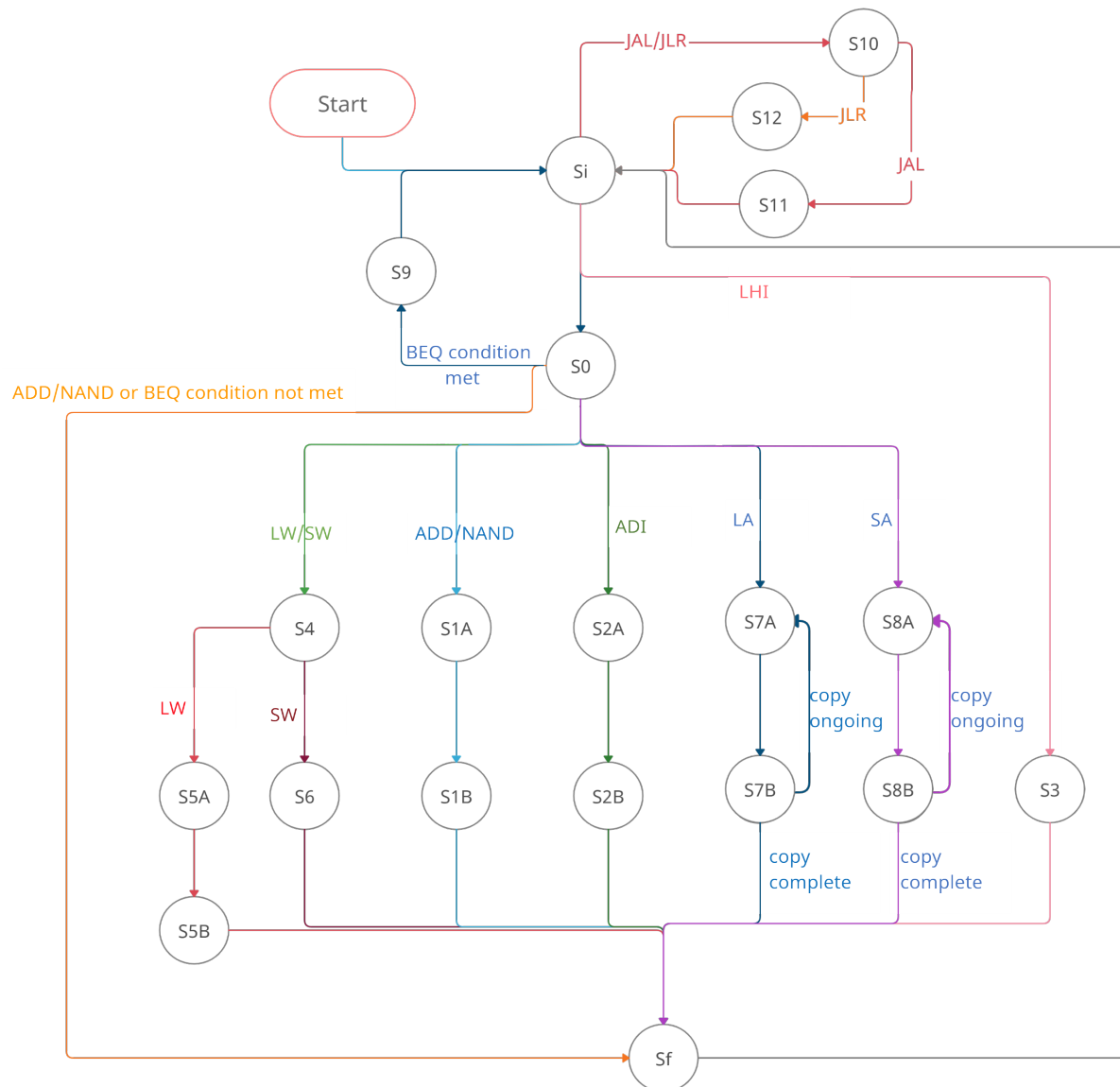
### Sf



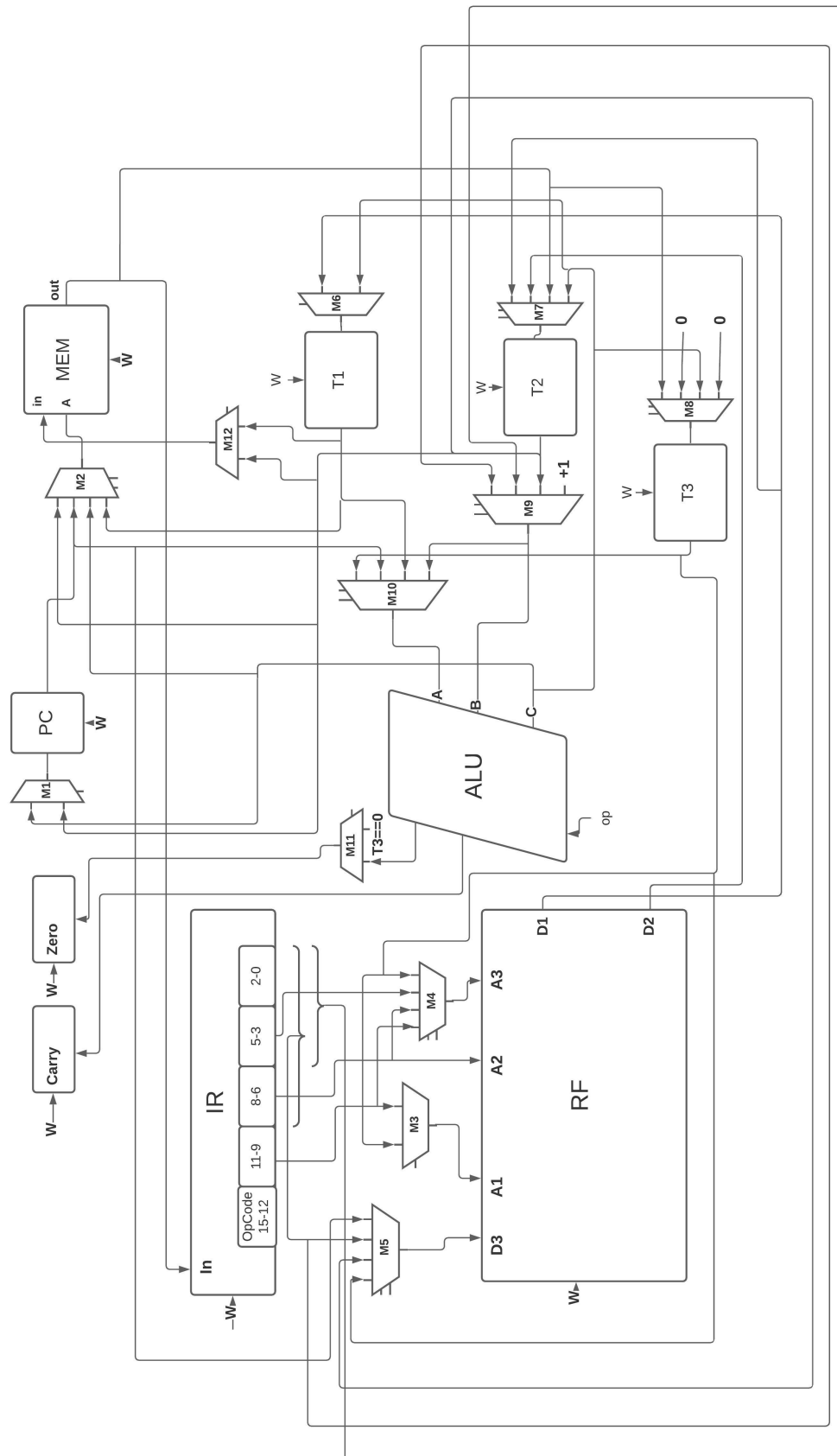
**Control pins:**  
Register PC write  
MUX 1 select 0  
MUX 9 select 11  
MUX 10 select 01



## State Transition Diagram



## Circuit Diagram



## State Machine Viewer

