OPTIMIZED GPU-BASED MATRIX INVERSION

THROUGH THE USE OF THREAD-DATA REMAPPING

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2024-05-31

Introduction

OVERVIEW

- cpu-inverse
 - ► Basic algorithm implementation to prove validity.

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OVERVIEW

cpu-inverse

► Basic algorithm implementation to prove validity.

inverse

- ► GPU implementation written in CUDA.
- ▶ Based on the works of Sharma et al [1] and DasGupta [2].

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inverse

- ► GPU implementation written in CUDA.
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■ tdr-inverse

- Utilizes Thread-Data Remapping (TDR) to more efficiently use the GPU.
- ► Actual TDR implementation is Dr. Cuneo's Harmonize library [3].

INTRODUCTION TO INVERSES

WHAT IS AN INVERSE?

Definition (Inverse)

The <u>inverse</u> of a is some value a^{-1} such that $a \star a^{-1} = i$ where i is the identity of \star .

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- For example, the set and operation (\mathbb{R} , ×) has the identity i = 1 since $1 \times x = x \times 1 = x$ for all $x \in \mathbb{R}$.
- Thus the inverse of a is $\frac{1}{a}$ since $a \times a^{-1} = 1 \rightarrow a = \frac{1}{a}$.
 - Note that this is only true because $a \times b = b \times a$ for all $a, b \in \mathbb{R}$.

USES

$$3x + 2y = 2$$

$$-7x - 5y = 4$$

$$\begin{bmatrix} 3 & 2 \\ -7 & -5 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 2 \\ 4 \end{bmatrix}$$

$$\begin{bmatrix} 3 & 2 \\ -7 & -5 \end{bmatrix}^{-1} \begin{bmatrix} 3 & 2 \\ -7 & -5 \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 3 & 2 \\ -7 & -5 \end{bmatrix}^{-1} \begin{bmatrix} 2 \\ 4 \end{bmatrix}$$

$$I_{2} \begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 5 & 2 \\ -7 & -3 \end{bmatrix} \begin{bmatrix} 2 \\ 4 \end{bmatrix}$$

$$\begin{bmatrix} x \\ y \end{bmatrix} = \begin{bmatrix} 18 \\ -26 \end{bmatrix}$$

METHODS OF MATRIX INVERSION

Definition (Matrix Inverse)

Let A be an
$$n \times n$$
 matrix,
 $AA^{-1} = I = A^{-1}A$

$$A^{-1} = \frac{1}{\det(A)}X$$

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Determinate: $det(\mathbb{R}^{n \times n}) \to \mathbb{R}$

$$\det\begin{pmatrix}\begin{bmatrix} a & b \\ c & d \end{pmatrix}\end{pmatrix} = ad - bc$$

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$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} x_1 & x_2 \\ x_3 & x_4 \end{bmatrix} = \begin{bmatrix} ad - bc & 0 \\ 0 & ad - bc \end{bmatrix}$$

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$$\begin{bmatrix} a & b \end{bmatrix} \begin{bmatrix} d & -b \end{bmatrix} \begin{bmatrix} ad - bc & 0 \\ 0 & ad - bc \end{bmatrix}$$

$$\begin{bmatrix} a & b \\ c & d \end{bmatrix} \begin{bmatrix} d & -b \\ -c & a \end{bmatrix} = \begin{bmatrix} ad - bc & 0 \\ 0 & ad - bc \end{bmatrix}$$

GAUSS-JORDAN METHOD

Augmented Matrix

$$\operatorname{aug}(A) = A | \mathbf{I} = \begin{bmatrix} a & b & 1 & 0 \\ c & d & 0 & 1 \end{bmatrix}$$

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Operations

- 1. Swap any two rows: $swap(R_i, R_j)$
- 2. Multiply any row by a non-zero value: $c \times R_i$
- 3. Add to any row a multiple of another row: $R_i + c \times R_j$

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$$\begin{bmatrix} 3 & 2 & 1 & 0 \\ -7 & -5 & 0 & 1 \end{bmatrix} \xrightarrow{R_1 \leftrightarrow R_2} \begin{bmatrix} -7 & -5 & 0 & 1 \\ 3 & 2 & 1 & 0 \end{bmatrix}$$

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```
Data: M is a matrix with N rows foreach row \ M_i do M_i \leftarrow M_i/M_{ii}; foreach row \ M_j in M where j \neq i do M_j \leftarrow M_j - M_{ji} \times M_i end end
```

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Data: M is a matrix with N rows
foreach row M; do
     M_i \leftarrow M_i/M_{ii};
     foreach row M_i in M where j \neq i do
         M_i \leftarrow M_i - M_{ii} \times M_i
     end
end
            \begin{bmatrix} 3 & 2 & 1 & 0 \\ -7 & -5 & 0 & 1 \end{bmatrix}
```

$$\begin{bmatrix} 3 & 2 & 1 & 0 \\ -7 & -5 & 0 & 1 \end{bmatrix} \xrightarrow{R_1/3} \qquad \begin{bmatrix} \mathbf{1} & 2/3 & 1/3 & \mathbf{0} \\ -7 & -5 & 0 & 1 \end{bmatrix}$$

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```

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end

$$\begin{bmatrix} 3 & 2 & 1 & 0 \\ -7 & -5 & 0 & 1 \end{bmatrix} \xrightarrow{R_1/3} \begin{bmatrix} \mathbf{1} & \mathbf{2/3} & 1/3 & \mathbf{0} \\ -7 & -5 & 0 & 1 \end{bmatrix} \xrightarrow{R_2-(-7)R_1} \begin{bmatrix} 1 & 2/3 & 1/3 & 0 \\ \mathbf{0} & -1/3 & 7/3 & 1 \end{bmatrix}$$
$$\xrightarrow{R_2/-1/3} \begin{bmatrix} 1 & 2/3 & 1/3 & 0 \\ \mathbf{0} & \mathbf{1} & -7 & -3 \end{bmatrix}$$

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$$\xrightarrow{R_2/-1/3} \begin{bmatrix} 1 & 2/3 & 1/3 & 0 \\ \mathbf{0} & \mathbf{1} & -7 & -3 \end{bmatrix} \xrightarrow{R_1-2/3R_2} \begin{bmatrix} \mathbf{1} & \mathbf{0} & \mathbf{5} & \mathbf{2} \\ 0 & 1 & -7 & -3 \end{bmatrix}$$

CLASS ACTIVITY

MATRIX EXAMPLE

$$M = \begin{bmatrix} 1 & 0 & 1 \\ 0 & 2 & 1 \\ 1 & 1 & 1 \end{bmatrix}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}$$

$$\begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 2 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 \end{bmatrix} \xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_2-0R_1}
\xrightarrow{R_3-1R_1}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1/1}$$

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0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_2-0R_1}
\xrightarrow{R_3-1R_1}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}$$

$$\xrightarrow{R_2/2}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0
\end{bmatrix}
\xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_2-0R_1}
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1 & 0 & 1 & 1 & 0 & 0 \\
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\end{bmatrix}$$

$$\xrightarrow{R_2/2}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 1/2 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1-0R_2}
\xrightarrow{R_3-1R_2}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 0 & 1/2 & 0 \\
0 & 0 & -1/2 & -1 & -1/2 & 1
\end{bmatrix}$$

SOLUTION

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
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\end{bmatrix}
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1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
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\end{bmatrix}$$

$$\xrightarrow{R_2/2}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
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0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1-0R_2}
\xrightarrow{R_3-1R_2}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 1/2 & 0 \\
0 & 0 & -1/2 & 1
\end{bmatrix}$$

$$\xrightarrow{R_3/-1/2}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 1/2 & 0 \\
0 & 0 & 1 & 2 & 1 & -2
\end{bmatrix}$$

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SOLUTION

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1/1}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
1 & 1 & 1 & 0 & 0 & 1
\end{bmatrix}
\xrightarrow{R_2-0R_1}
\xrightarrow{R_3-1R_1}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 2 & 1 & 0 & 1 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}$$

$$\xrightarrow{R_2/2}$$

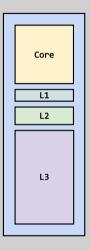
$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 1/2 & 0 \\
0 & 1 & 0 & -1 & 0 & 1
\end{bmatrix}
\xrightarrow{R_1-0R_2}
\xrightarrow{R_3-1R_2}
\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
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\end{bmatrix}$$

$$\xrightarrow{R_3/-1/2}$$

$$\begin{bmatrix}
1 & 0 & 1 & 1 & 0 & 0 \\
0 & 1 & 1/2 & 0 & 1/2 & 0 \\
0 & 0 & 1 & 2 & 1 & -2
\end{bmatrix}
\xrightarrow{R_1-1R_3}
\xrightarrow{R_2-1/2R_3}
\begin{bmatrix}
1 & 0 & 0 & -1 & -1 & 2 \\
0 & 1 & 0 & -1 & 0 & 1 \\
0 & 0 & 1 & 2 & 1 & -2
\end{bmatrix}$$

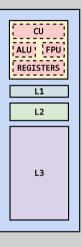
GPU PROGRAMMING

CPU ARCHITECTURE



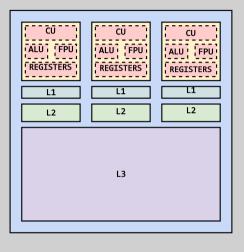
- Core
 - ► Processing unit
- L1 L2 L3
 - ► Caches for storing work

CPU ARCHITECTURE



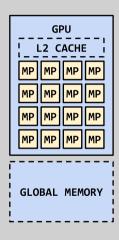
- Registers
 - Store localized data including the fetched instruction
- Control Unit (CU)
 - Decodes instruction and sends to appropriate logic unit
- Arithmetic Logic Unit (ALU) / Floating Point Unit (FPU)
 - ► Executes given instruction

CPU ARCHITECTURE



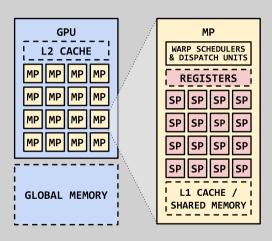
- Registers
 - Store localized data including the fetched instruction
- Control Unit (CU)
 - Decodes instruction and sends to appropriate logic unit
- Arithmetic Logic Unit (ALU) / Floating Point Unit (FPU)
 - ► Executes given instruction
- Each core has its own registers and control logic

SIMT ARCHITECTURE



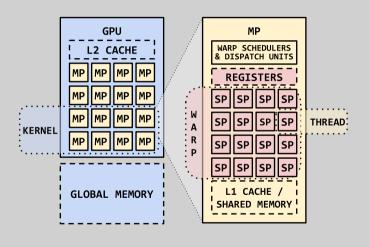
- Multiprocessor (MP)
 - ► A "core" that handles simultaneous execution of a vector of tasks

SIMT ARCHITECTURE



- Multiprocessor (MP)
 - A "core" that handles simultaneous execution of a vector of tasks
- Scalar processor (SP)
 - Executes a single scalar component

SIMT ARCHITECTURE



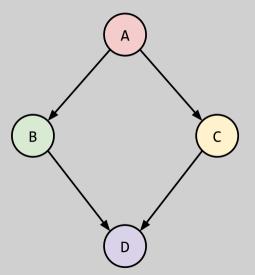
■ Warp

- Group of SPs in a MP that execute in lockstep
- Warps share registers; including the program counter

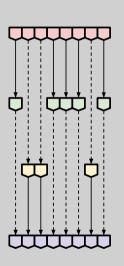
■ Kernel

Group of warps that operate on the same method

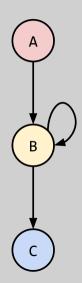
BRANCH DIVERGENCE

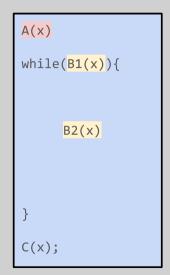


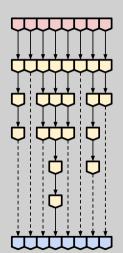
```
bool cond = A(x)
if( cond ){
     B(x);
  else {
     C(x);
D(x);
```



LOOP DIVERGENCE







BASIC CUDA PROGRAM

```
// A special method invoked by the
   // CPU to launch a GPU kernel
    global print(string message) {
       int idx = threadIdx.x:
       int jdx = blockIdx.x;
5
       printf("%s from (%d, %d)\n",
               message, idx, idx):
9
   // Standard C main
   int main() {
       // Call kernel launcher
12
       print<<<2, 4>>>("Hello World");
13
       // Wait for GPU to finish
14
       cudaDeviceSvnchronize():
15
16
```

Output

Hello World from (0, 0) Hello World from (0, 3) Hello World from (1, 2) Hello World from (1, 0) Hello World from (0, 2) Hello World from (1, 1) Hello World from (1, 3) Hello World from (0, 1)

CUDA MATRIX INVERSION: CPU LOOP

```
for (size_t j = 0; j < rows; j++) {
    fixRow<<<1, cols>>>(data_gpu, cols, j);
    auto_throw(cudaDeviceSynchronize());

fixColumn<<<rows, cols>>>(data_gpu, cols, j);
    auto_throw(cudaDeviceSynchronize());
}
```

CUDA MATRIX INVERSION: FIXROW

```
global void fixRow(
       float *matrix, int size, int rowId) {
     // the ith row of the matrix
     shared float Ri[MAX BLOCK SIZE];
     // The diagonal element for ith row
5
     shared float Aii;
     int colId = threadIdx.x:
     Ri[colId] = matrix[size * rowId + colId];
     Aii = matrix[size * rowId + rowId]:
9
10
     syncthreads();
     // Divide the whole row by the diagonal
     Ri[colId] = Ri[colId] / Aii;
13
     matrix[size * rowId + colId] = Ri[colId]:
14
15
```

Example

[1	0	1	1	0	0]
	0				0
1	1	1	0	0	1

¹⁵ 3

CUDA MATRIX INVERSION: FIXCOLUMN

```
global void fixColumn(
       float *matrix, int size, int colId) {
     int i = threadIdx.x, j = blockIdx.x;
     // The colld column
     shared float col[MAX BLOCK SIZE];
5
     // The ith element of the colld row
     __shared__ float AColIdj;
     // The ith column
     __shared__ float colj[MAX_BLOCK_SIZE];
9
     col[i] = matrix[i * size + colId]:
10
     syncthreads();
     colj[i] = matrix[i * size + j];
12
     AColIdj = matrix[colId * size + j];
13
     if (i != colId) {
14
       coli[i] = coli[i] - AColIdi * col[i]:
15
16
     matrix[i * size + i] = coli[i]:
17
18
```

Example

```
\begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 2 & 1 & 0 & 1 & 0 \\ 1 & 1 & 1 & 0 & 0 & 1 \end{bmatrix}
```

IN-PLACE OPTIMIZATION

$$\begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1/2 & 0 & 1/2 & 0 \\ 0 & 0 & -1/2 & -1 & -1/2 & 1 \end{bmatrix}$$

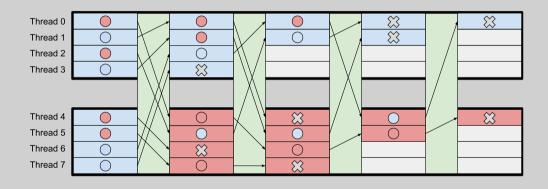
IN-PLACE OPTIMIZATION

$$\begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1/2 & 0 & 1/2 & 0 \\ 0 & 0 & -1/2 & -1 & -1/2 & 1 \end{bmatrix}$$

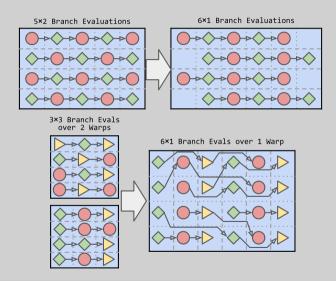
IN-PLACE OPTIMIZATION

$$\begin{bmatrix} 1 & 0 & 1 & 1 & 0 & 0 \\ 0 & 1 & 1/2 & 0 & 1/2 & 0 \\ 0 & 0 & -1/2 & -1 & -1/2 & 1 \end{bmatrix} \rightarrow \begin{bmatrix} 1 & 0 & 0 & 1 \\ 0 & 1/2 & 0 & 1/2 \\ -1 & -1/2 & 1 & -1/2 \end{bmatrix}$$

THREAD-DATA REMAPPING



THREAD-DATA REMAPPING



TDR MATRIX INVERSION: FIXROW

```
struct FixRow {
     using Type = void(*)(index t rowId. size t colId):
3
     template<typename PROGRAM>
     device static void eval(PROGRAM prog, index t rowId, size t colId) {
        index t size = prog.device.size.row;
       matrix t Ri = prog.device.matrix[size*rowId + colId];
       matrix t Aii = prog.device.Aij[rowId];
9
       Ri /= Aii;
10
        prog.device.matrix[size*rowId + colId] = Ri:
12
       if( Ri != 0.0 ) {
13
          prog.template async<SplitCol>(rowId, 0, prog.device.size.col-1, colId);
14
15
16
```

TDR MATRIX INVERSION: FIXCOLUMN

```
struct FixCol {
     using Type = void(*)(index t colId, index t i start,
                           index t i end. index t i):
3
     template<typename PROGRAM>
     device static void eval(
5
          PROGRAM prog, index t colld,
6
          index t i start, index t i end, index t i) {
       index t size = prog.device.size.row:
       for (index t i = i start; i <= i end; i++) {
         matrix t col = prog.device.Aii[i]:
10
11
         if (col != 0) {
12
           matrix t colj = prog.device.matrix[ i*size + j];
13
           matrix t AColIdi = prog.device.matrix[colId*size + i]:
14
           if (i != colId) {
15
             coli -= AColIdi * col;
16
             prog.device.matrix[i*size + i] = coli:
17
   }}};
18
```

RESULTS

COMPARISON

■ cpu-inverse

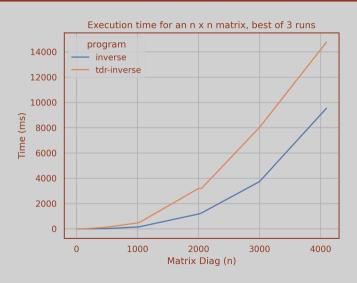
COMPARISON

- cpu-inverse
- inverse

COMPARISON

- cpu-inverse
- inverse
- tdr-inverse

RANDOM MATRICES



SPARSE MATRICES



Conclusion / Closing Thoughts

■ The use of TDR can offer fairly significant gains when applied to sparse matrix inversion.

Conclusion / Closing Thoughts

- The use of TDR can offer fairly significant gains when applied to sparse matrix inversion.
- Possible next step is to implement Strassen Inversion [4].

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QUESTIONS?

https://github.com/scrufulufugus/tdr-inverse-materials

