Faculty of Computing , Online Examinations 2022

STUDENT NAME	**ACJD Silva**		
INDEX NUMBER (NSBM)	**22795**	**YEAR OF STUDY AND SEMESTER**	**Year 1 Semester 2**
MODULE NAME **(As per the paper)**	CS104.3 – Computer Architecture		
MODULE CODE	**CS104.3**		
MODULE LECTURER	**Mr. Iman Ashley**	**DATE SUBMITTED**	✓ **15.08.2022**

For office purpose only:

GRADE/MARK	
COMMENTS	

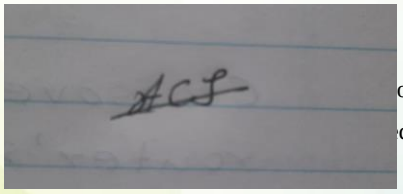
Declaration

PLEASE TICK TO INDICATE THAT YOU HAVE SATISFIED THESE REQUIREMENTS

- ✓ I have carefully read the instructions provided by the Faculty
- ✓ I understand what plagiarism is and I am aware of the University's policy in this regard.
- ✓ I declare that the work hereby submitted is my own original work. Other people's work has been used (either from a printed source, Internet or any other source), has been properly acknowledged and referenced in accordance with the NSBM's requirements.
- ✓ I have not used work previously produced by another student(s) or any other person to hand in as my own.
- ✓ I have not allowed, and will not allow, anyone to copy my work with the intention of passing it off as his or her own work.
- ✓ I hereby certify that the individual detail information given (name, index number and module details) in the cover page are thoroughly checked and are true and accurate.

I hereby certify that the statements I have attested to above have been made in good faith and are true and correct. I also certify that this is my own work and I have not plagiarized the work of others and not participated in collusion.

Date: 15.08.2022 **E- Signature:



of
d.

Question 1

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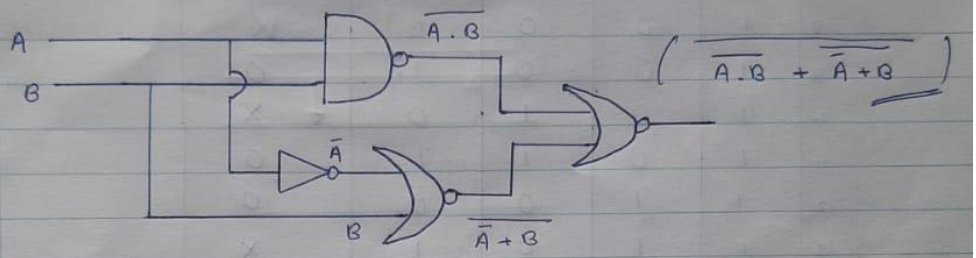
Question 01

i. Simplification and reduces the complexity of the circuit design.

Reduces the number of steps and increases the efficiency of the circuit.

Decreases the number of gates and cost of the hardware.

ii.



iii. a. $\overline{(\bar{x}+z)(\overline{xy})}$

$= \overline{(\bar{x}+z)} + \overline{(\overline{xy})}$

$= (\bar{\bar{x}} \cdot \bar{z}) + (\bar{\bar{x}}+\bar{\bar{y}})$

$= (x \cdot \bar{z}) + (x+y)$

$= x(\bar{z}+1+y)$

$= x(\bar{z}+1)$ //

b. $\overline{\overline{(x.\bar{y})}.(\bar{y}+z)}$

$= \overline{\overline{(x.\bar{y})} + (\overline{\bar{y}+z})}$

$= (x.\bar{y}) + (\bar{\bar{y}}.\bar{z})$

$= (x.\bar{y}) + (y.\bar{z})$

IV. a.

	A	B	C	D	Z
m_0	0	0	0	0	1
m_1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	1
6	0	1	1	0	0
7	0	1	1	1	1
8	1	0	0	0	X
9	1	0	0	1	0
10	1	0	1	0	X
11	1	0	1	1	0
12	1	1	0	0	0
13	1	1	0	1	X
14	1	1	1	0	0
15	1	1	1	1	X

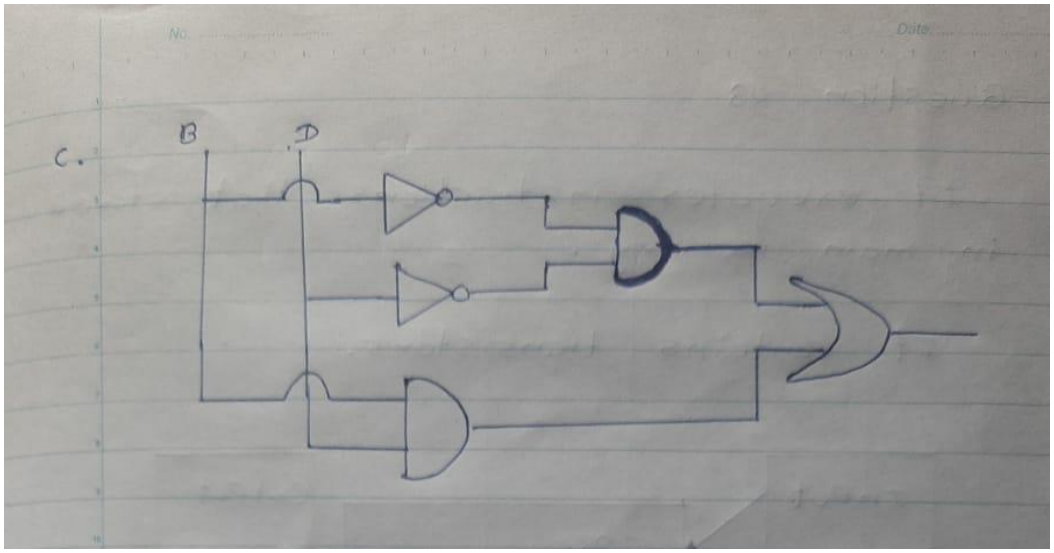
MSB LSB
ABCD

b.

AB \ CD	00	01	11	10
00	1	0	0	1
01	0	1	1	0
11	0	X	X	0
10	X	0	0	X

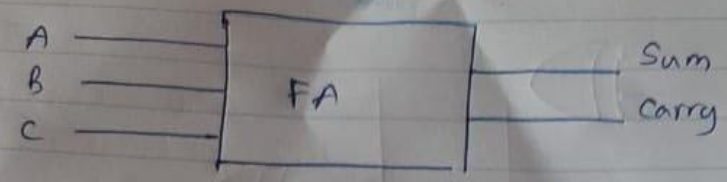
(I) (II)

(I) + (II) $\Rightarrow$ $\overline{B}.\overline{D} + B.D$


C.
B
D

Question 2

2)



A	B	C	carry	sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

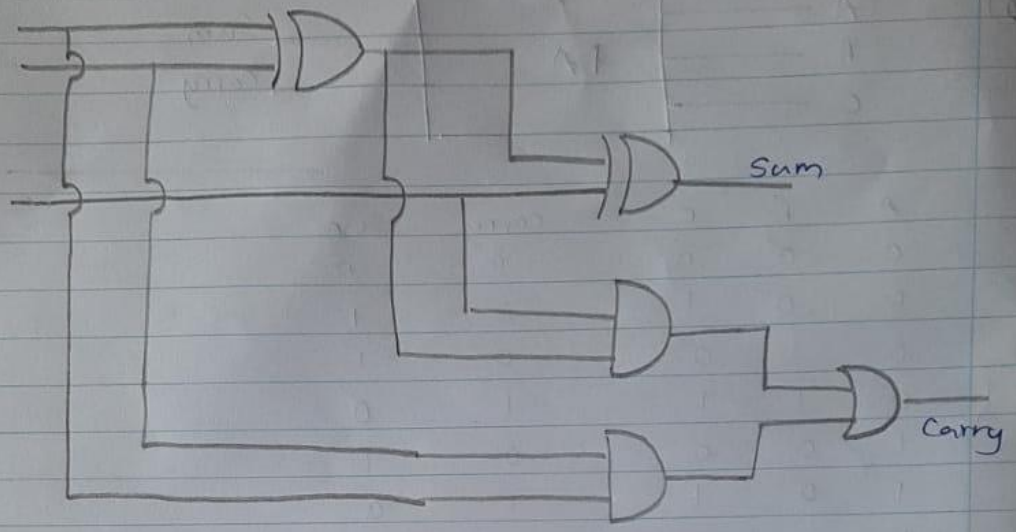
$$Sum = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$$
$$= \bar{A}(\bar{B}C + B\bar{C}) + A(\bar{B}\bar{C} + BC)$$
$$= \bar{A}(B \oplus C) + A\overline{(B \oplus C)}$$
$$= \bar{A}x + A\bar{x}$$
$$= A \oplus x$$
$$Sum = A \oplus B \oplus C$$

$\bar{B}C + B\bar{C}$

$B \oplus C$

$\therefore x = B \oplus C$

$$Carry = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$
$$= \bar{A}BC + A\bar{B}C + AB(\bar{C} + C)$$
$$= \bar{A}BC + A\bar{B}C + AB$$
$$= \bar{A}BC + A(\bar{B}C + B)$$
$$= \bar{A}BC + A(B + C)$$
$$= \bar{A}BC + AB + AC$$
$$= B(\bar{A}C + A) + AC$$
$$= B(A + C) + AC$$
$$= AB + BC + AC$$



ii) Fail safe switches :- f_1, f_2, f_3 System shutdown :- S
Emergency shut down :- E

F_1	F_2	F_3	E	S
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

Question 3

Question 03

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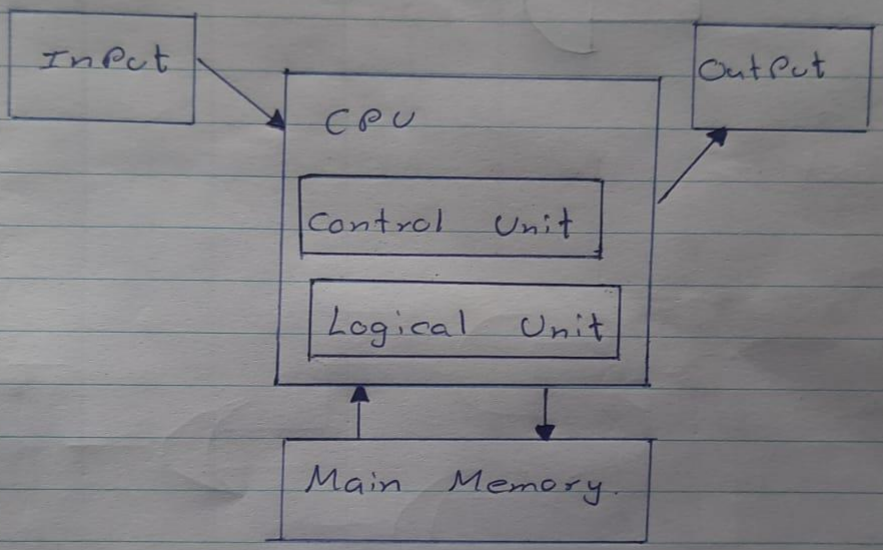
i. It executes instructions that stored in main memory.

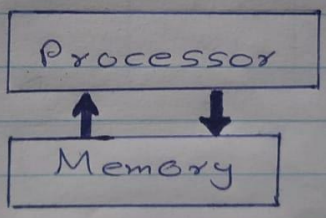
It contains transistors.

ii.



Every Computation fetches data from main memory then processes it and sends to memory.

a. When data moves between Processor and memory. it creates latency since they are seperated.



Even the Processor Perform tasks faster it will be idle for a time to fetch data from the memory. This creates the von-Neumann bottleneck.

b.

c. Caching → store the frequently used data in a special area.

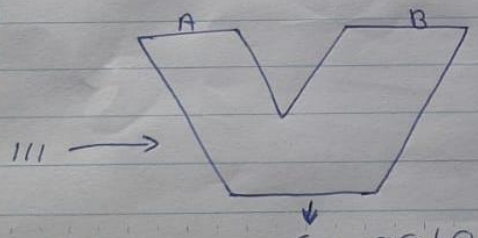
Pre fetching → Sending data to a specific location before it's being requested.

iii. Arithmetic logical unit performs Arithmetic operations such as Addition, Substraction, multiplication and division and logical operations like And, OR, NOT, XOR,

Example :-

A = 00100110 B = 00001001

control line = 111 (XOR)

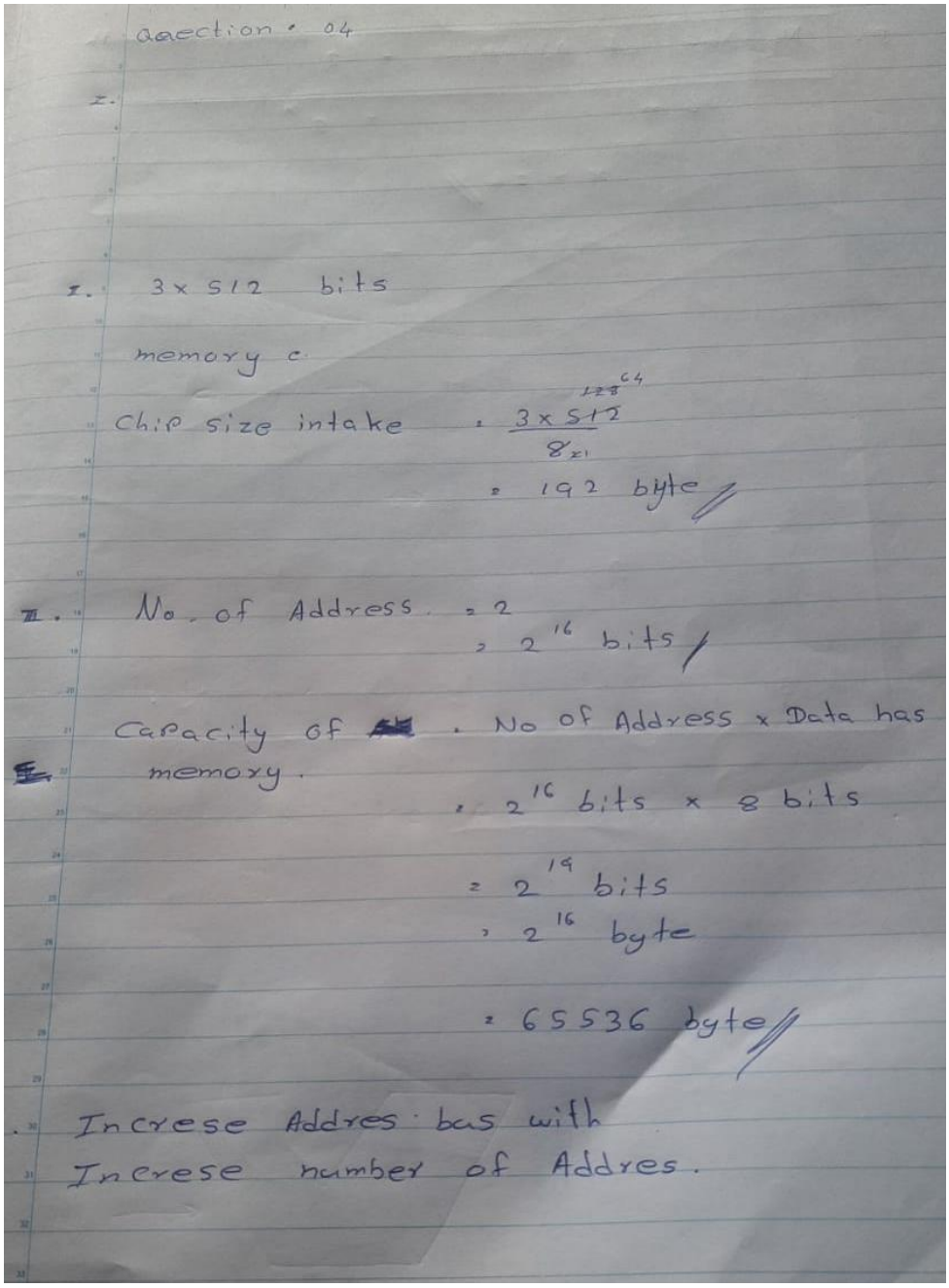


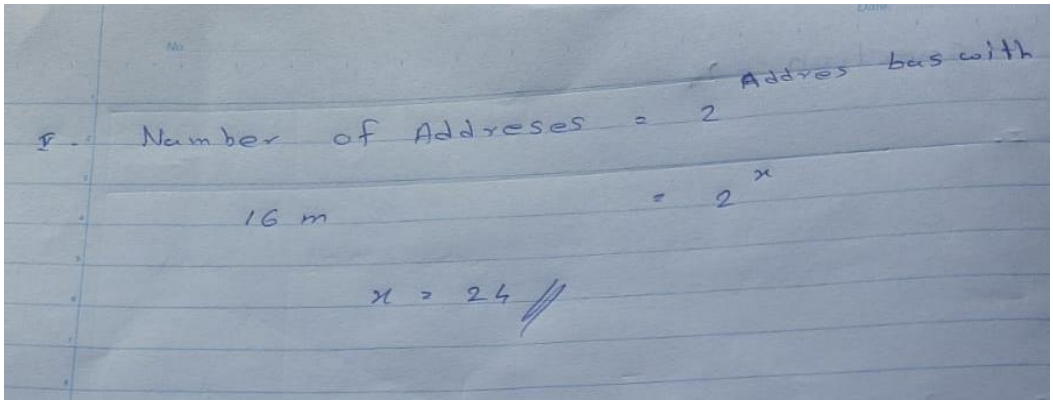
C = 00101111

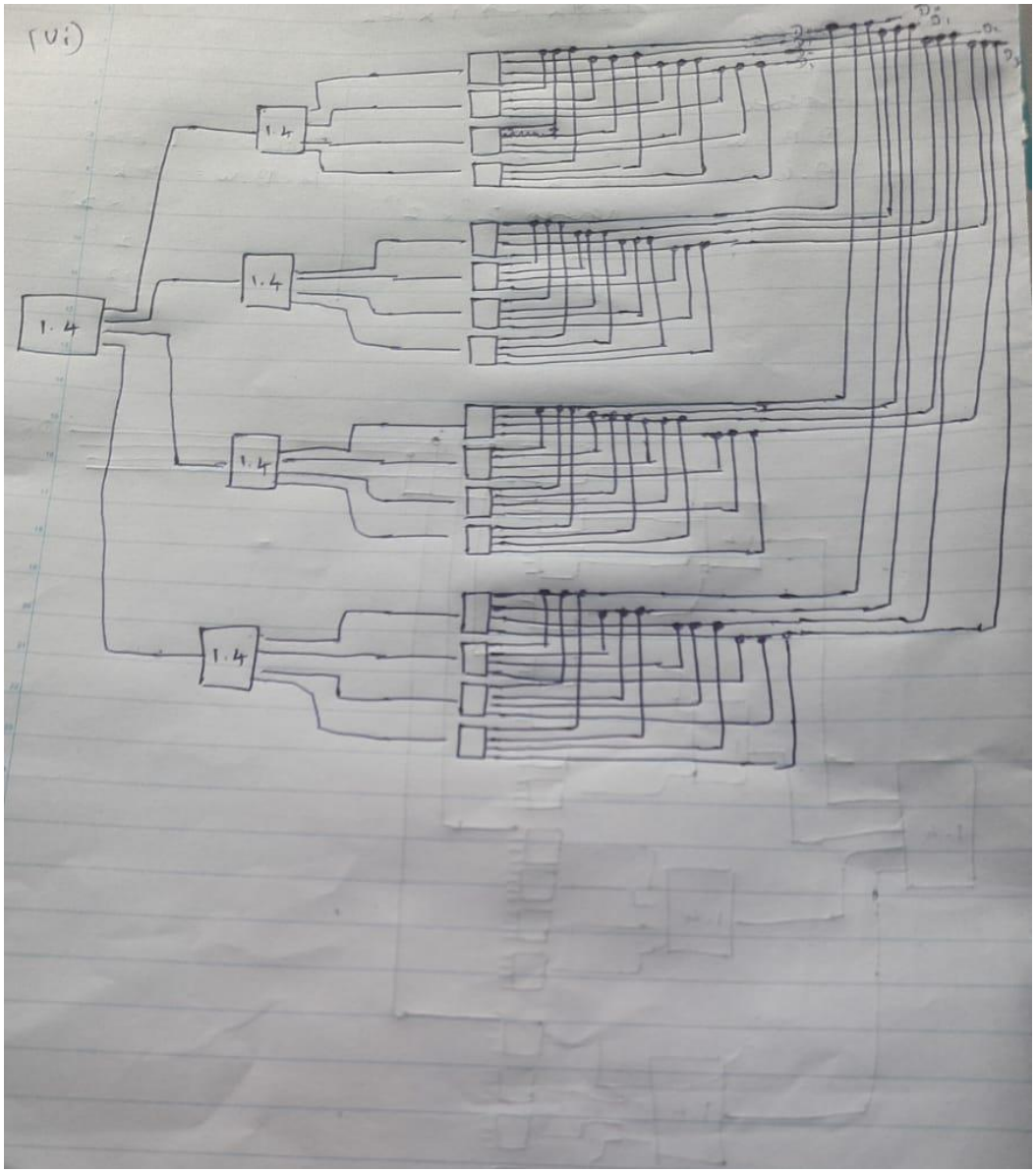
IV

Address	Contents	
499	LDA 1000	Load 1000 to memory address manager (MAR)
500	SUB 1001	-
501	STO 1002	Store the results in 1002.
502	JMP 600	Jump to instruction on 600.
1000	6	Contents at memory location 1000
1001	2	Contents at memory location 1001
1003		free memory.

Question 4


aaection : 04
I.
I. 3 x 512 bits
memory c
Chip size intake : 3 x 512 / 8
: 192 byte
II. No. of Address = 2
: 2^16 bits
Capacity of . No of Address x Data has
memory.
: 2^16 bits x 8 bits
= 2^19 bits
: 2^16 byte
: 65536 byte
Increse Addres bus with
Increse number of Addres.


I. Number of Addreses = 2 Addres bus with
16 m = 2^x
x = 24


(vi)
1:4
1:4
1:4
1:4
1:4

vii.

	4 x 16 k	1 x 4 k
Data bus with	4	1
No. of Address	16 k	4k
memory Capacity	16 kB	4k8
Address bus with	14	12