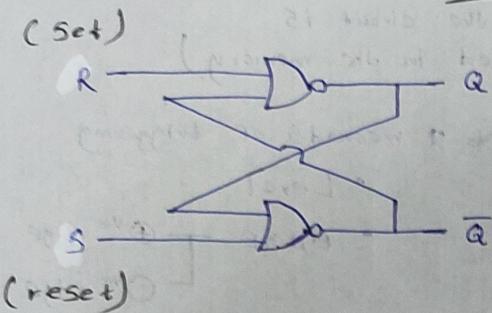
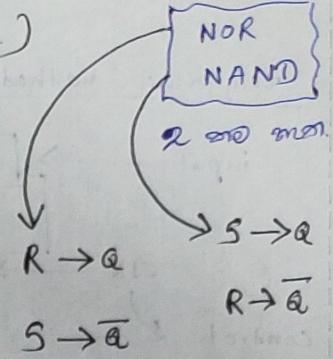


② SR Latch (set reset latch)



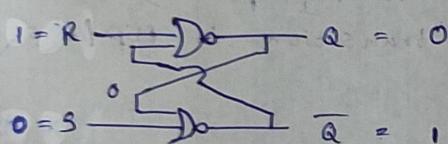
NOR gate T.T.		
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



- SR Latch using -
NOR gate.

(R) Reset Q = 0 NOR	(R) Reset Q = 1
(S) Set Q = 1 NOR	(S) Set Q = 0 NAND

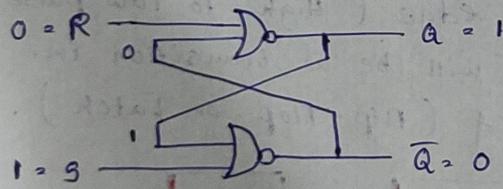
1) case ① $S=0 \mid R=1$, $Q=0 \mid \bar{Q}=1 \rightarrow \text{Reset}$



$$S=0, R=0, Q=0, \bar{Q}=1 \rightarrow \text{Hold State.}$$

S	R	Q	\bar{Q}	Qn
0	0	memory (before)		
0	1	0	1	
1	0	1	0	
1	1	not allowed		

2) case 1 (2) $B = 1 / R = 0$, $Q = 1 / \bar{Q} = 0 \rightarrow$ set



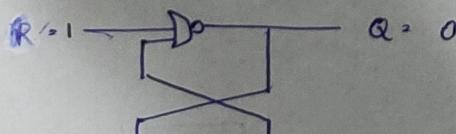
$$S=0 \quad R=0, \quad Q=1, \quad \bar{Q}=0$$

memory

State	S	R	Q	\bar{Q}	S	R	Qn+1
(A, 1, 1)	0	0	NA		0	0	NA
0	0	1	0	1	0	1	1
	1	1	Qn		1	0	0

- 5R Latch NOR T.T.-

③ Case ③ $S=1 / R=1, Q=0 / \bar{Q}=0$

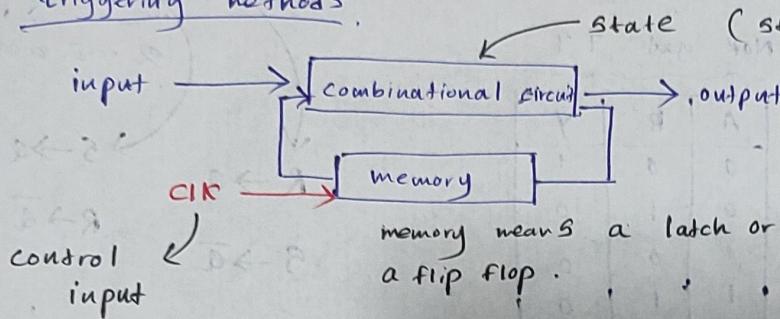


$$S=1 \quad \text{at } Q=0 \quad S=0 \text{ if } R=0, Q=1 \quad / \quad \bar{Q}=0$$

$$B = 0 \quad | \quad R = 0, \quad Q = 0 : \quad | \quad \bar{Q} = 1 \quad \boxed{\rightarrow \text{NOT Allowed}}$$

triggering methods

CA



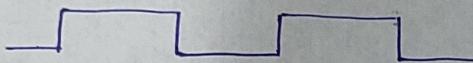
State (state of the circuit is stored in the memory)

* 2 methods of triggering

- Level

- EDGE

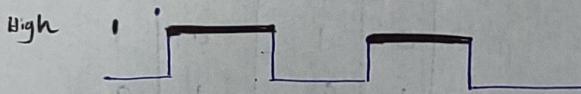
+ve edge
-ve edge.



→ normal clock signal.

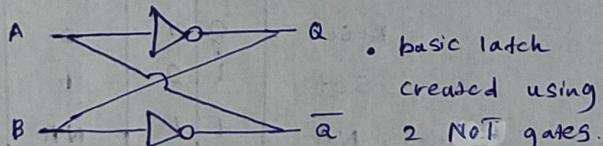
Level triggering

- whenever the clock remains in high there will be a transition in flip-flops / Latch



Latch

What is a latch.



- basic latch created using 2 NOT gates.

* A latch is a data storage device that can store 1 bit of information.

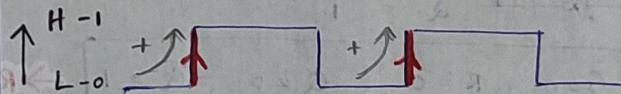
* The basic digital storage (Latch) made by crosscoupling two NOT gates.

* The output of each NOT gates are connect to the input of each other. This combination called latch.

edge triggering

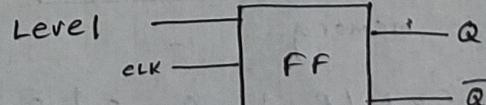
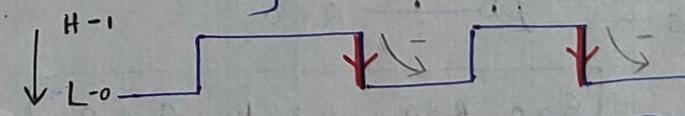
1) +ve edge triggering

- When the clock signal is in rising edge (low to High pulse) there will be a transition in flip-flops or Latch

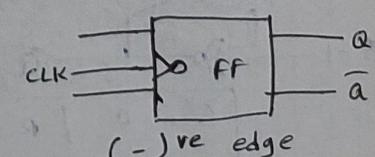
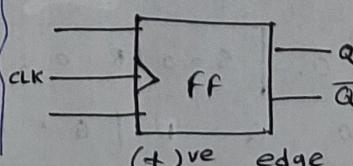


2) -ve edge triggering

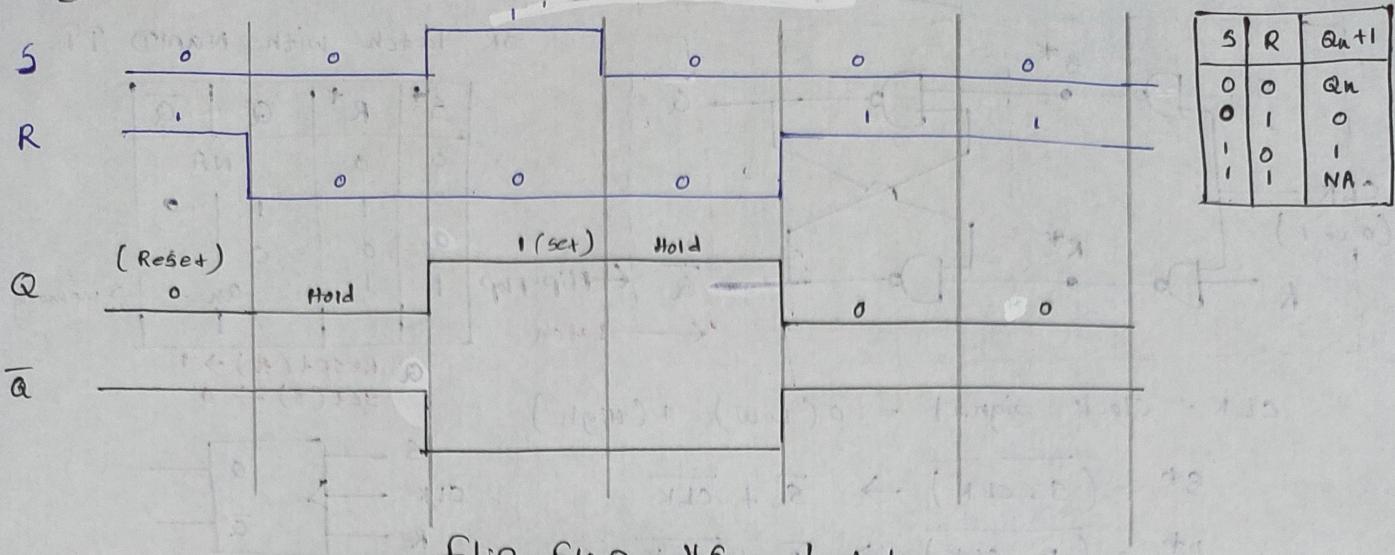
- When the clock signal in the falling edge (High-to-low pulse) there will be a transition in memory (flip-flop or Latch).



Edge triggering:



SR-Latch Timing Diagram (NOR gate) (3)

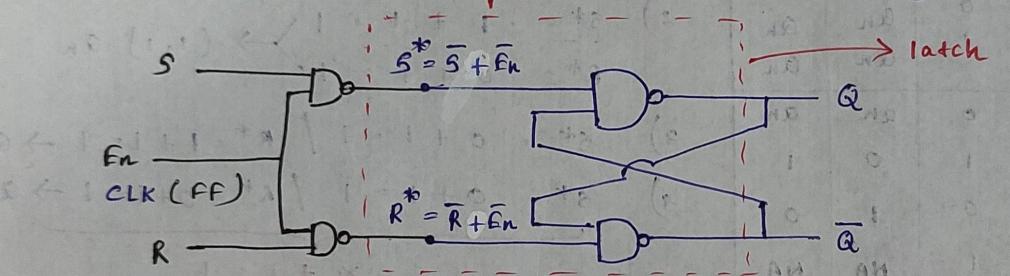


flip-flop VS Latch

flip-flop → Edge-triggering Sensitive

Latch → Level triggering ↗

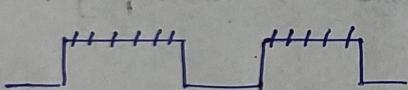
- SR latch controlled input. - (with NAND gate)



NAND T.T.

X	Y	Z
0	0	1
0	1	1
1	0	1
1	1	0

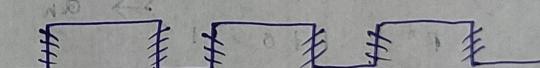
Latch control @ 25



level triggering

S	R	Q _{n+1}
0	0	NA
0	1	1
1	0	0
1	1	Q _n

Flip-flop control @ 25



edge triggering

SR Latch
NAND T.T.
Reduced

$$S^* = \overline{S} \cdot \overline{EN}$$

$$R^* = \overline{R} \cdot \overline{EN}$$

$$S = 0 \mid R = 0 \mid EN = 0$$

$$S^* = \overline{0 \cdot 0} = 1$$

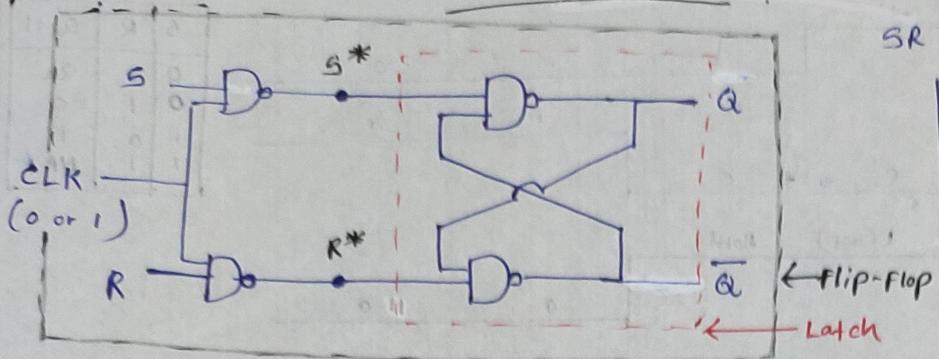
$$R^* = \overline{0 \cdot 0} = 1$$

$$(1, 1) = Q_n / \text{memory}$$

S	R	Q	\overline{Q}
0	0	NA	
0	1	1	0
1	0	0	1
1	1	Q _n	Q _n

SR Latch
with NAND
T.T.

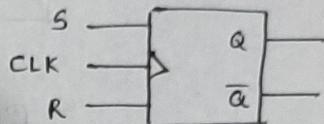
SR - Flip flop (NAND gate)



SR latch with NAND T.T.

S^*	R^*	Q	\bar{Q}
0	0	NA	
0	1	1	0
1	0	0	1
1	1	Qn	1

Reset (R) $\rightarrow 1$
Set (S) $\rightarrow 0$



SR - Flip flop. (Edge)

CLK	S	R	Q	\bar{Q}
Low	0	0	Qn	Qn
	0	1	Qn	Qn
	1	0	Qn	Qn
	1	1	Qn	Qn
High	1	0	Qn	Qn
	1	1	0	1
	1	0	1	0
	1	1	NA	NA

Low

- 1) $S^* = 1 + 1 = 1 \rightarrow (1, 1)$ Qn memory
 - 2) $S^* = 1 + 1 + 1 = 1 \rightarrow (1, 1)$ Qn
 - 3) $S^* = 0 + 1 = 1 / R^* = 1 + 1 = 1 \rightarrow Qn$
 - 4) $S^* = 0 + 1 = 1 / R^* = 0 + 1 = 1 \rightarrow Qn$
- $x + 1 = 1$

- 5) $S^* = 1 + 0 = 1 \rightarrow Qn$
- 6) $S^* = 1 + 0 = 1 \rightarrow 0, 1$
- 7) $S^* = 0 + 0 = 0 \rightarrow 1, 0$
- 8) $S^* = 0 + 0 = 0 \rightarrow 0, 0$

Truth table \rightarrow next p.g.

A	B	C	D	E	F	G	H
1	1	0	1	1	1	0	1
0	0	1	0	0	0	1	0
1	1	1	1	0	0	1	1
0	0	0	0	1	1	0	0

Tables \rightarrow SR - FLIP FLOP

20.3 / 21.2

Truth table.

CLK	S	R	Q _{n+1}
0	0	0	Q _n
0	0	1	Q _n
0	1	0	Q _n
1	1	1	Q _n
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	NA

$\xrightarrow{N.S.}$

characteristic table

S	R	Q _n	Q _{n+1}
0	0	0	0 (an)
		1	1 (an)
0	1	0	0
		1	0
1	0	0	1
		1	1
1	1	0	NA
		1	

$Q_{n+1} \rightarrow$ This
is depend on
your inputs
and previous
state.
(S, R, Q_n)

$Q_{n+1} \rightarrow$ next state

$Q_n \rightarrow$ present state.

excitation table

Q _n	Q _{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

When
 $CLK = 1$
(High)

Q _n	S	R	Q _{n+1}
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

3 inputs
 $2^3 = 8$ combinations.

inputs \rightarrow Q_n

Q_{n+1}

outputs \rightarrow S
R

$2^2 = 4$		find the value of Q_{n+1}			
SR		00	01	11	10
Q _n	Q _{n+1}	0	0	X	1
Q _n	Q _{n+1}	1	0	X	1

$$Q_{n+1} = 1 + 2 \\ = S + Q_n R$$

S R

D - Flip-flop (Data flip-flop)

D - flip flop using SR - flip flop

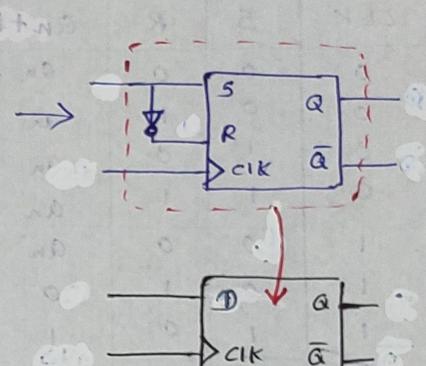
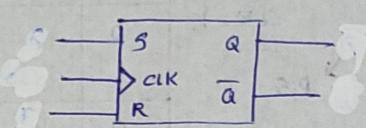
CLK	S	R	Q _{n+1}
0	0	0	Q _n
0	0	1	Q _n
0	1	0	Q _n
0	1	1	Q _n
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	NA

CLK	D	Q _{n+1}
0	0	Q _n
0	1	Q _n
1	0	0
1	1	1

Reduced T.T.

Q	Q _{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Excitation table.



$$D = 0, S = 0 | R = 1$$

$$D = 1, S = 1 | R = 0$$

D	Q _n	Q _{n+1}
0	0	0
1	0	1

complete T.T. character
Diagram $Q_{n+1} = D \oplus n$

$$Q_{n+1} = Q_n + D$$

to solve this next



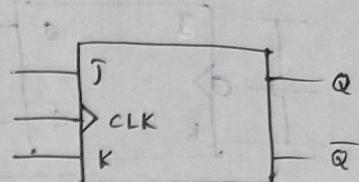
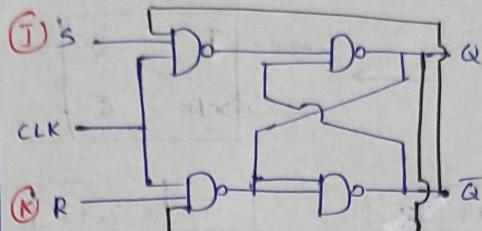
JK - flip-flop

(5)

o අං පෙනී.

- Using SR - flip flop.

CLK	S	R	Q _{n+1}
0	0	0	Q _n
0	0	1	Q _n
0	1	0	Q _n
Q	1	1	Q _n
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	Not used



- 1) CLK = 0 Q_n (memory)
- 2) CLK = 1 J = 0, K = 1, Q = 0, Q̄ = 1
- 3) CLK = 1 J = 1, K = 0, Q = 1, Q̄ = 0
- 4) CLK = 1 J = 0, K = 0, Q = Q_n, Q̄ = Q̄_n

Assume Q = 0, Q̄ = 1

Outputs, Q = 0, 1, 0, 1, ... →
 $\bar{Q} = 1, 0, 1, 0, \dots$

$Q_{n+1} = 0 \rightarrow 1$

$1 \rightarrow 0$

$Q_n = \bar{Q}_n$

Output = \bar{Q}_n

CLK	J	K	Q _{n+1}
0	0	0	Q _n
0	0	1	Q _n
0	1	0	Q _n
0	1	1	Q _n
1	0	0	Q _n
1	0	1	0
1	1	0	1
1	1	1	Q _n ← toggle

J	K	Q _{n+1}
0	0	Q _n
0	1	0
1	0	1
1	1	Q _n

reduced T.T.

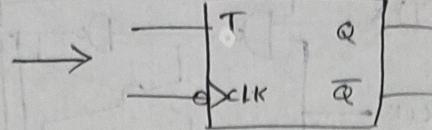
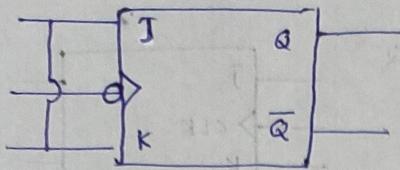
Q	Q _{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

T.T for JK - flip flop.

Q _n	J	K	Q _n	Q _{n+1}
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	1	0
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	0

Character [complete . T.T.]

T-Flip Flop (Toggle in JK-FF)



CLK	T	Q _{n+1}
low {	0	Q _n
	0	Q _n
High {	1	Q _n
	1	Q _n

Q	Q _{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

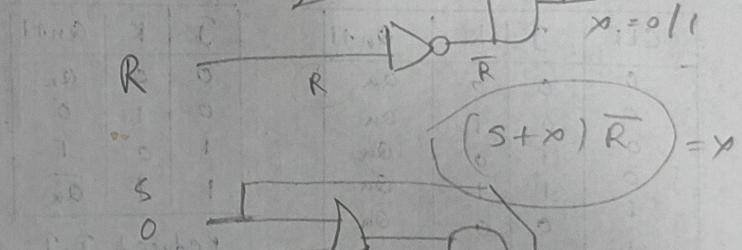
T	Q _{n+1}
0	Q _n
1	Q _n

reduced T.T.

T	Q _n	Q _{n+1}
0	0	0
1	0	1

Compleat T.T.

X	C	T ₁ + Q ₀	D
x	0	0	0
x	1	1	0
1	x	0	1
0	x	1	1



$$\begin{aligned} & \text{S} \rightarrow \text{S} + x \\ & \text{R} \rightarrow \text{R} \\ & \text{S} \rightarrow \text{S} \quad \text{R} \rightarrow \text{R} \\ & \text{S} \rightarrow \text{S} \quad \text{R} \rightarrow \text{R} \end{aligned}$$

$$(S+x)R = x$$

$$\overline{AB.C} \quad \overline{ABC}$$

$$\overline{AC} + \overline{AB}$$

$$\overline{AB} \quad \overline{ACB} + \overline{ACB}$$

0	0	0	0
0	0	1	1
1	0	1	1
1	0	0	0

(b)

Race-around condition - JK flip flop

toggle and Race-around are different.

toggle \rightarrow controlled , Race around - not controlled

