Faculty of Computing, Online Examinations 2021

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INDEX NUMBER (NSBM)	**21386**	**YEAR OF STUDY AND SEMESTER**	**Year 1 semester 2**
MODULE NAME **(As per the paper)**	**Computer architecture**		
MODULE CODE	**CS104.3**		
MODULE LECTURER	**Mr. Gayan Perera**	**DATE SUBMITTED**	**2021/10/11**

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GRADE/MARK	
COMMENTS	

Declaration

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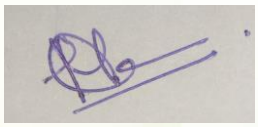

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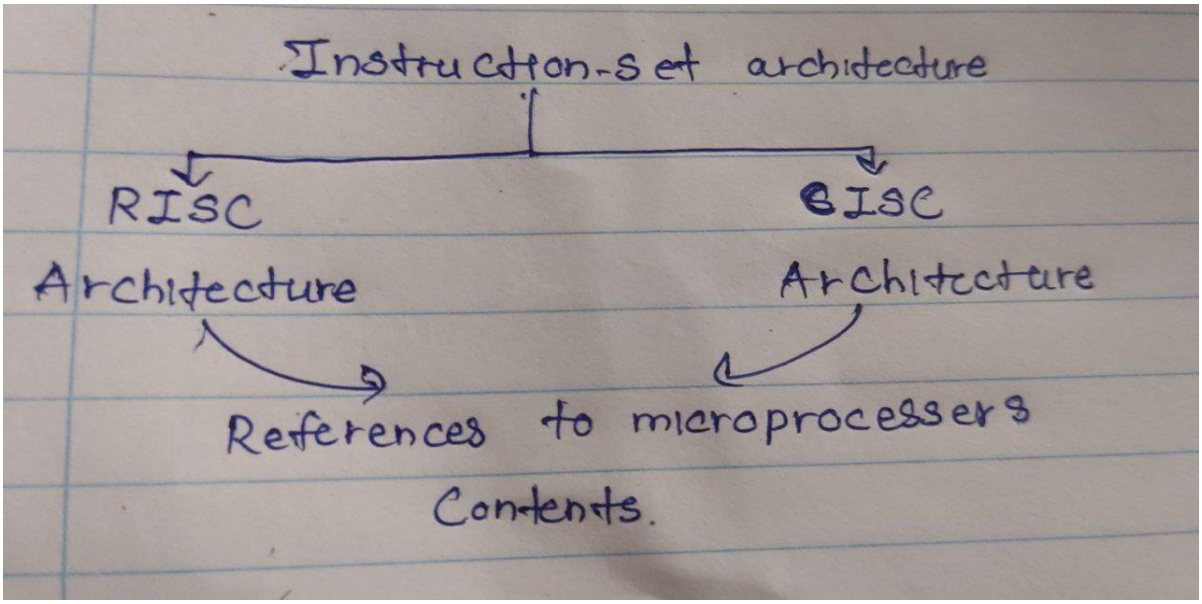
question 1

1.

Instruction set architecture is what the computers software preview. And it is a arithmetic and logical view. ISA provides all information needed for someone that wants to write a program in machine language. Simply ISA defines all of the programmer-visible components and operations of the computer.



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2) i) $16 + 48 = 64$ bits

ii) $2^{16} = 65536$ bits

iii) $2^{48} = 2^{20} \times 2^{20} \times 2^{8}$

$= 2^{28}$ Mb.

3)

Machine cycle

Fetch → decode → execute → store

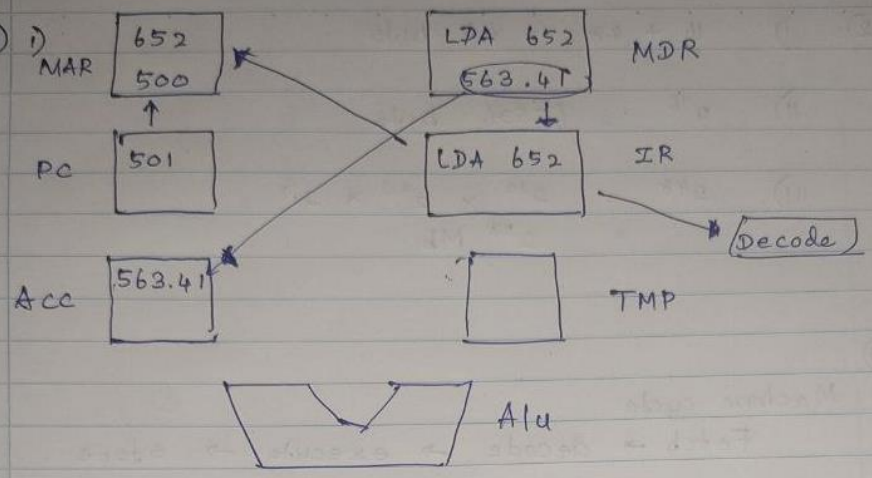
Fetch - In fetch, the control unit look ~~at~~ at the ~~program~~ program Counter register (PC) to get the memory address of next instruction. then request the ~~ins~~ instruction from main memory and places it in the IR.

Decode - decode the instructions ~~in~~ stored in the instruction register. (IR)

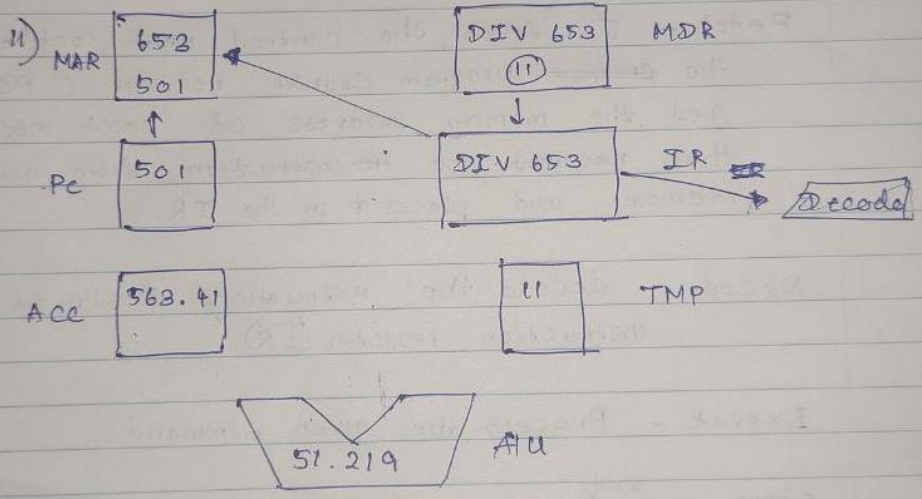
Execute - Process the given command.

Store - ~~write~~ write ~~the~~ result of the instruction in to main memory.

4) i)



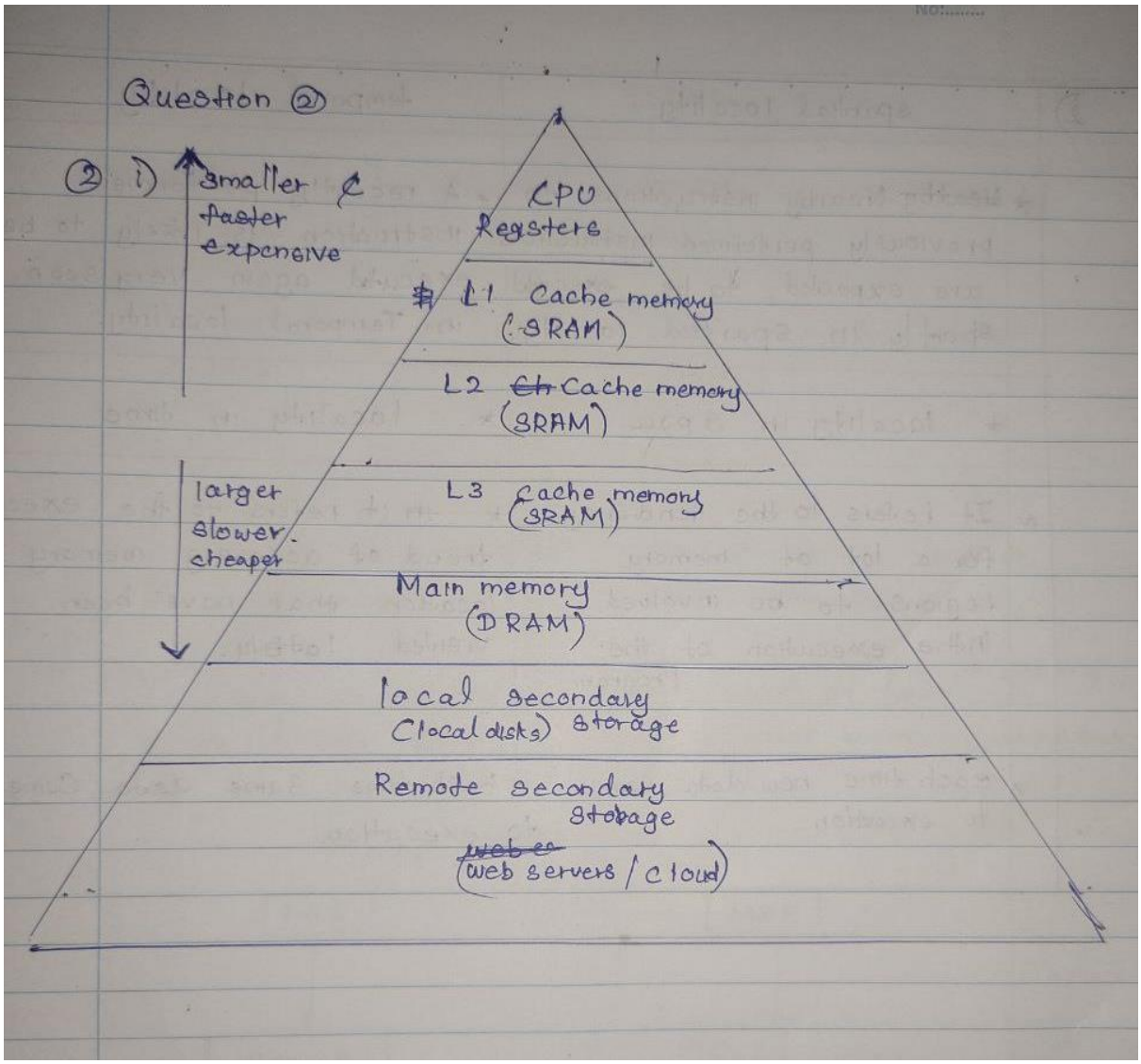
ii)



5)

fixed length	Varieble length
* All the records in the file are same size	* Different records in the file have different sizes
* leads to memory wastage	* Memory Efficient
* Access to records is faster	* Access to records is slower.

Question 2


Question (2)
(2) i)
smaller
faster
expensive
CPU
Registers
L1 Cache memory
(SRAM)
L2 Cache memory
(SRAM)
L3 Cache memory
(SRAM)
larger
slower
cheaper
Main memory
(DRAM)
local secondary
(local disks) storage
Remote secondary
storage
(web servers / cloud)

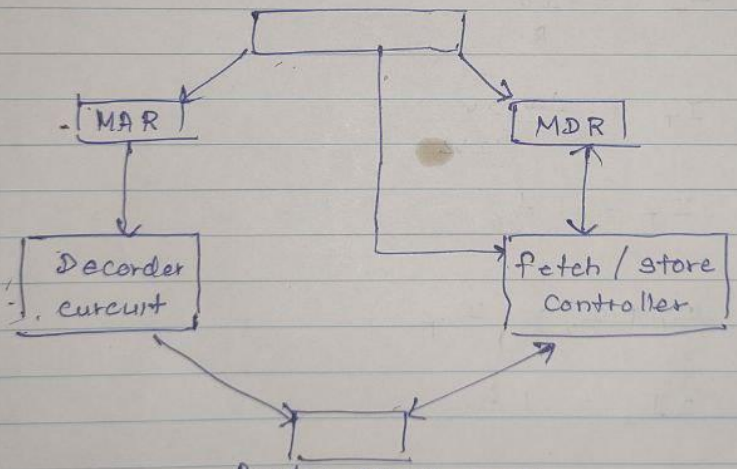
2)

spartial locality	temporal locality
* ~~Nearby~~ Nearby instructions to previously performed instructions are expected to be executed shortly. In Spartial locality.	* A recently performed instruction is likely to be executed again very soon in Temporal locality.
* locality in space	* locality in time
* It refers to the tendency for a lot of memory regions to be involved in the execution of the program.	* In it refers to the execution trend of accesing memory location that have been visited lately.
* each time new data comes to execution.	* Each time same data comes to execution.

3)

SRAM	DRAM
SRAMs are low density devices.	DRAMs are high density devices.
they are used in cache memories.	they are used in main memories
faster than DRAM.	slower
transistors are used to store information	Capacitors are used to store information.
advantages. low power consumption and faster access speed.	low cost of manufacturing memory and greater memory capabilities.

4)



MAR - Holds the address of the memory location from which information will be read from or to which data will be written to.

MDR - used to temporary store information read from a written to memory.

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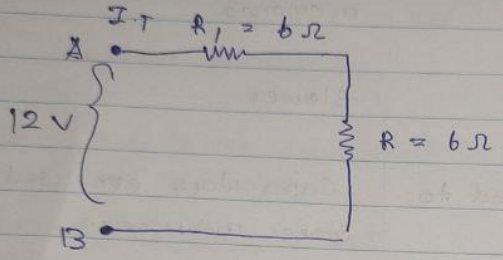
(5)

$\Delta V = IR$

$R_2 + R_3 = 8\Omega + 4\Omega$

$\therefore I_1 = I_2$ (Because the potential difference and the current are the same)



i) $\Delta V = IR$

$I_T = \frac{\Delta V}{R}$

$I_T = \frac{\Delta V\ 12\ V}{12\ \Omega}$

$I_T = 1\ A$

ii) $I_1 + I_2 = I_T$

$2I_2 = 1\ A$

$I_2 = \frac{1}{2}\ A$

$I_2 = 0.5\ A$

RICHARD

Question 3

Question (3)

(3) 1) a) temperature ~~temperitade~~ of Engine - x

Cabin pressure - y

rotation speed of the shaft - z

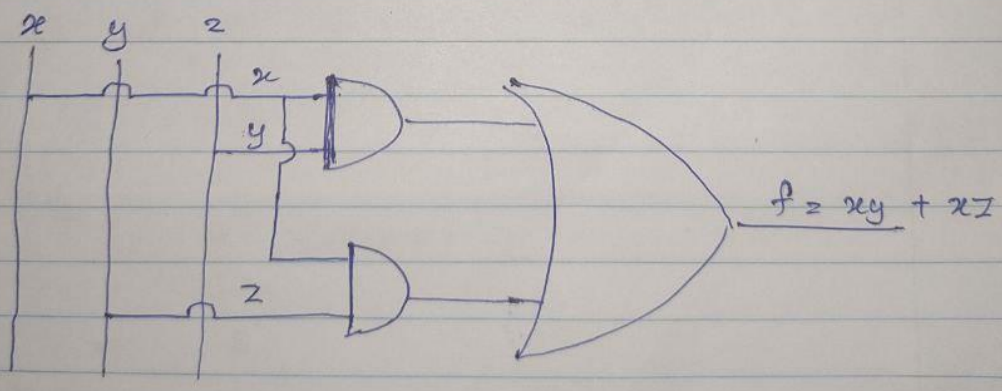
f = output

x	y	z	y+z	F = x(y+z)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	1	1
1	1	1	1	1

b)

$$F = x\bar{y}z + xy\bar{z} + xyz$$
$$= x\bar{y}z + xyz + xy\bar{z} + xyz$$
$$= xz + xy$$

c)



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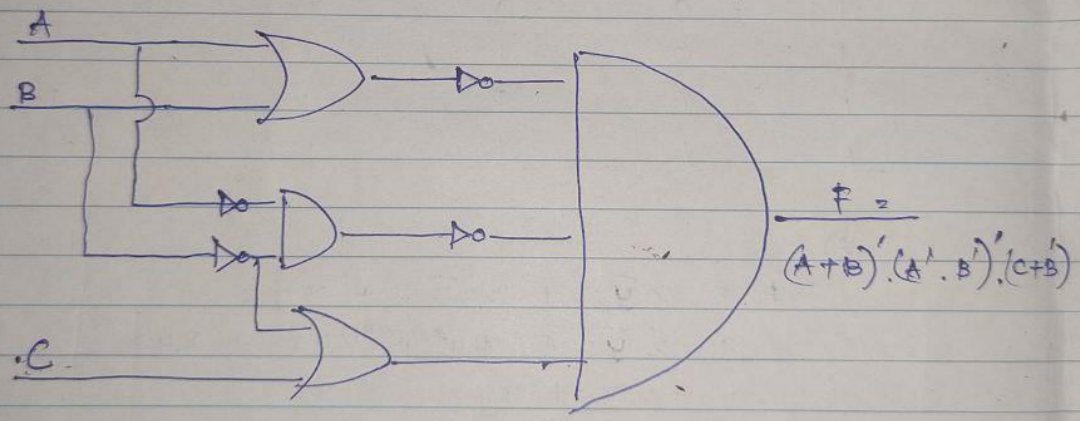
2) $F = (A+B)' \cdot (A' \cdot B')' \cdot (C+B')$

A	B	C	A'	B'	(A+B)'	(A'.B')'	(C+B')	F = (A+B)'.(A'.B')'.(C+B')
0	0	0	1	1	1	0	1	0
0	0	1	1	1	1	0	1	0
0	1	0	1	0	0	1	0	0
0	1	1	1	0	0	1	1	0
1	0	0	0	1	0	1	1	0
1	0	1	0	1	0	1	1	0
1	1	0	0	0	0	1	0	0
1	1	1	0	0	0	1	1	0



Q. 3 a) $F = A + (A' \cdot B)$

~~$F = (A+C)(AD + AD')$~~

$F = A \cdot 1 \cdot (A' \cdot B)$

$= A(1 + B)$

$= A \cdot 1 = A$

$F = A + (A' \cdot B)$

$F = (A + A')(A + B)$

$= 1 \cdot (A+B)$

$= (A+B)$

b) $F = (A+C)(AD + AD') + AC + C$

$F = (A+C) \cdot A \cdot (D + D') + C(A+1)$

$F = (A+C) \cdot A + AC + C$

$= AA + AC + C$

$= A + AC + C$

$= A(1 + C) + C$

$= A + C$ //

c) $F = A'B'C' + A'B'C + A'B'C$

$F = A'B'C' + A'B'C + AB'C' + AB'C$

$= A'B'(CC' + C) + AB'(CC' + C)$

$= A'B' + AB'$

$= B'(CA' + A)$

$= B'$ //

4)

functionality of the Multiplexer

Various devices can share multiple input signals from a single device or resource, such as a single digital converter that converts one analog signal to one digital signal, or a single communication transmission line. Boolean functions can be executed on many variables using multiplexers.

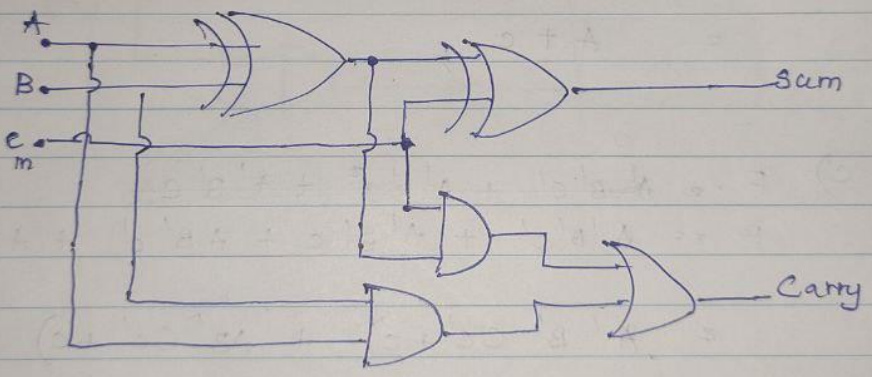
Full adder.

~~functionality of Multiplexer.~~

truth table

Input			Output	
A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

logic ~~ckt~~ circuit



* ~~Multiple devices can exchange multiple input signal from one device or resource.~~

Question 4

Question (4)

1) register is a temporary memory storage, which stores data and instructions that are being used by the CPU. There are 4 main types of registers.
   1) Program Counter (PC)
   2) instruction register (IR)
   3) Memory Address register (MAR)
   4) Memory data register (MDR)

1) ~~PC~~ Program Counter - It holds the address of the function.
2) instruction register - It holds instruction code
3) Memory address register - It holds address for the memory.
4) Memory data register - It holds memory operand.

2) Number of addresses = $2^{\text{Address bus width}}$
   = 2^{64}

   Capacity of memory = $2^{64} \times 8$ bits
   = $2^{64} \times 2^3$ bits
   = 2^{64} bytes
   = 2^{32} TB.

3) Number of addresses = $2^{\text{Address bus width}}$
   $8\,M = 2^{\text{Address bus width}}$
   $8 \times 2^{20} = 2^{\text{Address bus width}}$
   $2^3 \times 2^{20} = 2^{\text{Address bus width}}$

   therefore,
   Address bus width = 23 bits.

4) Number of addresses = $2^{\text{Address bus width}}$

$= 2^{32}$

Capacity of memory $= 2^{32} \times 8$ bits

$= 2^{32} \times 2^{3}$ bits

$= 2^{32}$ bytes

$= 2^{2}$ GB

$= 4$ GB,

5) 4 x 8 K

Question (4)

Part [E]

4 × 8k memory.

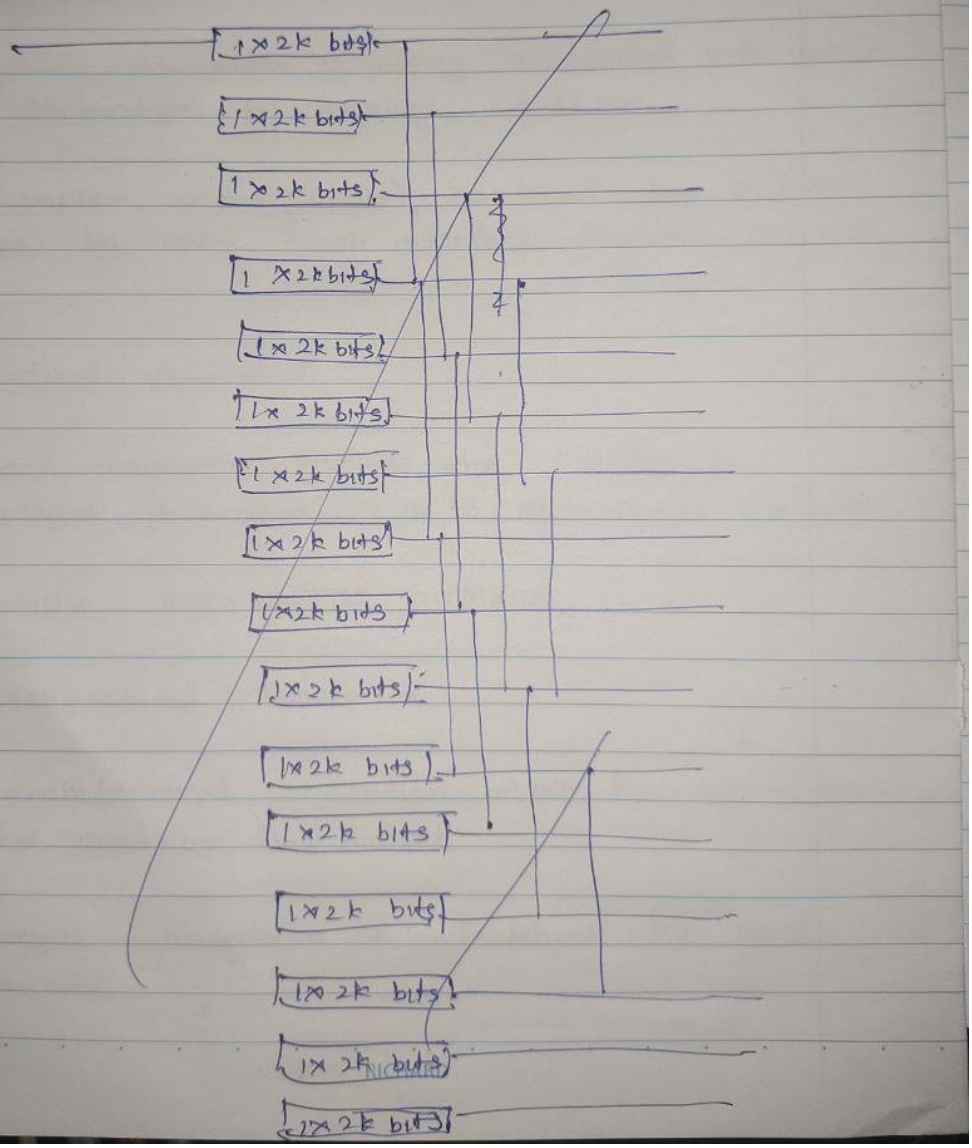
5) width of address bus = 8k = $2^3 \times 2^{10}$ = 2^{13} = 13 bits.

width of data bus = 8 bits.

1 × 2k memory.

width of address bus = 2k = $2^1 \times 2^{10} = 2^{11}$ = 11 bits.

width of data bus = 1 bits.

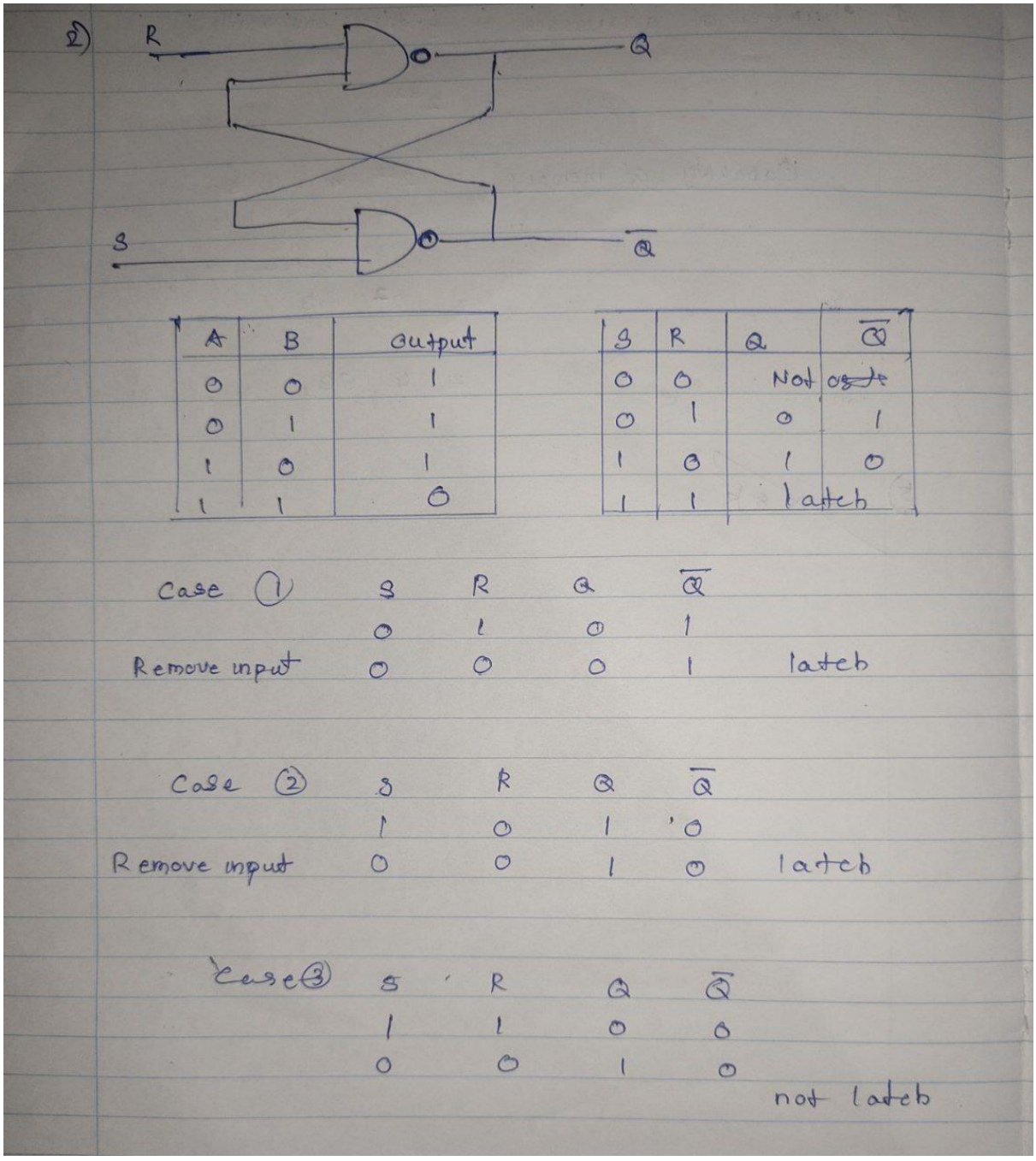


Question 5

1)

- ✓ Because sequential circuits contain a memory element, they may be utilized to store digital data.
- ✓ Because the output of sequential circuits is dependent on the current and previous inputs, they may be used to compare the condition of a panel.
- ✓ Because the clock signal is so important to the system, we may utilize it as the system's power value, which can then be used as the system's primary switch.

2)



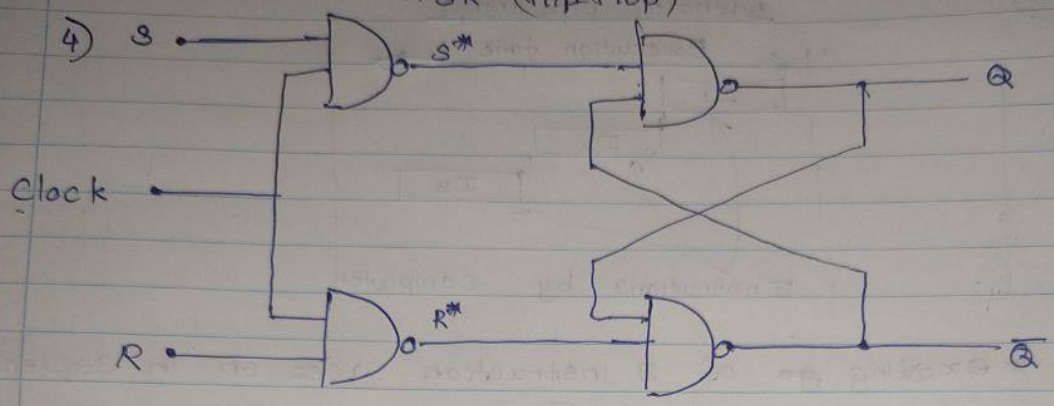
3)

The "Data" input is referred to as the single input "D." As a result, it will not change its state and will store the data that was present on its output before to the clock shift. To put it another way, the output is "latched" at 0 or 1.

4)

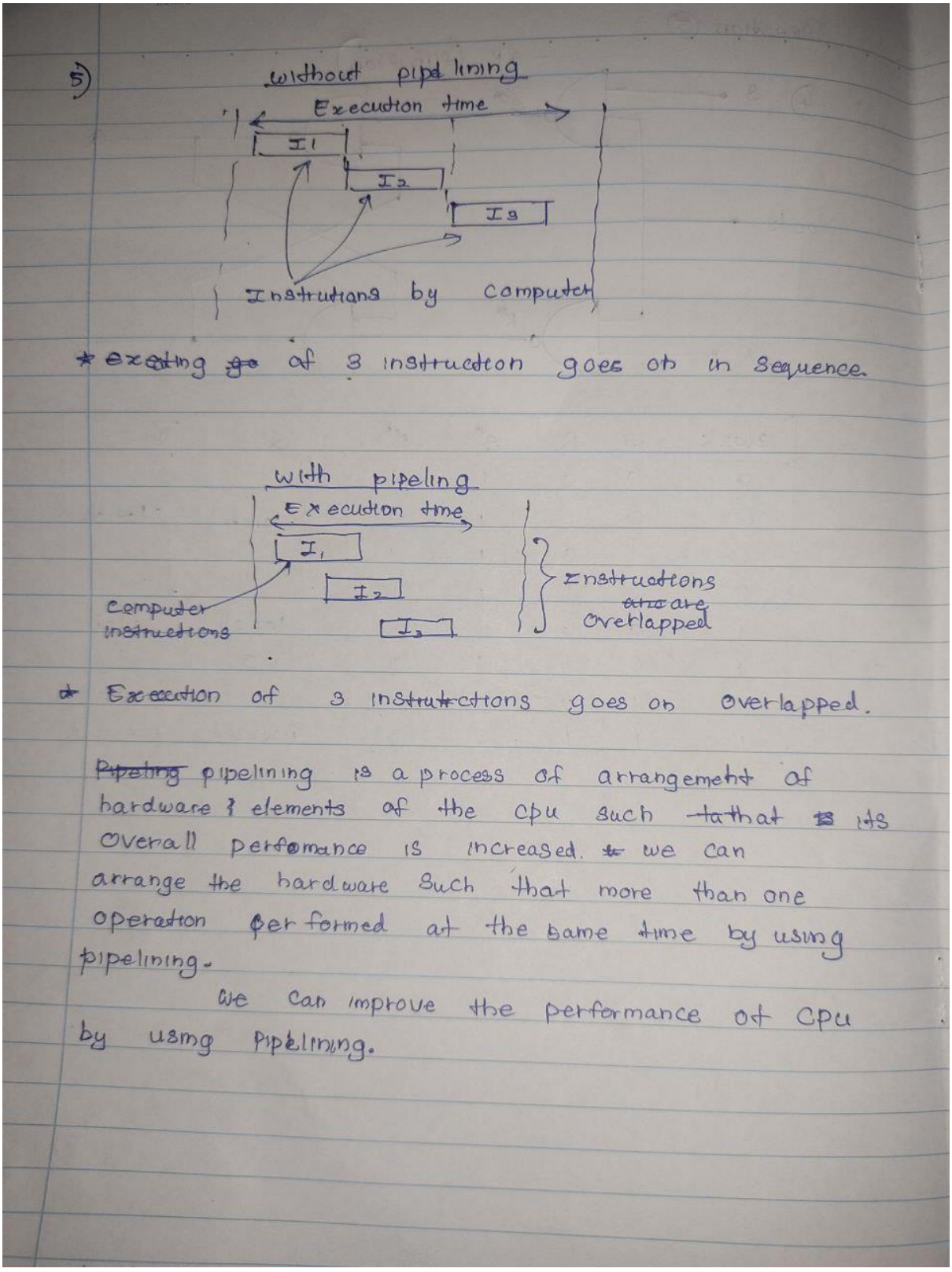
Question (5)

- SR (flip-flop)



clock	S	R	S^*	R^*	Q	$\overline{Q}$
0	0	0	1	1	latch	latch
0	0	1	1	1		
0	1	0	1	1		
0	1	1	1	1		
1	0	0	1	1	latch	latch
1	0	1	1	0	0	1
1	1	0	0	1	1	0
1	1	1	0	0	not used	not used

5)



* Execution of 3 instructions goes on in sequence.

* Execution of 3 instructions goes on overlapped.

Pipelining is a process of arrangement of hardware elements of the cpu such that its overall performance is increased. we can arrange the hardware such that more than one operation performed at the same time by using pipelining.

We can improve the performance of cpu by using pipelining.

6)

Because the output remains constant unless the state of the D input is altered followed by a rising clock signal, the D Flip Flop functions as an electronic memory component.

The D Flip Flop is a shift register building piece. For example, after 8 clock cycles, a byte (8 bits) of information may be stored by cascading eight D Flip Flops in sequence.

A simple divide by two circuit is built by connecting the inverting output of the D Flip Flop to the D input, in which the D output changes state at half the frequency of the clock signal. A countdown timer may be made by cascading D flip flops and using the right combination of external combinational logic gates.