ECEN 2350 Spring 2017 Homework 4
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1. *Book Problems: 5.7, 5.10, 5.16, 5.25*

   5.7: *Show how a JK flip-flop can be implemented with a T flip-flop and other gates.*
   Placeholder answer

   5.10: *Write the behavioral Verilog code for a JK flip-flop.*
   Placeholder answer

   5.16: *Design a three bit up/down counter using T flip-flops, using a control signal of* $\overline{UP}/DOWN$.
   Placeholder answer

   5.25: *Using the circuit shown in the book, complete the below timing diagram.*
   Placeholder answer

2. *Draw a 4-bit Universal shift register that can parallel load, shift left, shift right, and synchronously clear. Provide a characteristic table for the control operations.*

   Placeholder answer

3. *Implement a 3-bit up-counter using only one D flip-flop, one T flip-flop, one JK flip-flop and one AND gate. Assume all flip-flops are positive edge triggered. Show your circuit and a timing diagram.*

   Placeholder answer

4. *Write the behavioural Verilog for 5.16, calling the module* `up_down_counter`.

   Placeholder answer