ECEN 2350 Spring 2017 Homework 8
Samuel Cuthbertson

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1. *Book Problems: 6.9, 6.11*

   6.9: *A sequential circuit has two inputs, w_1 and w_2, and an output z. Its function is to compare the input sequences on the two inputs. If $w_1 = w_2$ during any four consecutive clock cycles, the circuit produces $z = 1$; otherwise, $z = 0$. Derive a suitable circuit.*

   6.11: *A given FSM has an input, w, and an output, z. During four consecutive clock pulses, a sequence of four values of the w signal is applied. Derive a state table for the FSM that produces $z = 1$ when it detects that either the sequence $w : 0010$ or $w : 1110$ has been applied; otherwise, $z = 0$. After the fourth clock pulse, the machince has to be again in the reset state, ready for the next sequence. Minimize the number of states needed.*

2. *Book Problem: B.2*

   a: *Show that the circuit in Figure PB.2 is fuctionally equivalent to the circuit in Figure PB.1.*

   b: *How many transistors are needed to build this CMOS circuit? Draw the CMOS circuit.*

3. *Book Problem: B.7*

   a: *Give the truth table for the CMOS circuit in the Figure PB.5.*

   b: *Derive the simplest sum-of-products expression for the truth table in (a). How many transistors are needed to build the sum-of-products circuit using the CMOS AND, OR and NOT gates?*

4. *Given the following schematic from the Texas Instruments CMOS BCD to 7-segment decoder CD4511B, estimate the number of transistors this circuit needs. You cannot ignore the FlipFlops at the inputs to the circuit (the box that is labeled as a PTGN). These are toggle flip flops with preset/clear. Model these like the example from class.*