ECEN 2350 Spring 2017 Homework 4
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1. *Book Problems: 2.77 and 2.78*

(2.77) *What is the cost of the circuit shown in the book, assuming the input variables are available in both true and complemented forms? Redesign the circuit to implement the same functions, but at as low a cost as possible. What is the cost of your circuit?*

Noting that the circuit can be expressed as the logic equations:

$$f = \overline{(x_1 + x_3 + x_4)} + x_4(x_1 + x_3) + \overline{x_1}\,\overline{x_2}x_3 + x_1x_2\overline{x_3}\,\overline{x_4}$$
$$g = x_1x_2\overline{x_3}\,\overline{x_4} + \overline{x_2}x_4 + x_3(\overline{x_1} + \overline{x_4}) + \overline{(x_1 + x_4)}$$

Which, noting that $x_1x_2\overline{x_3}\,\overline{x_4}$ is in both equations and only in the circuit once, as well as assuming that the complemented form of each variable is available for free, has the cost of $((1+2+1+1)+1)+((1+2+1)+1) = 6+5 = 11$ gates and $((3+(2+2)+3+4)+4)+((2+(2+2)+2)+4) = 18+12 = 30$ inputs. Total cost is then $30+11 = \boxed{41}$
Additionally, the logic equations above can be expanded into:

$$f = \overline{x_1}\,\overline{x_3}\,\overline{x_4} + x_4x_1 + x_4x_3 + \overline{x_1}\,\overline{x_2}x_3 + x_1x_2\overline{x_3}\,\overline{x_4} \quad \textit{Distributive, DeMorgan's}$$
$$g = x_1x_2\overline{x_3}\,\overline{x_4} + \overline{x_2}x_4 + x_3\overline{x_1} + x_3\overline{x_4} + \overline{x_1}\,\overline{x_4} \quad \textit{Distributive, DeMorgan's}$$

$f = \overline{x_1}\,\overline{x_3}\,\overline{x_4} + x_4x_1 + x_4x_3 + \overline{x_1}\,\overline{x_2}x_3 + x_1x_2\overline{x_3}\,\overline{x_4}$

x_1x_2 \ x_3x_4	00	01	11	10
00	1	0	1	1
01	1	0	1	0
11	1	1	1	0
10	0	1	1	0

x_1x_2 \ x_3x_4	00	01	11	10
00	1	1	1	1
01	1	0	1	1
11	1	0	0	1
10	0	1	1	1

$g = x_1x_2\overline{x_3}\,\overline{x_4} + \overline{x_2}x_4 + x_3\overline{x_1} + x_3\overline{x_4} + \overline{x_1}\,\overline{x_4}$

Maximizing shared terms, we can further simplify the above into:

$f = \overline{x_1}\,\overline{x_2}\,\overline{x_4} + x_4 x_1 + \overline{x_1} x_3 x_4 + x_2 \overline{x_3}\,\overline{x_4}$

x_1x_2 \ x_3x_4	00	01	11	10
00	1	0	1	1
01	1	0	1	0
11	1	1	1	0
10	0	1	1	0

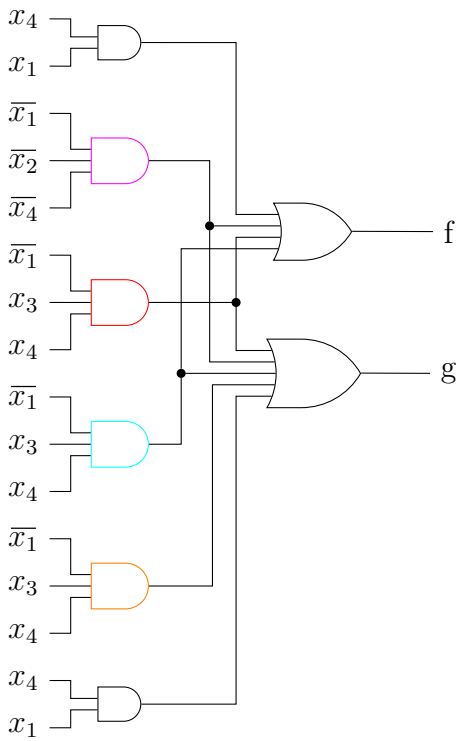
x_1x_2 \ x_3x_4	00	01	11	10
00	1	1	1	1
01	1	0	1	1
11	1	0	0	1
10	0	1	1	1

$g = \overline{x_1}\,\overline{x_2}\,\overline{x_4} + x_3 \overline{x_4} + \overline{x_1} x_3 x_4 + x_2 \overline{x_3}\,\overline{x_4} + \overline{x_1}\,\overline{x_2} x_4$

The above equations share terms $\overline{x_1}\,\overline{x_2}\,\overline{x_4}$, $\overline{x_1} x_3 x_4$, $x_2 \overline{x_3}\,\overline{x_4}$. They can also be simplified further:

$$f = \overline{x_1}\,\overline{x_2}\,\overline{x_4} + x_4 x_1 + \overline{x_1} x_3 x_4 + x_2 \overline{x_3}\,\overline{x_4}$$
$$g = \overline{x_1}\,\overline{x_2}\,\overline{x_4} + x_3 \overline{x_4} + \overline{x_1} x_3 x_4 + x_2 \overline{x_3}\,\overline{x_4} + \overline{x_1}\,\overline{x_2} x_4$$

Thus the cost of the circuit would be $((1+1+1+1)+1)+((1+1)+1) = 5+3 = 8$ gates and $((3+2+3+3)+4)+((2+3)+5) = 15+10 = 25$ inputs, for a total cost of $8+25 = \boxed{33}$



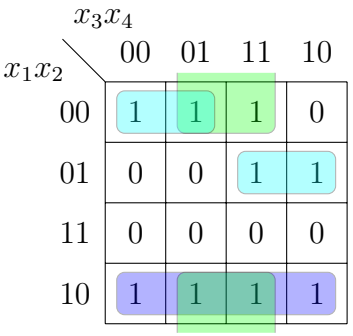
(2.78) *What is the cost of the circuit shown in the book, assuming the input variables are available in both true and complemented forms? Redesign the circuit to implement the same functions, but at as low a cost as possible still using only NAND gates. What is the cost of your circuit?*

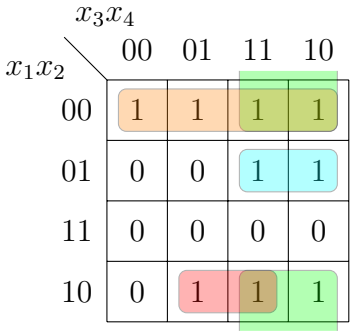
Noting that the circuit can be expressed as the logic equations:

$$f = x_1\overline{x_2} + \overline{x_1}(x_2 \otimes x_3) + \overline{x_2}x_4$$
$$g = \overline{x_2}x_3 + \overline{x_1}x_3 + \overline{x_1}\,\overline{x_2} + \overline{x_2}x_4$$

Which can be examined in the below K-Maps:

$f = x_1\overline{x_2}+\overline{x_1}(x_2 \otimes x_3)+\overline{x_2}x_4$

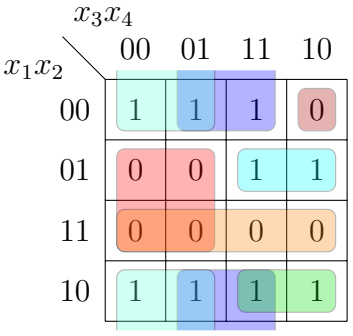


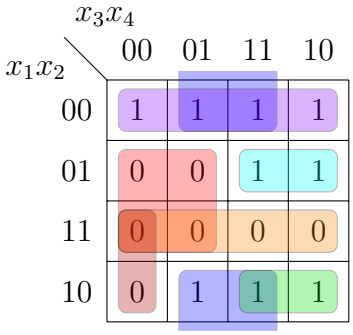


$g = \overline{x_2}x_3+\overline{x_1}x_3+\overline{x_1}\,\overline{x_2}+\overline{x_2}x_4$

Simplifying the above maps into optimal covers, we see:

$f = (\overline{x_2} + \overline{x_2})(\overline{x_2} + x_3)(x_1 + x_2 + \overline{x_3} + x_4)$
$f = \overline{x_2}x_4+\overline{x_1}x_2x_3+x_1\overline{x_2}x_3+\overline{x_2}\,\overline{x_3}$





$g = (\overline{x_1} + \overline{x_2})(\overline{x_2} + x_3)(\overline{x_1} + x_3 + x_4)$
$g = \overline{x_2}x_4+\overline{x_1}x_2x_3+x_1\overline{x_2}x_3+\overline{x_1}\,\overline{x_2}$

And in analayzing the cost:

$$POS = \text{Gates} + \text{Inputs} = (3 + 1 + 1 + 1) + (2 + 2 + 4 + 3 + 3 + 3) = 23$$
$$SOP = \text{Gates} + \text{Inputs} = (4 + 1 + 1 + 1) + (2 + 3 + 3 + 2 + 2 + 4 + 4) = 27$$

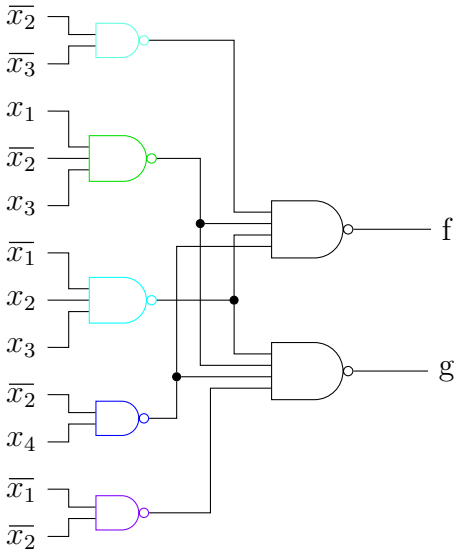
However, SOP has zero additional cost in converting to NANDs while this POS will have at least an addition of 6, as each output (f and g) will have to be inverted

and a NAND inverter has cost 3 (2 inputs, 1 gate). Therefor, as $23+6=29>27$ SOP is the cheapest option for NAND implementation.

Also noting that the SOP equations can be manipulated into NANDs as follows:

$$f = \overline{x_2}x_4 + \overline{x_1}x_2x_3 + x_1\overline{x_2}x_3 + \overline{x_2}\,\overline{x_3}$$
$$g = \overline{x_2}x_4 + \overline{x_1}x_2x_3 + x_1\overline{x_2}x_3 + \overline{x_1}\,\overline{x_2}$$

The circuit is shown below:

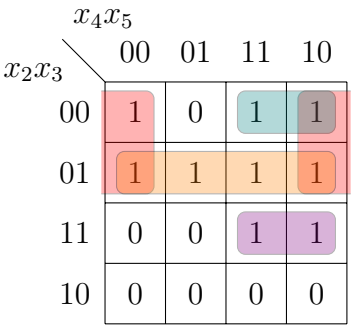


And cost can be counted out as 20 inputs and 7 gates, for a total cost of $\boxed{27}$

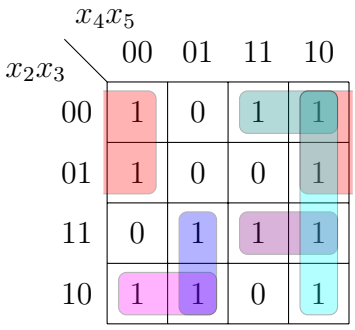
2. *Given the 5 variable logic function below, determine:*

$$f(x_1, x_2, x_3, x_4, x_5) = \sum m(0, 2, 3, 4, 5, 6, 7, 14, 15, 16, 18, 19, 20, 22, 24, 25, 26, 29, 30, 31)$$

(a) *A minimum cost SOP implementation*



$x_1 = 0$



$x_1 = 1$

Thus, our logic equation is

$$f = \overline{x_2}\,\overline{x_4} + \overline{x_1}\,\overline{x_2}x_4 + x_2x_3x_4 + \overline{x_2}x_3\overline{x_1} + x_1\overline{x_5}x_4 + x_2\overline{x_4}x_5x_1 + x_2\overline{x_3}\,\overline{x_4}x_1$$

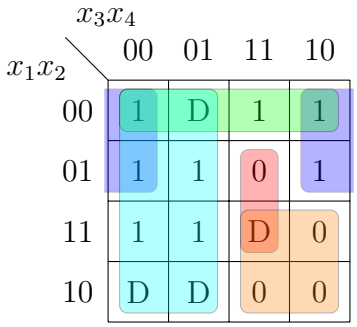
(b) *The cost of the SOP implmentation (ANDs, ORs and NOTs)* We have our cost as follows:

$$\text{ANDs} + \text{ORs} + \text{NOTs} + \text{AND Inputs} + \text{OR Inputs} + \text{NOT Inputs} = \text{Cost}$$
$$7 + 1 + 5 + (2 + 3 + 3 + 3 + 3 + 4 + 4) + 7 + 5 = \boxed{47}$$

3. *Given the incompletly specified logic function, determine the following:*

$$f(x_1, x_2, x_3, x_4) = \sum m(0, 2, 3, 4, 5, 6, 12, 13) + D(1, 8, 9, 15)$$

(a) *Minimum cost SOP and POS implementations*



$$SOP = \overline{x_3} + \overline{x_1}\,\overline{x_2} + \overline{x_1}\,\overline{x_4}$$
$$POS = (\overline{x_2} + \overline{x_3} + \overline{x_4})(\overline{x_1} + \overline{x_3})$$

(b) *The cost of the SOP and POS implmentation (Including NOT gates)*
The cost of the SOP implementation would be:

$$4 + 2 + 1 = 7 \text{ gates}$$
$$4 * 1 + 2 * 2 + 1 * 3 = 11 \text{ inputs}$$
$$= \boxed{18 \text{ total cost}}$$

And for POS:

$$4 + 2 + 1 = 7 \text{ gates}$$
$$4 * 1 + 1 * 3 + 1 * 2 + 1 * 2 = 11 \text{ inputs}$$
$$= \boxed{18 \text{ total cost}}$$

4. *Derive the logical equations for the multiple output circuit for a 7-Segment Decoder. It should have inputs b_3, b_2, b_1, b_0 and outputs a, b, c, d, e, f, g. Your circuit should be able to display all 16-Hex Characters.*

   Assuming that the 7-segment display is formatted as a-f being top to top left segments clockwise, with g as the middle segment, and that our LEDs are high activated.

   We then can create the truth table for our decoder:

v	$b_0..b_3$	a	b	c	d	e	f	g
0	0000	1	1	1	1	1	1	0
1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	0	0	0	0	0	0	0
4	0100	0	1	1	0	0	1	1
5	0101	1	0	1	1	0	1	1
6	0110	1	0	1	1	1	1	1
7	0111	1	1	1	0	0	0	0
8	1000	1	1	1	1	1	1	1
9	1001	1	1	1	1	0	1	1
a	1010	1	1	1	0	1	1	1
b	1011	0	0	1	1	1	1	1
c	1100	0	0	0	1	1	0	1
d	1101	1	1	1	1	1	0	1
e	1110	1	0	0	1	1	1	1
f	1111	1	0	0	0	1	1	1

Which allows us to take the set of b's for each instance of an LED being hot, or 1, and combine logic terms into an expression for that LED.

$$a = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}\overline{b_1}b_2\overline{b_3} + \overline{b_0}b_1\overline{b_2}b_3 + \overline{b_0}b_1b_2\overline{b_3} + \overline{b_0}b_1b_2b_3 + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3} + b_0b_1b_2b_3$$

$$b = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}\overline{b_1}\overline{b_2}b_3 + \overline{b_0}\overline{b_1}b_2\overline{b_3} + \overline{b_0}b_1\overline{b_2}\overline{b_3} + \overline{b_0}b_1b_2b_3 + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3}$$

$$c = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}\overline{b_1}\overline{b_2}b_3 + \overline{b_0}b_1\overline{b_2}\overline{b_3} + \overline{b_0}b_1\overline{b_2}b_3 + \overline{b_0}b_1b_2\overline{b_3} + \overline{b_0}b_1b_2b_3 + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2\overline{b_3} + b_0\overline{b_1}b_2b_3 + b_0b_1\overline{b_2}b_3$$

$$d = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}\overline{b_1}b_2\overline{b_3} + \overline{b_0}b_1\overline{b_2}b_3 + \overline{b_0}b_1b_2\overline{b_3} + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2b_3 + b_0b_1\overline{b_2}\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3}$$

$$e = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}\overline{b_1}b_2\overline{b_3} + \overline{b_0}b_1b_2\overline{b_3} + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}b_2\overline{b_3} + b_0\overline{b_1}b_2b_3 + b_0b_1\overline{b_2}\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3} + b_0b_1b_2b_3$$

$$f = \overline{b_0}\overline{b_1}\overline{b_2}\overline{b_3} + \overline{b_0}b_1\overline{b_2}\overline{b_3} + \overline{b_0}b_1\overline{b_2}b_3 + \overline{b_0}b_1b_2\overline{b_3} + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3} + b_0b_1b_2b_3$$

$$g = \overline{b_0}\overline{b_1}b_2\overline{b_3} + \overline{b_0}b_1\overline{b_2}\overline{b_3} + \overline{b_0}b_1\overline{b_2}b_3 + \overline{b_0}b_1b_2\overline{b_3} + b_0\overline{b_1}\overline{b_2}\overline{b_3} + b_0\overline{b_1}\overline{b_2}b_3 + b_0\overline{b_1}b_2\overline{b_3} + b_0\overline{b_1}b_2b_3 + b_0b_1\overline{b_2}\overline{b_3} + b_0b_1\overline{b_2}b_3 + b_0b_1b_2\overline{b_3} + b_0b_1b_2b_3$$

5. *Given the circuit in the homework that has a* $4:1$ *Multiplexer, what is the logical equation f(a,b)?*

   Note that the following truth table describes the multiplexer shown, where m is which variable the multiplex outputs, and f is the actual output value:

a	b	s_0	s_1	m	f
0	0	0	0	a	0
0	0	0	1	b	0
0	0	1	0	a	0
0	0	1	1	b	0
0	1	0	0	a	0
0	1	0	1	b	1
0	1	1	0	a	0
0	1	1	1	b	1
1	0	0	0	a	1
1	0	0	1	b	0
1	0	1	0	a	1
1	0	1	1	b	0
1	1	0	0	a	1
1	1	0	1	b	1
1	1	1	0	a	1
1	1	1	1	b	1

   As $\bar{a} = s_0 = s_1$, we can exclude lines where $\bar{a} \neq s_0 \neq s_1$, leaving us with the below:

a	b	s_0	s_1	m	f
0	0	1	1	b	0
0	1	1	1	b	1
1	0	0	0	a	1
1	1	0	0	a	1

   And thus our logic equation is:

$$\boxed{f = a + b}$$