Digital Logic: Project 2 Block Diagrams

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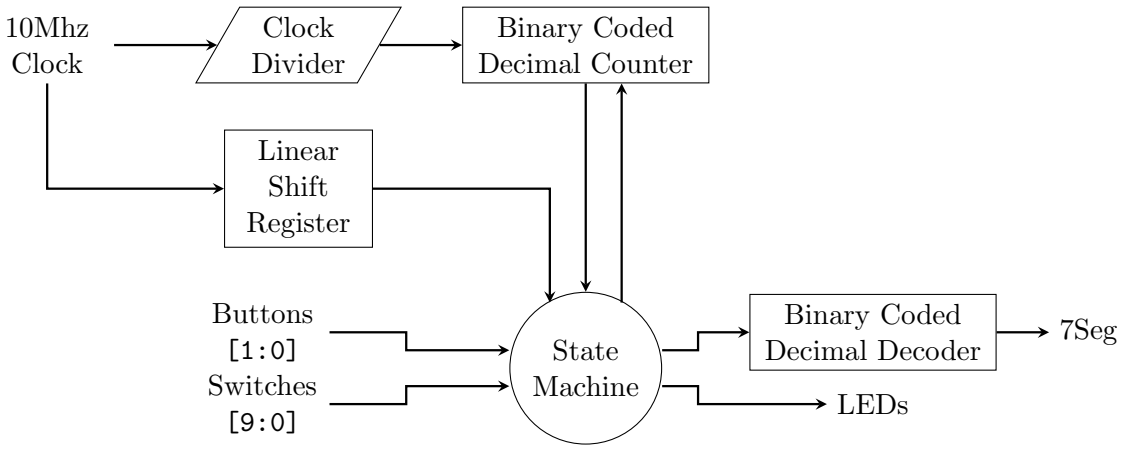
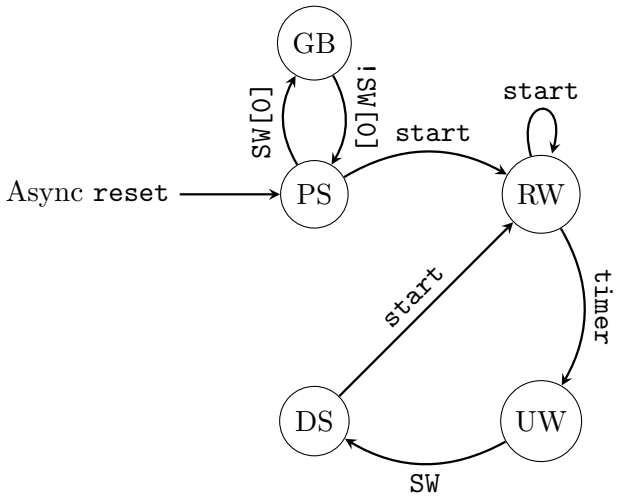


Figure 1: Our block diagram for top.v.



State Name	Description
PS	Mode we boot into, displays highscore.
GB	Diplays a scrolling "Go Buffs".
RW	Waits a random time interval.
UW	Counts the time spent here.
DS	Displays the value from the counter, updates highscore.

Figure 2: Our graph for the State Machine in top.v, where `B0` is the start button, `B1` is the reset button, and `SW` is assumed to be the correct switch. Additionally, all buttons are assumed to be active-low and all switches are assumed to be active-high.