LCD Driver Amplifier Design

Chandrahaas Vadali

EE240A Project Report

1 Overview

This report presents the design and implementation of an amplifier tailored for driving a specific LCD sub-pixel in a smartwatch application. The subsequent sections detail the complete design flow, beginning at the derivation of high-level design metrics from the given specifications, preliminary design calculations, and the realization of a functional design. The final design meets all specified requirements, as summarized in table 1. All the transistors used in this design are nmos/pmos2v while the passive components are implemented using mimcap and resnsnpoly.

Parameter	**Target Spec**	**Design Spec**
Settling Time (T_{set})	$\leq$ 180 ns	154.6 ns (-14%)
Total error	$\leq$ 0.2%	$\leq$ 0.1%
Power Consumption	$\leq$ 1.5 mW	0.33 mW (-78%)
Max Current Mirror Ratio	10	10
Max Total Capacitance	5 pF	75 fF
Max Total Resistance	100 kΩ	6.5 kΩ
CMRR at DC	$\geq$ 70 dB	70.14 dB
PSRR (VDDL) at DC	$\geq$ 50 dB	51.53 dB
PSRR (VDDH) at DC	$\geq$ 50 dB	62.42 dB
Phase Margin (PM)	$\geq$ 45°	51.53°
Figure of Merit	$\geq$ 3.70	19.53 (+427%)

Table 1: LCD Driver Amplifier specs reported 350 mV input step

1.1 Gain stages

Figure 1 illustrates the complete schematic of the amplifier, comprising two gain stages and an associated biasing network. The first gain stage employs a telescopic cascode configuration to achieve high gain while operating at a low supply voltage V_{DDL}. The single-ended output of the first stage connects to the NMOS input of the second stage, which is implemented as a class AB common-source amplifier. A PMOS-based source follower is incorporated to perform level-shifting and provide the input to the PMOS device of the second stage.

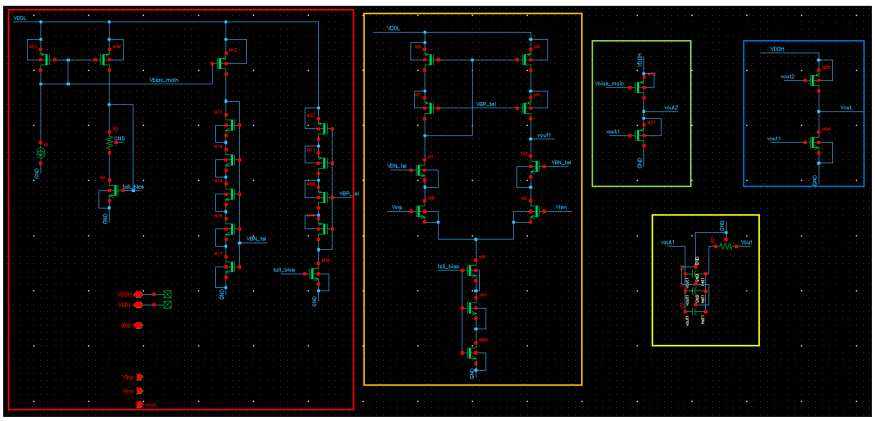

Figure 1: Amplifier schematic: red - biasing network, orange - telescopic cascode, green - source follower, blue - Class-AB stage, yellow - Miller compensation.

The schematic on the left side in Figure 2 depicts the first gain stage, which is implemented as a telescopic cascode amplifier. M0 and M2 serve as the input transistors, receiving the differential inputs V_{inp} and V_{inn}, respectively. Transistors M1 and M3 form the cascode configuration on the input side, enhancing gain and output impedance. The PMOS transistors M4 and M5, along with their biasing counterparts M6 and M7, function as the active load. Notably, M6 is implemented in a wide-swing configuration, enabling operation at lower supply voltages. This choice will be discussed in greater detail in subsequent sections. M8, M31, and M32 are used to generate the tail current.

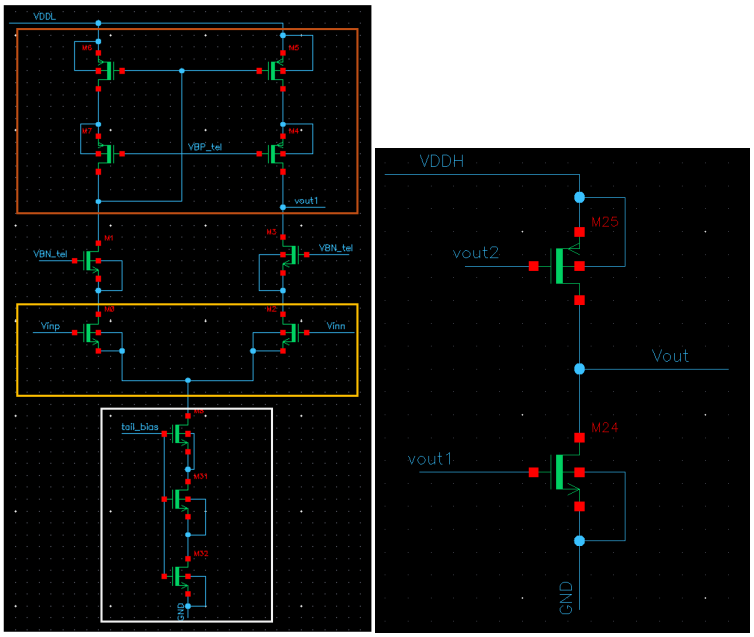

Figure 2: (Left) First stage - telescopic cascode (right) second stage - class AB common source amplifier

The schematic on the right side in Figure 2 illustrates the second gain stage, implemented as a class AB common-source amplifier. Transistors M25 and M24 constitute the PMOS and NMOS

devices in the inverter-based configuration, respectively. This stage is designed to address slew-rate limitations while delivering sufficient overall gain.

1.2 Biasing

Figure 3 shows the biasing network, which primarily biases the first gain stage and the source follower preceding the second stage. Transistor M11 generates the main bias voltage, which is then replicated across each branch to bias the tail, NMOS cascode, and PMOS cascode devices.

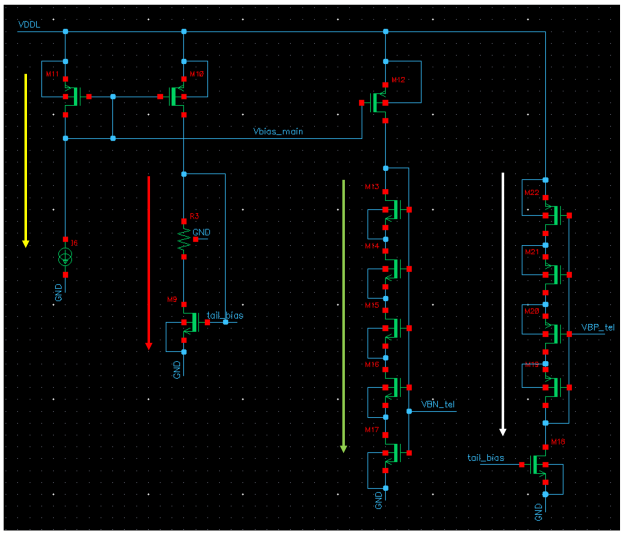

Figure 3: Biasing network: Yellow - primary bias generator, red - bias for tail transistor, green - for NMOS cascode load, white - for PMOS cascode load

1.3 Source Follower

Figure 4 illustrates the source follower used as a level-shifter to bias the PMOS transistor in the class AB stage. The output of this stage is then connected to the sub-pixel load model.

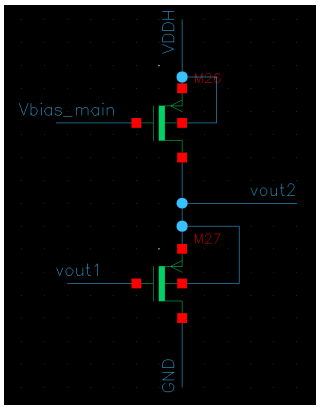

Figure 4: Source Follower - level-shifts the input from first stage to feed to the PMOS of the class AB stage

2 Design

In this section, the process of extracting relevant high-level amplifier specifications from the given design parameters is outlined. The initial design approach is presented, including high-level amplifier specs, the selection of the basic topology for each stage, followed by a description of how the g_m/I_D methodology scripts were set up to guide the design.

2.1 Derivation of High-Level Amplifier Specifications

Settling time (T_{set}) and the error budget (ϵ_{bud}) provide a starting point to our design. With a refresh rate of 60 Hz and a display resolution of 272 x 340 pixels, T_{set} is roughly

$$T_{set} = \frac{1}{Refresh\ rate\ \times\ Resolution} = \frac{1}{60 \times (272 \times 340)} \approx 180\ ns$$

The first design choice involves partitioning ϵ_{bud} into a static error (ϵ_s) and a dynamic error (ϵ_d). For a given feedback f, the minimum open loop DC gain A_0 is given by

$$A_0 = \frac{1}{f}\left(\frac{1-\epsilon_s}{\epsilon_s}\right)$$

Since we have constraints on phase margin (PM) and T_{set}, we can design our unity gain frequency (f_u) of the loop gain from ϵ_d,

$$f_u \approx \frac{-ln(\epsilon_d)}{T_{set}} = \frac{-ln(0.002-\epsilon_s)}{T_{set}}$$

Figure 5 shows the minimum values for A_0 and f_u as a function of static error. It is evident that for a smaller static error (and consequently, a larger dynamic error budget), the amplifier requires a very high DC gain and a relatively relaxed unity gain frequency. In the design, I made the decision to prioritize higher gain rather than evenly distributing the 0.1% allocation between ϵ_s and ϵ_d. This was based on the belief that designing a transistor with high gain using the g_m/I_D method would be more straightforward compared to the complexities of tuning the non-dominant pole and f_u. Pole placement could be challenging due to the potential influence of parasitics, especially considering that the output stage might need to be sufficiently large to prevent slewing with a 0.35 V input step.

The starting point of the design was to create an amplifier capable of achieving an open-loop gain of approximately 7500 (77.5 dB) and a unity gain frequency of around 36 MHz, as indicated by the star in figure 5.

2.2 Topology Selection

The gain was distributed between the two stages, as depicted in figure 6. The selection of the first stage was straightforward due to the high-gain requirement, leading to the choice of a telescopic cascode configuration to fulfill this criterion. For the output stage, additional considerations were necessary, as it needed to supply substantial current to prevent slewing with a 0.35 mV step input.

$$\frac{dV_{out}}{dt} = \frac{1.4\ V}{T_{set}} = 7.76\ V/\mu S \approx \frac{I_{out,max}}{C_L} \implies I_{out,max} \approx 388\ \mu A$$

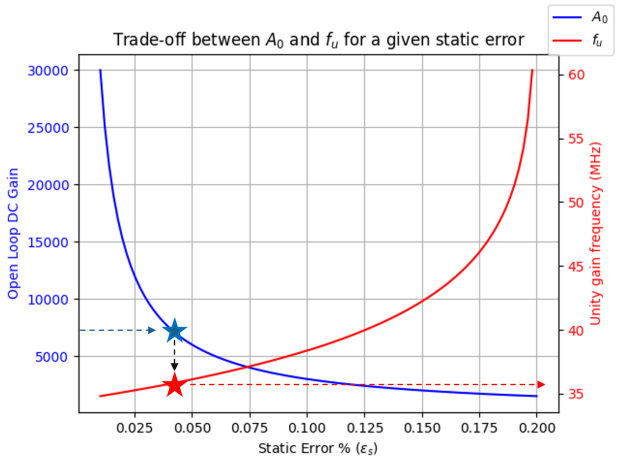

Figure 5: Trade-off between A_v and f_u as a function of static error

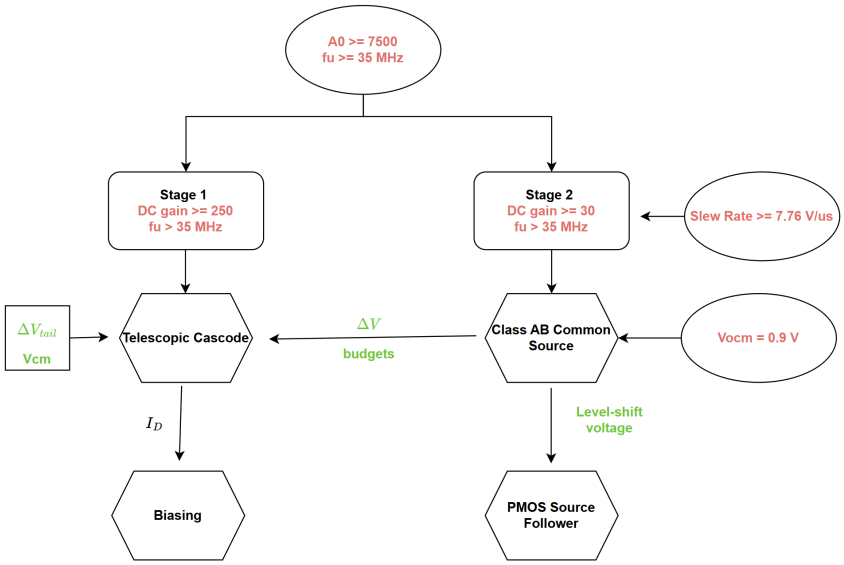

Figure 6: Algorithm for topology selection

Given that a standard common-source configuration might not supply the required current, a class AB common-source design was selected to address this limitation.

2.3 Design Approach

Since V_{ocm} at the output was fixed at 0.9 V and to achieve an output swing $\geq$ 1.4 V, the output stage was first designed to meet the criteria outlined in figure 6. This provided an estimate of the gate voltages required for the NMOS and PMOS transistors in the class AB stage, which in turn set the output bias voltage for the first stage. Using these values, I derived the ΔV budgets for both the NMOS and PMOS in the telescopic stage. Next, a source follower stage was selected to take the input from the first stage, level-shift it as needed, and pass it to the second stage. Finally, I designed the biasing circuits for the telescopic stage. Both gain stages were sized using

the g_m/I_D method to meet the constraints on each stage's gain and overall f_u. In the biasing circuit, the transistors were sized to match the current in each branch to the desired values. The source follower was designed to drop a V_{SG} equal to the level-shifting voltage.

2.3.1 Output Stage

From figure 6, we see the constraints on the class AB stage. In order to use the look up tables (LUTs), necessary constraints on V_{DS} were imposed while sweeping over different values of L and g_m/I_D. A sample of the code snippet is shown below.

```
L_range = nch2['L']
gm_ID_range = np.linspace(3,25,31)
ftn = look_up_vs_gm_id(nch,'GM_CGG',gm_ID_range,l=L_range,vds=
    Vout2CM)/2/np.pi
gdsn = look_up_vs_gm_id(nch,'GDS_ID',gm_ID_range,l=L_range,vds=
    Vout2CM)
gmn = gm_ID_range
... #similarly for PMOS
...
Avtot = (gmn+gmp)/(gdsn+gdsp) #Total gain for class AB CSA
... #Code for finding desired design points
... #Gate voltages for N and PMOS
desired_VGS_n = look_up_vgs_vs_gm_id(nch, desired_gm_ID, l=desired_L
    , vds=Vout2CM)
desired_VGS_p = look_up_vgs_vs_gm_id(pch, desired_gm_ID, l=desired_L
    , vds=Vout2CM)
```

This search, combined with the constraints of $A_{0,out} \geq 30$ and $f_u \geq 35$ MHz (f_t could be much higher), first yields a small set of g_m/I_D and L. Two design choices were made: first, a relatively high g_m/I_D was selected from the available set, followed by choosing the longest length among the available options. The bias voltages and transistor sizing were then determined using the LUTs, along with a preliminary estimate for $g_{mn} + g_{mp}$. Exact details are provided in the discussion section.

2.3.2 First Stage

Starting with the constraint $A_{0,first} \geq 250$ and $f_u \geq 35$ MHz (again, f_t could be much higher), along with the total budget of V_{DS} drops across the tail and the two NMOS cascode transistors which was given by the biasing voltages of the second stage, a similar script was used to filter through g_m/I_D and L candidates. The following equations guided the design to achieve the high gain (fig. 2):

$$A_{0,first} \approx g_{mn,M2} \times (g_{mn,M3} r_{0n,M3} r_{0n,M2} \,||\, g_{mp,M4} r_{0p,M4} r_{0p,M5})$$

Since the output stage was expected to consume significant power, the highest g_m/I_D available was chosen for this stage. A Miller compensation capacitor (C_c) was employed to set the g_m for each transistor. The method used to determine the initial estimate for C_c is detailed in a later section.

$$g_{mn} \approx C_C \times 2\pi f_u$$

The search space was set at the beginning when the input common-mode voltage (V_{cm}) was set to approximately 0.55 V, with a V_{DS} drop of 100 mV across the tail. Subsequently, V_{cm} was fine-tuned during simulations to enhance performance.

A critical decision at the first stage involved selecting between V_{DDL} and V_{DDH}, which depended on whether the output of the first stage would connect to the PMOS or NMOS of the class AB stage. To minimize power consumption in this stage, the output of the first stage was biased to allow a direct connection to the NMOS of the class AB stage. This design choice is elaborated in the discussion section.

With VDDL powering the first stage, a wide-swing configuration was necessary for the PMOS load to reduce the V_{DS} drop across each transistor, as illustrated in **Figure 7**. This configuration defined the V_{GS} and V_{DS} parameters on the LUT for the PMOS transistors, differentiating them from those of the NMOS transistors.

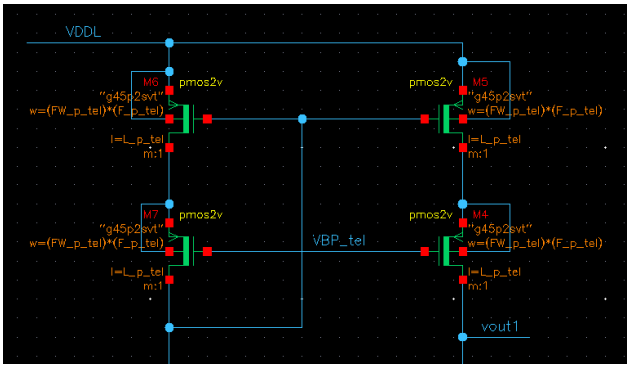

Figure 7: Active PMOS load with biasing for low-voltage applications

2.3.3 PMOS Source Follower

Designing the PMOS source follower was a straightforward process. The level-shifting voltage was calculated based on the output stage, as shown below:

$$V_{LS} = V_{GS,PMOS} - V_{GS,NMOS}$$

The V_{DS} for this stage was effectively the $V_{GS,NMOS}$ of the class AB stage. The transistor length was chosen to match those used in stage 1, and the LUT was employed to size it accordingly.

2.3.4 Miller Compensation

A standard Miller compensation capacitor, C_c, and a resistor, R_c, were connected between the outputs of the two stages, as shown in Fig. 8. With $g_{m,output}$ representing the total g_m of the class AB stage, R_c was calculated to push the right-half-plane (RHP) zero associated with the compensation technique to infinity using the following formula:

$$R_c \approx \frac{1}{g_{m,output}}$$

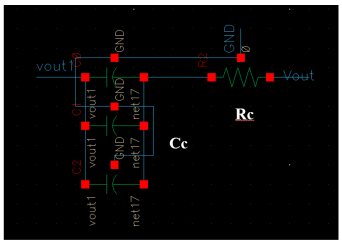

Figure 8: Miller compensation

2.3.5 Biasing network

To achieve additional power savings, the main bias generator was designed to be ten times smaller than the transistors in other branches and was biased with a current ten times lower than what was required to bias the first stage as shown in figure 9.

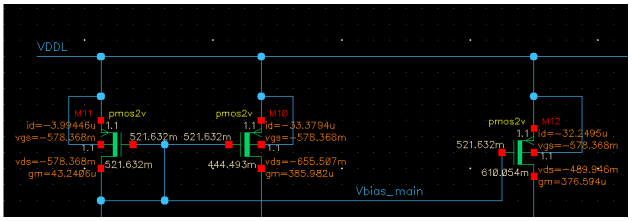

Figure 9: Primary bias generator with current mirror ratio of 10 between M11 ans M12

Another significant design choice involved stacking transistors to minimize variability and mismatch, as discussed in the following section.

2.4 Variability and Mismatch

A Monte Carlo Simulation was done on the AC test bench and the results are summarized in the table 2.4.

Parameter	**Mean**	**Std Dev**
DM Gain at DC	78.05 dB	75.76 dB
CM Gain at DC	24 dB	21.67 dB
CMRR at DC	52.25 dB	10.72 dV
PSRR VDDL at DC	48.16 dB	13.42 dB
PSRR VDDH at DC	61.34 dB	19.61 dB
Phase Margin	52.5 dB	4.73 dB
Unity gain OL	19.47 MHz	743.5 kHz

Table 2: Simulation Results

The design could be made more robust to process variations. Although the same-sized transistors were used as much as possible, mismatches in V_{DS}, sub-threshold operation, and other factors contribute to the variations observed. To improve the variation in the current mirrors, one possible solution is to stack identical transistors, rather than sizing them differently as was done in the current design to generate the additional ΔV_{tail} drop required to bias the NMOS cascode transistor

at $\Delta V_{tail} + 2\Delta V + V_{th}$. Finally, the amplifier's high gain ($\geq$ 85 dB) makes it susceptible to being thrown off-bias by noise at the input. A common-feedback technique could be employed to address this issue.

3 Transistor and Bias Summary

Table 3 shows a summary of dimensions and operating points for each transistor in the amplifier. Table 4 summarizes the passive components used.

XTOR	**Purpose**	**L (μm)**	**W (μm)**	I_D **(μA)**	V_{GS} **(V)**	g_m **(μS)**	g_m/I_D	g_{DS} **(μS)**
M0	Vinp	1	36	5.09	0.405	111.53	21.91	7.78
M1	NMOS cascode	1	36	5.09	0.393	111.89	21.98	3.61
M2	Vinn	1	36	5.09	0.405	111.52	21.91	7.78
M3	NMOS cascode	1	36	5.09	0.393	111.88	21.98	3.62
M8	Cascode tail	1	90	10.18	0.403	218.43	21.46	72.38
M33	Cascode tail	1	90	10.18	0.427	185.59	18.23	325.87
M34	Cascode tail	1	90	10.18	0.444	167.86	16.49	519.64
M4	PMOS cascode	1	6.7	5.09	-0.504	95.77	18.81	3.36
M5	PMOS cascode	1	6.7	5.09	-0.501	97.3	19.12	1.93
M6	PMOS cascode	1	6.7	5.09	-0.501	97.3	19.12	1.94
M7	PMOS cascode	1	6.7	5.09	-0.504	95.73	18.81	3.41
M11	Primary Bias Generator	1	1.34	3.99	-0.578	43.24	10.84	0.8
M10	Current source	1	13.4	33.37	-0.578	358.98	10.76	6.56
M12	Current source	1	13.4	32.24	-0.578	376.59	11.68	7.19
M9	Bias for tail xtor	1	90	33.37	0.444	647.59	19.41	29.53
M13	Bias for NMOS cascode	1	36	32.24	0.485	532.01	16.50	13.66
M14	Bias for NMOS cascode	1	36	32.24	0.534	361.02	11.20	493.90
M15	Bias for NMOS cascode	1	36	32.24	0.567	285.34	8.85	860.40
M16	Bias for NMOS cascode	1	36	32.24	0.592	243.47	7.55	1143.6
M17	Bias for NMOS cascode	1	45	32.24	0.61	214.01	6.64	1784
M22	Bias for PMOS cascode	1	6.7	20.61	-0.807	46.67	2.26	328
M21	Bias for PMOS cascode	1	6.7	20.61	-0.75	60.27	2.92	269
M20	Bias for PMOS cascode	1	6.7	20.61	-0.682	89.18	4.33	182.7
M19	Bias for PMOS cascode	1	6.7	20.61	-0.592	218.11	10.58	4.06
M18	Current source	1	54	20.61	0.444	397.94	19.31	15.9
M26	PMOS load for SF	4	1.8	18.20	-1.278	19.26	1.05	19.58
M27	SF PMOS	1	2.6	18.20	-0.597	121.90	6.69	2.13
M24	Class AB CSA PMOS	0.7	28	46.42	-0.628	740.66	16.08	11.28
M25	Class AB CSA NMOS	0.7	24	131.41	0.596	1411.07	10.73	24.20

Table 3: Transistor Parameters

Component	**Purpose**	**Value**	**L (μm)**	**W (μm)**
R3	Matching VDS for tail XTORs biasing	6000	30	1
C0	Miller Cap	30	5	5
C1	Miller Cap	30	5	5
C2	Miller Cap	15	2	5.5
R2	Resistor to cancel RHP from Miller Cap	500	2	5

Table 4: Component Parameters

4 Discussion and Results

This section provides an in-depth exploration of the design process, covering the methodology, deliberate design decisions, discrepancies between calculations and simulation results, and how these differences were addressed. A comprehensive analysis of the results is included, highlighting factors that contributed to meeting specifications as well as aspects that posed challenges. Finally, potential avenues for improvement are discussed.

4.1 Key Design Choices and Initial Setup

Several questions raised in Section 2, Design, are addressed and expanded upon in this section.

4.1.1 Class AB Common Source Amplifier

As outlined earlier, the design process began by addressing the constraints on DC gain (A_0), unity-gain frequency (f_u), slew rate, and the fixed V_{ocm}.

$$A_0 \geq 30$$

$$f_u \geq 35\ MHz$$

$$V_{DS,n} = V_{DS,p} = 0.9\ V$$

$$V_{DDH} = 1.8\ V$$

The g_m/I_D search space was defined within the range of 3 to 25, and the full range of transistor lengths available in the LUTs, spanning from 150 nm to 10 μm, was considered.

The left plot in **Figure 17** illustrates the values of g_m/I_D that meet the specified conditions. Each point on the plot corresponds to a different transistor length for a given g_m/I_D that satisfies the constraints. To mitigate variations and avoid short-channel effects, such as drain-induced barrier lowering, the transistor lengths were primarily set to 1 μm wherever feasible.

The first design choice was made here to choose a g_m/I_D of 12 as shown by the dotted line in **Figure 17**. I prioritized achieving high drive from this stage and opted not to start with an "efficient" transistor and then incrementally increase its width to meet the current requirements. I was concerned that a transistor with high transconductance efficiency might require a larger width, which could introduce parasitics and disrupt the non-dominant pole placement. To size the transistors, this estimate of g_m was then utilized

$$g_m = 2\pi f_u C_L$$

where C_L represents the load model that needs to be driven for the sub-pixel.

Summarized in Table 5 below are the starting points for the design of the output stage

Later in the simulations, it became apparent that the transistors were too wide, leading to significant parasitics and excessive quiescent power consumption. Consequently, adjustments were made to reduce the transistor sizes and decrease the quiescent current draw.

4.1.2 Telescopic Cascode Amplifier

From the V_{GS} values calculated in Table 5, two choices emerge for the bias point of the output of the first stage. If the output is to be connected directly to the PMOS, we have the following considerations:

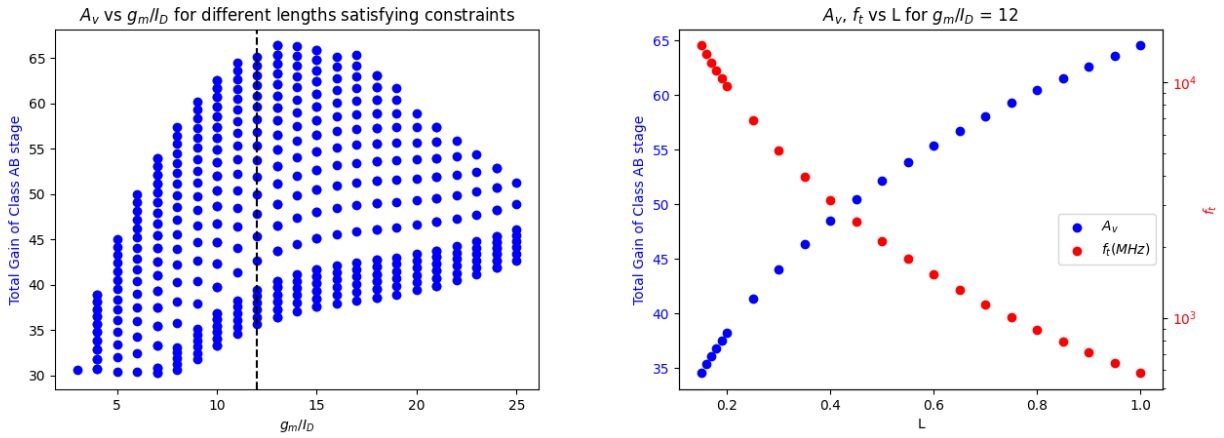

Figure 10: (Left) - Total gain of the class AB stage vs g_m/I_D for different lengths, (right) - A_v and f_t vs g_m/I_D for L = 1 μm

Parameter	Calculated Value
L_n and L_p	1 μm
W_n	449 μm
W_p	490 μm
g_{mn}+g_{mp}	17.27 mS
I_{DS}	1.57 mA
$V_{GS,N}$	0.575 V
$V_{GS,P}$	-0.579 V
$\lvert V_{LS}\rvert$	0.645 V

Table 5: Initial Class AB design parameters

$$V_{out1,CM} = V_{DDH} - V_{SG,p} = 1.22\ V$$

This would imply the use of V_{DDH} as the power supply. On the other hand, if the output of stage 1 is connected to the NMOS, we would have the following considerations:

$$V_{out1,CM} = V_{GS,n} = 0.575\ V$$

To conserve power, I opted to use V_{DDL} for the first stage. This decision introduced an additional constraint, further narrowing the design space for the first stage. Figure 11 summarizes the two choices.

On the PMOS active load side, I opted for a low-voltage cascode current mirror, as shown in figure 12. This choice reduces the voltage drop by V_{th}, increasing the total voltage budget to $V_{out11,CM} = V_{DD} - (2\Delta V + V_{th})$ [1].

Another design choice for the first stage was selecting the total $V_{DS} = \Delta V_{tail}$ drop across the tail transistor. I set this to 100 mV and chose V_{icm} to be 550 mV before starting the exploration. V_{cm} was later tuned to maximize a few performance metrics.

Unlike the earlier class AB stage design, the current stage requires selecting two distinct g_m/I_D values and channel lengths—one each for the NMOS and PMOS transistors. The following constraints were applied for each:

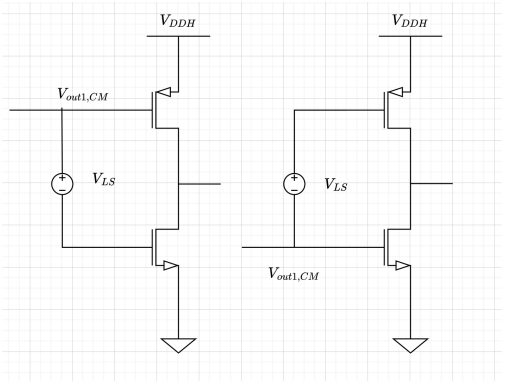

Figure 11: V_{LS} schemes based on which transistor in the Class-AB stage receives input directly from the first gain stage.

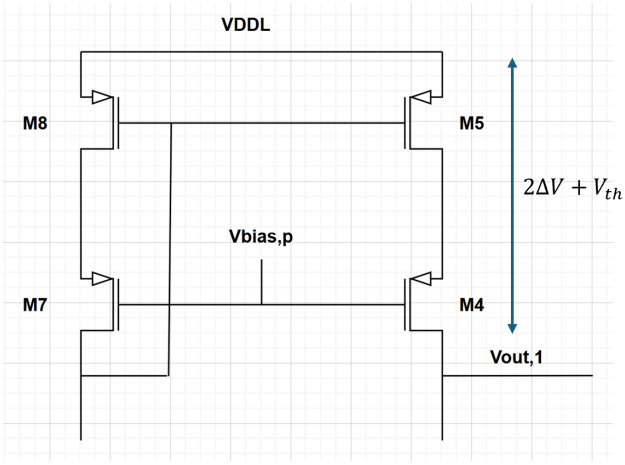

Figure 12: Low-voltage Cascode Current Mirror

$$A_0 \geq 250$$
$$f_u \geq 35\ MHz$$
$$\Delta V_{tail} = 100\ mV$$
$$V_{DS,n} = (V_{out1,CM} - \Delta V_{tail})/2 = V_{GS,N,AB} - 100\ mV$$
$$V_{DS,p} = (V_{DDL} - V_{out1,CM})/2 = 1.1\ - V_{GS,N,AB}$$
$$V_{GS,n} = V_{cm} - \Delta V_{tail} = 450\ mV$$
$$V_{GS,p} = V_{DS,p}$$
$$V_{DDL} = 1.1\ V$$

After exploring the design space, a high g_m/I_D value of 19 was chosen for the NMOS to ensure efficient signal amplification and high gain. For the PMOS, a moderate g_m/I_D value of 14 was selected. The lengths for both the NMOS and PMOS were set to 1 μm to minimize mismatch, consistent with the previously discussed design strategy. The value for g_{mn} for the first stage transistor was determined based on f_u and C_c. An initial choice for C_c was set at 0.5 pF since

the gain across the capacitor was anticipated to exceed 30, considering the class AB design. The starting points for the design are summarized in table 6

Parameter	Calculated Value
L_n and L_p	1 μm
C_c	0.5 pF
g_m/I_D NMOS	19
g_m/I_D PMOS	14
W_n	31.26 μm
W_p	6.72 μm
g_{mn}	0.236 mS
I_{DS}	12.4 μA
$I_{DS,tail}$	24.8 μA
$V_{GS,N}$	0.446 V
$V_{GS,P}$	-0.547 V

Table 6: Initial telescopic cascode design parameters

4.1.3 Tail Transistor

I fixed the length to 1 μm and used the LUTs by setting $V_{GS} = \Delta V_{tail} + V_{th}$ and as shown in the snipped below

```
1    #tail xtor
2    id_tail = 2*ID
3    gm_ID_tail = look_up_basic(nch,'GM_ID',vgs=deltaV_tail+Vt,vds=
         deltaV_tail,l=desired_L_n)
4    gm_tail = gm_ID_tail*id_tail
5
6    n_jd_tail = look_up_basic(nch,'ID_W',vgs=deltaV_tail+Vt,vds=
         deltaV_tail,l=desired_L_n)
7    wn_tail = id_tail/n_jd_tail
```

4.1.4 Source Follower

The source follower stage was not designed using LUTs. Instead, the same PMOS transistor as the telescopic stage was selected, and its width was reduced incrementally until the desired V_{GS} was achieved.

$$W_{p,SF} = \frac{V_{GS,P,tel}}{|V_{LS}|} \times W_{p,tel} \approx 0.84 \times 6.72\ \mu m = 5.69\ \mu m$$

The PMOS load for the source follower was initially sized to match the transistor whose current it was copying. Subsequently, its dimensions were adjusted to achieve the desired V_{DS} drop.

4.1.5 Biasing network

Figure 3 is replicated here in figure 13 for the reader's convenience. Figure 13 shows the schematic for the biasing network. A total of four biasing voltages were required: one for the tail transistor, one for the cascode NMOS, one for the cascode PMOS, and one for the source follower load PMOS.

The first step, however, was to generate the primary bias from the ideal current source provided. I used a current mirror ratio of 10 to 1.

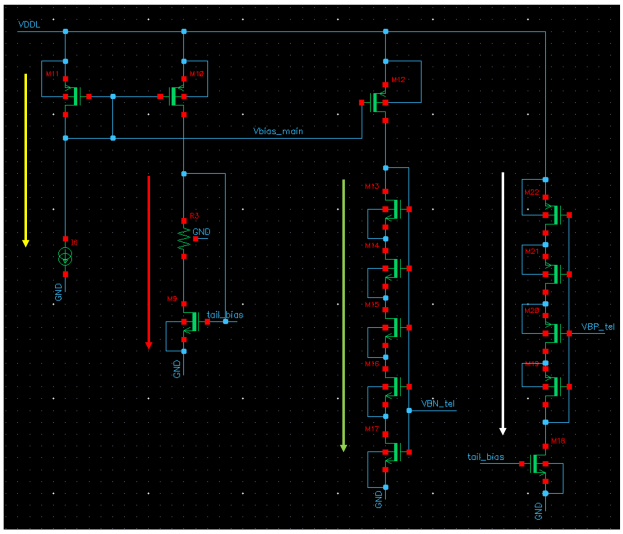

Figure 13: Biasing network: Yellow - primary bias generator, red - bias for tail transistor, green - for NMOS cascode load, white - for PMOS cascode load

To reduce power draw, I picked a 10× smaller drain current for M11 and sized the transistor M11 10× smaller than the PMOS load in the telescopic cascode. This branch is shown with a yellow arrow in figure 13.

The red branch has a PMOS current source M12 and an NMOS M9, which is the same size as the tail transistor. The resistor R3 was used for better matching V_{DS} so that the current can be copied accurately. This current matching was later sacrificed intentionally to increase ΔV_{tail} across the tail transistors and improve CMRR. This will be discussed later.

The white branch was used to generate $2\Delta V + V_{th}$ for the bottom PMOS cascode device, $V_{bias,p}$, as shown in Fig. 12. The bottom NMOS current source on this branch was sized half of the tail transistor since it needs only half the current and was biased from the red branch discussed previously. The green branch needed to generate a bias of $\Delta V_{tail} + 2\Delta V + V_{th}$. Similar to the white branch, four transistors were stacked with their gates tied together to generate the $2\Delta V$ part, and then an additional transistor, whose size was half that of the tail transistor, was placed to give the extra ΔV_{tail}.

The starting points for the current through each branch are summarized below in table 7.

Branch	**Purpose**	I_{DS}	**Sizing**
Yellow	Primary bias generator	$I_{DS,p,tel}/20 = I_{DS,tail}/10$	$W_{p,tel}/5$
Red	Biasing tail transistor	$I_{DS,tail}$	$W_{n,tail}$, 2*$W_{p,tel}$
Green	NMOS cascode load	$I_{DS,tail}/2$	$W_{n,tail}/2$, $W_{n,tel}$, 2*$W_{p,tel}$
White	PMOS cascode load	$I_{DS,tail}/2$	$W_{n,tail}/2$, $W_{p,tel}$

Table 7: Biasing network summary

The design was implemented in Cadence, and simulations were run across various test benches.

4.2 Test Benches

From the perspective of the test benches, the only parameter adjusted was the input DC bias point for the amplifier (V_{cm}), which was set to 0.5 V instead of 0.55 V. The supply voltages, VDDL and VDDH, remained unchanged at their specified values, while a common GND was used across all tests.

4.2.1 AC Test Benches

Figure 14 illustrates the setup used to extract the common-mode and differential-mode responses of the amplifier. **Figure 15** presents the test bench schematic for measuring the loop gain magnitude and phase. It is important to note that, since the positive and negative inputs of the amplifier schematic were not flipped to account for the two inverting stages, they were swapped in this test bench. Finally, **Figure 16** depicts the test setup for evaluating the power supply rejection ratios (PSRR).

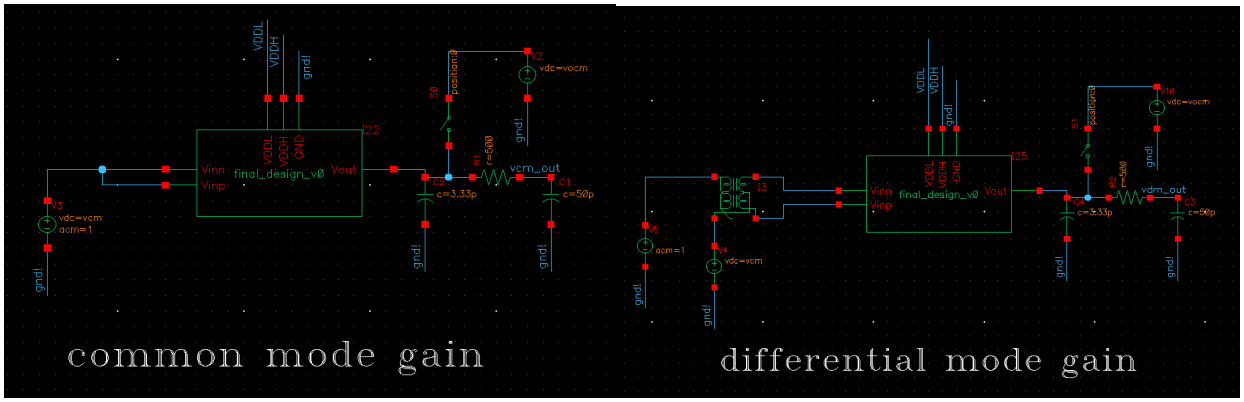

Figure 14: Common mode and differential mode test bench

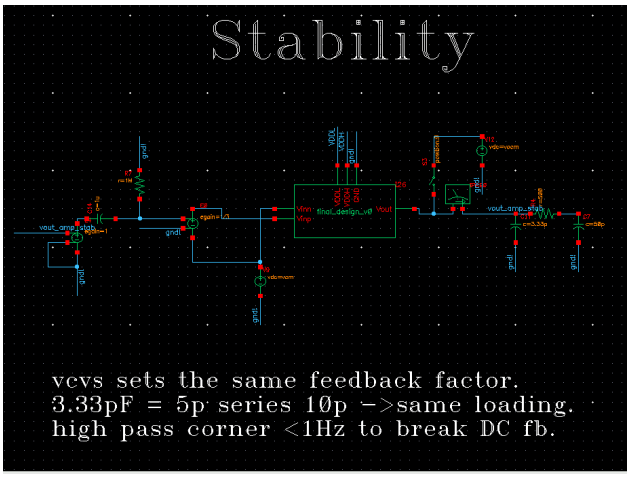

Figure 15: Stability test bench: inputs are flipped here as they were not inverted within the amplifier design

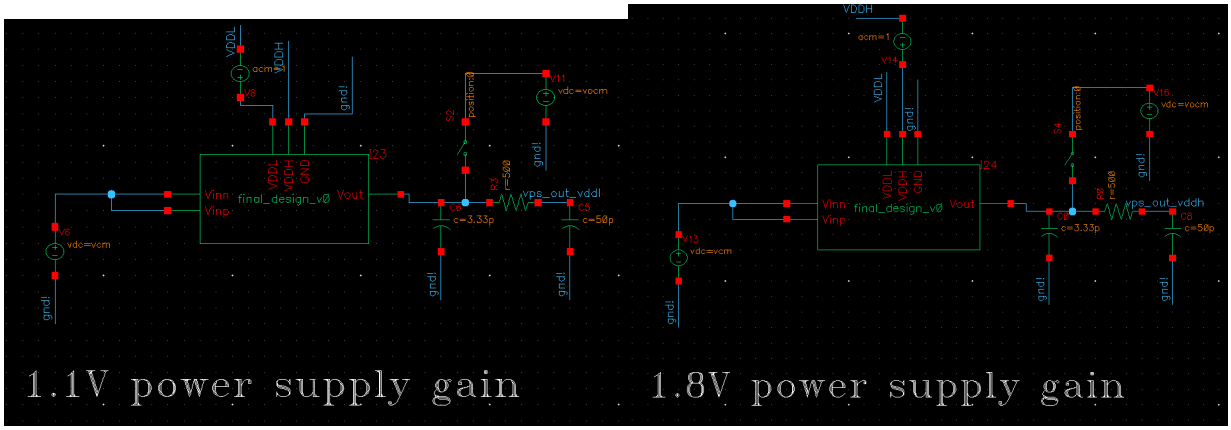

Figure 16: PSSR test bench

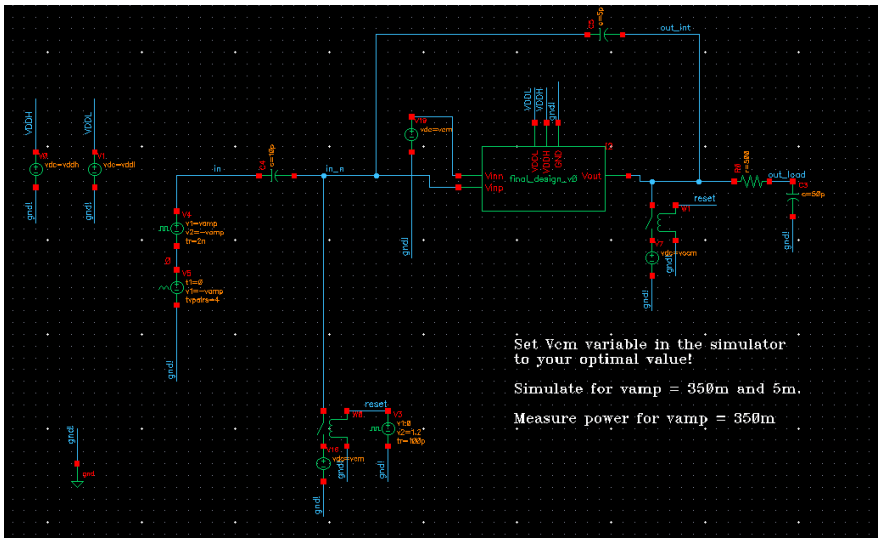

Figure 17: Transient test bench

4.2.2 Transient Test Bench

Figure 17 illustrates the transient test bench setup. As with the stability test bench shown in **Figure 15**, the inputs are flipped in this schematic to prevent positive feedback.

4.3 Calculations vs Simulations

Several optimizations were made to the design based on the simulation results to enhance transistor performance. These changes are summarized here. Note that the same changes were applied consistently across all corresponding transistors. For example, if the tail transistor sizing was modified in the telescopic cascode, identical changes were made to the biasing transistors. Similarly, if the PMOS cascode load was altered, all related transistors—from the primary bias generator to the stacked PMOS transistors generating $2\Delta V + V_{th}$—were adjusted accordingly. Another significant change was the use of three tail transistors instead of one, aimed at improving CMRR at the expense of current matching as shown in figure 18. This will be discussed in more detail later. Only the changes for the gain stages are summarized below in Table 8 - any parameter not

listed is assumed to remain the same as in the initial calculations. The biasing network and source follower underwent minor redesigns to accommodate these changes in the gain stages but are not summarized in this table.

Parameter	Purpose	Calculated Value	Optimized Parameter Values
$L_{n,AB}$, $L_{P,AB}$	Class AB CSA transistors	1 μm	0.7 μm
$W_{n,AB}$	Class AB CSA transistors	449 μm	24 μm
$W_{p,AB}$	Class AB CSA transistors	490 μm	28 μm
$V_{GS,N,AB}$	Class AB CSA transistors	0.575 V	0.596 V
$V_{GS,P,AB}$	Class AB CSA transistors	-0.579 V	-0.533 V
$\|V_{LS}\|$	Level-shift voltage	0.645 V	0.663 V
$I_{DS,bias}$	Bias current	2.48 μA	4 μA
$W_{n,tel}$	Cascode NMOS	31.26 μm	36 μm
$W_{p,tel}$	Cascode PMOS	6.72 μm	6.70 μm
V_{cm}	Input Common Mode	0.55 V	0.5 V
$V_{GS,N}$	Cascode NMOS	0.446 V	0.405 V
$V_{GS,P}$	Cascode PMOS	-0.547 V	-0.504
C_c	Compensation Capacitor	500 fF	75 fF

Table 8: Key differences between calculated and simulated amplifier parameters

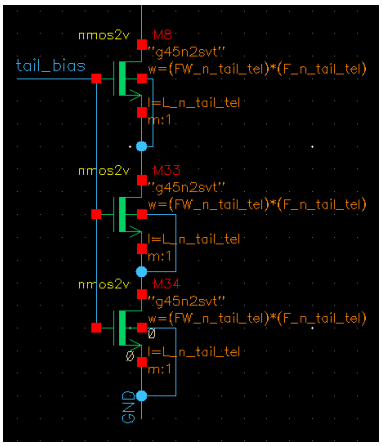

Figure 18: Poor man's Cascode for improving CMRR

As seen in Table 8, the first significant change was made to the class-AB stage. The initial design consumed power in the milliwatt range and introduced substantial parasitic capacitance, which severely degraded the small-signal step response. From the initial calculations, we know that a maximum current (I_{max}) of approximately 400 μA is sufficient to avoid slewing. Using this value, we can back-calculate the quiescent current (I_q) and determine the transistor sizing, given a ΔV_q overdrive across both transistors.

$$I_{max} = k \times \Delta V_{max}^2$$

$$I_q = \frac{I_{max}}{\Delta V_{max}^2} \times \Delta V_q$$

The new sizing was determined for a ΔV_q of approximately 140 mV, corresponding to a ΔV_{max} of around 680 mV. The latter was identified by plotting the node voltages of the gates and observing the point at which one transistor fully turns off while the other reaches its maximum overdrive, as illustrated in Figure 19.

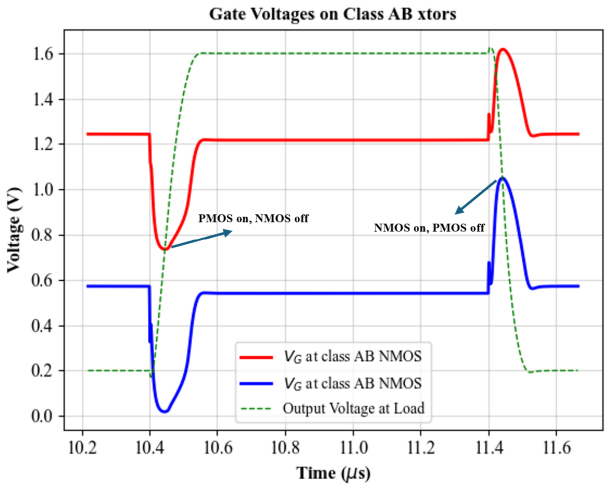

Figure 19: Gate voltages on class AB stage NMOS and PMOS can help identify maximum ΔV across the devices

Finally, to meet the settling time specifications, adjustments were made to increase the overdrive and drive more current to the load. Reducing the transistor length helped boost current, but the resulting increase in threshold voltage (due to shorter channel lengths) began to reduce the overdrive. To compensate, the overdrive of the class AB stage was increased by raising $V_{out1,CM}$ and reducing the level-shifting voltage $|V_{LS}|$.

The final major change involved lowering the input common-mode voltage (V_{cm}) for the telescopic transistor from 550 mV to 500 mV. This adjustment was necessary to force higher V_{DS} drops across the tail and the two cascode devices for a fixed current draw, aligning with the new input bias voltage ($V_{out1,CM}$) of the class AB stage. Adjusting V_{cm} was chosen over resizing the transistors, as many other dimensions depended on the initial sizing, making this approach more practical. This idea is illustrated in figure 20.

4.4 Sub-threshold conduction and maximizing g_m/I_D

Before discussing the results, it is crucial to examine the operating points of the transistors in the final design in detail. As shown in Table 3, the V_{GS} values for the transistors in the telescopic cascode stage are either slightly below V_{th} (which typically ranged from 450 mV to 480 mV) or just above it. This deserves closer scrutiny. For transistors operating in the subthreshold region, where $V_{DS} > 3kT/q \approx 78$ mV at room temperature, the drain current can be approximated using the following relation [4]:

$$I_{DS,sub} \propto exp\left(\frac{\Delta V}{\eta V_{th}}\right)$$

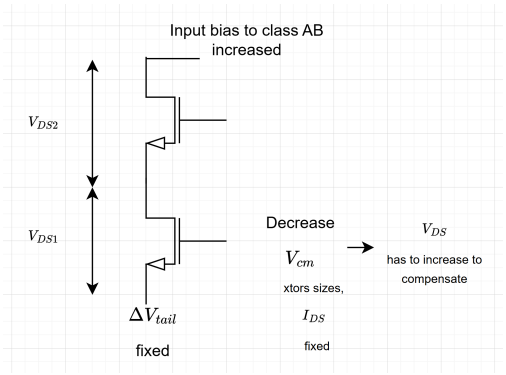

Figure 20: Decreasing V_{cm} helps boost V_{DS} across the NMOS transistors for fixed sizing and I_{DS}

We made a deliberate design choice to maximize g_m/I_D for the input transistors, aiming to achieve the highest possible gain from this stage while minimizing power consumption. We can show that g_m/I_D is maximized in the sub-threshold region since the derivative of I_{DS} is now exponential instead of linear as was the case in strong inversion and saturation regions [5]. Hence, the transistors in the telescopic cascode stage operate predominantly in the subthreshold regime or just slightly above it.

When using the g_m/I_D methodology, the overall gain depends on the ratio g_m/I_D rather than the individual terms g_m or I_D. While this might seem obvious, it proved useful for optimizations later on in the design process. To highlight this point, let's take a brief detour to examine how the improvement in CMRR was achieved by modifying the tail transistor design. This modification significantly impacted the operating points of the entire first stage. The initial design, featuring a single tail transistor, aimed to faithfully copy the current from the red branch shown in Fig. 13. To achieve this, a resistor in the red branch was used to tune the V_{DS} drop across the biasing transistor to match that of the tail transistor.

This had two issues - firstly, the tail transistor was sized such that for the given $I_{DS,tail}$ value, it did not require a ΔV_{tail} of 100 mV to sustain it. Tweaking its size made the current copying less faithful instead of boosting the necessary V_{DS} drop. It also had a lower output resistance when looking from the drain since $r_0 \propto 1/I_{DS}$ and the tail current was around 26 μA (78% current copying efficiency).

Since the g_m/I_D constraints I used to design the input transistors of the cascode stage focused on determining the appropriate V_{GS} and, more importantly, V_{DS} for the LUT, I realized that faithfully copying the current was less critical. It was more important to maintain the correct voltages across the transistors. Consequently, I added two more tail transistors in series, such that the sum of the V_{DS} drops across all three transistors results in a 100 mV drop, which was the necessary source voltage that the input transistors were optimized for in the script. ΔV_{tail} was set to 100 mV in the script, and achieving this was prioritized over providing the exact I_D value specified in the script. This is because I_D was derived from an estimate of g_m using the compensation capacitor, which turned out to be significantly different (500 fF vs 75 fF) from the initial value.

With this in hand, I was able to maintain high g_m/I_D while reducing current in the telescopic cascode branch and improving r_0 of the tail, thereby improving CMRR. However, there was a sweet spot of decreasing current draw for a given g_m/I_D beyond which improvement in gain and CMRR did not matter, and the bottleneck was the actual value of the current that was charging C_c and other parasitics, which affected settling time.

4.5 Results

The results of the entire design process are summarized in this section. The amplifier's response to both the 5 mV input step and the 350 mV input step is presented and discussed in this section.

4.5.1 AC Results

Table 9 summarizes the steady state AC response.

Parameter	Target/Calculated Spec	Design Spec
DM gain at DC (A_0)	77.50 dB	86.19 dB ↑
CMRR at DC	$\geq$ 70 dB	70.14 dB ↔
PSRR (VDDL) at DC	$\geq$ 50 dB	51.53 dB ↔
PSRR (VDDH) at DC	$\geq$ 50 dB	62.42 dB ↑
Phase Margin	$\geq 45^\circ$	51.53° ↔
Unity Gain Frequency (f_u)	35 MHz	19.03 MHz ↓

Table 9: AC results summary

4.5.2 Common Mode and Differential Mode Behavior

Figure 21, on the left, shows the Bode plot of the common-mode and differential-mode signals. On the right, the common-mode rejection is plotted, and the amplifier design clearly demonstrates that the specification is met at DC with a value of 70.14 dB.

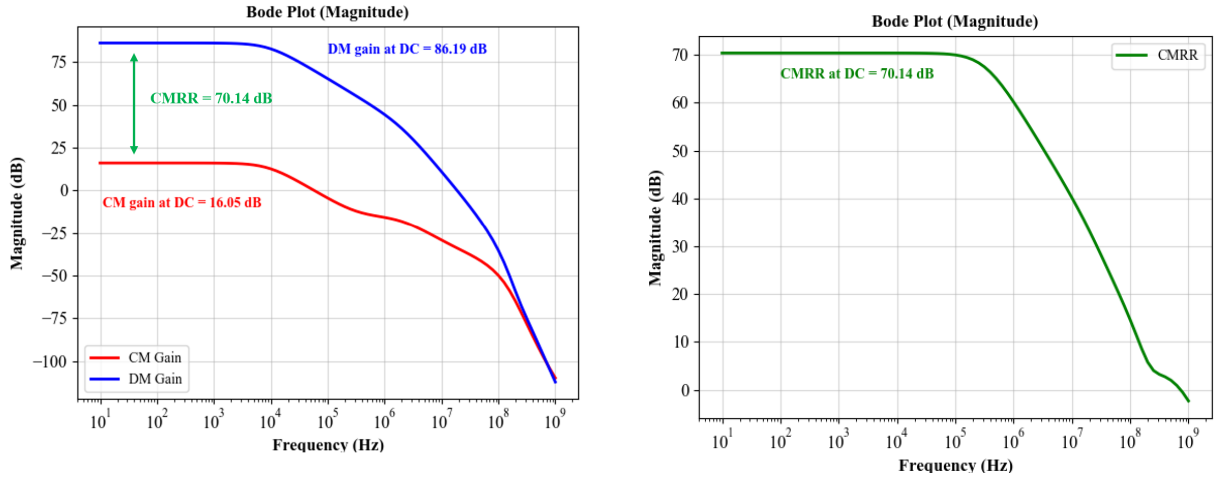

Figure 21: (Left) Common mode and differential mode response, (right) CMRR

4.5.3 Loop Gain Behavior

Figure 22 plots the loop gain of the system. The phase plot shows a phase margin of 51.53^0 and confirm that the feedback is stable with f_u at 19.03 MHz. However, looking at the phase plot in figure 22, we see a flattening of the loop gain phase roughly around $f_u/5$. A *pz analysis* on cadence shows us that there is an early non-dominant pole around 2 MHz and we then have a LHP zero near the unity gain frequency. This is summarized in table 10.

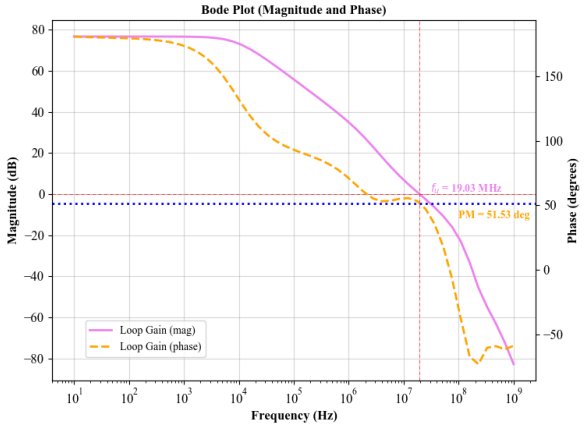

Figure 22: Loop gain Bode plot - magnitude and phase

Parameter	Value
Dominant pole (f_{p1})	9.10 kHz
Non-dominant pole (f_{p2})	1.94 MHz
Zero (f_{z1})	19.3 MHz

Table 10: Pole/Zero Summary

Since $\omega_{z1}/10$ slightly precedes ω_{p2}, the phase drops are canceled just before ω_{p1} and ω_{p2} combine to produce a phase drop of -135° at ω_{p2}. This small difference between $\omega_{z1}/10$ and ω_{p2} provides a 6.53° cushion, ensuring the phase margin exceeds the required 45° specification.

4.5.4 Parasitic Capacitors

Let us investigate the origin of these two poles and the zero. Initially, we estimated that the dominant pole, ω_{p1}, is given by the formula below. We now aim to compare this estimate with the results from our final simulation to determine where this actually lands.

$$f_{p1} \approx \frac{f_u}{A_0\beta} = \frac{g_{m1}}{2\pi A_0\beta \times C_c} = \frac{3 * 111.59\ \mu S}{2\pi * 19173 * 75\ fF} = 12.27\ kHz$$

This estimated value is indeed close to the final f_{p1} observed in table 10. Therefore, the dominant pole is set by the Miller capacitor. However, the non-dominant pole was not far behind because C_c needs to be much greater than the parasitic capacitors at the second stage. As shown in Figure 23, while $C_{gs,SF}$ adds in parallel to C_c and increases the effective compensation, however, it is dwarfed by the C_{gs} of the output stage. The values are summarized below in table 11.

Capacitor	Value
C_c	75 fF
$C_{gs,SF}$	23 fF
Effective compensation $C_c + C_{gs,SF}$	98 fF
$C_{GS,AB}$ (NMOS + PMOS)	288 fF

Table 11: Parasitic Capacitor

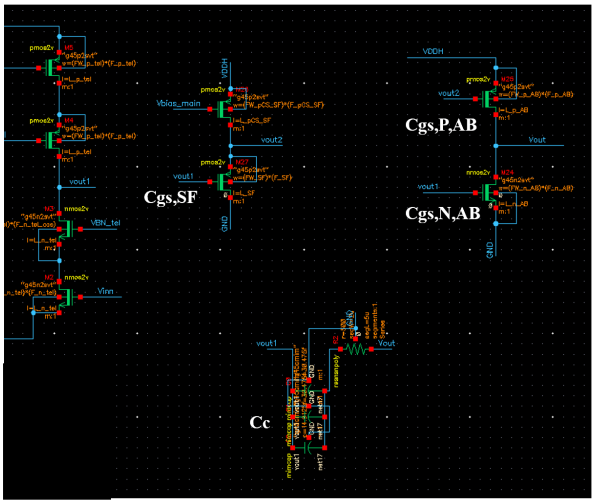

Figure 23: The parasitic capacitors on the source follower and class AB stage influence pole placement

Therefore, the non-dominant pole f_{p2}, set by the load capacitor, adversely impacts feedback stability. Without the left-half-plane (LHP) zero at f_z, the phase margin would have been approximately 5.53°.

4.5.5 Investigating the LHP Zero

The right-half-plane (RHP) zero resulting from the Miller compensation is located far away from f_u due to the small value of C_c and the relatively high g_m of the output stage. Consequently, the left-half-plane (LHP) zero introduced by R_c cannot account for the LHP zero observed at f_z, as shown in Table 10. Recollecting that single-ended differential amplifiers inherently exhibit a pole-zero doublet due to the active load, we attribute the observed zero to the cascoded load formed by transistors M6, M7 in figure 7 [3].

4.5.6 Power Supply Rejection

Finally, figure 24 shows the power supply rejection for both the low and high voltage supplies. PSRR (VDDH) comfortably beats the spec. PSRR (VDDL), on the other hand, has multiple paths and was harder to improve upon.

4.6 Transient Results

Table 12 summarizes the transient response of the amplifier to a 5 mV and a 350 mV step input.

4.6.1 Output Waveforms

The plots in Fig. 25, 26 illustrate the output waveform for a 5 mV and a 350 mV input step respectively. The plot on the left depicts the amplifier's output, while the plot on the right shows the output at the load. The sub-pixel load exhibits low-pass filter behavior, effectively attenuating spikes in the amplifier's output and ensuring smoother output waveforms.

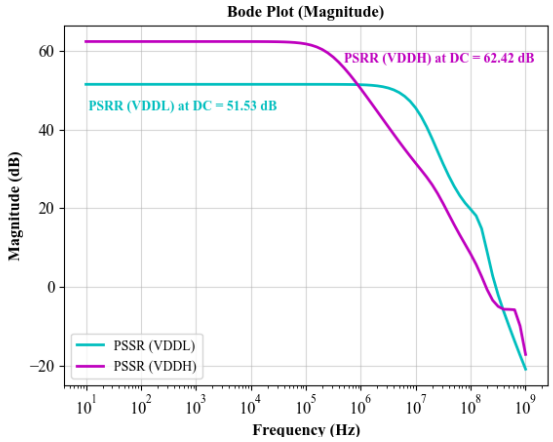

Figure 24: PSRR for V_{DDH} and V_{DDL}

Parameter	**Target Spec**	**5 mV step input**	**350 mV step input**
Rise Time	$\leq$ 180 ns	112.4 ns $\downarrow$	147.1 ns $\downarrow$
Fall Time	$\leq$ 180 ns	111.1 ns $\downarrow$	154.6 ns $\downarrow$
Settling Time (T_{set})	$\leq$ 180 ns	112.4 ns $\downarrow$	154.6 ns $\downarrow$
Error on Rising Step	$\leq$ 0.2%	$\leq$ 0.1 %$\downarrow$	$\leq$0.1% $\downarrow$
Error on Falling Step	$\leq$ 0.2%	$\leq$ 0.1 %$\downarrow$	$\leq$0.1% $\downarrow$
Average Power Consumption (VDDL)	-	0.11 mW	0.11 mW
Average Power Consumption (VDDH)	-	0.17 mW	0.22 mW
Average Total Power Consumption	$\leq$ 1.5 mW	0.28 mW $\downarrow$	0.33 mW $\downarrow$
FoM	$\geq$ 3.70	31.08 $\uparrow$	19.53 $\uparrow$

Table 12: Transient results summarized for 5 mV and 350 mV input steps

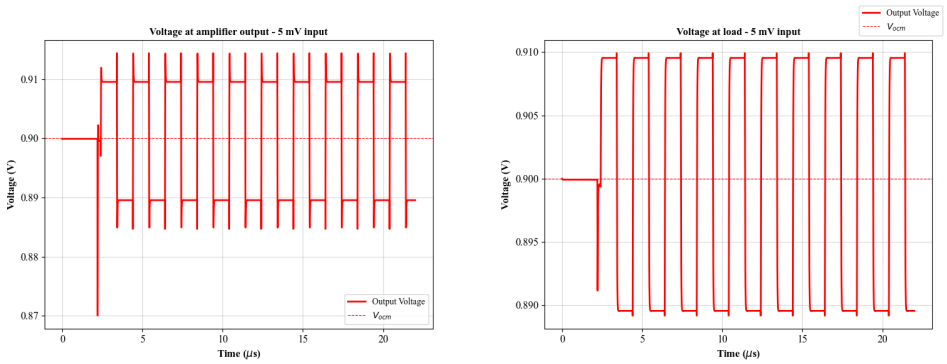

Figure 25: (Left) Amplifier output, (Right) output at C_L for 50 mV input step

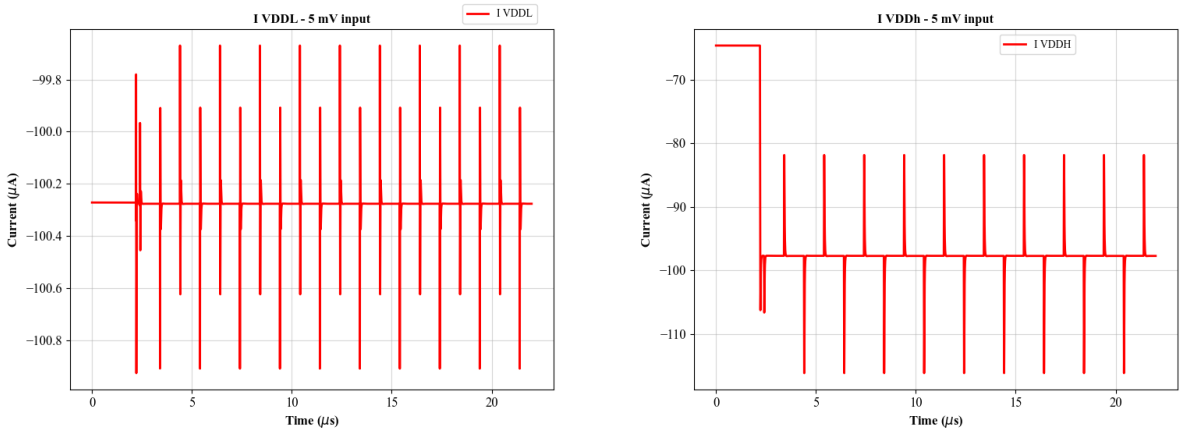

Figure 26: (Left) Current draw from V_{DDL}, (Right) current draw from V_{DDH} for 50 mV input step

An interesting observation in Fig. 26 and Fig. 28 is that the current drawn by the PMOS transistor in the Class-AB stage exceeds that of the NMOS transistor. This disparity is particularly pronounced for a 350 mV step input, indicating an asymmetry where the PMOS consumes more power to supply current during the rise time.

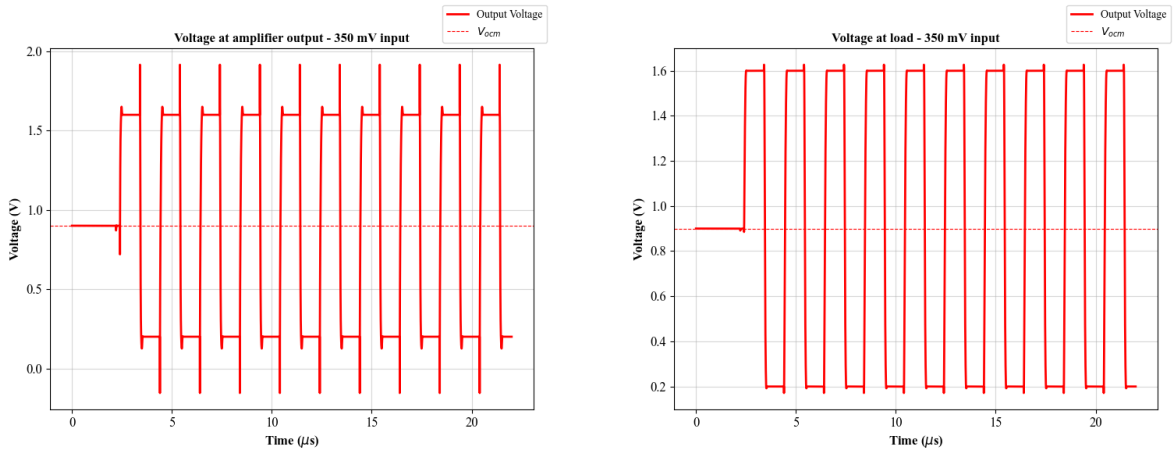

Figure 27: (Left) Amplifier output, (Right) Output at C_L for 350 mV input step

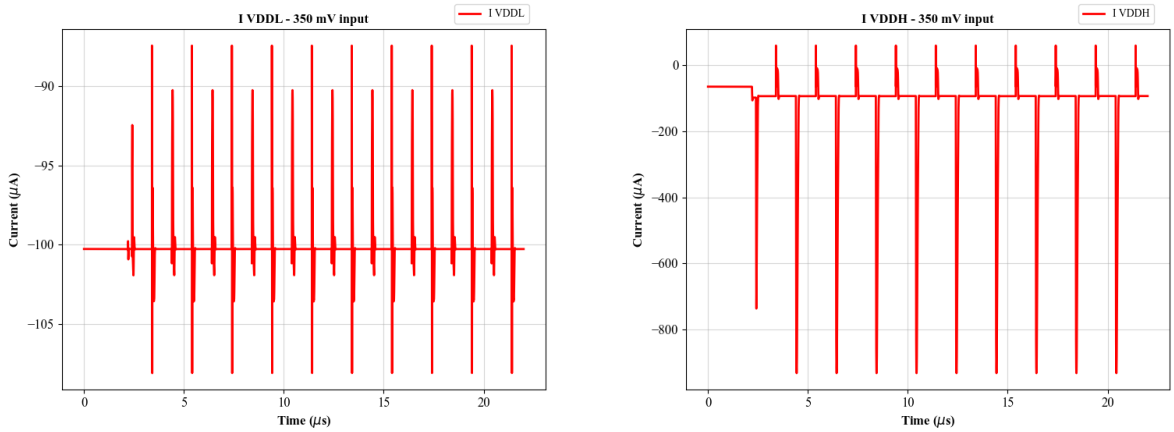

Figure 28: (Left) Current draw from V_{DDL}, (Right) current draw from V_{DDH} for 350 mV input step

4.6.2 Settling Errors

In **Figure 27**, zooming in on one period allows calculation of the rise and fall times for a given settling error threshold of 0.2%. **Figure 29** illustrates the rise and fall times for the 350 mV step, highlighting the points where the error falls below the threshold and remains there. The settling time (T_{set}) is defined as the maximum of the two times obtained. The results confirm that the amplifier settles within the required time.

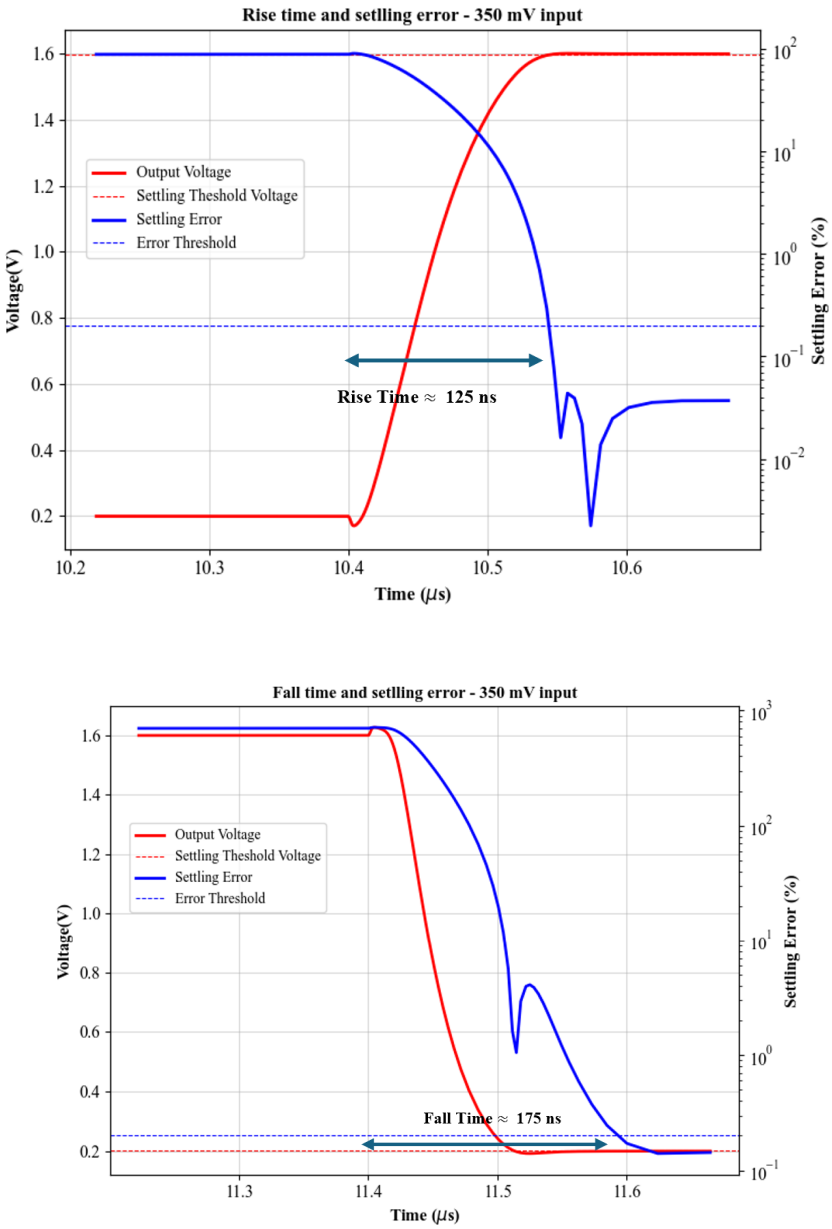

Figure 29: (Left) Rise time, settling error (right) fall time, settling error for 350 mV step

Similarly, **Figure 30** shows the rise and fall times for the 5 mV step. Notably, the settling times extracted from the plot differ by nearly a factor of two from those reported by Cadence. Despite this discrepancy, the Cadence report has been used for the FoM calculation to prevent presenting an overly optimistic estimate.

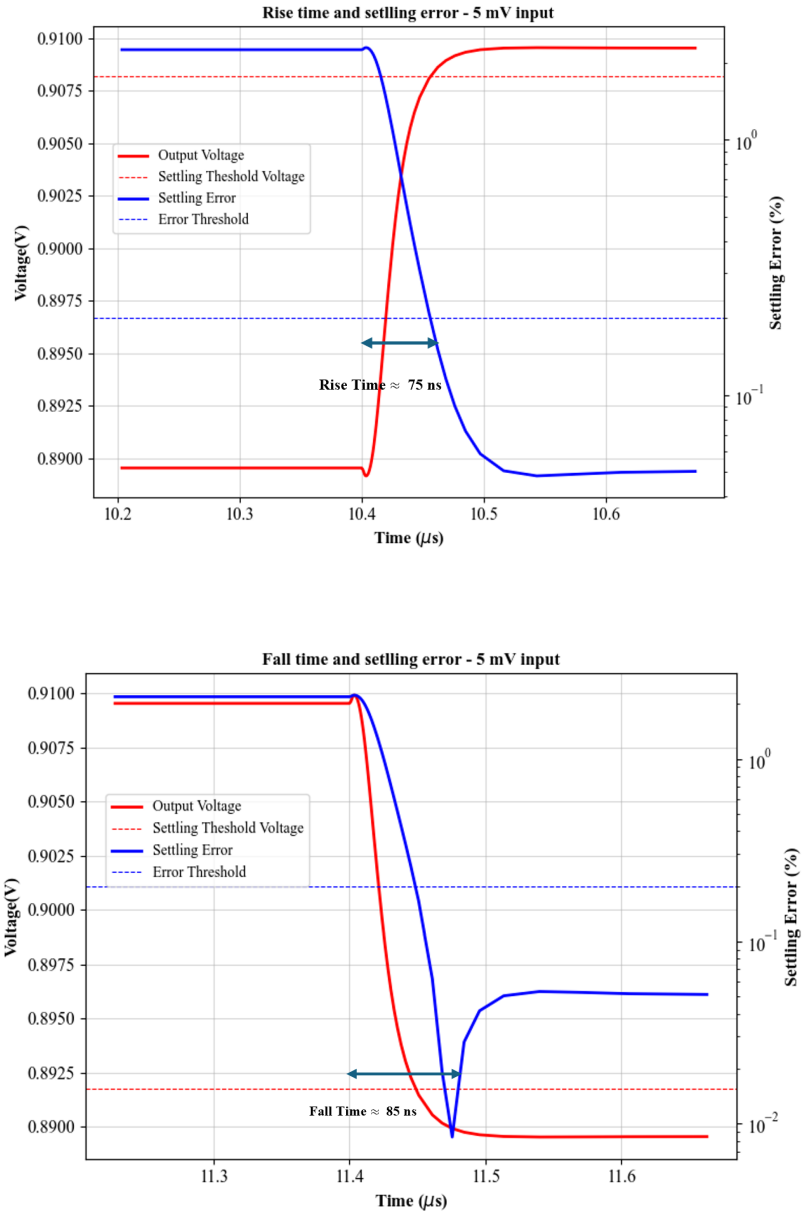

Figure 30: (Left) Rise time, settling error (right) fall time, settling error for 50 mV step

4.7 Area of the design

The total area of the design was calculated by multiplying the length and width of each transistor and passive component from Tables 3 and 4. The entire amplifier occupies an area of 975.9 μm^2. Given that each sub-pixel is driven by one such amplifier, the total area occupied by the LCD

driver can be calculated as follows:

$$\begin{aligned}\text{Total Area} &= \#\,\text{Sub-pixels} \times \text{Resolution} \times \text{Area of single amplifier} \\ &= 3 \times 272 \times 340 \times 975.9\,\mu m^2 \\ &= 270.7\ mm^2\end{aligned}$$

A typical 38 mm Apple Watch Series 1, which has the same resolution (though with an OLED display instead), has a display area of 564 mm^2 [2]. Therefore, the entire LCD driver unit occupies approximately 48% of the display area. This is certainly quite large and presents an opportunity for optimization.

4.8 Potential Improvements in Design

4.8.1 Better control over frequency response

In this design, controlling the placement of the non-dominant pole and other parasitic poles or zeros near f_u was a significant challenge. As evident in the Bode plot of the loop gain in figure 22, the phase margin exceeding 45° is primarily due to a parasitic LHP zero, which incidentally worked to our advantage rather than being a deliberate design choice. This issue might have been mitigated by iteratively calculating C_{gg} in the script and subsequently updating the I_D and W values for the class-AB transistors. The mismatch between C_c and the C_{gs}, of the class AB transistors contributed to reduced control over the placement of the non-dominant pole.

Another potential optimization could involve selecting the source follower sizing more carefully to introduce an LHP zero near f_u, which could have helped in improving the phase margin. This zero can be expressed as:

$$f_{z,SF} = \frac{g_{m,SF}}{C_{gs,SF}}$$

4.8.2 Class AB Stage Burns Excessive Power

Another significant optimization could have been reducing the quiescent current of the class-AB stage and improving the matching between the NMOS and PMOS devices. As shown in figure 28, the PMOS struggles during the rise time and ends up consuming significantly more power. Conversely, while the NMOS performs relatively well in terms of power draw during the fall time, it still consumes excessive quiescent current. Balancing the two devices could have mitigated these inefficiencies and improved overall power performance.

4.8.3 Marginal Gains in Power

For marginal gains in power efficiency, I could have leveraged the current mirror ratio of 10 more effectively across the branches. In the current design, current multiplication was only applied in the primary bias generator. By geometrically cascading the current multiplication, achieving a 100× current mirror ratio would have been feasible. However, this approach could introduce potential challenges, such as the unwanted poles and zeros associated with the current mirrors, which could impact stability and performance.

4.9 Area optimization

We could potentially eliminate the biasing branch for the PMOS cascode load by employing a self-biasing technique as shown in figure 31 [1].

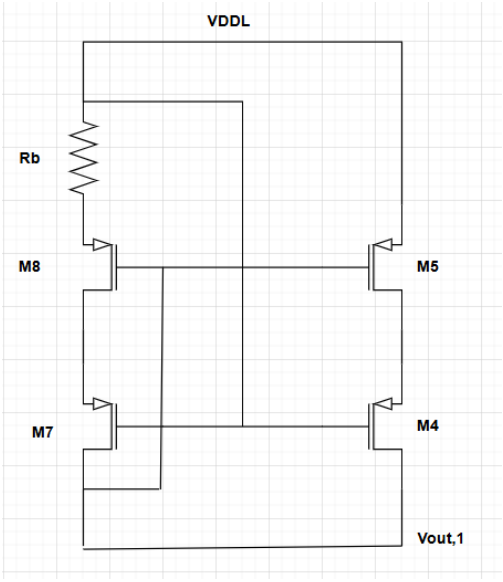

Figure 31: Self-biased PMOS current mirror

This approach could have resulted in approximately a 6% savings in area (though the resistor R_b would partially offset the area benefit) and a 6% reduction in power consumption. However, it would have introduced additional design complexity.

5 Conclusion

This report presented the entire design process of an LCD driver amplifier. The initial steps included amplifier specification extraction, topology selection, and obtaining preliminary design points using the g_m/I_D methodology. Post-simulation adjustments aimed at optimizing the figure of merit (FoM) were highlighted, with key deviations from the initial calculations discussed in detail. Comprehensive analyses of both AC and transient simulation results were provided, along with a brief evaluation of parasitic effects. Lastly, potential optimizations were proposed based on the loop gain and rise-time performance of the amplifier for a 350 mV input step. The overall performance is summarized in table 13

Parameter	Target Spec	Design Spec 5 mV input	Design Spec 5 mV input
Settling Time (T_{set})	$\leq$ 180 ns	112.4 ns	154.6 ns
Total error	$\leq 0.2\%$	$\leq 0.1\%$	$\leq 0.1\%$
Power Consumption	$\leq$ 1.5 mW	0.28 mW	0.33 mW
Figure of Merit	$\geq$ 3.70	31.08	19.53
CMRR at DC	$\geq$ 70 dB	70.14 dB	70.14 dB
PSRR (VDDL) at DC	$\geq$ 50 dB	51.53 dB	51.53 dB
PSRR (VDDH) at DC	$\geq$ 50 dB	62.42 dB	62.42 dB
Phase Margin (PM)	$\geq 45^\circ$	51.53°	51.53°

Table 13: LCD Driver Amplifier overall perforamance

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