Berkeley
UNIVERSITY OF CALIFORNIA

# EE 240A

## Final Project Presentation

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# Contents

# Op-amp Overview

- 2-stage op-amp with Miller Compensation
- Input stage: Telescopic Cascode for high gain
- Output stage: Class-AB common source for improved slew rate

**AC Results Summary**

| Parameter | Value |
|---|---|
| **DC Gain** | **86 dB** |
| **GBW** | **18.54 MHz** |
| **CMRR** | 70 dB |
| **PSRR** | 51 dB (VDDL)<br>64 dB (VDDH) |
| **Phase Margin** | **52.3 deg** |

**Transient Results Summary – 350 mV input**

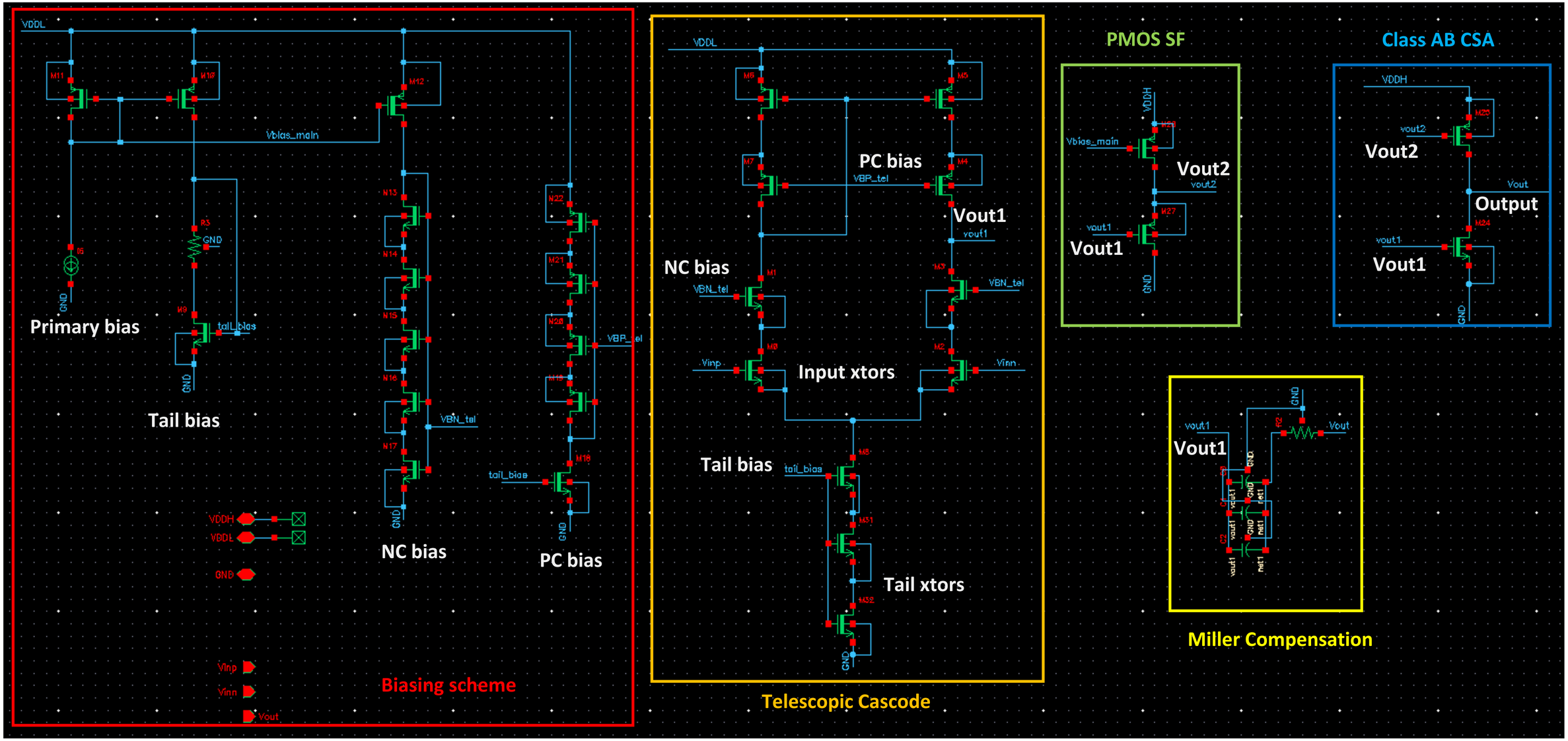
| Parameter | Value |
|---|---|
| **Settling time** | **159.2 ns** |
| **Avg Power Consumed** | **0.312 mW** |
| **Current Efficiency (Imax/Ibias)** | 10.66 |
| **SR+ Max** | **17.6 V/us** |
| **SR- Max*** | 17.2 V/us |
| **FoM** | **20.08** |

**Misc. Results**

| Parameter | Value |
|---|---|
| **Area** | 970 um^2 |
| **Mismatch** | Poor |

*estimate

# Op-amp Overview - Schematic



# High-level Specs

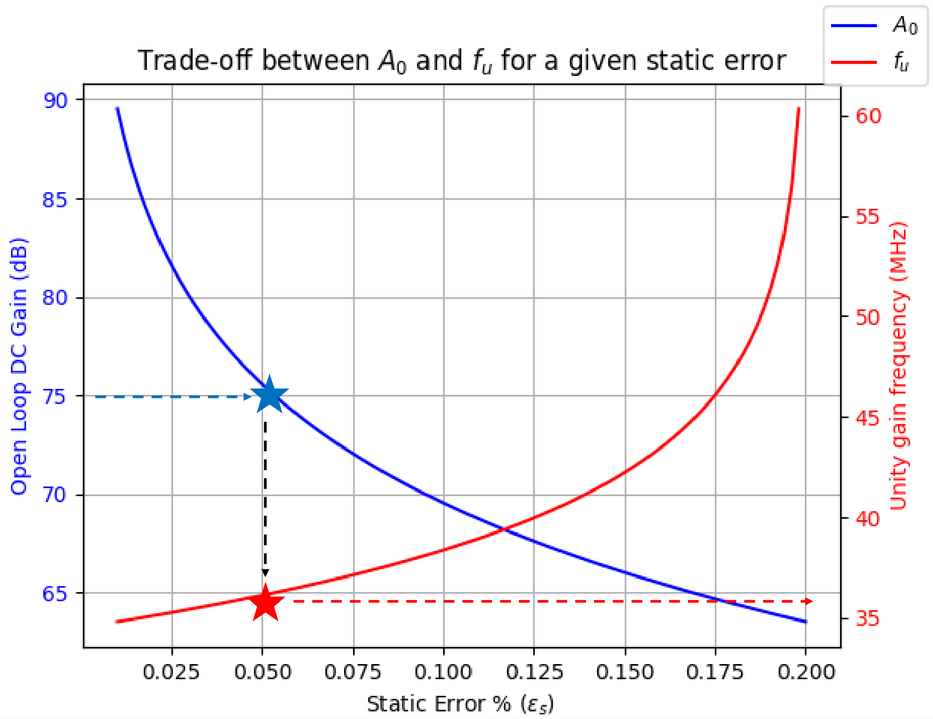
| Spec | Value |
|---|---|
| Settling Time | < 180 ns |
| Total Error | < 0.2% |

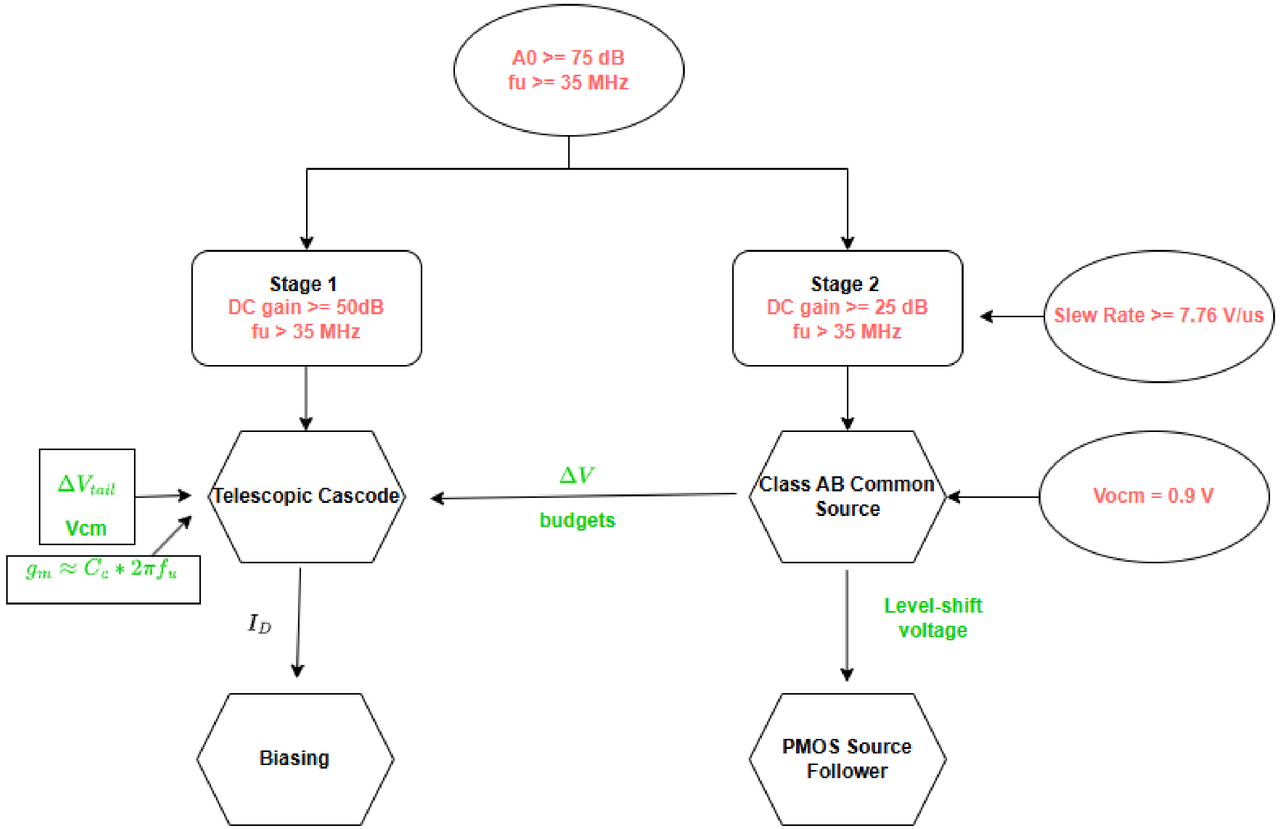
$$f_u \approx \frac{-ln(\epsilon_d)}{T_{set}} = \frac{-ln(0.002 - \epsilon_s)}{T_{set}}$$

$$A_0 = \frac{1}{f}\left(\frac{1-\epsilon_s}{\epsilon_s}\right)$$

$$\frac{dV_{out}}{dt} = \frac{1.4\ V}{T_{set}} = 7.76\ V/\mu S$$

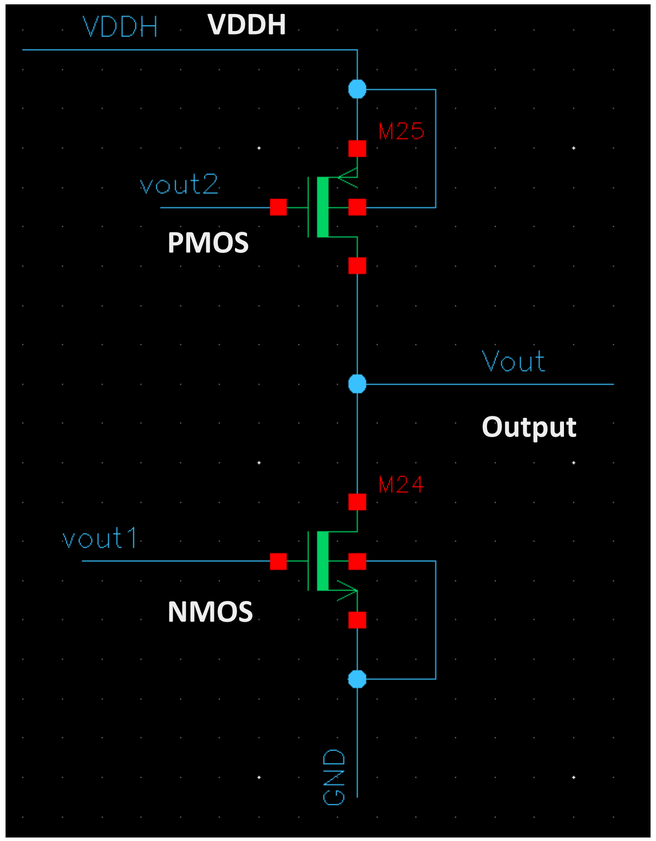
$\epsilon_s$ - static error
$\epsilon_d$ - dynamic error
$A_0$ - open loop DC gain
$f$ - feedback factor
$V_{out}$ - output voltage
$T_{set}$ - settling time



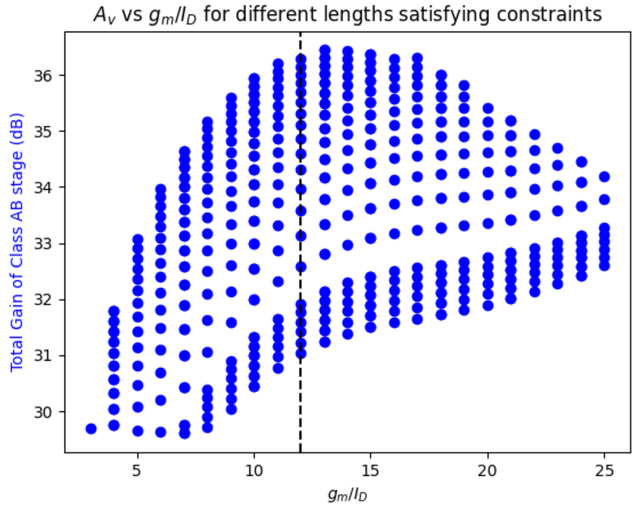



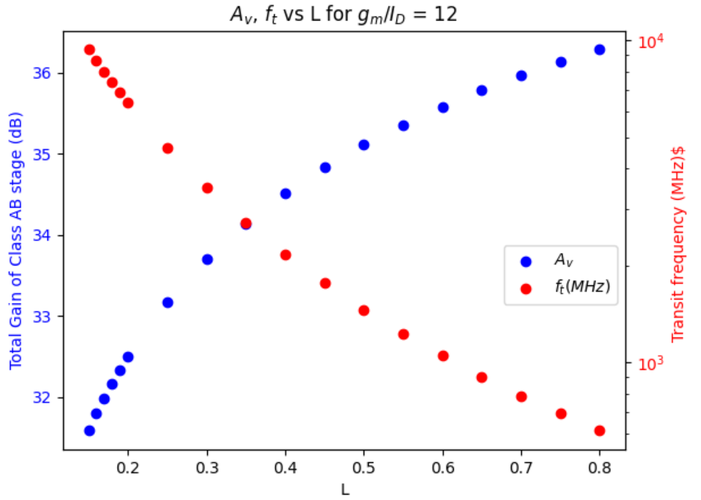

- More constraints → narrower design space
- gm/ID methodology to size xtors and bias voltages
- Start design with output stage → has max constraints
- Biasing voltages of output stage give more constraints for input stage
- Compensation design → set by phase margin, sets gm of input stage
- Make Design choices in stage 1- power supply, tail VDS drop, etc.

# Class AB CSA- Design




| Parameter | Value |
|---|---|
| Ln, Lp | 0.7 um |
| Wn | 28 um |
| Wp | 24 um |
| VGS,n | 0.597 V |
| \|VGS,p\| | 0.512 V |

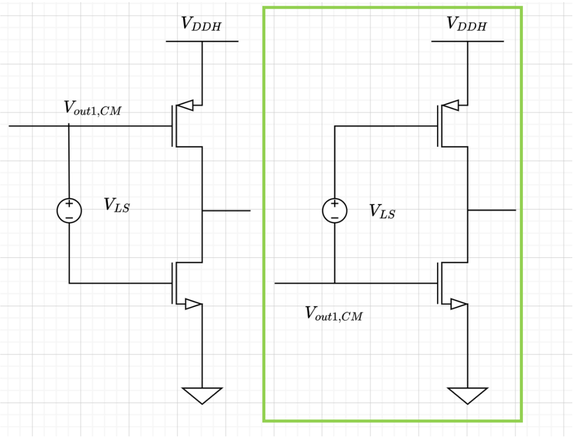


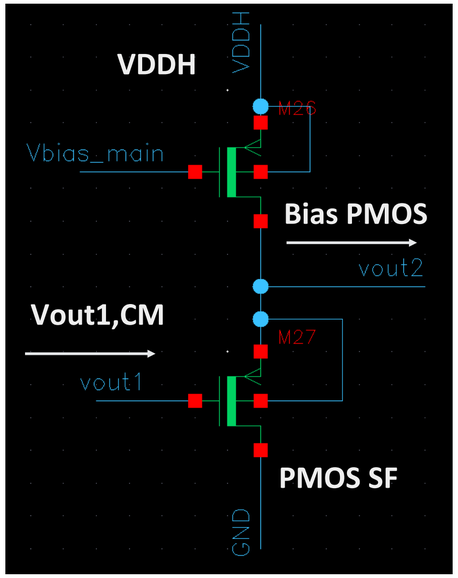

- Given constraints → pick suitable gm/ID → pick L
- Estimate gm using CL
- LUTs give sizing and biasing

## Source Follower – Level-shifting

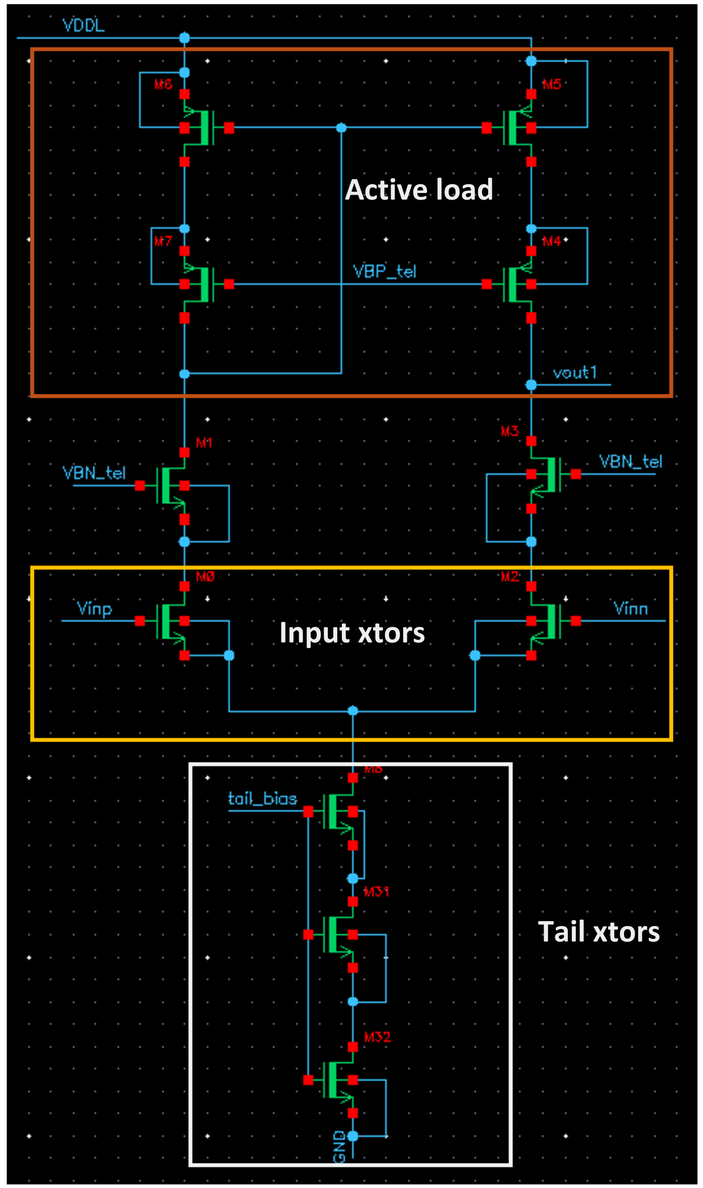
Which biasing scheme to pick?




- **Vout1,CM to PMOS (left)** → needs higher Vout1,CM → can't use VDDL for first stage
- Vout1,CM to NMOS (right) → low Vout1,CM low → VDDL for first stage → save power!



# Telescopic Cascode - Design

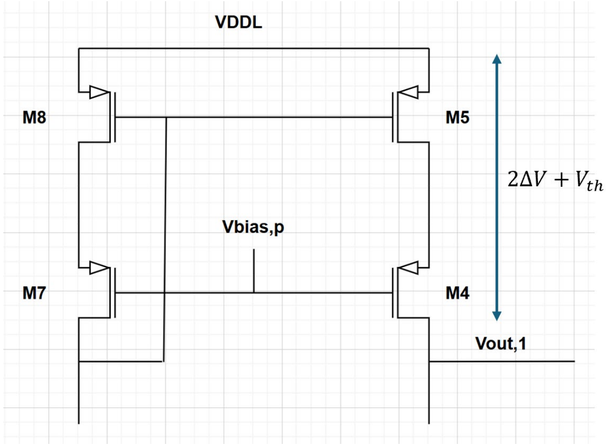



- Designed for high gm/ID → max gain, min power
- $\Delta V$ across tail = 100 mV
- Estimate gm using Cc (500 fF starting value)
- LUTs give sizing and biasing
- Operates in sub-threshold region for max gm/ID [1]

| Parameter | Value |
|---|---|
| Ln, Lp | 2 um |
| Wn (input) | 36 um |
| Wp (load) | 6.7 um |
| gm/ID (input) | ≈ 22 |
| Ibias (tail current/2) | 5 uA |
| Vicm | 0.5 V |

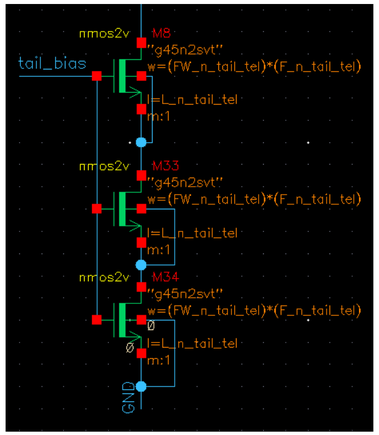
[1] F. Silveira, D. Flandre, and P.G.A. Jespers. A g/sub m//i/sub d/ based methodology for the design of cmos analog circuits and its application to the synthesis of a silicon-on-insulator micropower ota. IEEE Journal of Solid-State Circuits, 31(9):1314–1319, 1996.

## Active Load Design



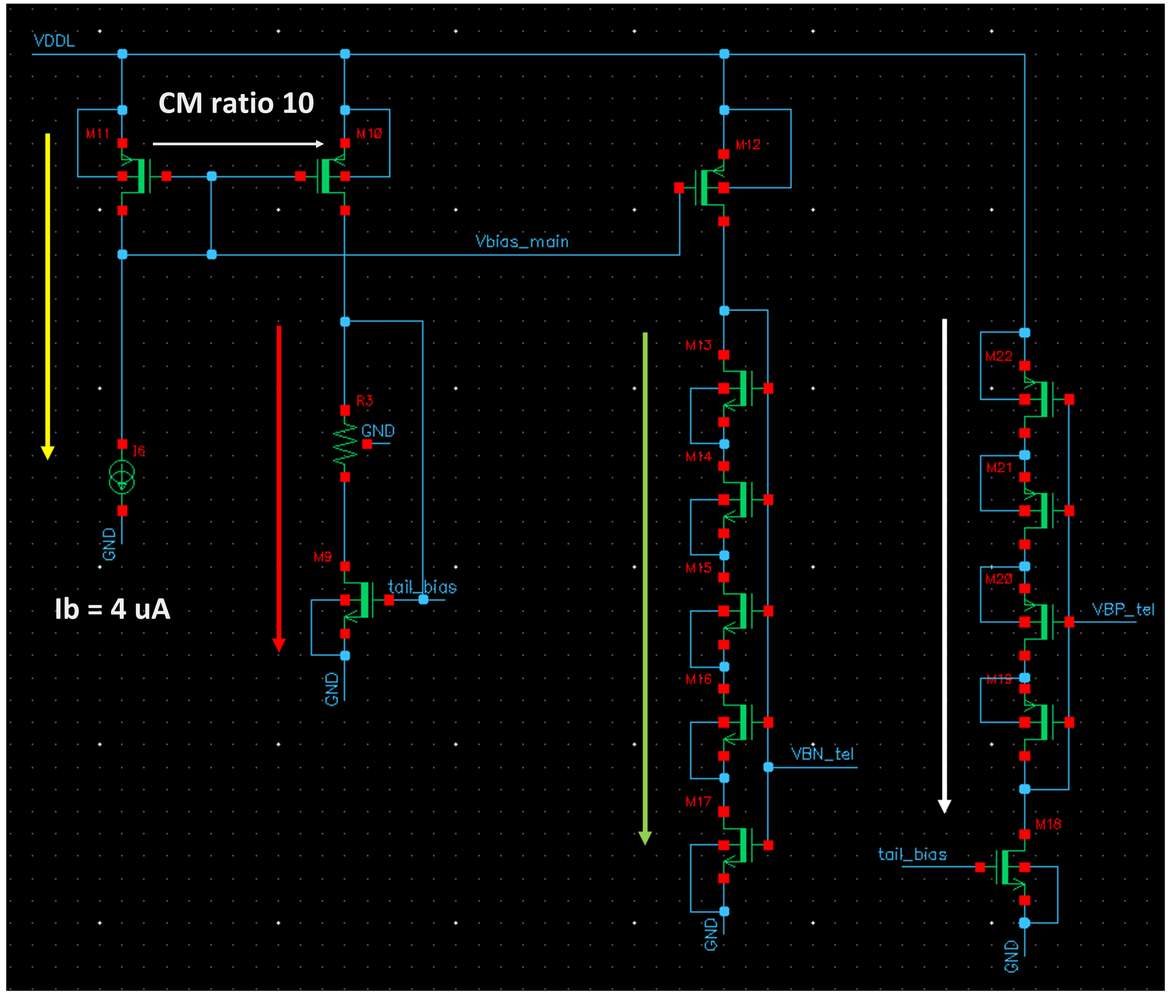

- Save a Vth (≈ 430 mV) drop across the load!

## Tail xtor – Poor man's cascode




- Increase VDS drop across to 100 mV
- Improve CMRR

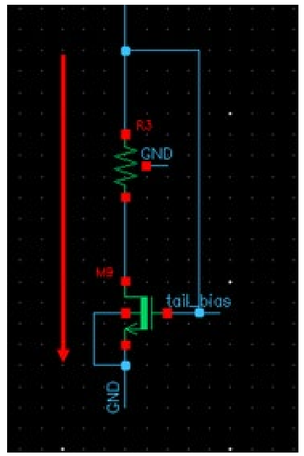
# Biasing network



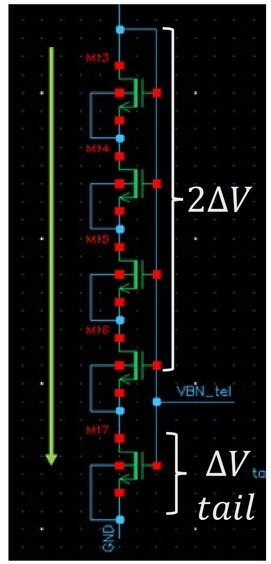

| Branch | Purpose |
|---|---|
| Yellow | Primary bias generator |
| Red | Bias tail xtors in first stage |
| Green | Bias NMOS cascode devices in first stage |
| White | Bias PMOS cascode devices in first stage |

## Design choices

1. Current mirror ratio = 10 from primary bias generator to other branches

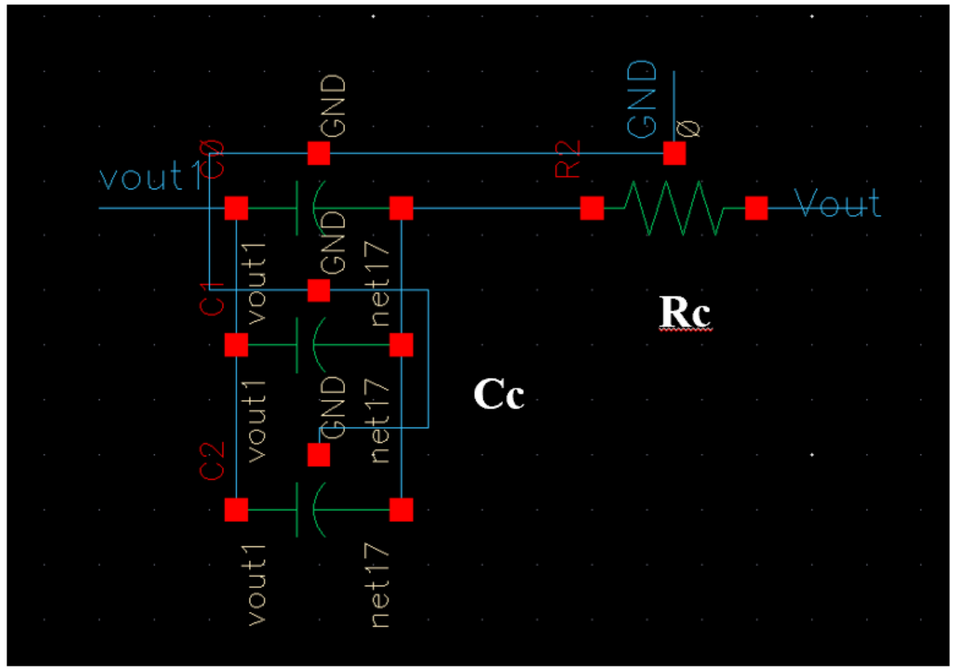



2. Resistor to better match VDS across current mirror for tail xtor




3. Cascode NMOS device needs $2\Delta V + \Delta V_{tail}$

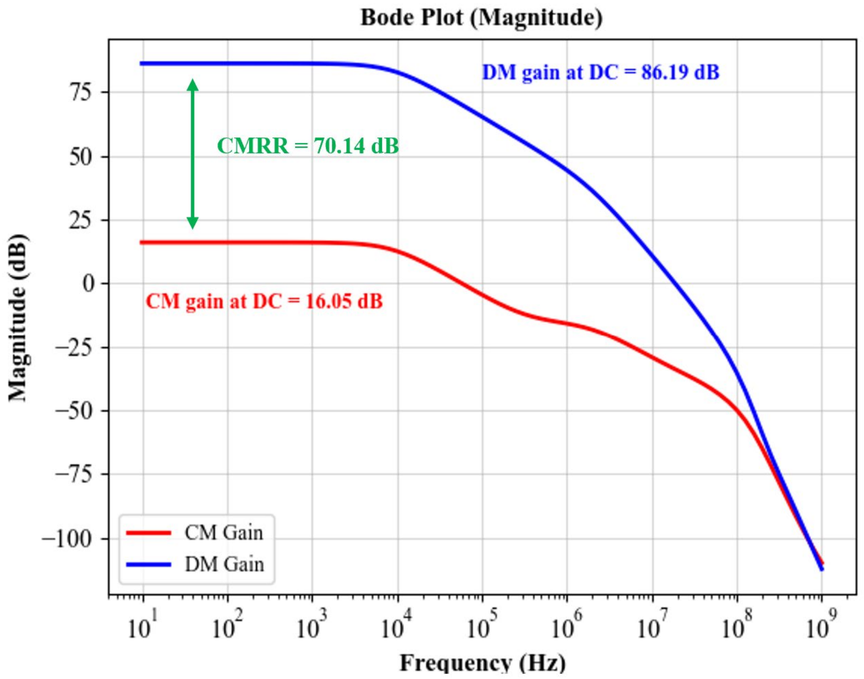
# Miller Compensation

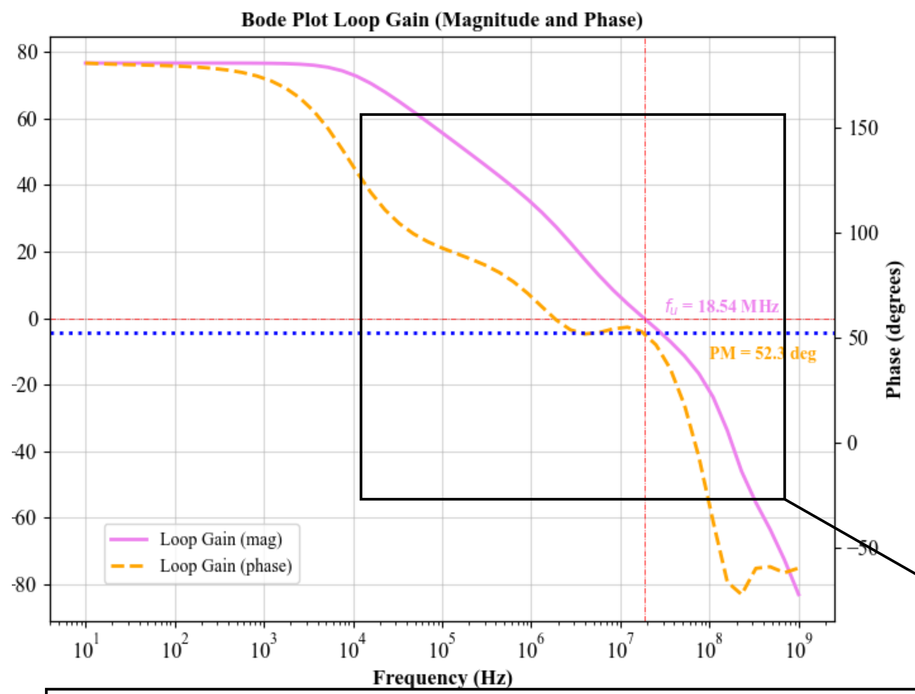



| Parameter | Value |
|---|---|
| Cc | 75 fF |
| Rc | 500 ohm |

- Start with Cc 500 fF
- $R_c = 1/gm_{out}$ to push the RHP from compensation to infinity
- Tune these values as necessary looking at frequency response

# Frequency response




| Parameter | Value |
|---|---|
| DC Gain | 86 dB |
| fu | 18.54 MHz |
| CMRR | 70 dB |
| Phase Margin | 52.3 deg |
| Dom pole | 9.03 kHz |
| Non-dom pole | 1.84 MHz |
| Dom zero | 19.2 MHz |

## Miller Cap sets first pole

$$f_{p1} \approx \frac{f_u}{A_0\beta} = \frac{g_{m1}}{2\pi A_0\beta \times (C_c + C_{gs,SF})} = \frac{3 * 111.59\ \mu S}{2\pi * 20390 * (75 + 20)\ fF} = 27.50\ kHz$$

- If we include other parasitics, we can get a better estimate of dominant pole, unity gain freq.
- However, since Cc is smaller than parasitic caps at the output stage, second pole is before unity gain frequency!

| Capacitor | Value |
|---|---|
| $C_c$ | 75 fF |
| $C_{gs,SF}$ | 20 fF |
| $C_{GS,AB}$ (NMOS + PMOS) | 288 fF |

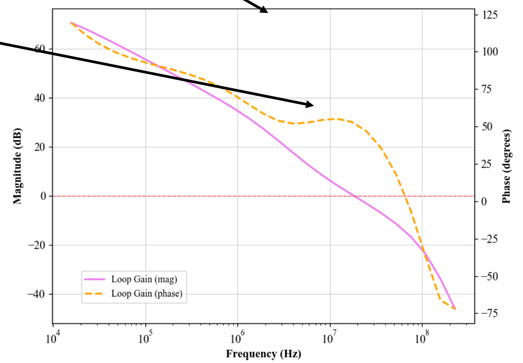
## LHP zero helps phase margin!

- Proven by phase bump and magnitude plot!
- Where is it coming from?

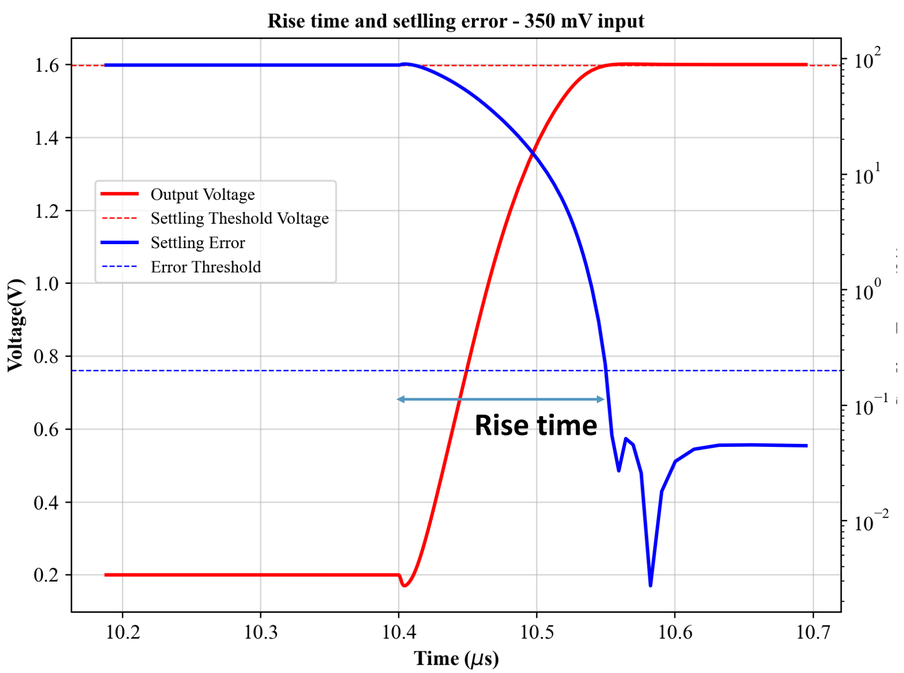
Zero from Miller compensation and its cancellation are at a very high frequency (GHz)

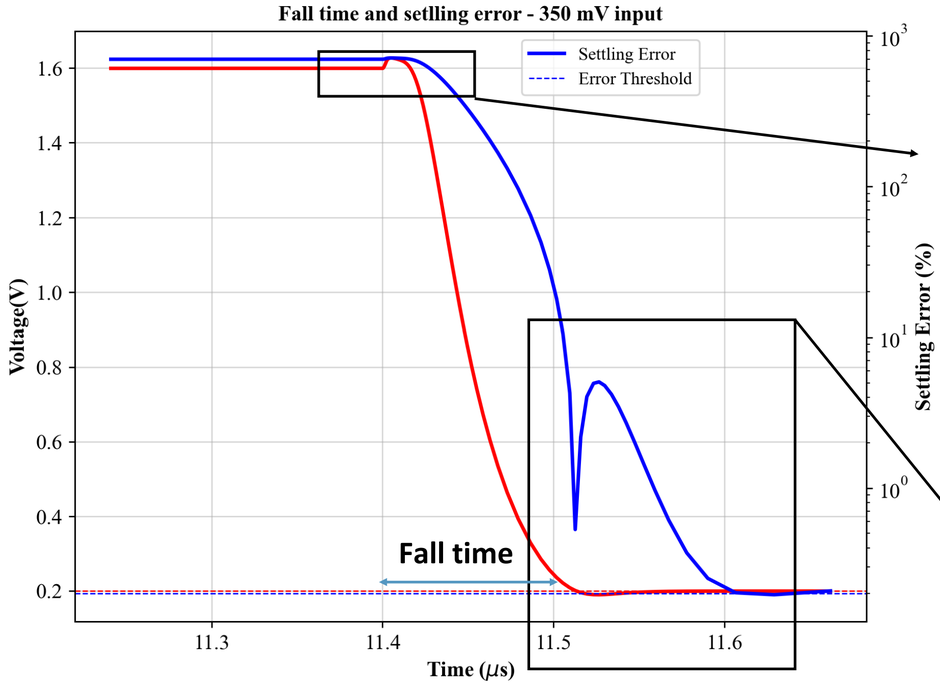
Maybe PMOS active load? (gm/Cgs around 4 MHz)

- How does it affect transient response?

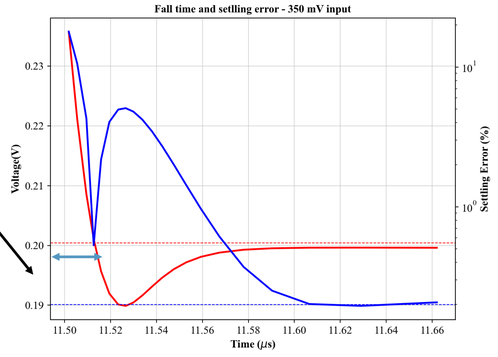


# Transient Response



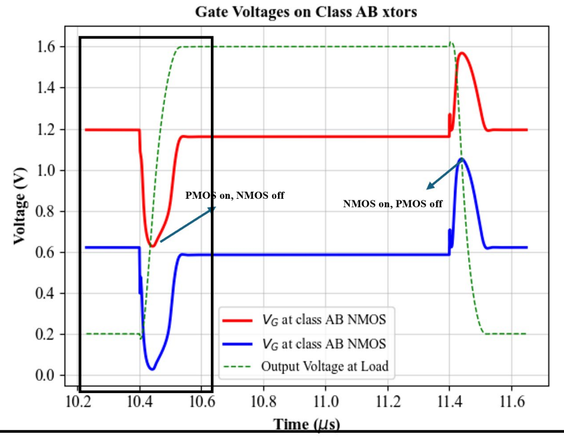



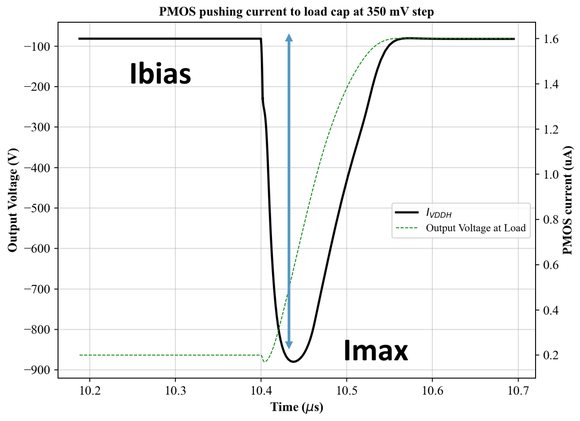

- LHP zero causing an overshoot




| Parameter | 5 mV input step | 350 mV input step |
|---|---|---|
| Rise Time | 104.6 ns | 152.5 ns |
| Fall Time | 102.9 ns | 159.2 ns |
| Settling Time | 104.6 ns | 159.2 ns |
| SR+ max | - | 17.6 V/us |
| SR- max | - | 17.2 V/us |
| CE (Imax/Ibias) | - | 10.66 |
| Error | < 0.1% | < 0.1% |
| Avg Power (VDDL) | 0.110 mW | 0.110 mW |
| Avg Power (VDDH) | 0.154 mW | 0.202 mW |
| Avg Total Power | 0.264 mW | 0.312 mW |
| FoM | 36.10 | 20.08 |

## Class-AB stage provides huge current for large input!

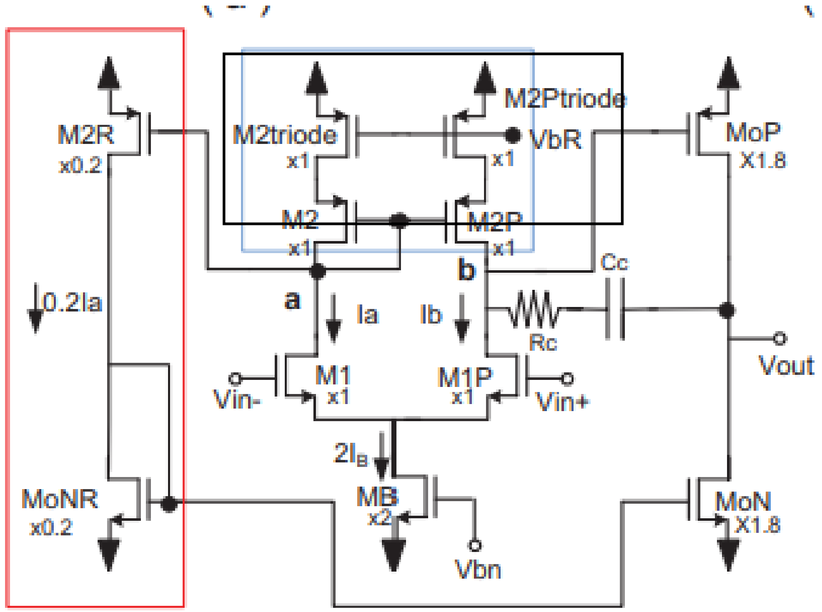



- High slew rate!

# Potential Improvements

## Improving class AB slew rate [3]



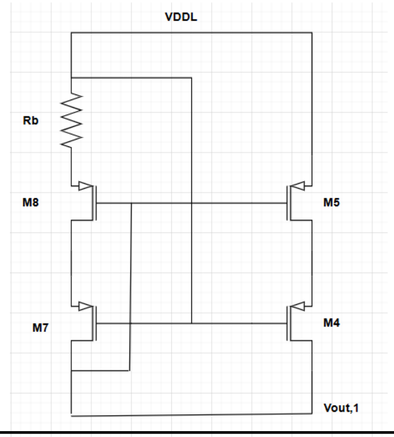

- M2/M2P – biased on brink of saturation
- If they're thrown into triode (say current in branch changes), to support the tail current, their VDS drop has to increase!
- This sets a large VGS for MoP and is copied by the red branch to MoN

## Better control over frequency response

- During initial sizing of xtors, width was not extracted by iteratively accounting for parasitic Cgs → underestimated parasitics and therefore, Cc
- Rc could have been tuned to control LHP zero!

$$R_c = \frac{1}{gm_{out}}\left(1 + \frac{C_L}{C_c}\right)$$

## Marginal gains in Power/Area




- Self-biased current mirror at telescopic active load [2]
- Can reduce power and area by removing one biasing branch
- Resistor occupies area – total savings about 6% estimated for typical values of Rb
- 6% power improvement estimated


[2] Bhawna Aggarwal, Maneesha Gupta, and A.K. Gupta. A comparative study of various current mirror configurations: Topologies and characteristics. Microelectronics Journal, 53:134–155,2016.

[3] Aguado-Ruiz, J., Lopez-Martin, A., Lopez-Lemus, J., & Ramirez-Angulo, J. (2014). Power efficient class AB op-amps with high and symmetrical slew rate. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, *22*(4), 943–947. doi:10.1109/tvlsi.2013.2256946

# Acknowledgements


- Thanks to Prof. Muller for setting us up for success with her class!
- Chun-yen and Rahul helped with the take-off on this project – thanks a lot to both!
- Joosung, Sarah, Aniket – thanks for enduring the endless discussions on the design!

# Back up

# 3 Transistor and Bias Summary

Table 3 shows a summary of dimensions and operating points for each transistor in the amplifier. Table 4 summarizes the passive components used.

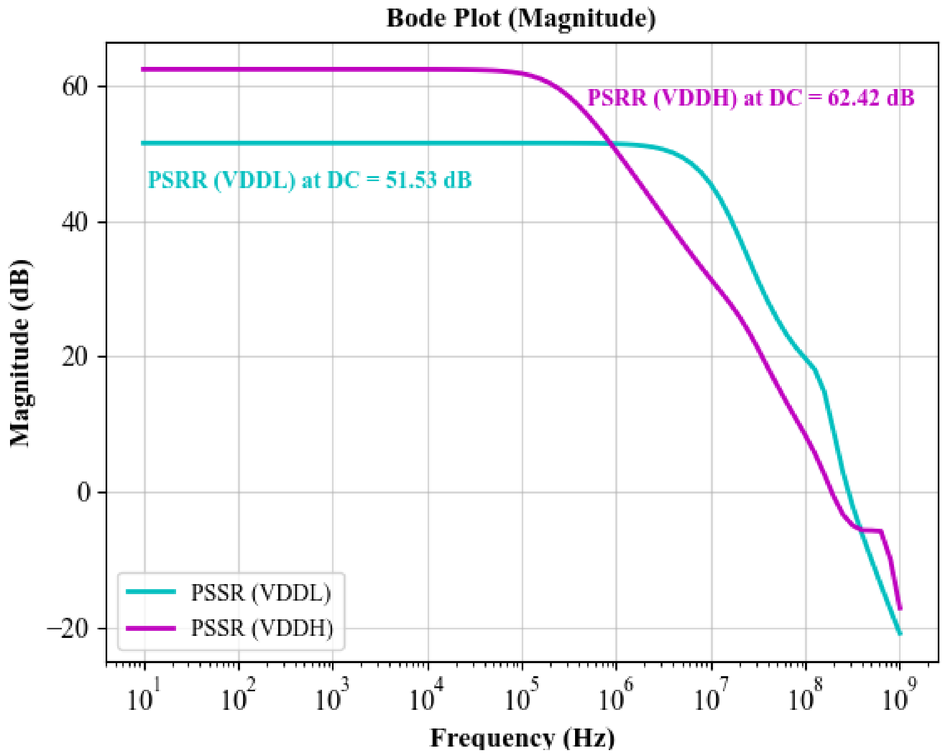
| XTOR | Purpose | L ($\mu$m) | W ($\mu$m) | $I_D$ ($\mu$A) | $V_{GS}$ (V) | $g_m$ ($\mu$S) | $g_m/I_D$ | $g_{DS}$ ($\mu$S) |
|---|---|---|---|---|---|---|---|---|
| M0 | Vinp | 1 | 36 | 5.09 | 0.405 | 111.53 | 21.91 | 7.78 |
| M1 | NMOS cascode | 1 | 36 | 5.09 | 0.393 | 111.89 | 21.98 | 3.61 |
| M2 | Vinn | 1 | 36 | 5.09 | 0.405 | 111.52 | 21.91 | 7.78 |
| M3 | NMOS cascode | 1 | 36 | 5.09 | 0.393 | 111.88 | 21.98 | 3.62 |
| M8 | Cascode tail | 1 | 90 | 10.18 | 0.403 | 218.43 | 21.46 | 72.38 |
| M33 | Cascode tail | 1 | 90 | 10.18 | 0.427 | 185.59 | 18.23 | 325.87 |
| M34 | Cascode tail | 1 | 90 | 10.18 | 0.444 | 167.86 | 16.49 | 519.64 |
| M4 | PMOS cascode | 1 | 6.7 | 5.09 | -0.504 | 95.77 | 18.81 | 3.36 |
| M5 | PMOS cascode | 1 | 6.7 | 5.09 | -0.501 | 97.3 | 19.12 | 1.93 |
| M6 | PMOS cascode | 1 | 6.7 | 5.09 | -0.501 | 97.3 | 19.12 | 1.94 |
| M7 | PMOS cascode | 1 | 6.7 | 5.09 | -0.504 | 95.73 | 18.81 | 3.41 |
| M11 | Primary Bias Generator | 1 | 1.34 | 3.99 | -0.578 | 43.24 | 10.84 | 0.8 |
| M10 | Current source | 1 | 13.4 | 33.37 | -0.578 | 358.98 | 10.76 | 6.56 |
| M12 | Current source | 1 | 13.4 | 32.24 | -0.578 | 376.59 | 11.68 | 7.19 |
| M9 | Bias for tail xtor | 1 | 90 | 33.37 | 0.444 | 647.59 | 19.41 | 29.53 |
| M13 | Bias for NMOS cascode | 1 | 36 | 32.24 | 0.485 | 532.01 | 16.50 | 13.66 |
| M14 | Bias for NMOS cascode | 1 | 36 | 32.24 | 0.534 | 361.02 | 11.20 | 493.90 |
| M15 | Bias for NMOS cascode | 1 | 36 | 32.24 | 0.567 | 285.34 | 8.85 | 860.40 |
| M16 | Bias for NMOS cascode | 1 | 36 | 32.24 | 0.592 | 243.47 | 7.55 | 1143.6 |
| M17 | Bias for NMOS cascode | 1 | 45 | 32.24 | 0.61 | 214.01 | 6.64 | 1784 |
| M22 | Bias for PMOS cascode | 1 | 6.7 | 20.61 | -0.807 | 46.67 | 2.26 | 328 |
| M21 | Bias for PMOS cascode | 1 | 6.7 | 20.61 | -0.75 | 60.27 | 2.92 | 269 |
| M20 | Bias for PMOS cascode | 1 | 6.7 | 20.61 | -0.682 | 89.18 | 4.33 | 182.7 |
| M19 | Bias for PMOS cascode | 1 | 6.7 | 20.61 | -0.592 | 218.11 | 10.58 | 4.06 |
| M18 | Current source | 1 | 54 | 20.61 | 0.444 | 397.94 | 19.31 | 15.9 |
| M26 | PMOS load for SF | 4 | 1.8 | 18.20 | -1.278 | 19.26 | 1.05 | 19.58 |
| M27 | SF PMOS | 1 | 2.6 | 18.20 | -0.597 | 121.90 | 6.69 | 2.13 |
| M24 | Class AB CSA PMOS | 0.7 | 28 | 46.42 | -0.628 | 740.66 | 16.08 | 11.28 |
| M25 | Class AB CSA NMOS | 0.7 | 24 | 131.41 | 0.596 | 1411.07 | 10.73 | 24.20 |

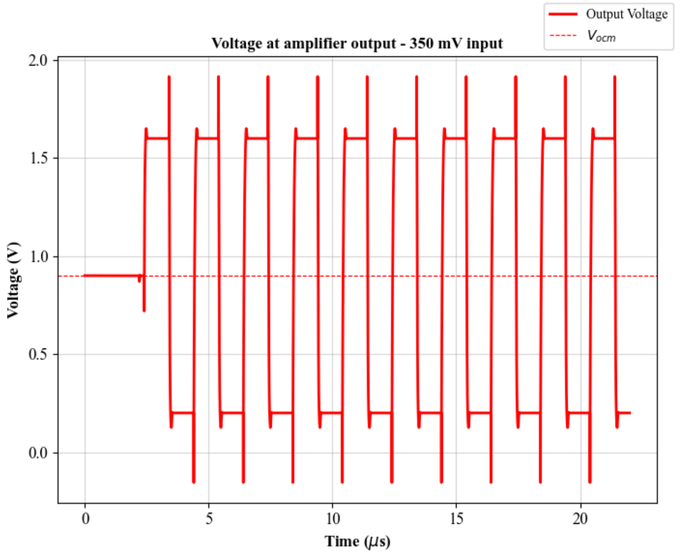
Table 3: Transistor Parameters

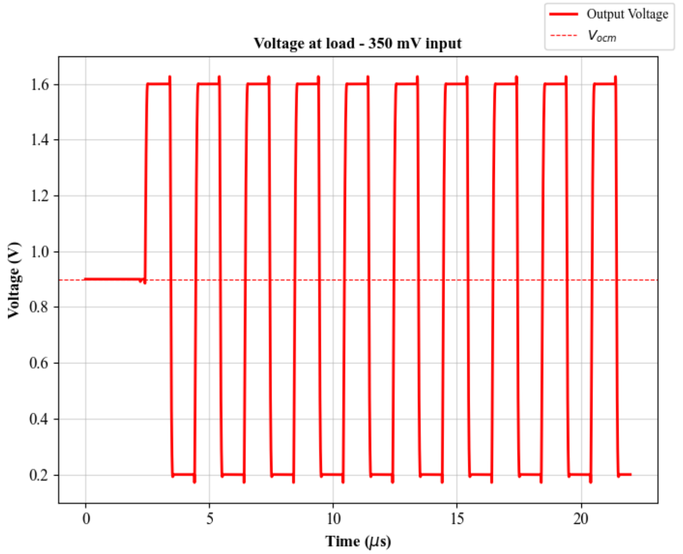
| Component | Purpose | Value | L ($\mu$m) | W ($\mu$m) |
|---|---|---|---|---|
| R3 | Matching VDS for tail XTORs biasing | 6000 | 30 | 1 |
| C0 | Miller Cap | 30 | 5 | 5 |
| C1 | Miller Cap | 30 | 5 | 5 |
| C2 | Miller Cap | 15 | 2 | 5.5 |
| R2 | Resistor to cancel RHP from Miller Cap | 500 | 2 | 5 |

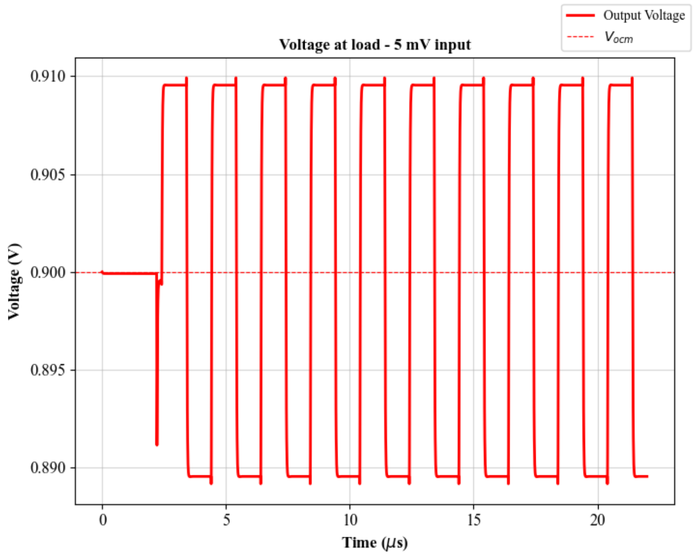
Table 4: Component Parameters

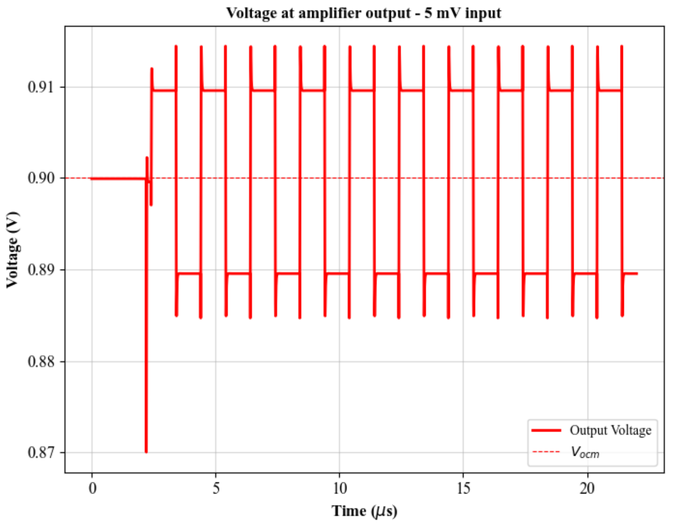
# PSRR

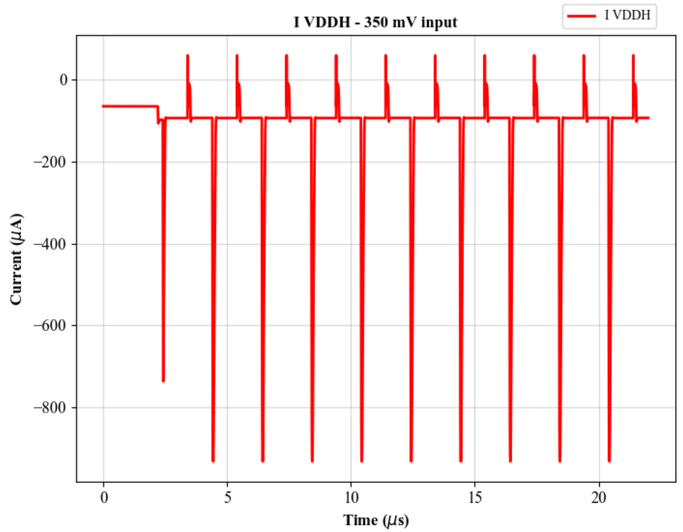

Bode Plot (Magnitude)
PSRR (VDDH) at DC = 62.42 dB
PSRR (VDDL) at DC = 51.53 dB
PSSR (VDDL)
PSSR (VDDH)
Magnitude (dB)
Frequency (Hz)
60
40
20
0
−20
$10^1$
$10^2$
$10^3$
$10^4$
$10^5$
$10^6$
$10^7$
$10^8$
$10^9$

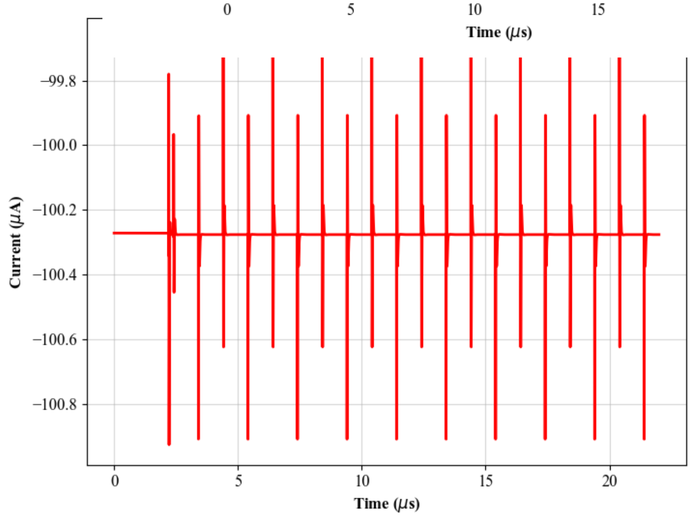

Voltage at amplifier output - 350 mV input
Output Voltage
$V_{ocm}$
Voltage (V)
Time ($\mu$s)

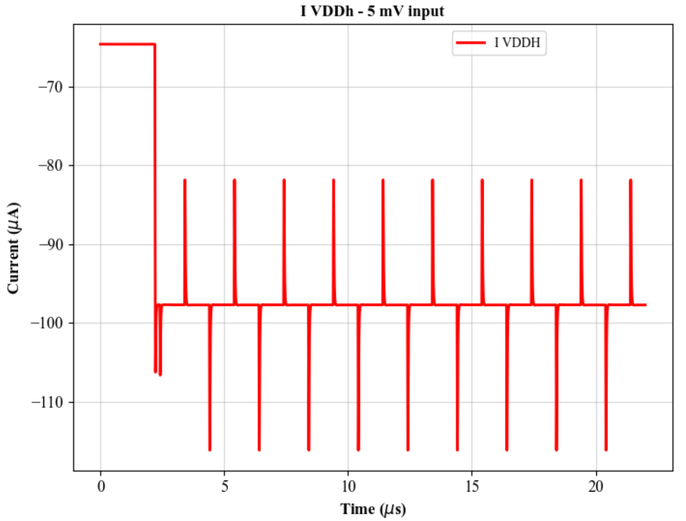

Voltage at load - 350 mV input
Output Voltage
$V_{ocm}$
Voltage (V)
Time ($\mu$s)

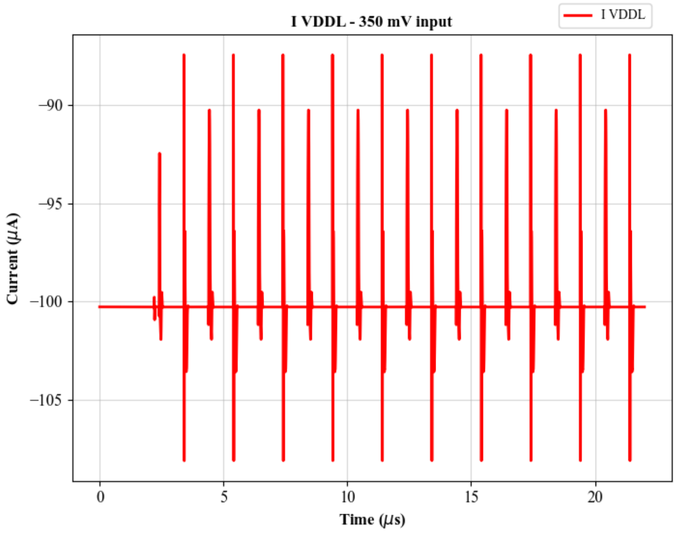

Voltage at load - 5 mV input
Output Voltage
$V_{ocm}$
Voltage (V)
Time ($\mu$s)

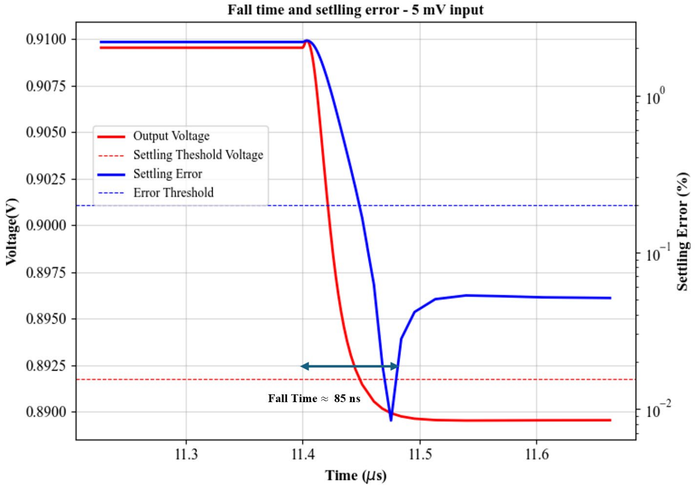

Voltage at amplifier output - 5 mV input
Output Voltage
$V_{ocm}$
Voltage (V)
Time ($\mu$s)

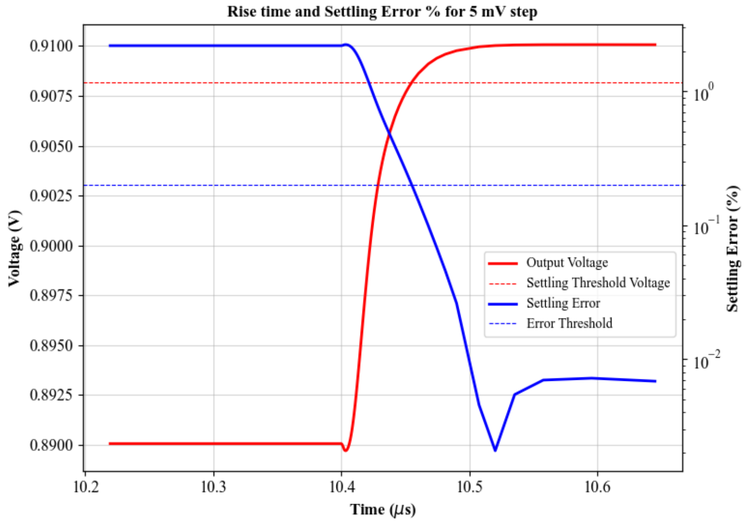

I VDDH - 350 mV input
I VDDH
0
−200
−400
−600
−800
Current (μA)
0
5
10
15
20
Time (μs)


−99.8
−100.0
−100.2
−100.4
−100.6
−100.8
Current (μA)
0
5
10
15
20
Time (μs)


I VDDh - 5 mV input
I VDDH
−70
−80
−90
−100
−110
Current (μA)
0
5
10
15
20
Time (μs)


I VDDL - 350 mV input
I VDDL
−90
−95
−100
−105
Current (μA)
0
5
10
15
20
Time (μs)


Fall time and settling error - 5 mV input
Output Voltage
Settling Theshold Voltage
Settling Error
Error Threshold
Fall Time ≈ 85 ns
Voltage(V)
Settling Error (%)
Time (μs)


Rise time and Settling Error % for 5 mV step
Output Voltage
Settling Threshold Voltage
Settling Error
Error Threshold
Voltage (V)
Settling Error (%)
Time (μs)