# AHD - LAB #7

Complete RC5 on FPGA

Due on 03/12/2016 (6 P.M)

# Lab #7 – Complete RC5 on FPGA

1. Implement the complete RC5 on FPGA
   - Implement both encryption, decryption and key expansion on FPGA.
     - Use structural modelling to integrate the modules from earlier lab.
     - You can use a switch to select between encryption/decryption.
   - You can use switches/push buttons to change input Din and Key (Facilitate changing at least 32 bits of input)
   - Display the output on 7-segment LED display

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- The DELIVERABLES are:
  - VHDL code (Submit the file(s) in zip file – Don't include in the lab report).
  - Write on the methodology you used to send inputs and capture the outputs. (Eg: How the switches/push buttons are mapped and how they select the different segments of your inputs)
  - Test cases: 2 different values of Input
  - Report the resource utilization (After synthesis and after Place-and-Route (PAR)).
  - Functional Simulation: Screen-shots of Isim/Modelsim wave window for all test cases.
  - Block diagram, FSM (if any) and schematic
  - Timing simulation: Screen-shot of Isim/ModelSim wave window for all test cases.
  - Report the critical path delay.
  - Demo Video

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- Upload the demo video on YouTube and place the link in report.
- Maximum length of the video 4 mins.

- VHDL Code naming the zip folder guidelines:
  - Name your code zip folder →NETID_lab7_vhd.zip

# Lab #7 – Complete RC5 on FPGA

- Submit a single report. Name it NETID_lab7_report.pdf
- You can reuse codes from your previous labs.

# CAUTION – READ CAREFULLY

- **Important: We are using a Plagiarism checking service. Only one submission is available. You cannot resubmit/modify the report after submission. Please heed caution when submitting the report. Submit only the final version. Sending a modified report to TA/Professor is not allowed.**