PHASE3

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Approved by	Name	Signature	Date

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EE 477

Revision History

Date	**Version**	**List of changes**	**Author + Signature**

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4.4 REPORT **ERROR! BOOKMARK NOT DEFINED.**

1 General Guidelines

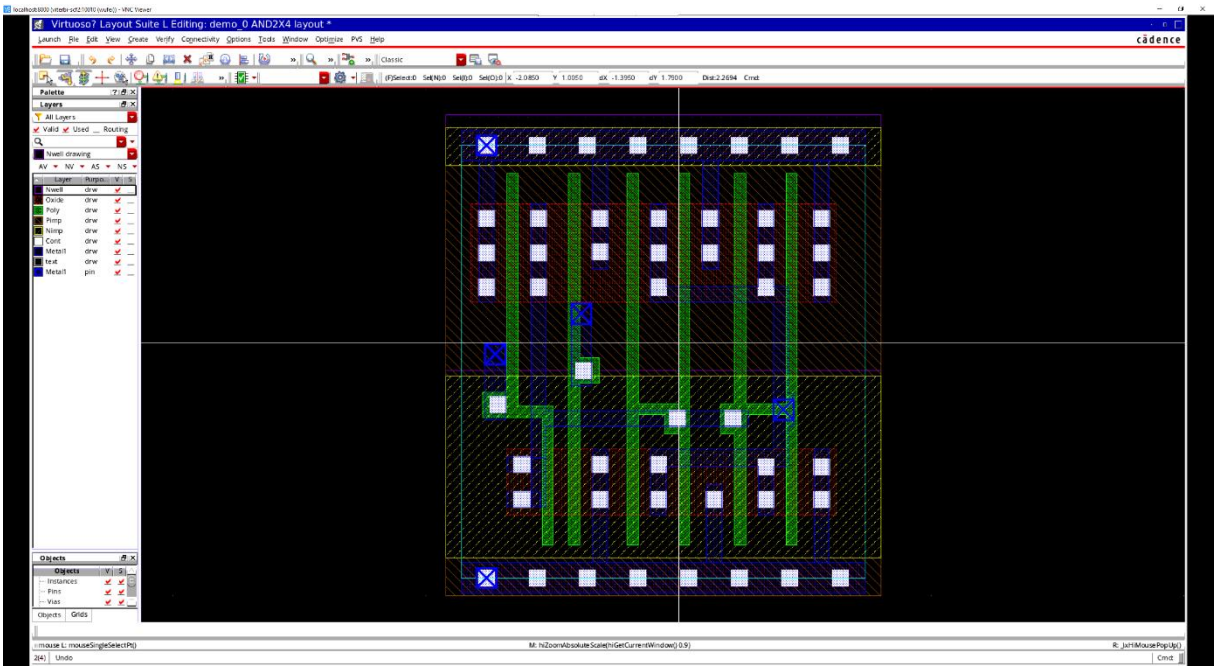
General Guidelines

You are allowed to use the logic cells and circuits you designed in previous labs, or redesign them.
Use Vdd = 1.8V
Use rise and fall time for all input stimuli = 10ps (Note that it is NOT 100)
Every primary input and primary output of the design should be connected a flip-flop.

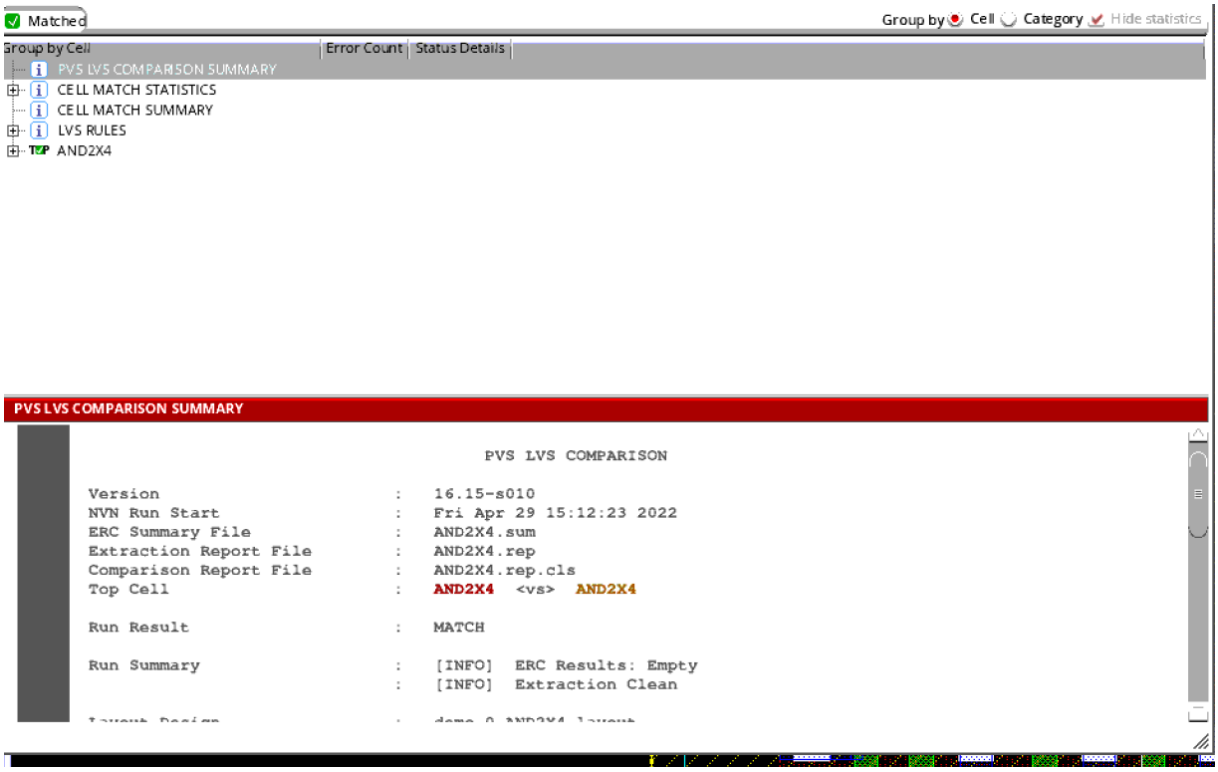
2 MUL

2.1 AND2X4

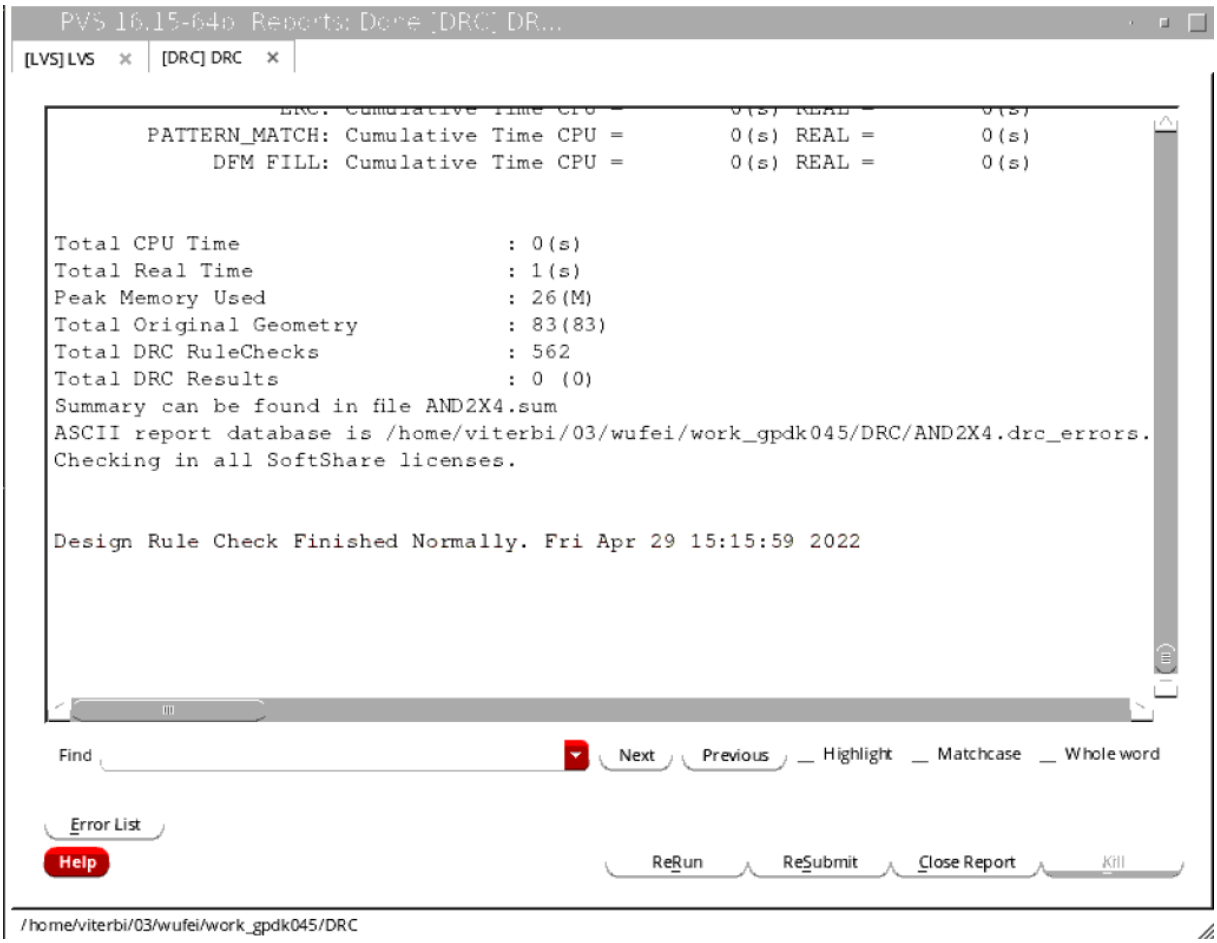
2.1.1 Layout



2.1.2 LVS

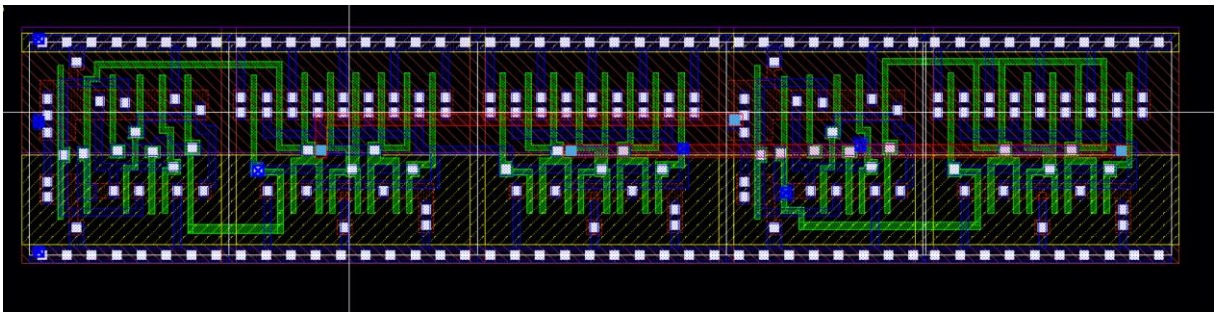


2.1.3 DRC



2.2 ADDER1bit

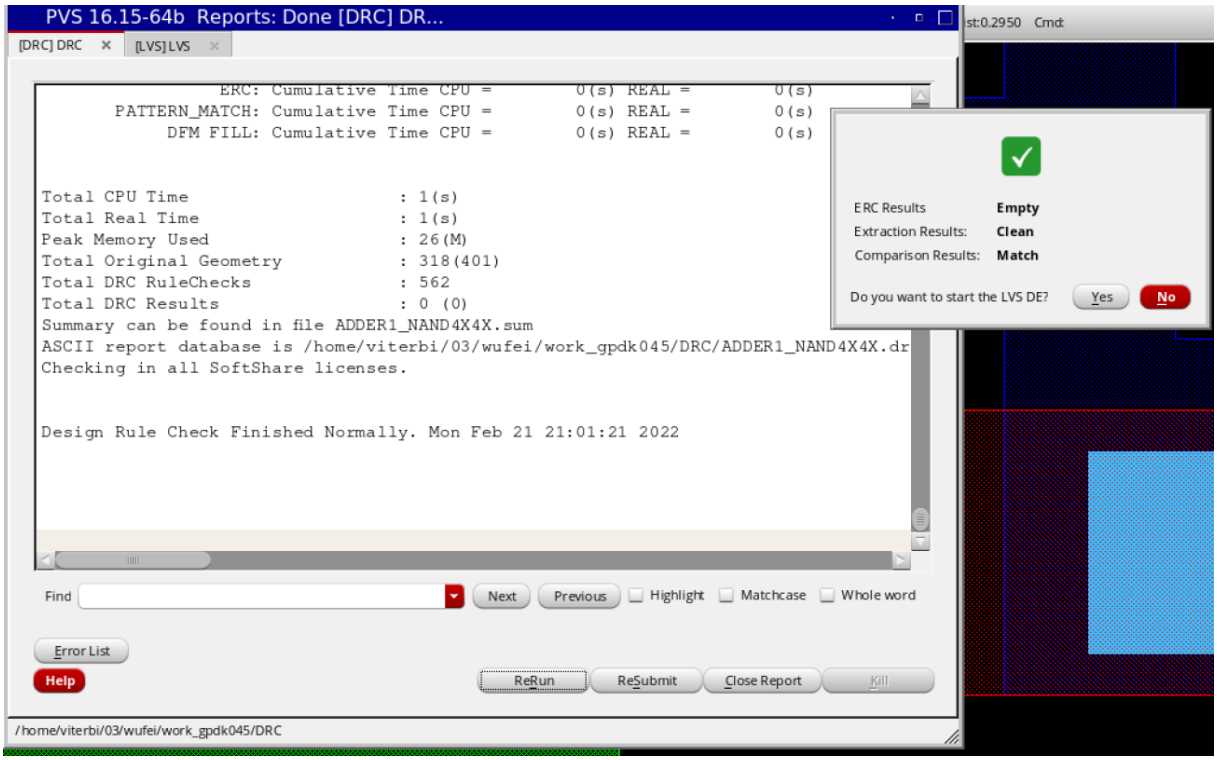
2.2.1 Layout



2.2.2 DRC

```
Peak Memory Used        : 234.57(M)

    ##########################################################
    #                                                        #
    # Run Result              : MATCH                        #
    #                                                        #
    # Run Summary             : [INFO]  ERC Results: Empty   #
    #                         : [INFO]  Extraction Clean     #
    #                                                        #
    # ERC Summary File        : ADDER1_NAND4X4X.sum          #
    # Extraction Report File  : ADDER1_NAND4X4X.rep          #
    # Comparison Report File  : ADDER1_NAND4X4X.rep.cls      #
    #                                                        #
    ##########################################################

Checking in all SoftShare licenses.
```

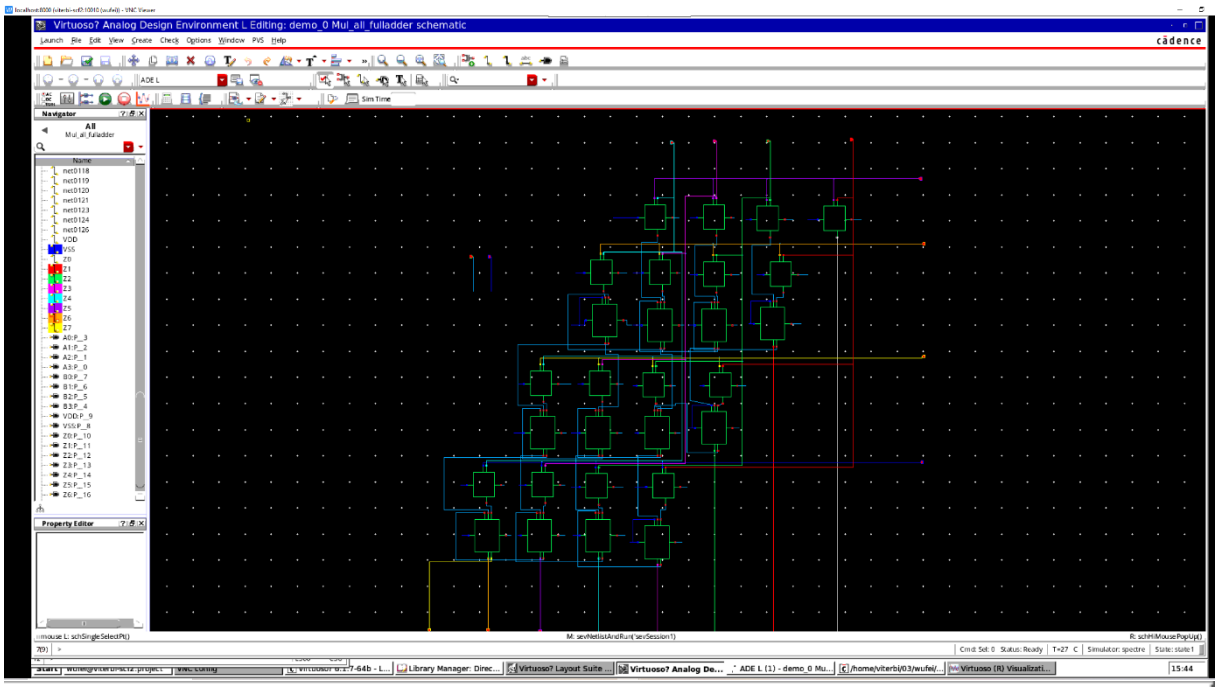
2.2.3 LVS



2.3 MUL

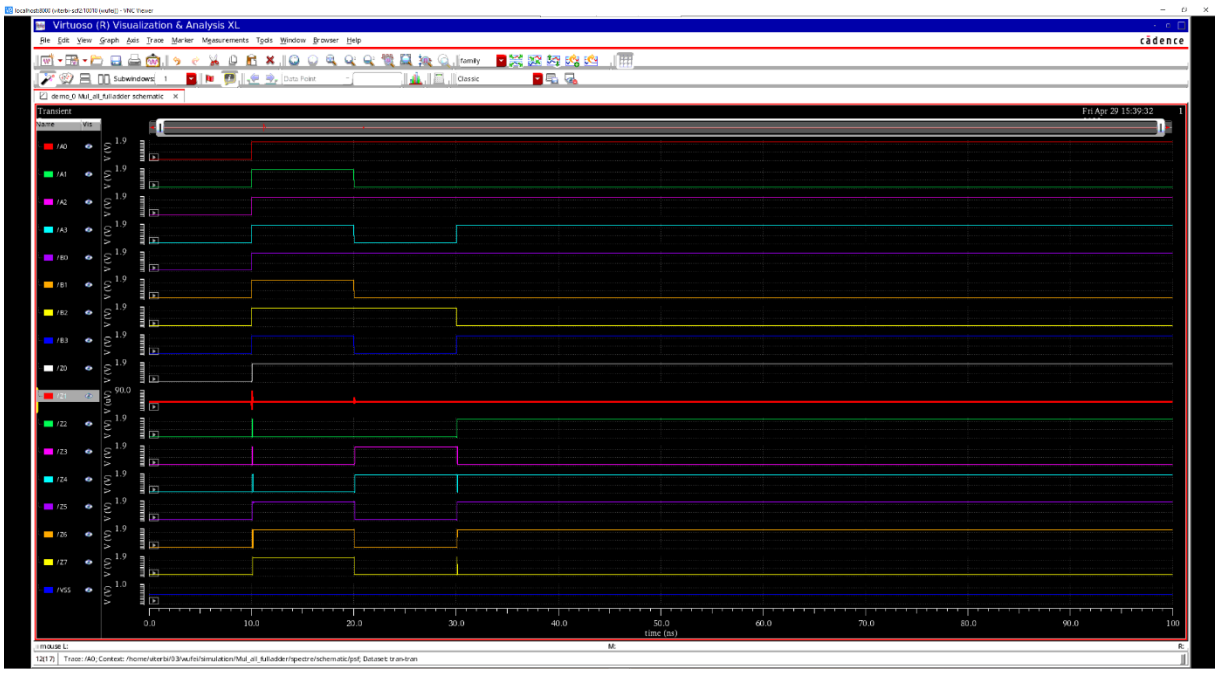
2.3.1 Changes

Some slight changes on the mul.
Choosing to use the full adder1 to consist the multiplexer, which will make the layout much more structured.
By changing the schematic, retest the logic correct

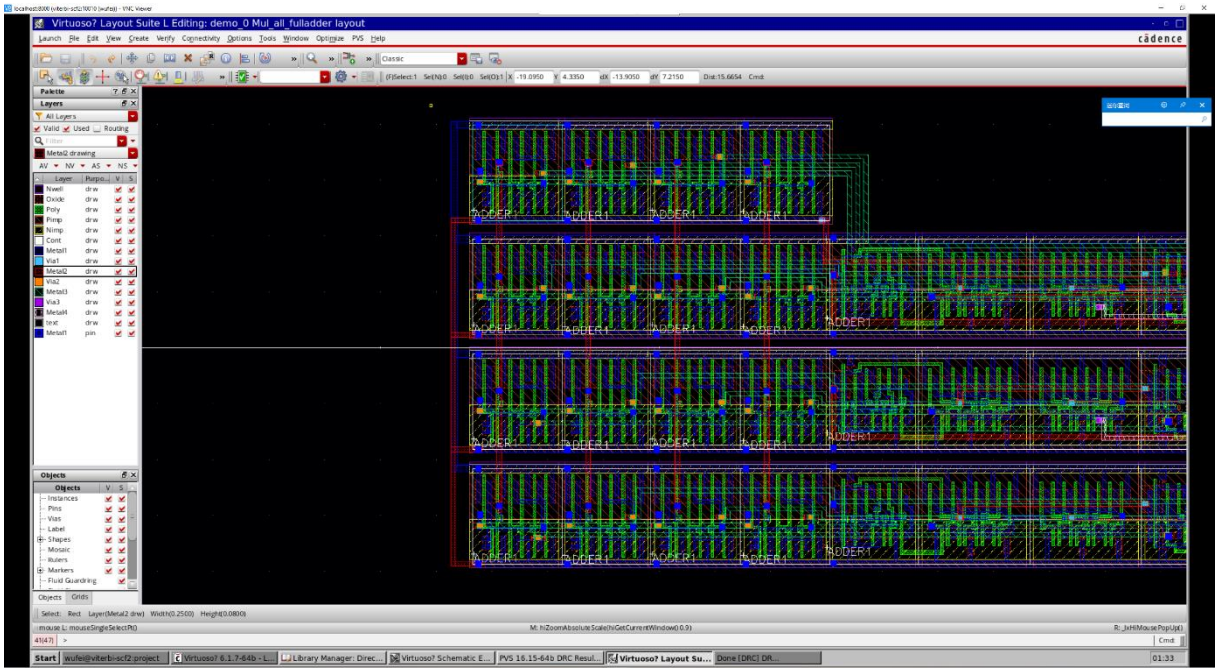


wufei@viterbi-scf2:project

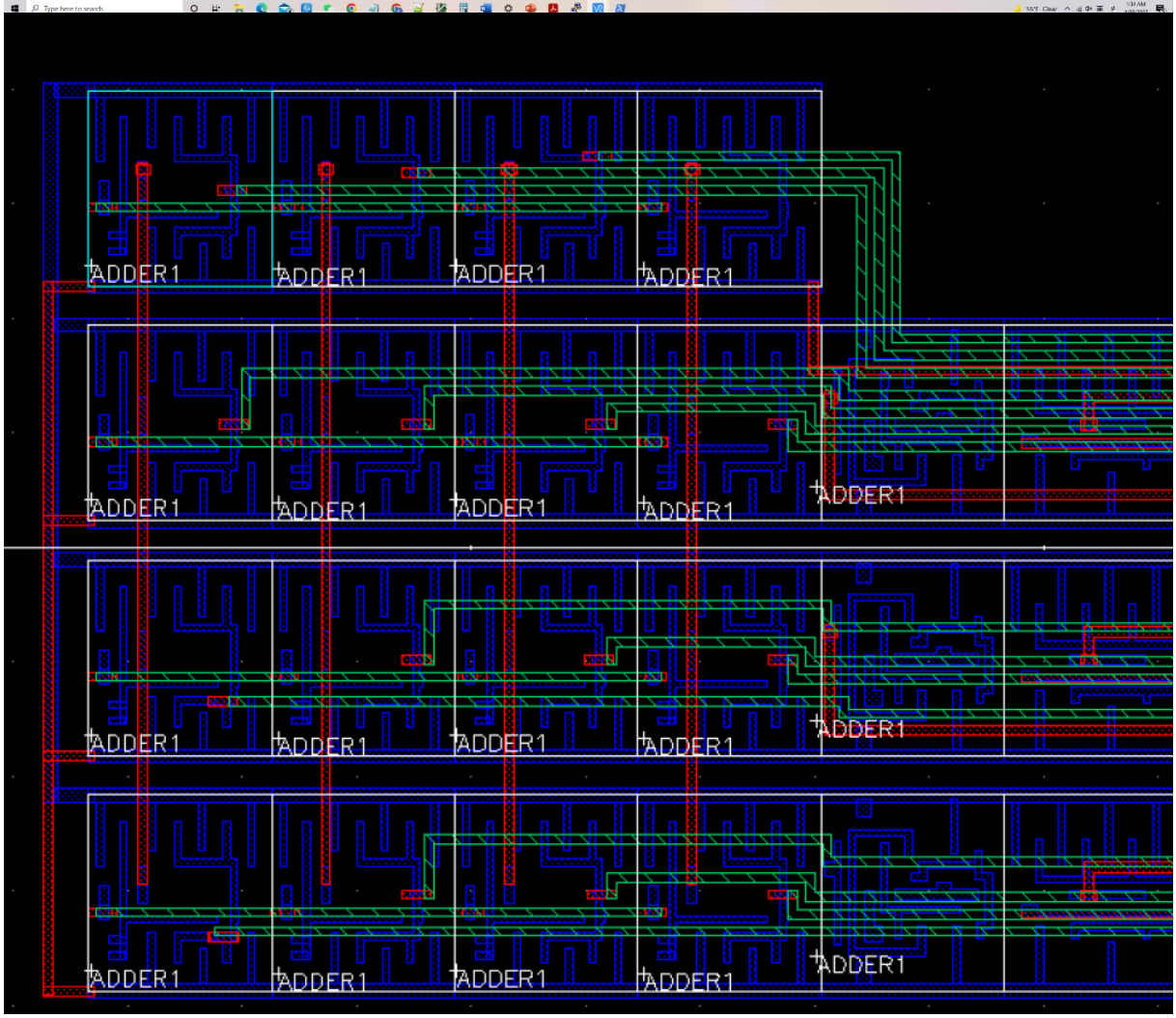
```
radix 1    1    1    1    1    1    1    1
vname A3   A2   A1   A0   B3   B2   B1   B0
io    i    i    i    i    i    i    i    i

tunit 10ns
vih 1.8
vil 0
voh 1.8
vol 0
trise 10p
tfall 10p

tdelay 0 0 0 0 0 0 0 0 0

;mul

0 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1
2 0 1 0 1 0 1 0 1
3 1 1 0 1 1 0 0 1
```

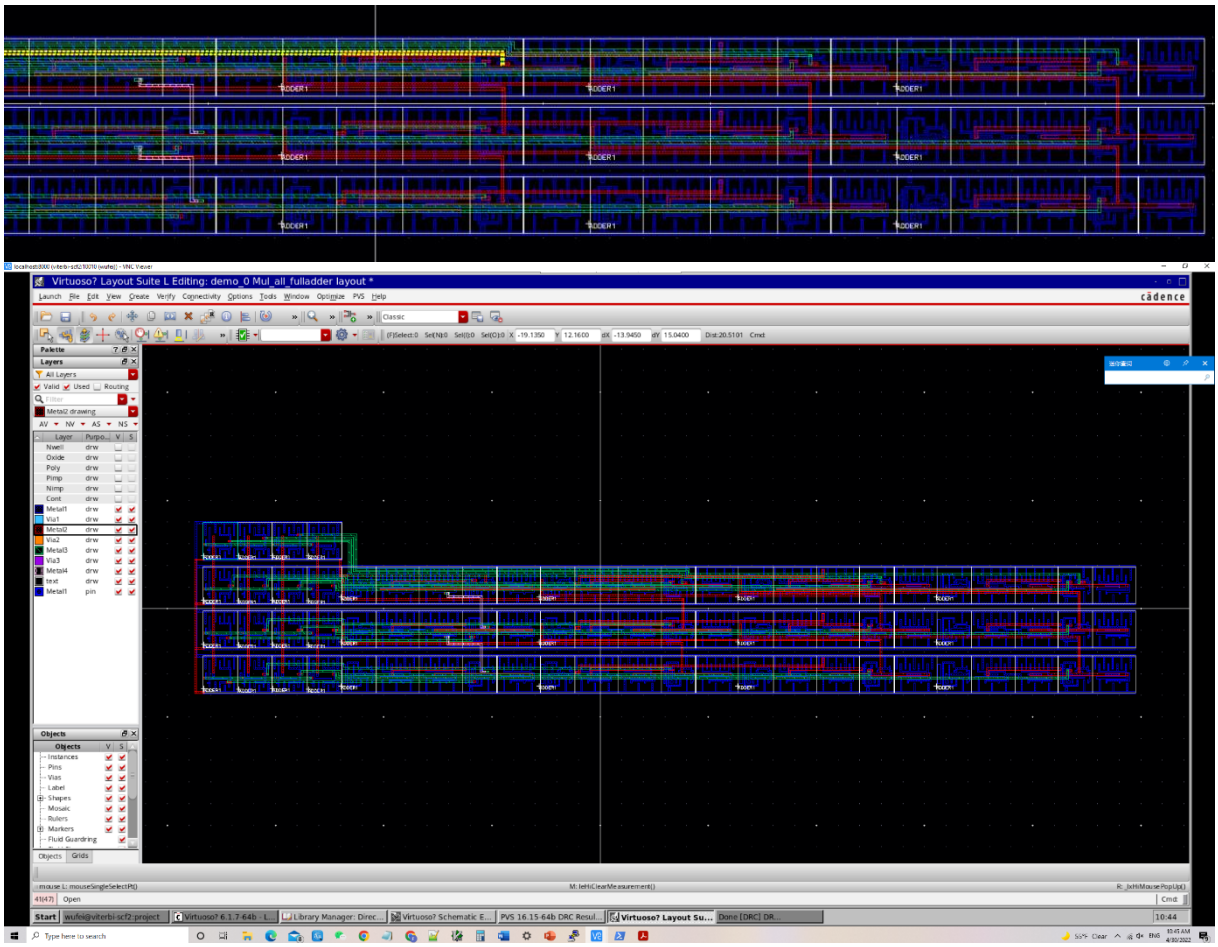

Virtuoso (R) Visualization & Analysis XL
cadence
demo_0 Mul_all_fulladder schematic
Transient
Fri Apr 29 15:39:32
time (ns)

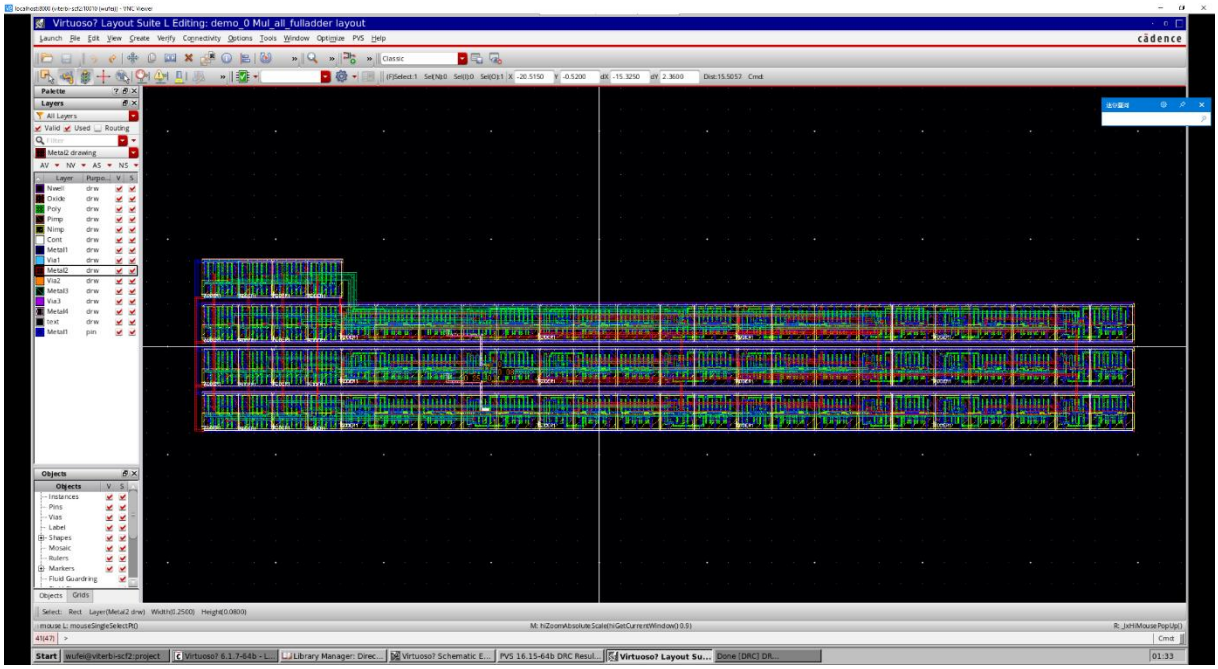
2.3.2 Layout


Virtuoso? Layout Suite L Editing: demo_0 Mul_all_fulladder layout
cadence
ADDER1

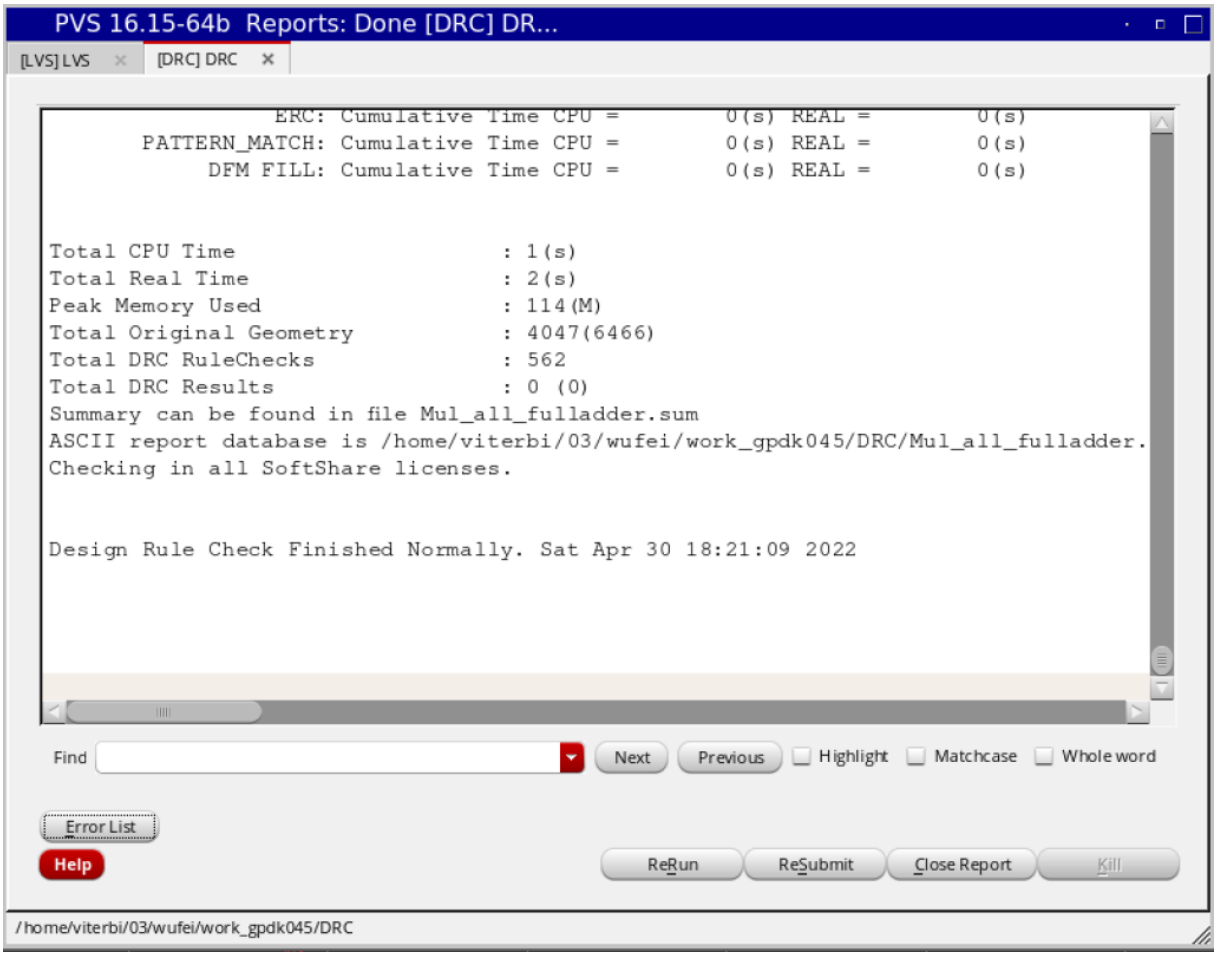
Virtuoso? Layout Suite L Editing: demo_0 Mul_all_fulladder layout
cadence
ADDER1


ADDER1

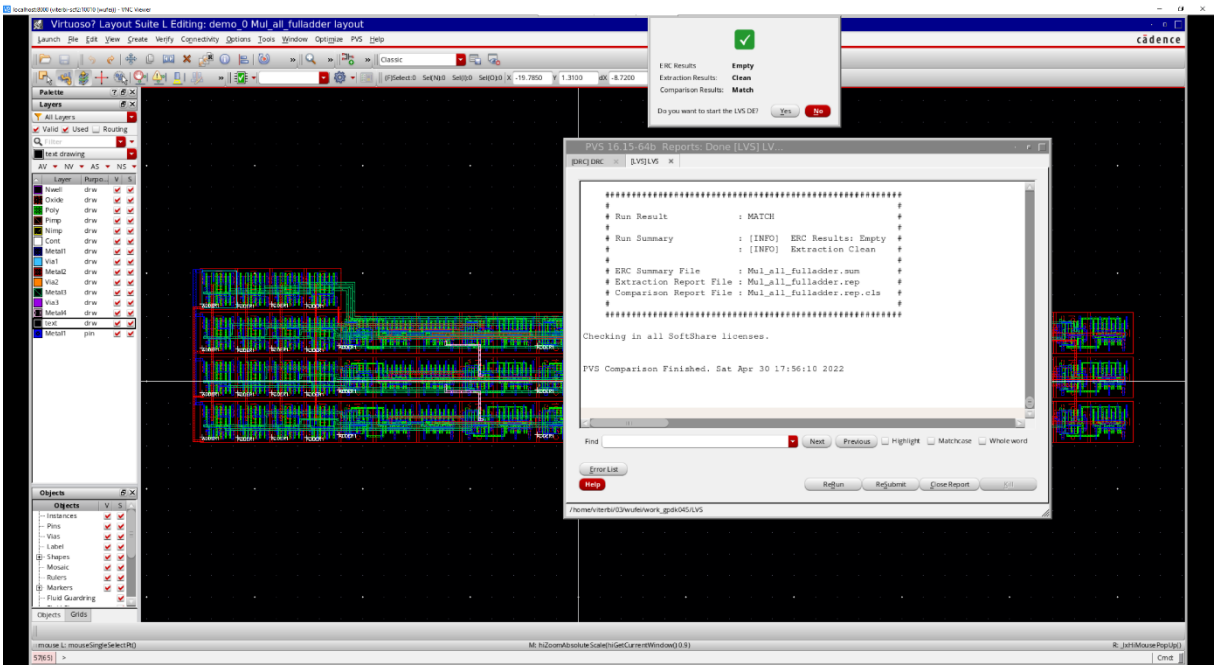

Virtuoso? Layout Suite L Editing: demo_0 Mul_all_fulladder layout *
cadence


Virtuoso? Layout Suite L Editing: demo_0 Mul_all_fulladder layout
cadence

2.3.3 DRC

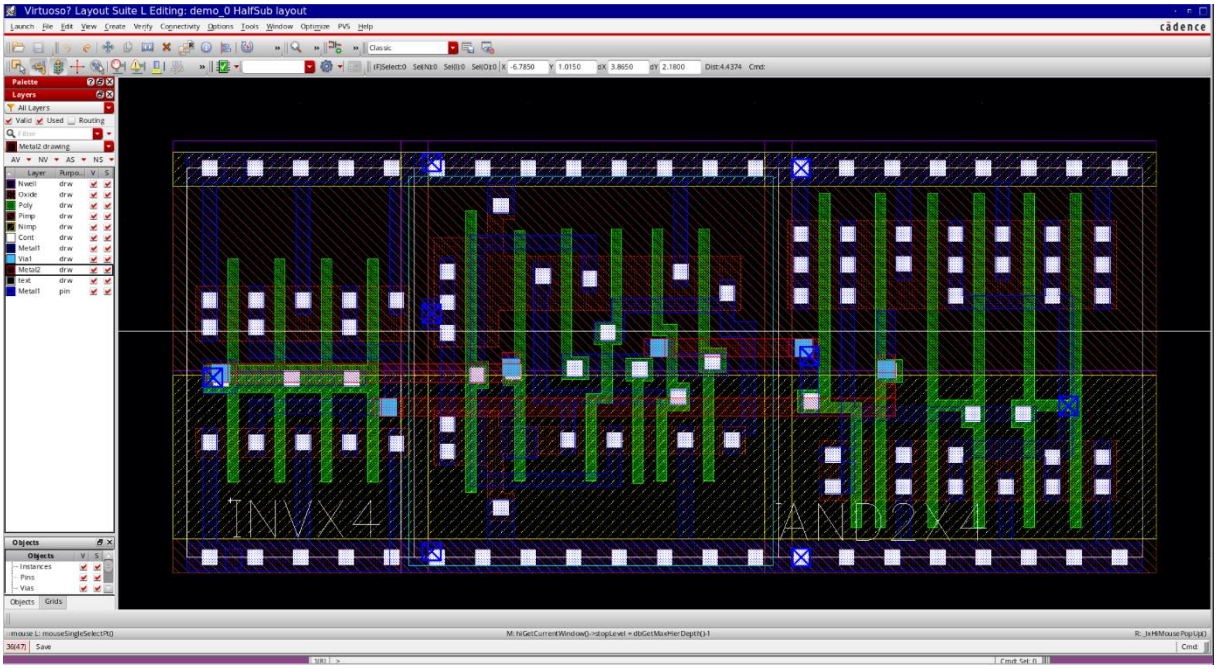


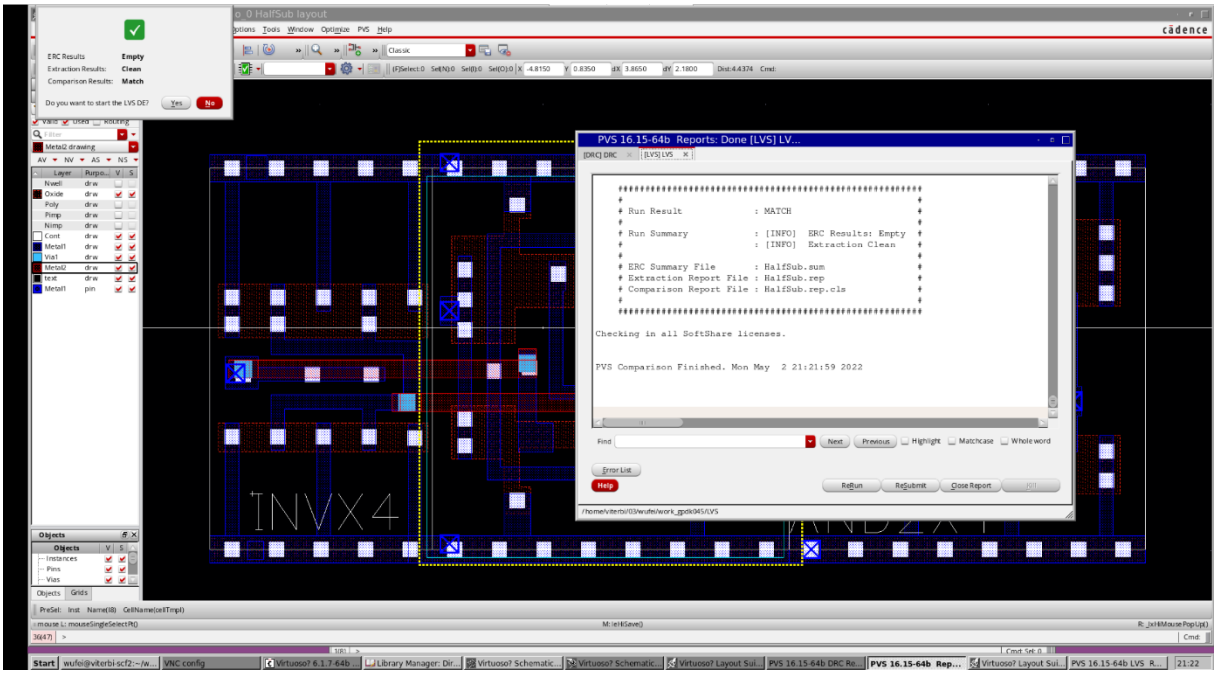
2.3.4 LVS

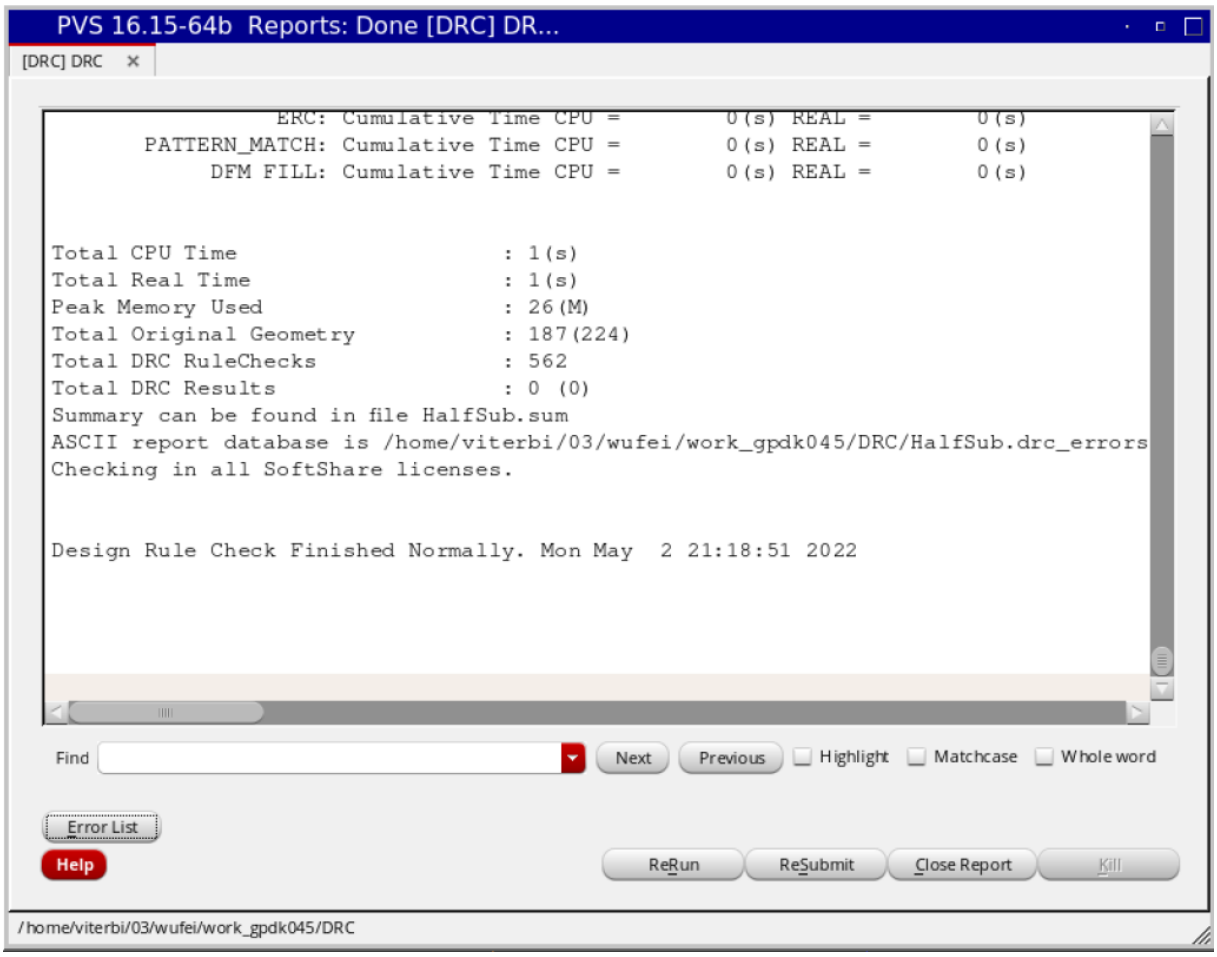


3 Divider

3.1 Halfsub

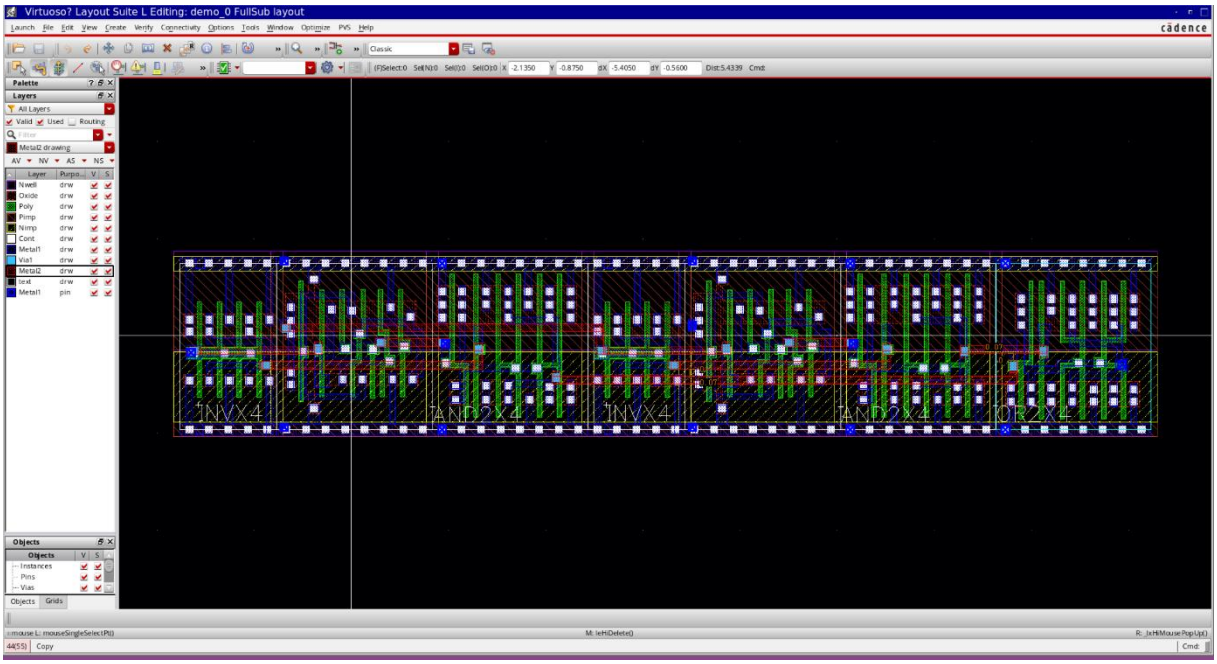




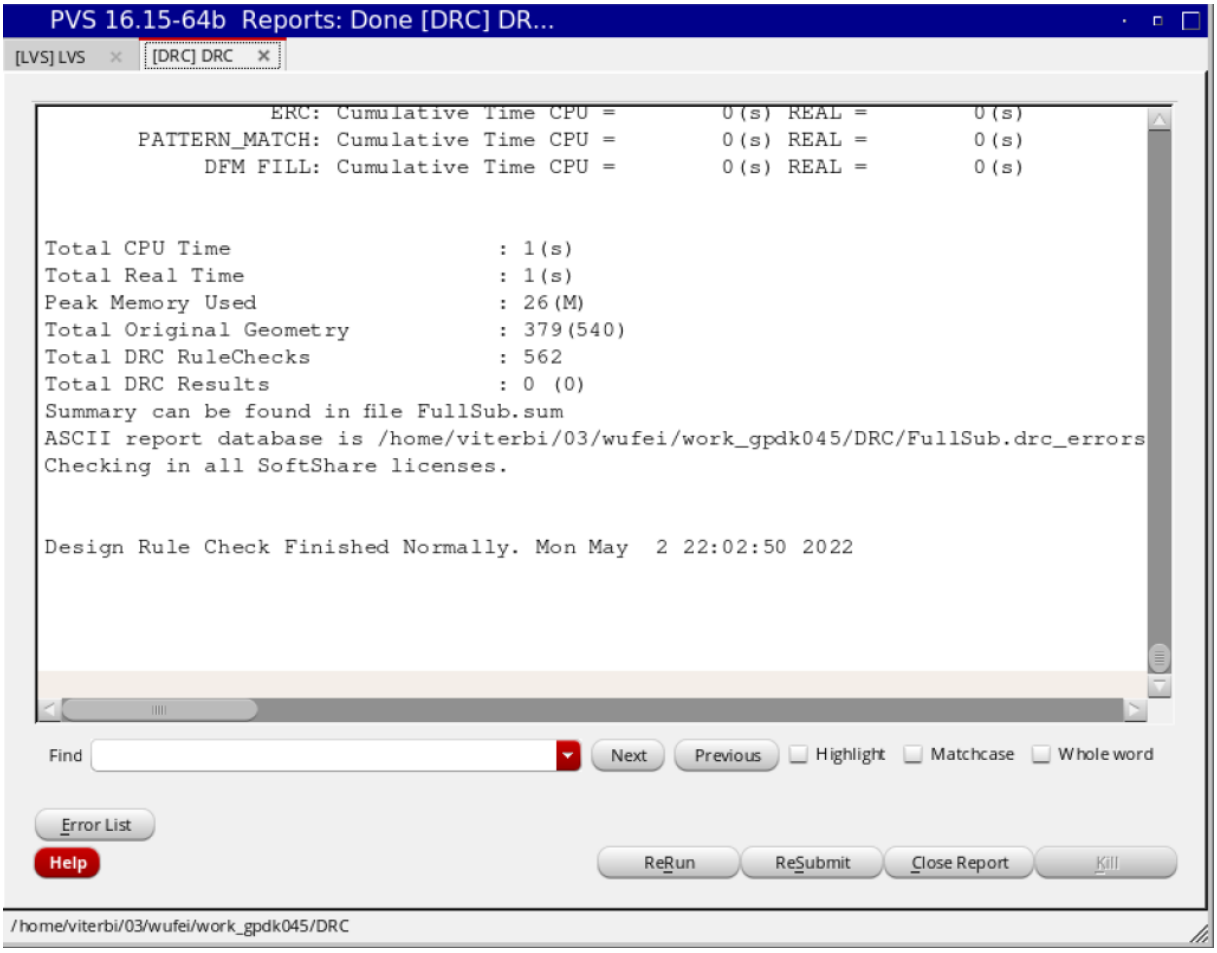


3.2 Fullsub

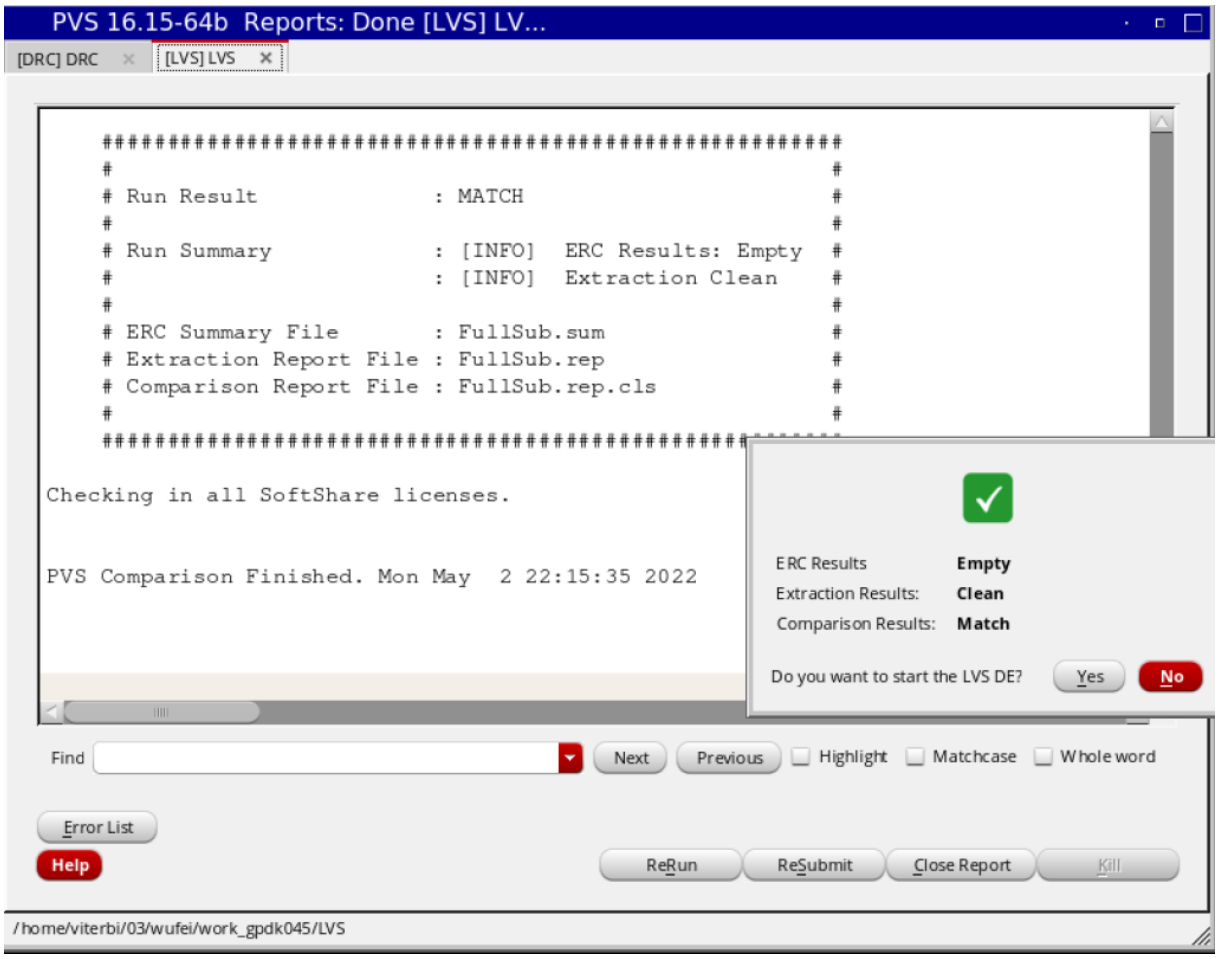
3.2.1 Loyout



3.2.2 LVS

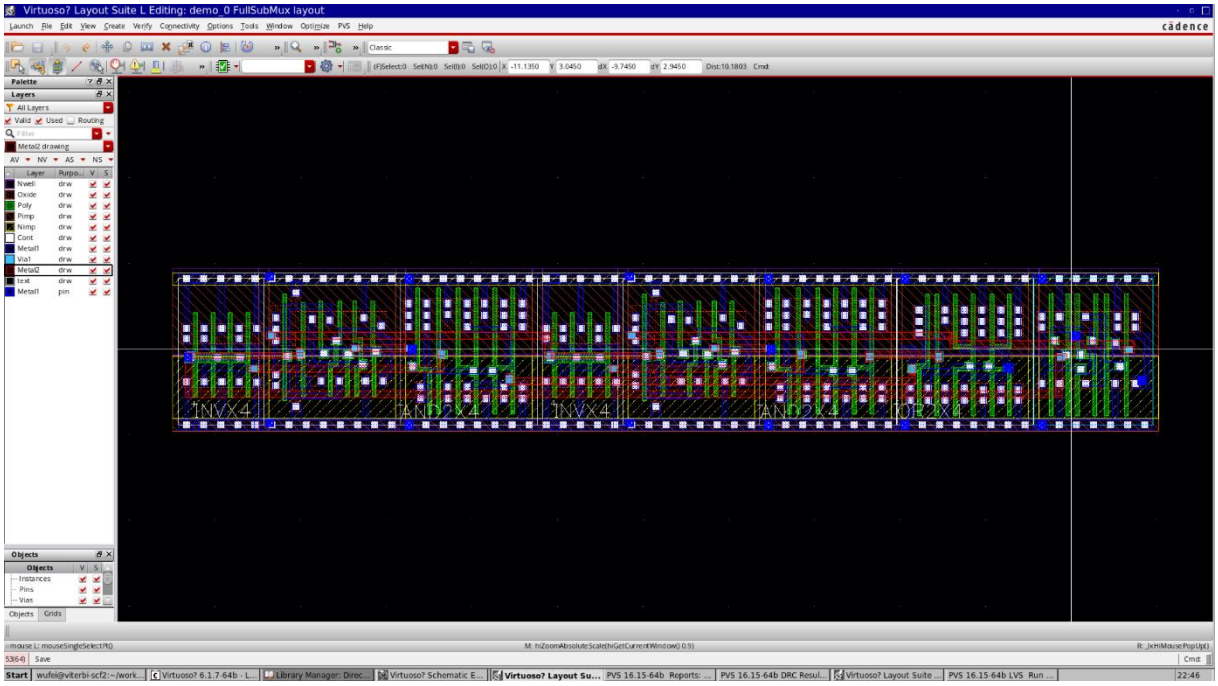

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 1(s)
Peak Memory Used : 26(M)
Total Original Geometry : 379(540)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file FullSub.sum
ASCII report database is /home/viterbi/03/wufei/work_gpdk045/DRC/FullSub.drc_errors
Checking in all SoftShare licenses.
Design Rule Check Finished Normally. Mon May 2 22:02:50 2022
Find
Next
Previous
Highlight
Matchcase
Whole word
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/03/wufei/work_gpdk045/DRC

3.2.3 DRC

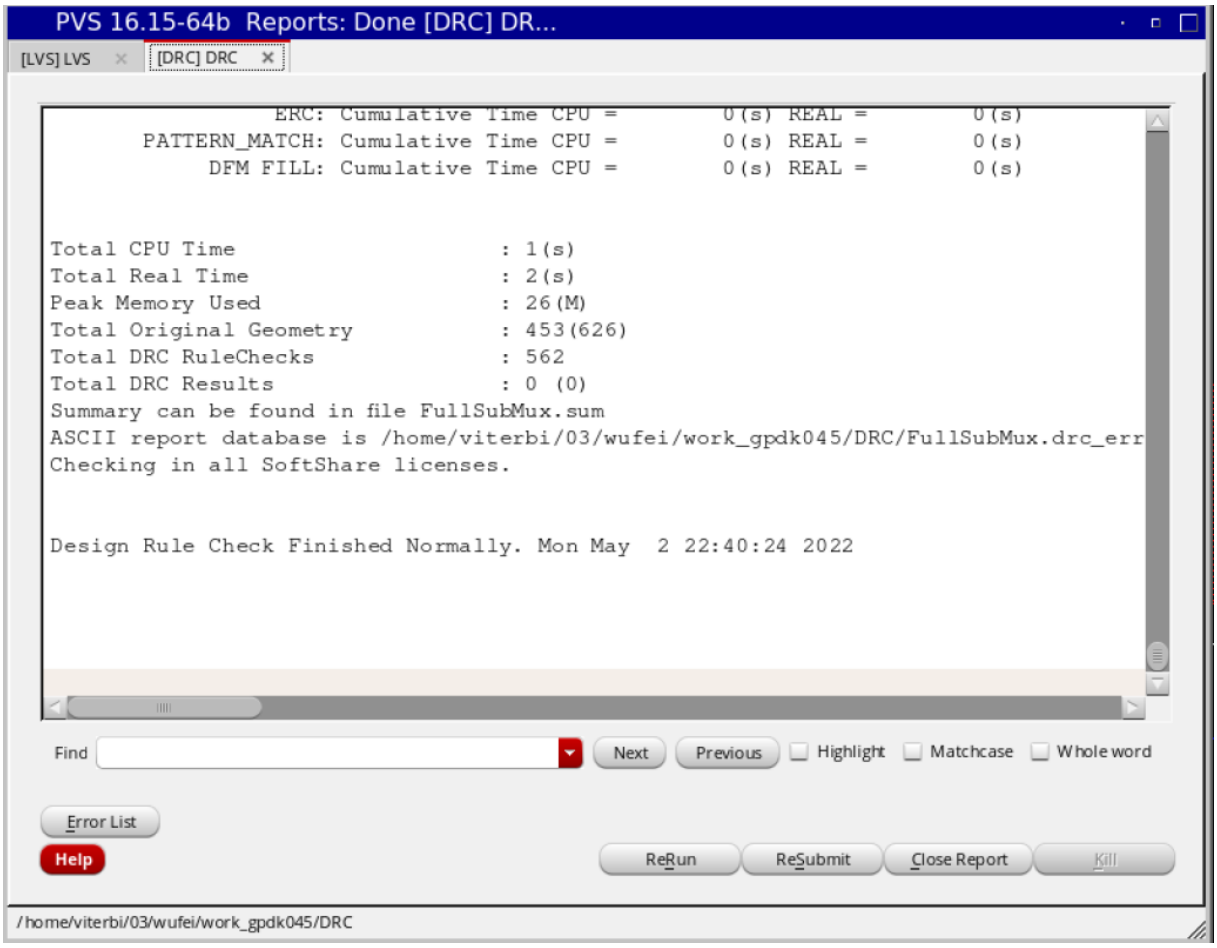

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : FullSub.sum
Extraction Report File : FullSub.rep
Comparison Report File : FullSub.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Mon May 2 22:15:35 2022
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Previous
Highlight
Matchcase
Whole word
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/03/wufei/work_gpdk045/LVS

3.3 FullSubmux

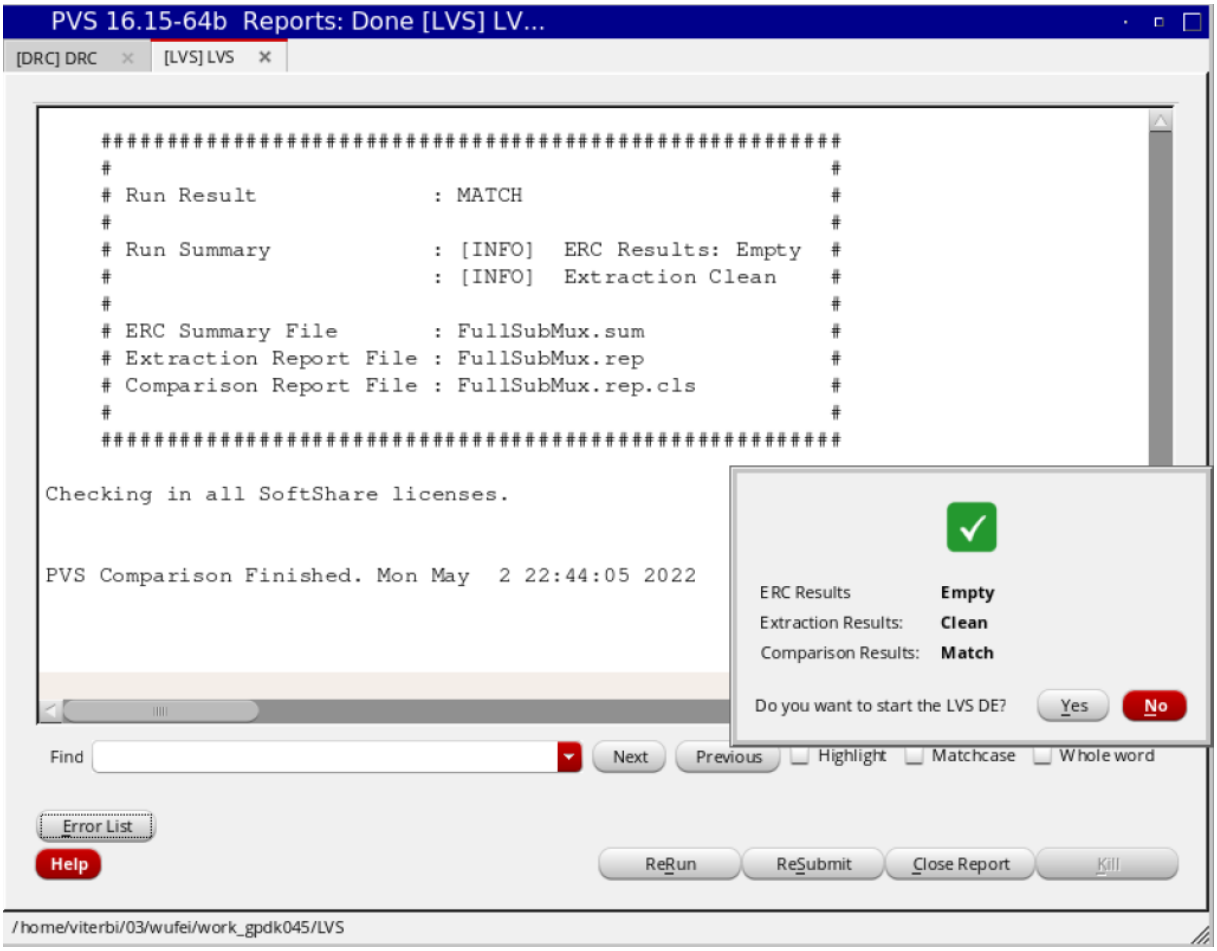
3.3.1 Layout



3.3.2 DRC

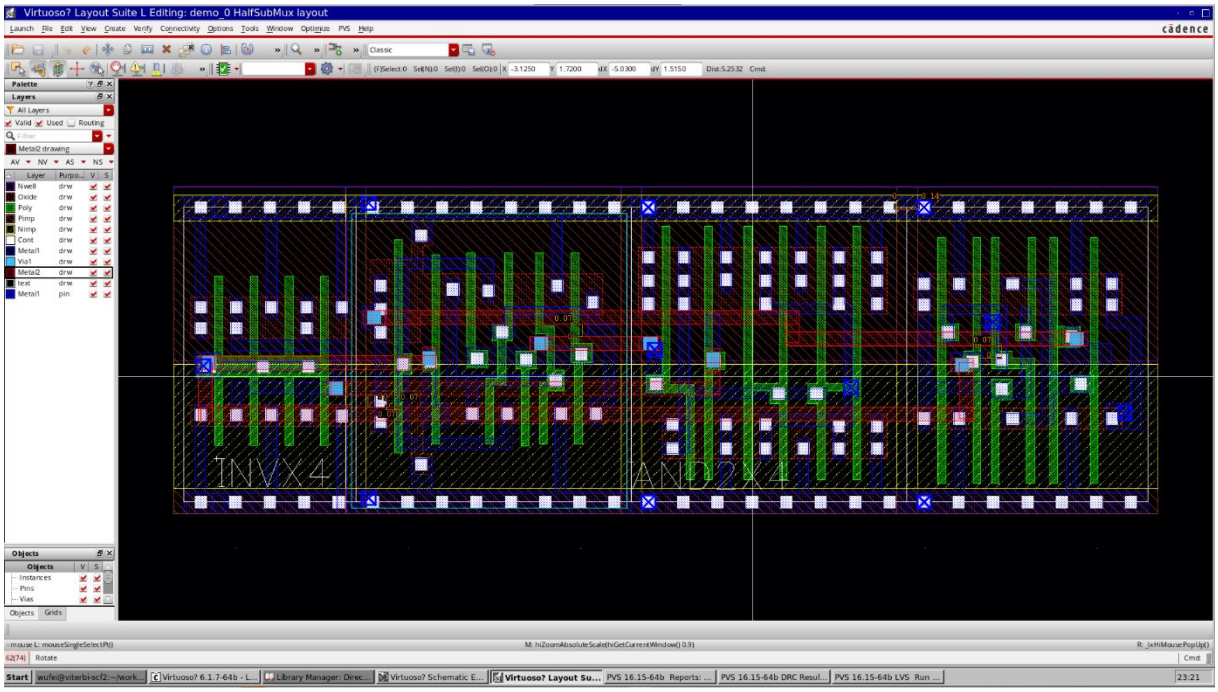

PVS 16.15-64b Reports: Done [DRC] DR...
[LVS] LVS
[DRC] DRC
ERC: Cumulative Time CPU = 0(s) REAL = 0(s)
PATTERN_MATCH: Cumulative Time CPU = 0(s) REAL = 0(s)
DFM FILL: Cumulative Time CPU = 0(s) REAL = 0(s)
Total CPU Time : 1(s)
Total Real Time : 2(s)
Peak Memory Used : 26(M)
Total Original Geometry : 453(626)
Total DRC RuleChecks : 562
Total DRC Results : 0 (0)
Summary can be found in file FullSubMux.sum
ASCII report database is /home/viterbi/03/wufei/work_gpdk045/DRC/FullSubMux.drc_err
Checking in all SoftShare licenses.
Design Rule Check Finished Normally. Mon May 2 22:40:24 2022
Find
Next
Previous
Highlight
Matchcase
Whole word
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/03/wufei/work_gpdk045/DRC

3.3.3 LVS

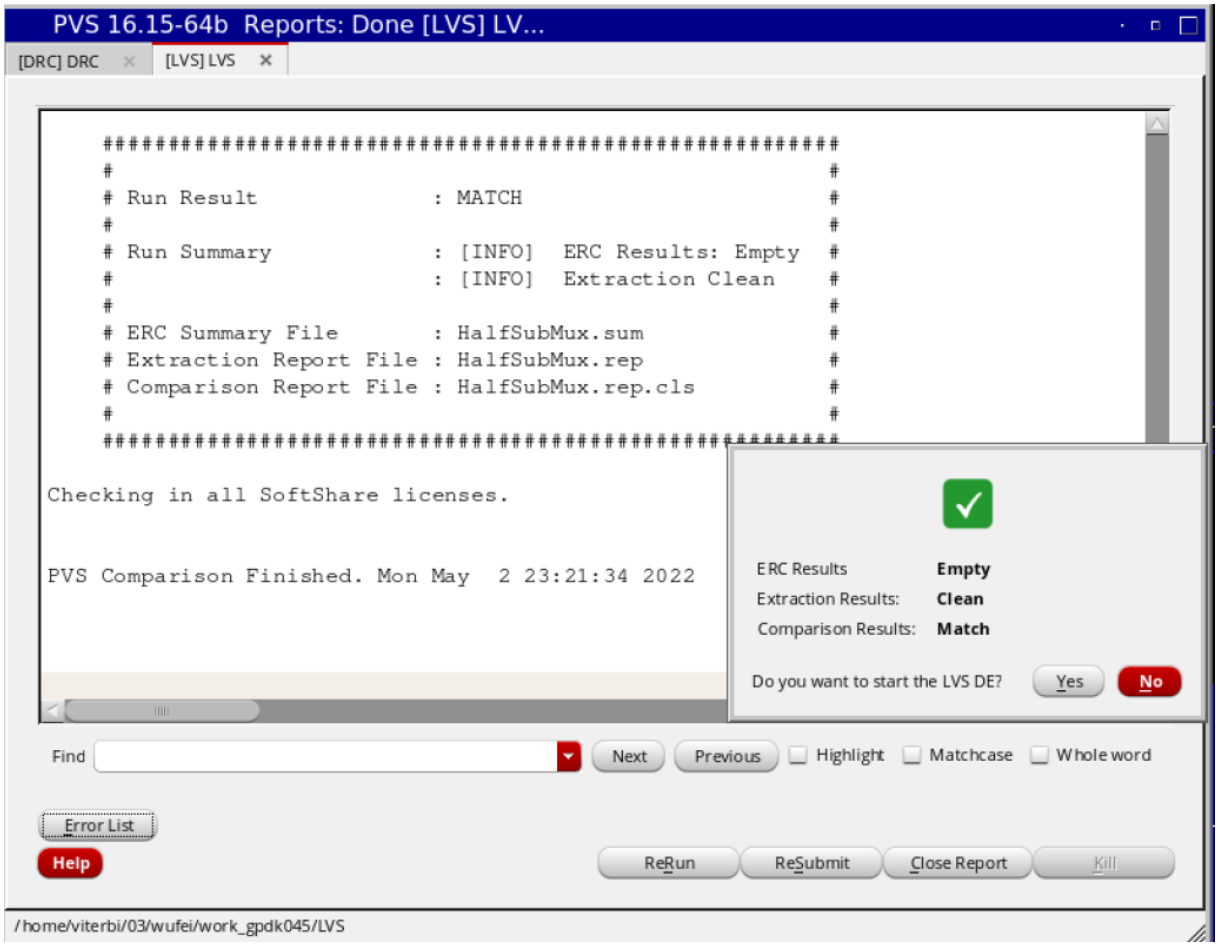

PVS 16.15-64b Reports: Done [LVS] LV...
[DRC] DRC
[LVS] LVS
Run Result : MATCH
Run Summary : [INFO] ERC Results: Empty
: [INFO] Extraction Clean
ERC Summary File : FullSubMux.sum
Extraction Report File : FullSubMux.rep
Comparison Report File : FullSubMux.rep.cls
Checking in all SoftShare licenses.
PVS Comparison Finished. Mon May 2 22:44:05 2022
ERC Results Empty
Extraction Results: Clean
Comparison Results: Match
Do you want to start the LVS DE?
Yes
No
Find
Next
Previous
Highlight
Matchcase
Whole word
Error List
Help
ReRun
ReSubmit
Close Report
Kill
/home/viterbi/03/wufei/work_gpdk045/LVS

3.4 HalfsubMux

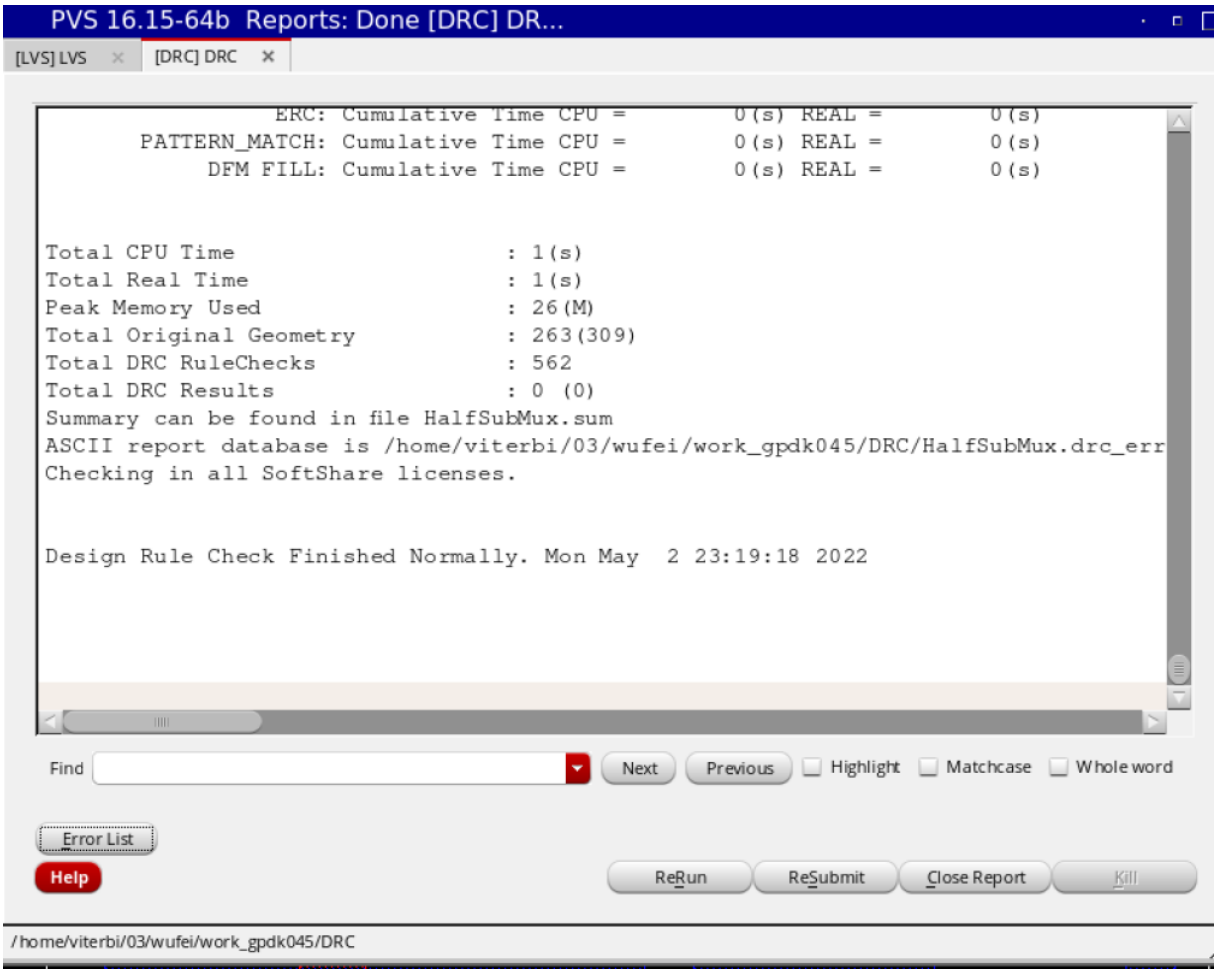
3.4.1 Layout



3.4.2 LVS

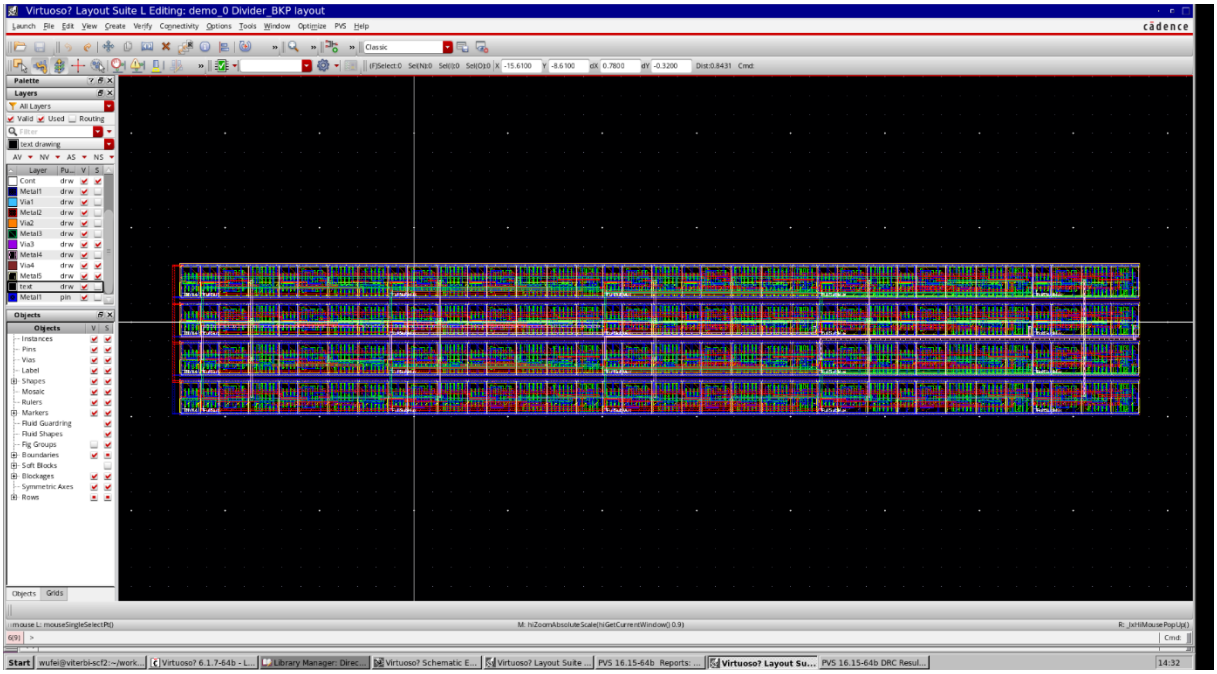


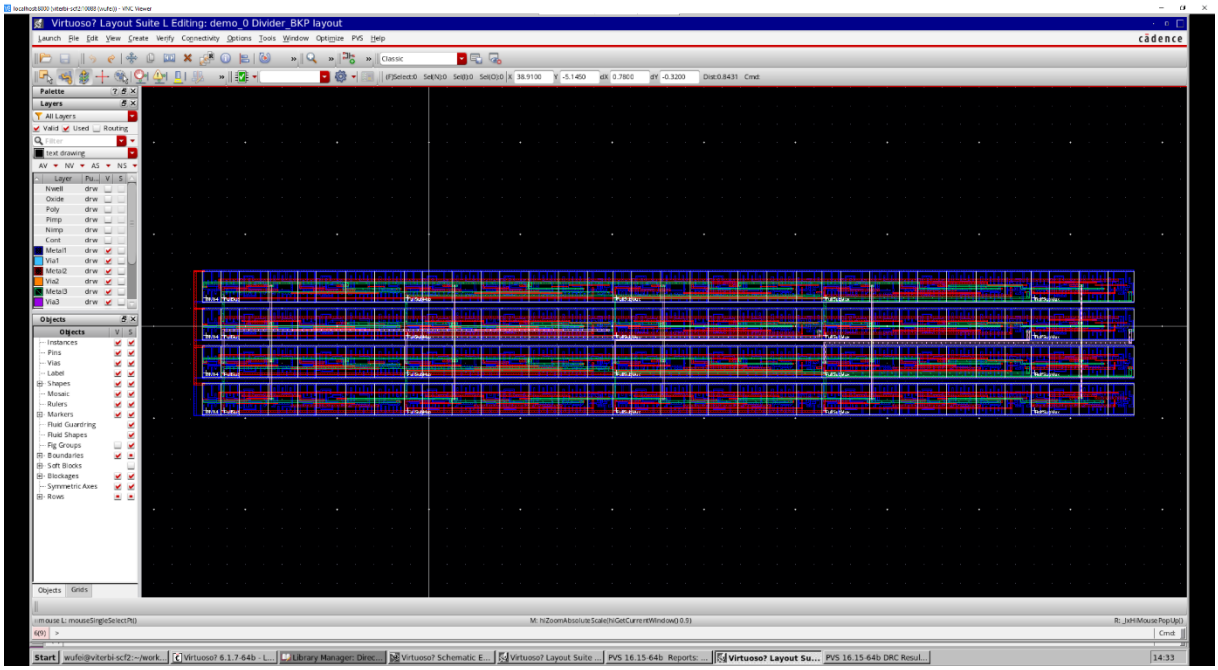
3.4.3 DRC

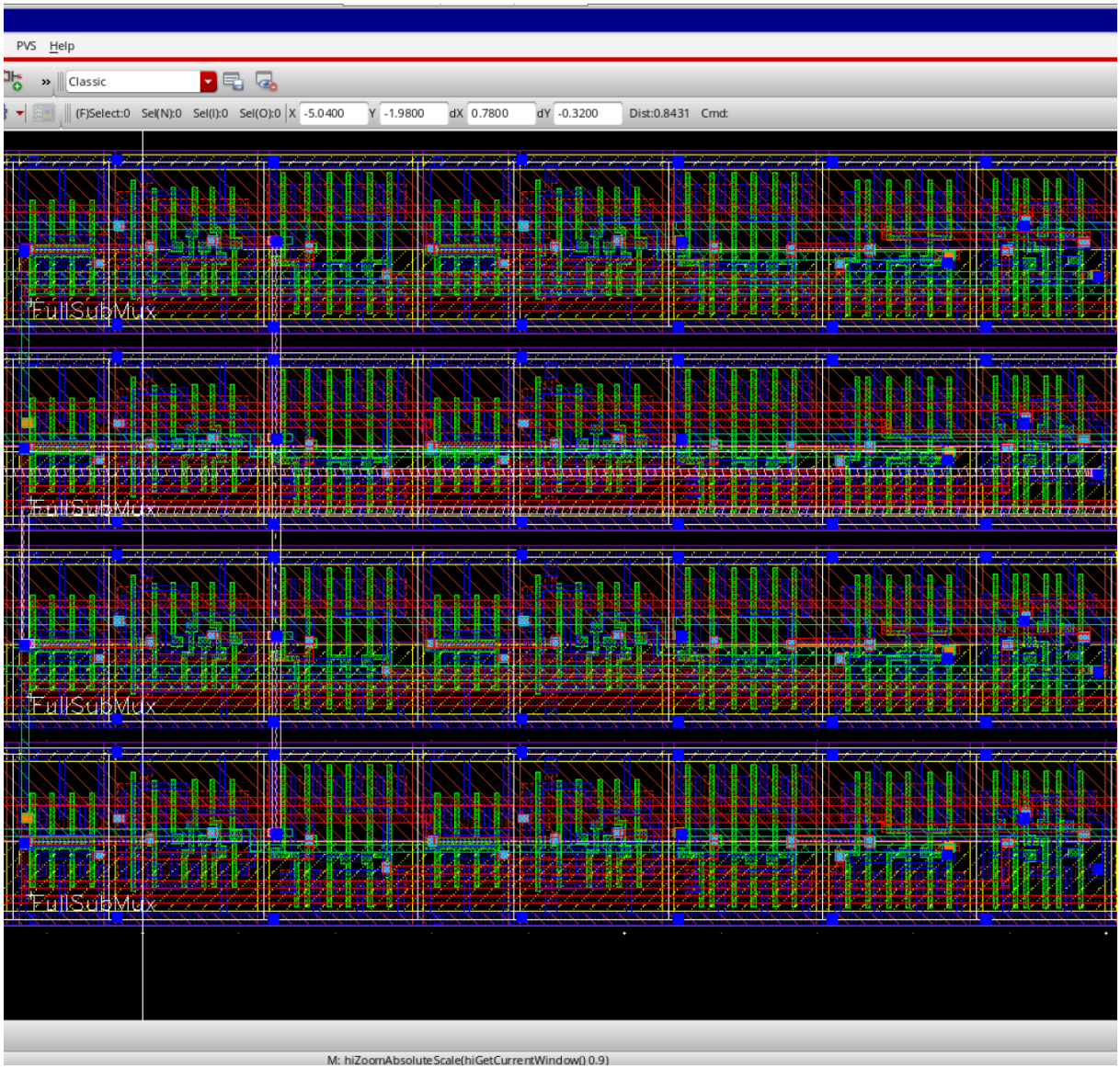


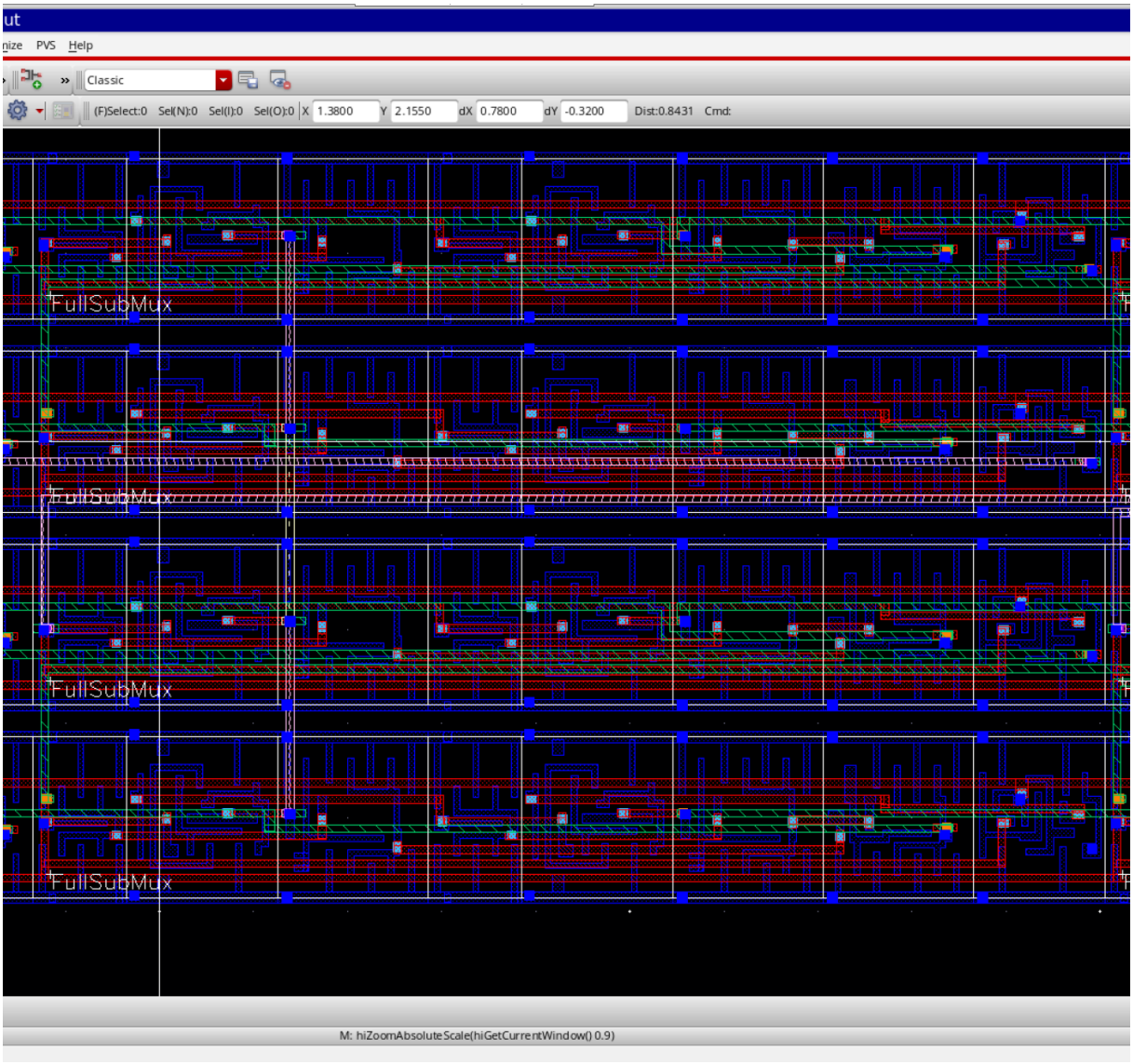
3.5 Divider

3.5.1 Layout

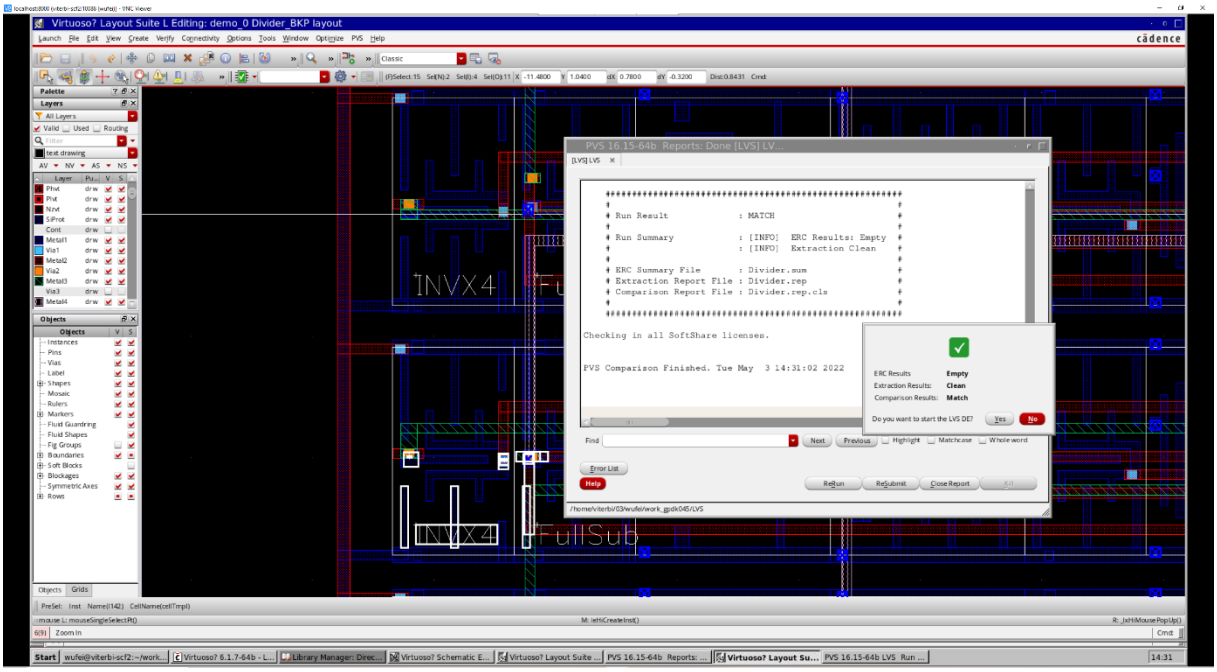



Virtuoso? Layout Suite L Editing: demo_0 Divider_BKP layout
cadence

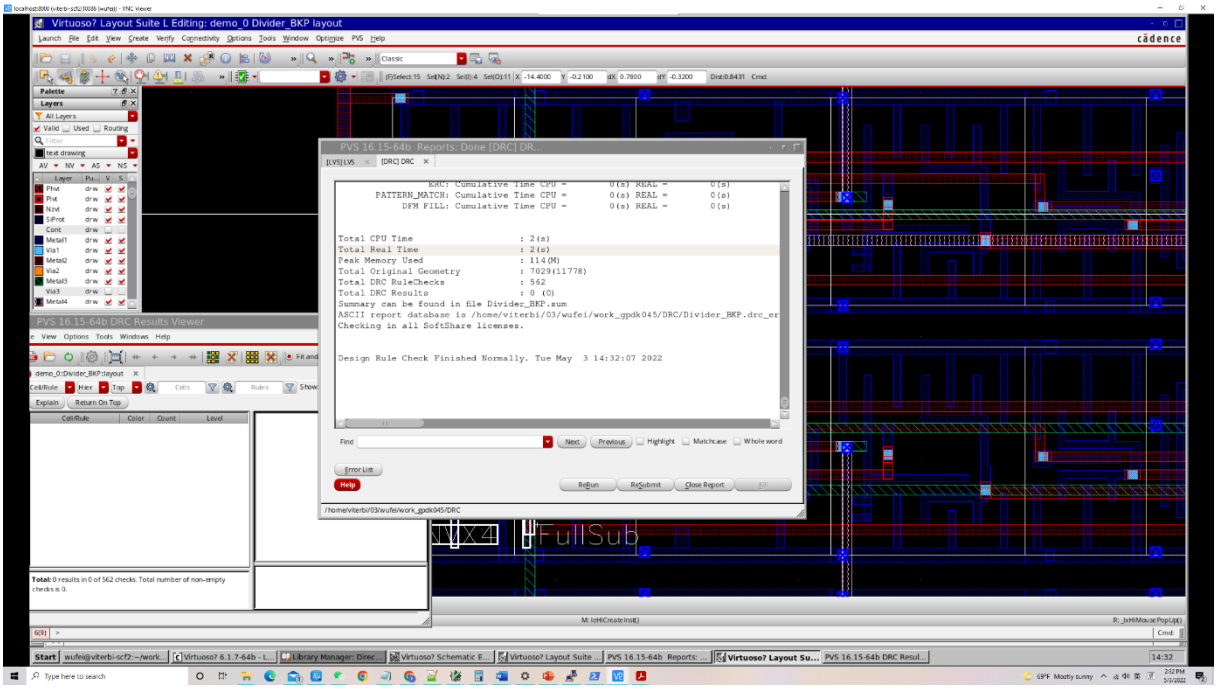

PVS Help
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X -5.0400 Y -1.9800 dX 0.7800 dY -0.3200 Dist:0.8431 Cmd:
FullSubMux
FullSubMux
FullSubMux
FullSubMux
M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)


ut
nize PVS Help
Classic
(F)Select:0 Sel(N):0 Sel(I):0 Sel(O):0 X 1.3800 Y 2.1550 dX 0.7800 dY -0.3200 Dist:0.8431 Cmd:
FullSubMux
FullSubMux
FullSubMux
FullSubMux
M: hiZoomAbsoluteScale(hiGetCurrentWindow() 0.9)

3.5.2 LVS



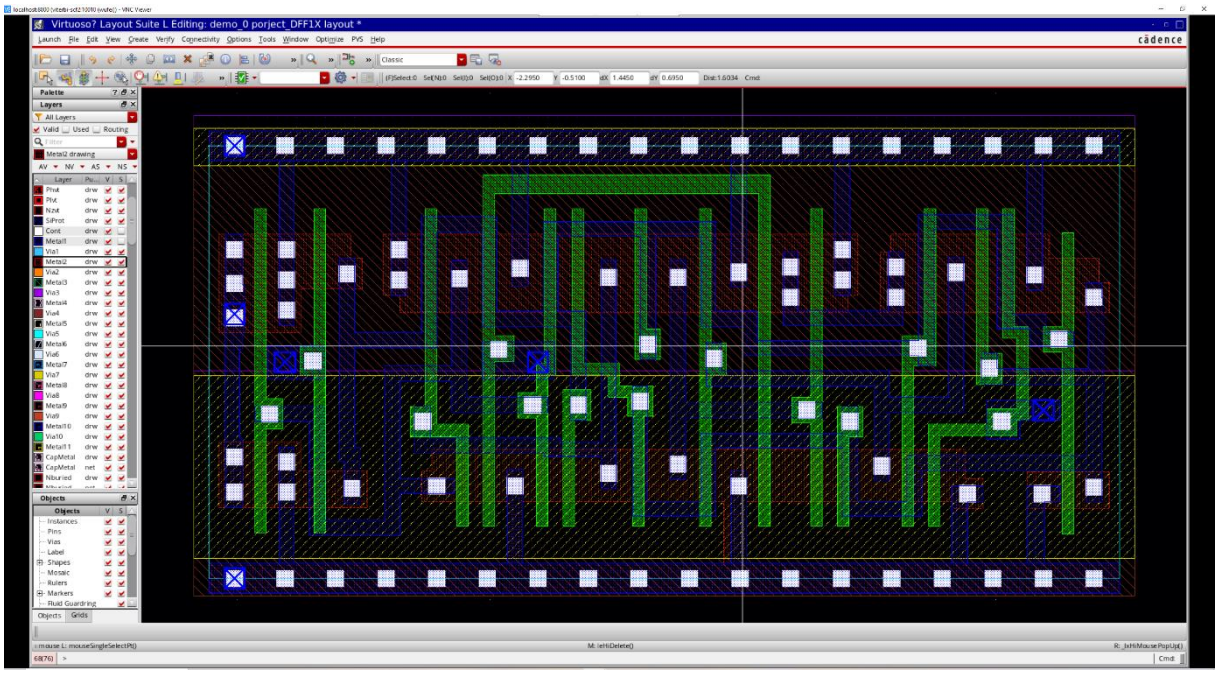
3.5.3 DRC



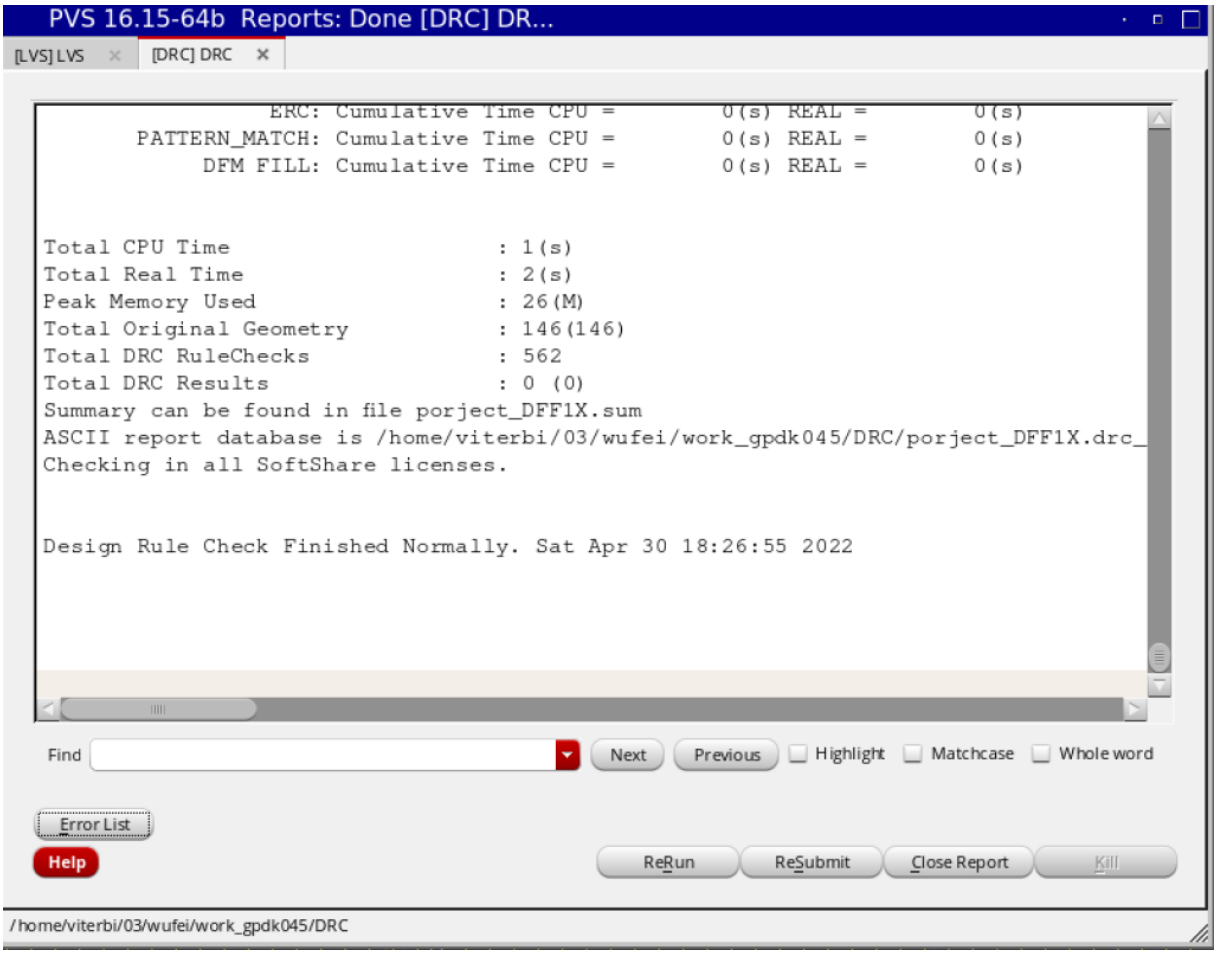
4 FSM

4.1 DFF

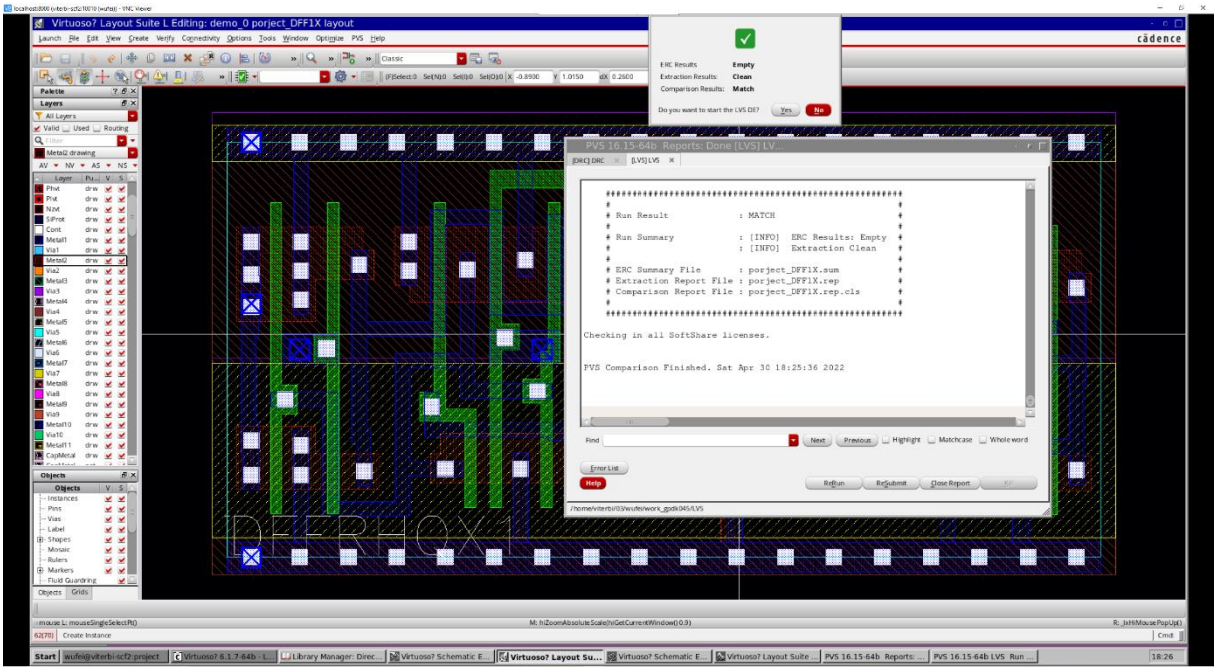
4.1.1 Layout



4.1.2 DRC



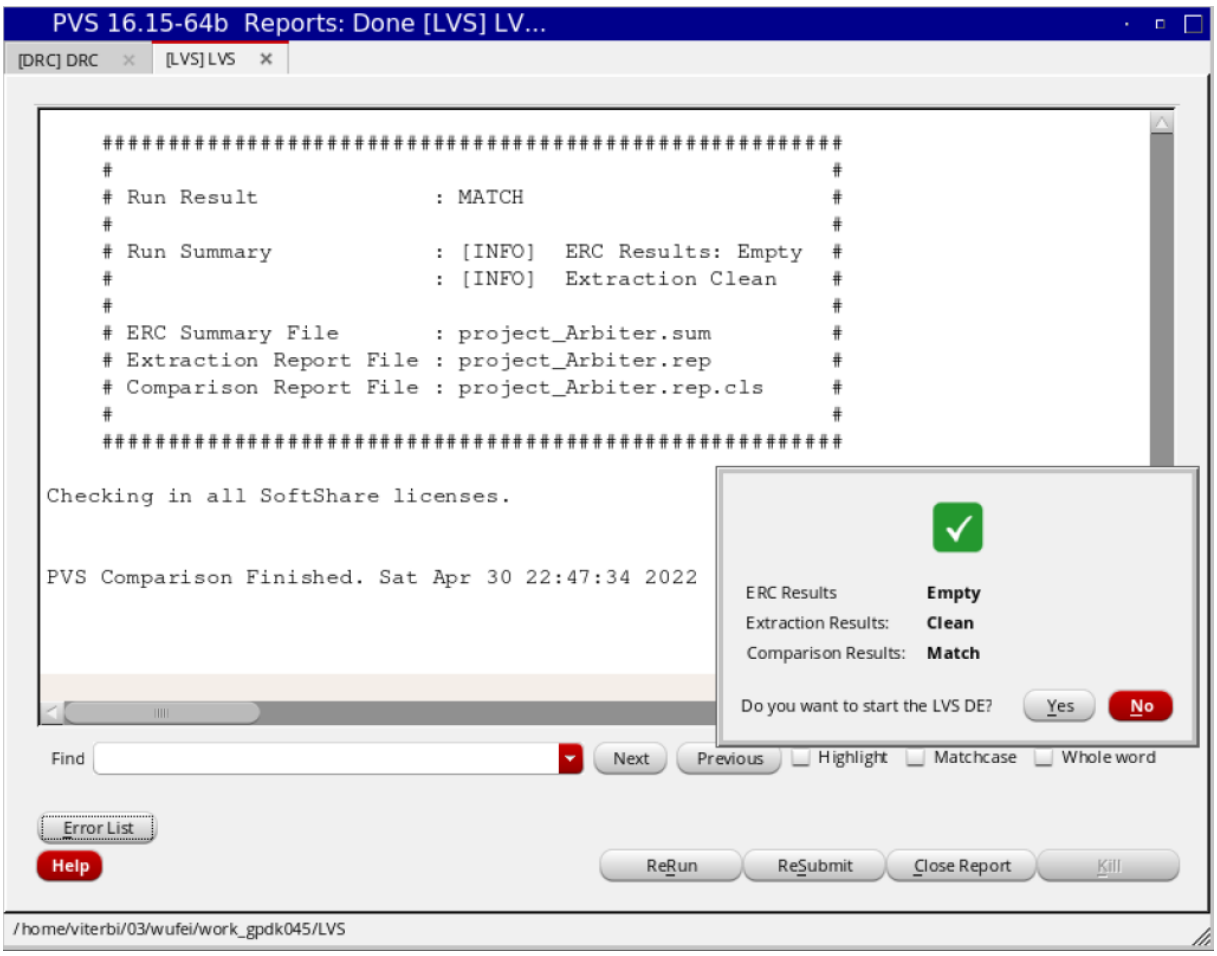
4.1.3 LVS



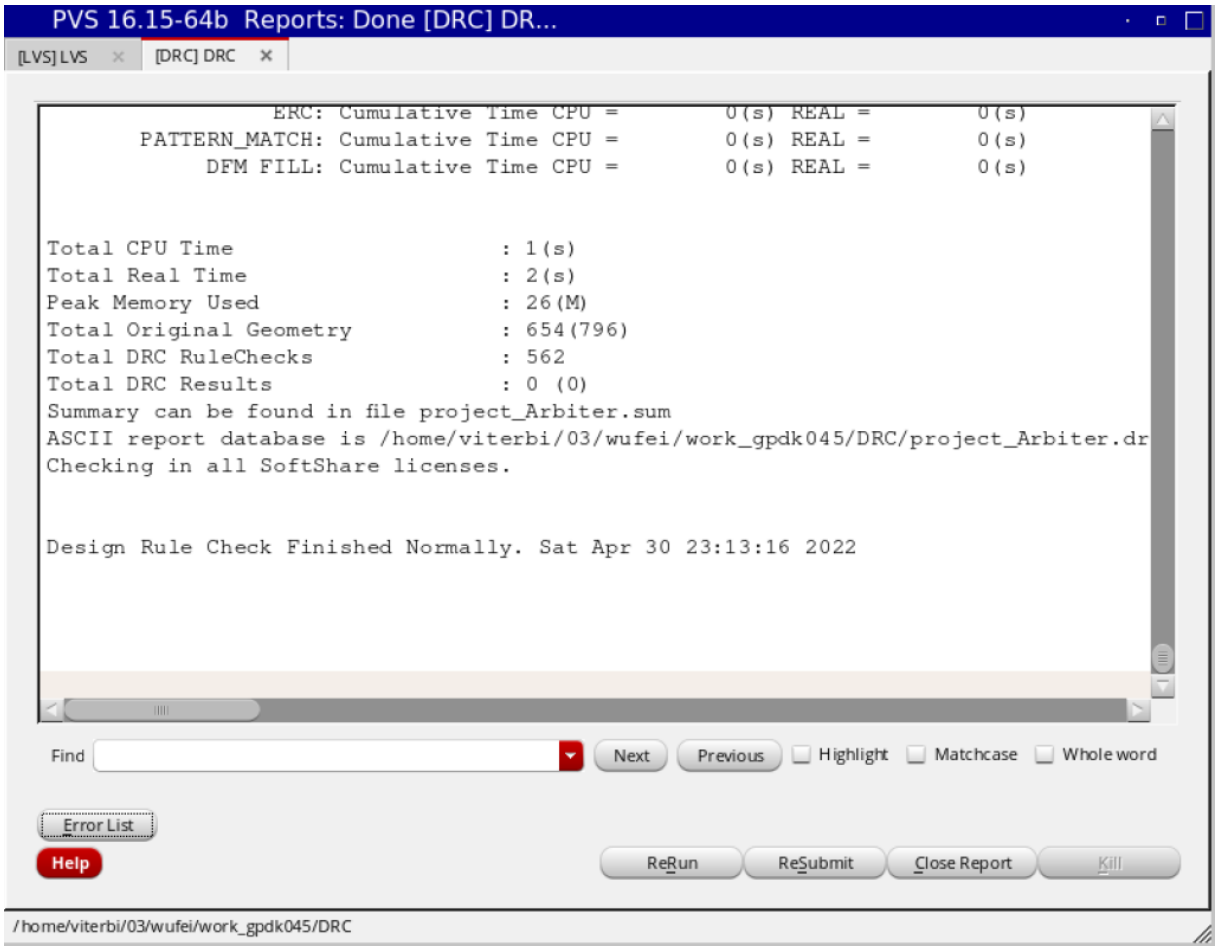
4.2 Arbiter

4.2.1 Layout

4.2.2 LVS



4.2.3 DRC



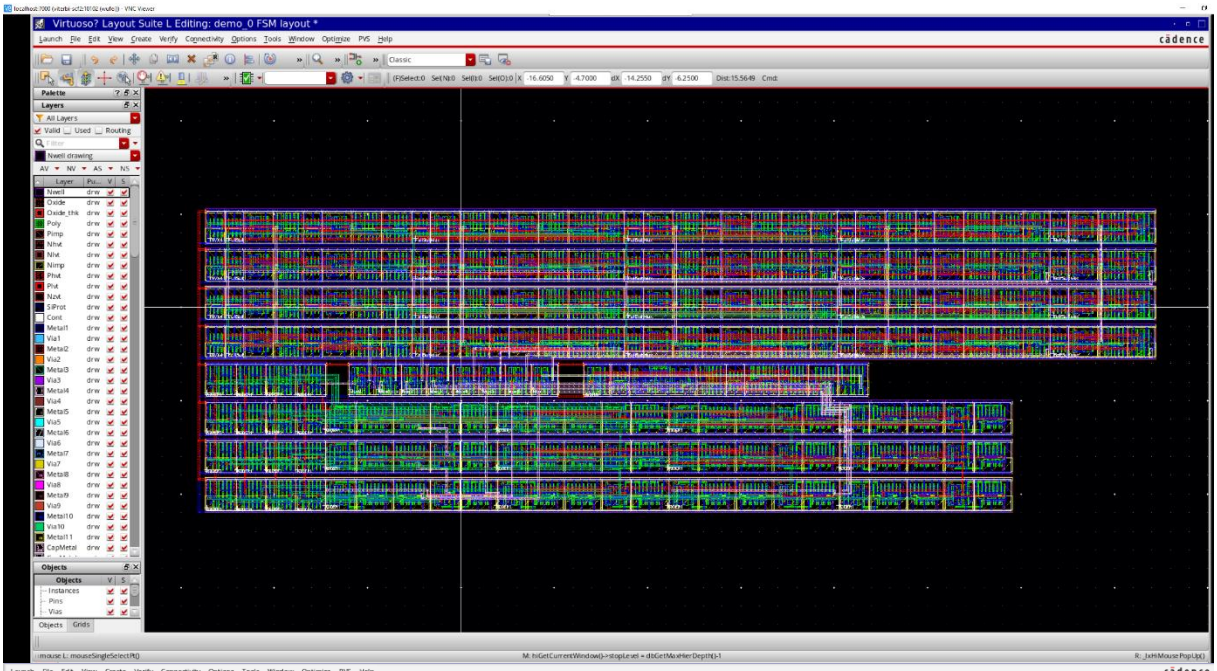
4.3 FSM

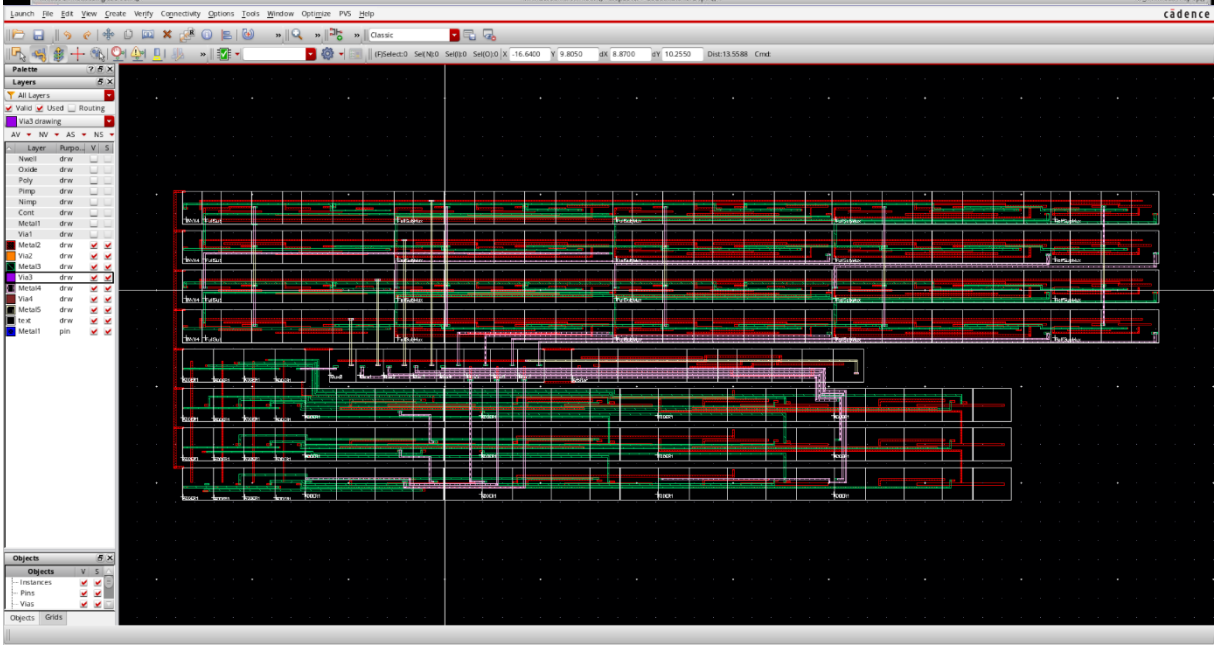
4.3.1 Layout

3layer:

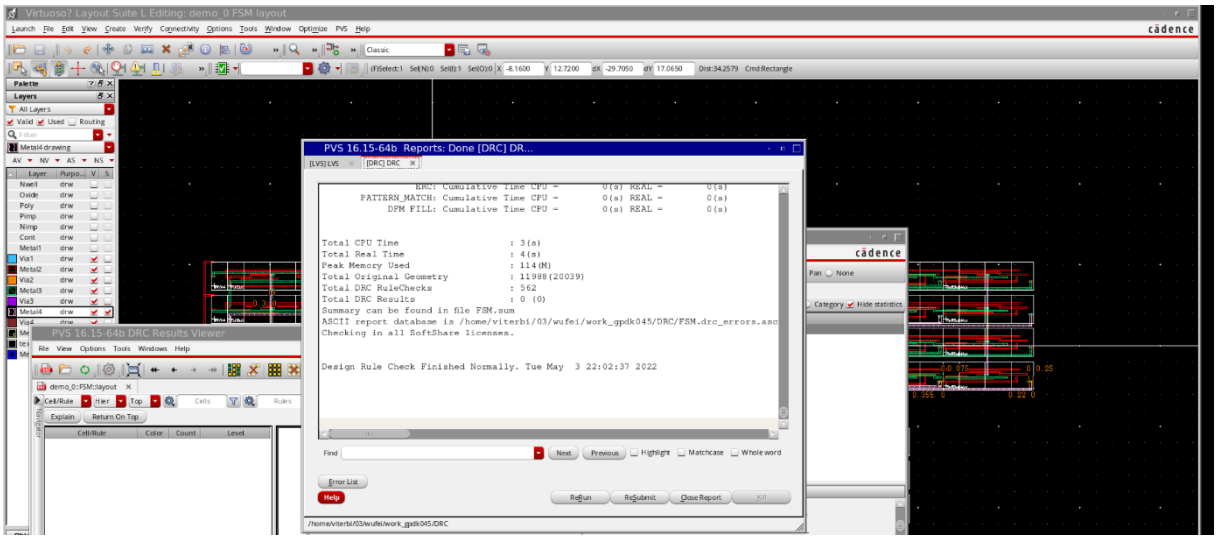
1. Divider
2. Arbiter and Mux set
3. Multiplexer

I have showed all the detail above, the following image just the overview of the FSM and the interconnection of the components.

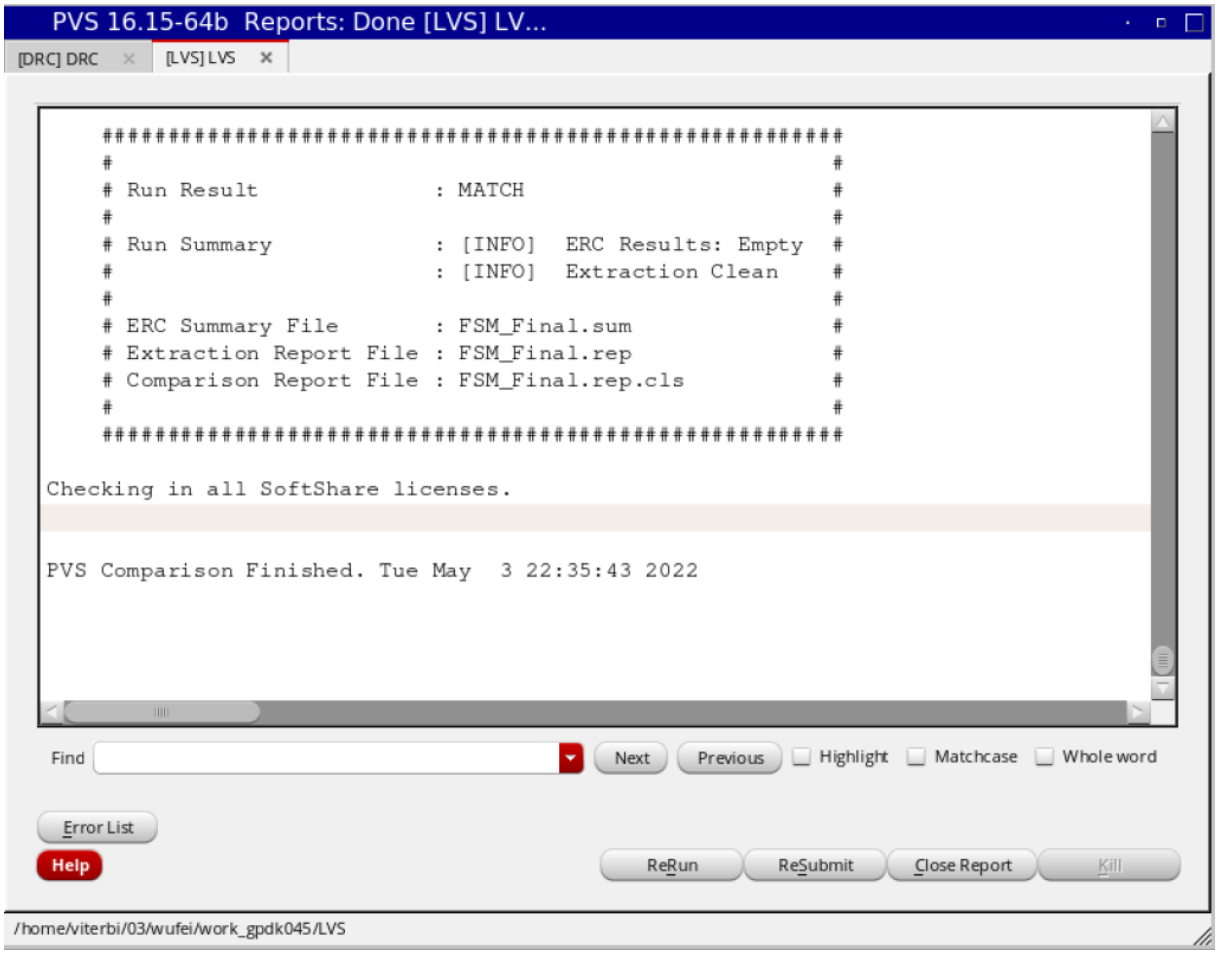

Virtuoso? Layout Suite L Editing: demo_0 FSM layout *
Launch File Edit View Create Verify Connectivity Options Tools Window Optimize PVS Help
cadence
Palette
Layers
All Layers
Nwell drawing
Objects
Instances
Pins
Vias
Objects Grids


Launch File Edit View Create Verify Connectivity Options Tools Window Optimize PVS Help
cadence
Palette
Layers
All Layers
Via3 drawing
Objects
Instances
Pins
Vias
Objects Grids

4.3.2 DRC



4.3.3 LVS



5 Test Conclusion

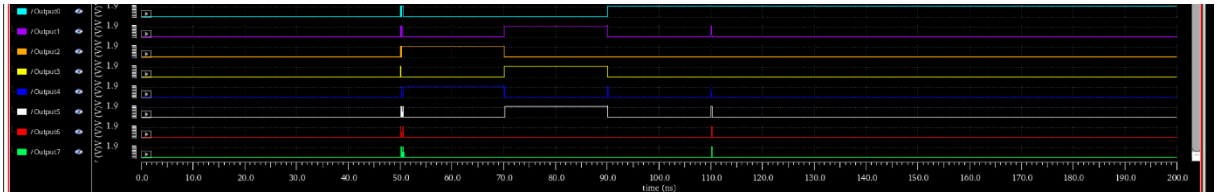
Minimum time period: 0.234ns

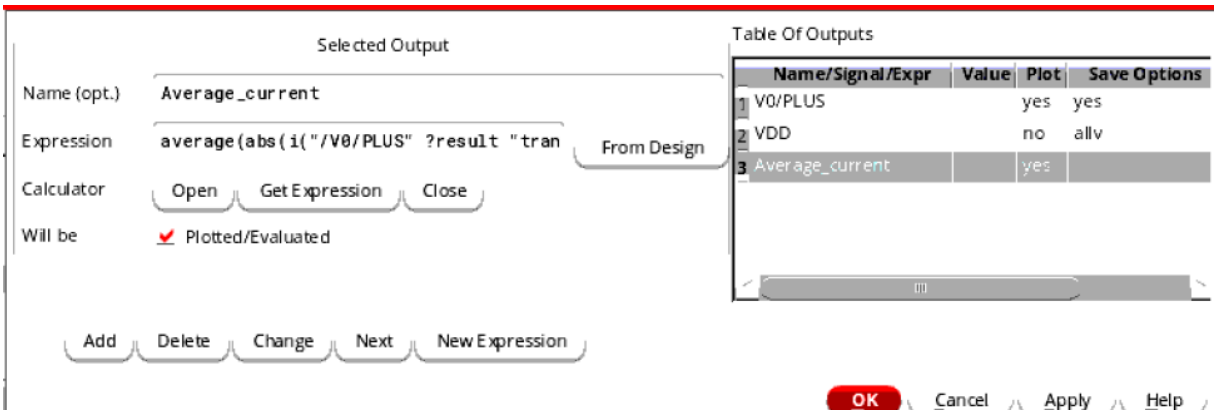
```
ON   VSS /gnd! Voltage dc "DC voltage"=0
ON   VDD /gnd! Voltage dc "DC voltage"=1.8
OFF  B0 /gnd! Voltage bit
OFF  B1 /gnd! Voltage bit
OFF  B2 /gnd! Voltage bit
OFF  B3 /gnd! Voltage bit
OFF  A0 /gnd! Voltage bit
OFF  A1 /gnd! Voltage bit
OFF  A2 /gnd! Voltage bit
OFF  A3 /gnd! Voltage bit
OFF  D1 /gnd! Voltage bit
OFF  di3 /gnd! Voltage bit
OFF  di2 /gnd! Voltage bit
OFF  di1 /gnd! Voltage bit
OFF  di0 /gnd! Voltage bit
OFF  D0 /gnd! Voltage bit
OFF  D3 /gnd! Voltage bit
```

Open FSM.vec ~/work_gpdk045/input/project Save

```
radix 1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1
vname CLK  RST  M    D    A3   A2   A1   A0   B3   B2   B1   B0   D3   D2   D1   D0   di3  di2  di1  di0
io    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i

tunit 10ns
vih 1.8
vil 0
voh 1.8
vol 0
trise 10p
tfall 10p

tdelay 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

;mul

0  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1  1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
2  0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
3  1 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
4  0 1 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

5  1 1 1 1 0 1 0 0 1 0 0 1 1 1 0 1 0 0 1 1
6  0 1 1 1 0 1 0 0 1 0 0 1 1 1 0 1 0 0 1 1

7  1 1 1 1 0 1 1 0 0 1 1 1 0 1 0 1 1 0 1 1
8  0 1 1 1 0 1 1 0 0 1 1 1 0 1 0 1 1 0 1 1

9  1 1 0 1 0 0 0 1 0 0 0 1 0 1 1 1 0 0 1 0
10 0 1 0 1 0 0 0 1 0 0 0 1 0 1 1 1 0 0 1 0

11 1 1 1 0 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 1
12 0 1 1 0 0 0 0 1 0 1 1 0 0 0 0 1 0 0 0 1
```

Plain Text Tab Width: 8 Ln 30, Col 11 INS





Power = 13.1881uA * 1.8V = 23.73858 uW