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| Document ref |  | | |
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| Author | Wu Fei | | |
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**Spring 2022**

**EE 477**

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| Date | Version | List of changes | Author + Signature |
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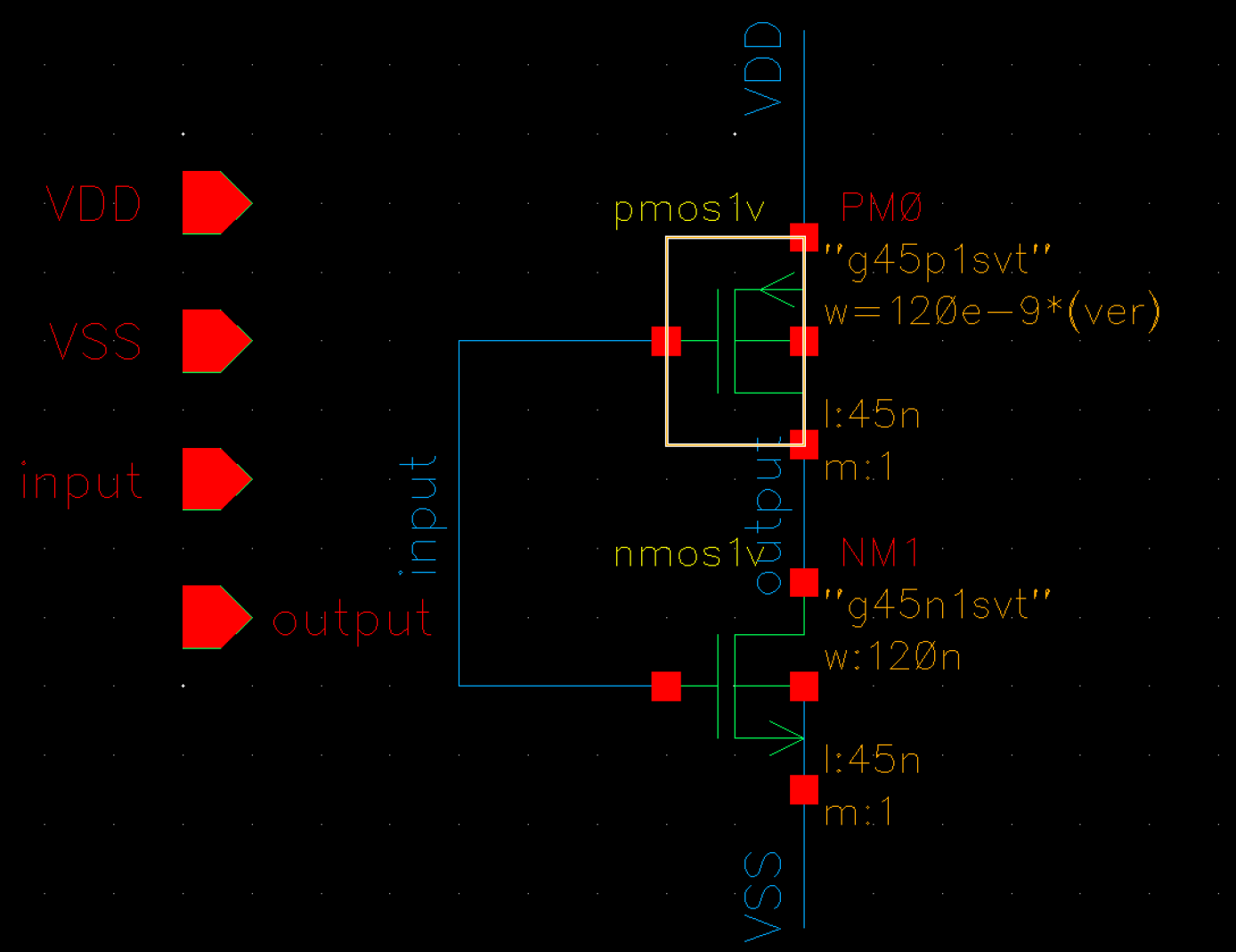
# Action items

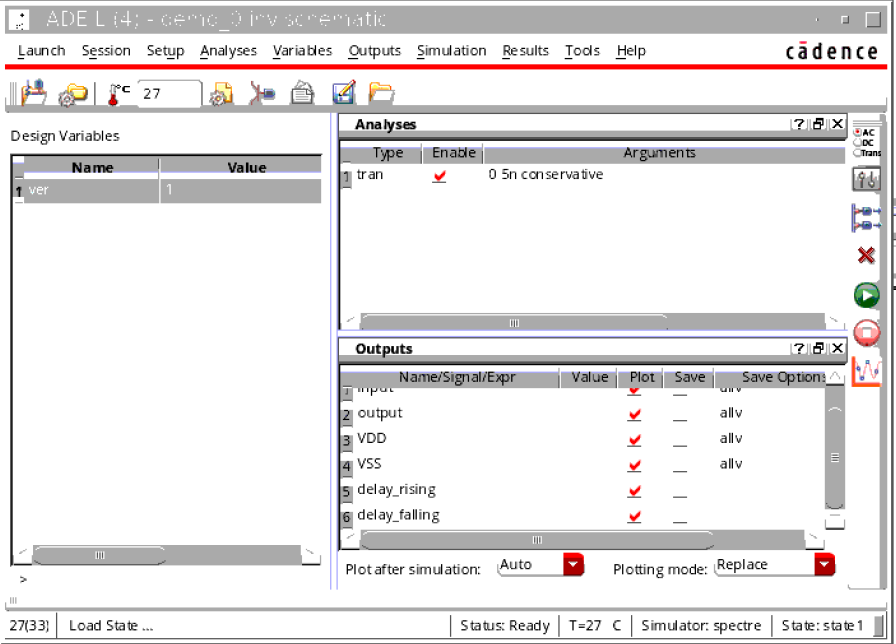
## Step1

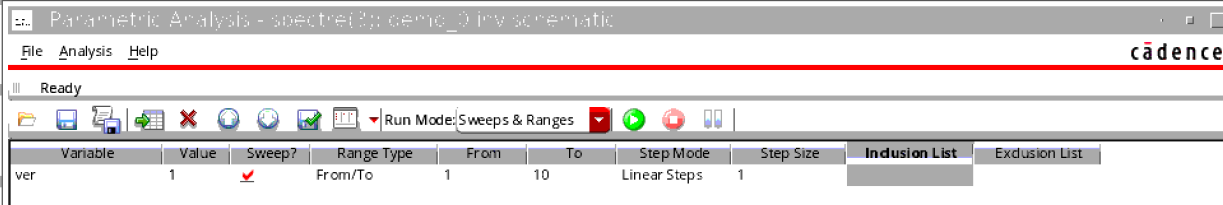
Measurement of k-ratio: Draw the schematic of an inverter in Cadence using minimum width (120nm) for the NMOS. Experiment with the PMOS width until the propagation delays are within 10% of each other, i.e.

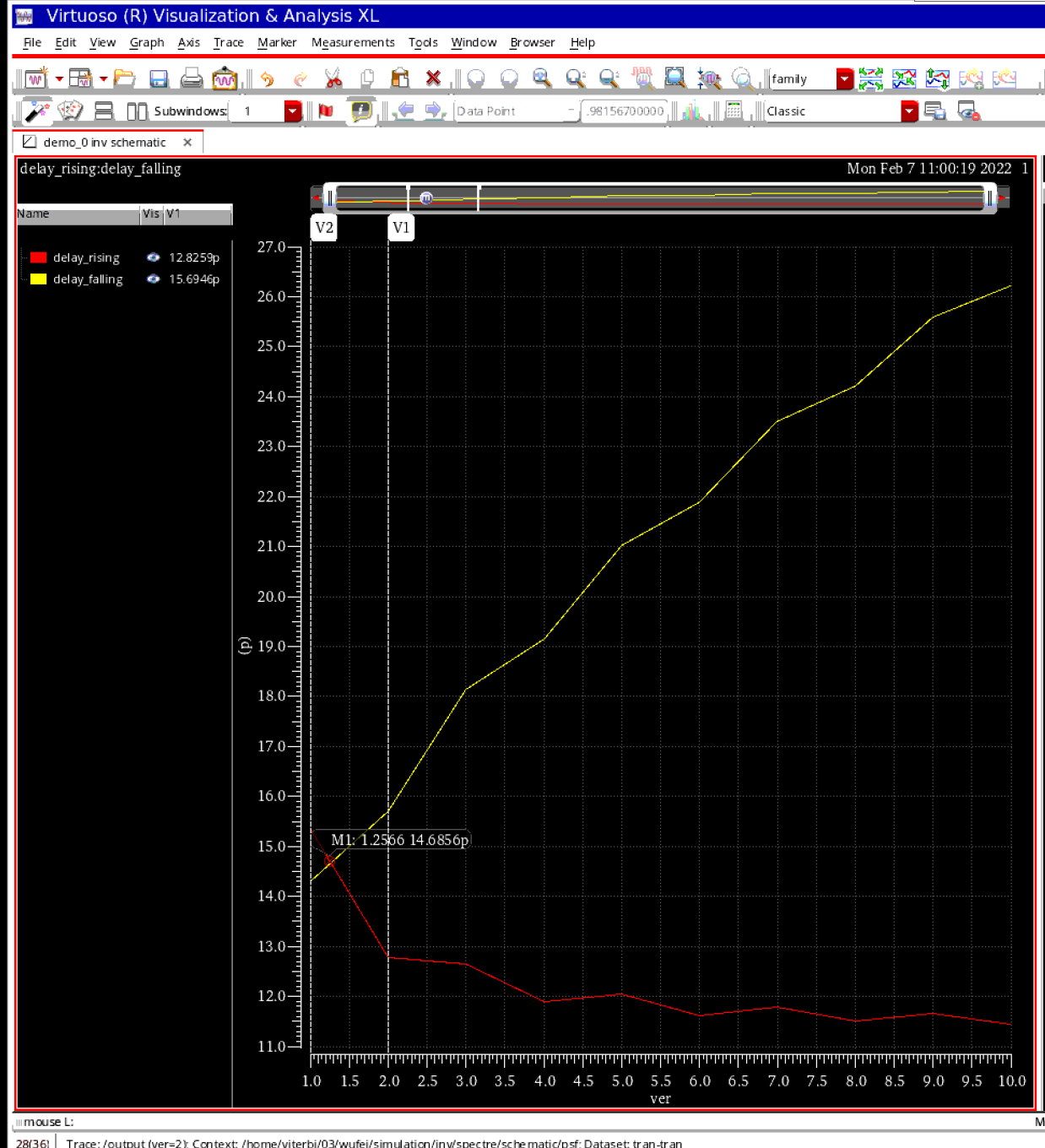
 | Tphl − Tplh |  / min (Tphl, Tplh) < 0.1

Then calculate k = WPMOS/WNMOS

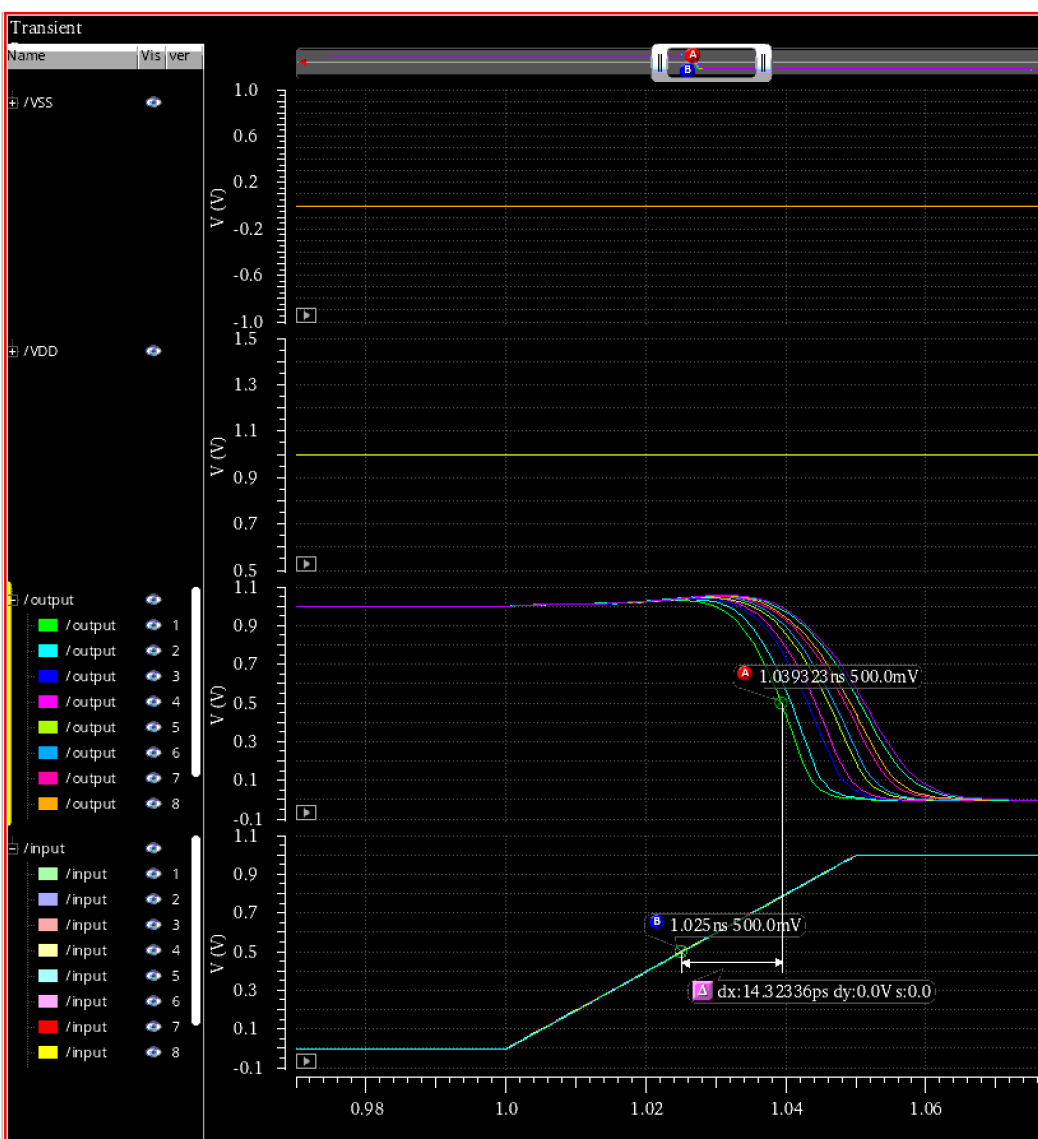


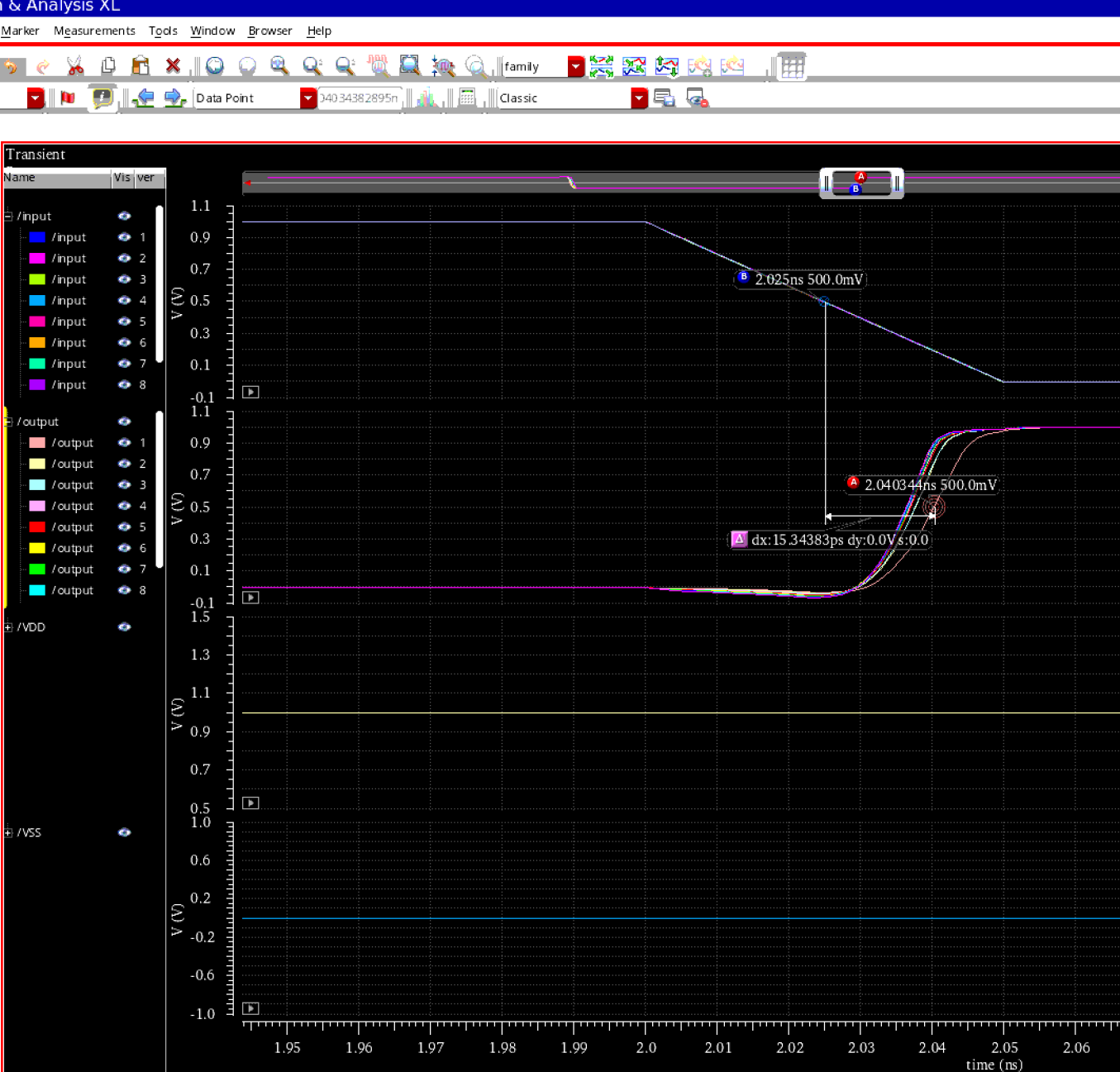






Showing as the delay in different ver value, it is clear that the best choice is the ver is equal to 1.

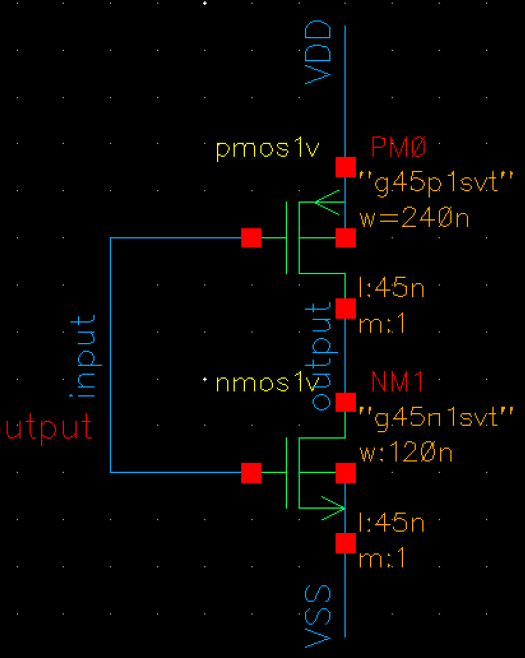




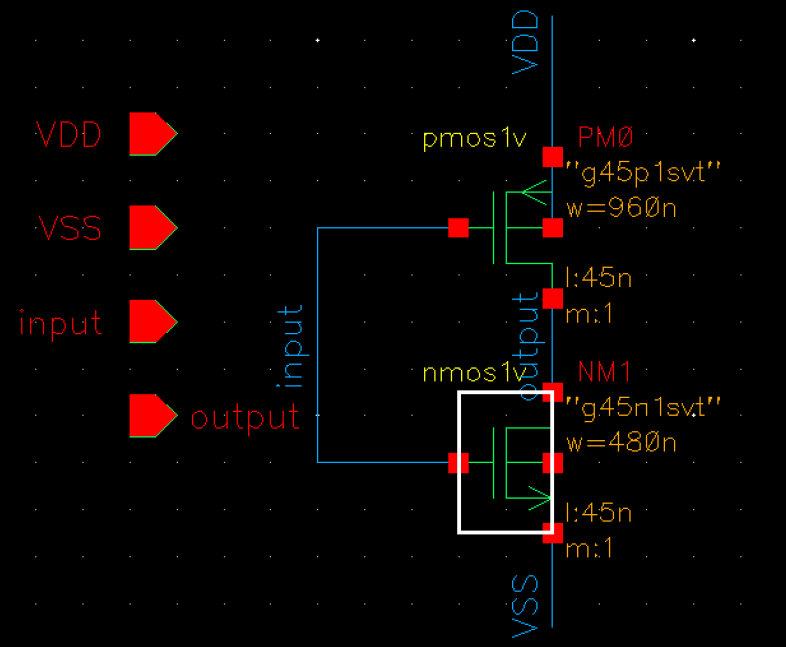
# Step2/step3

Schematic design and delay measurement of gates: Whatever you calculated in Step 1, use k=2 from here on to maintain consistency.

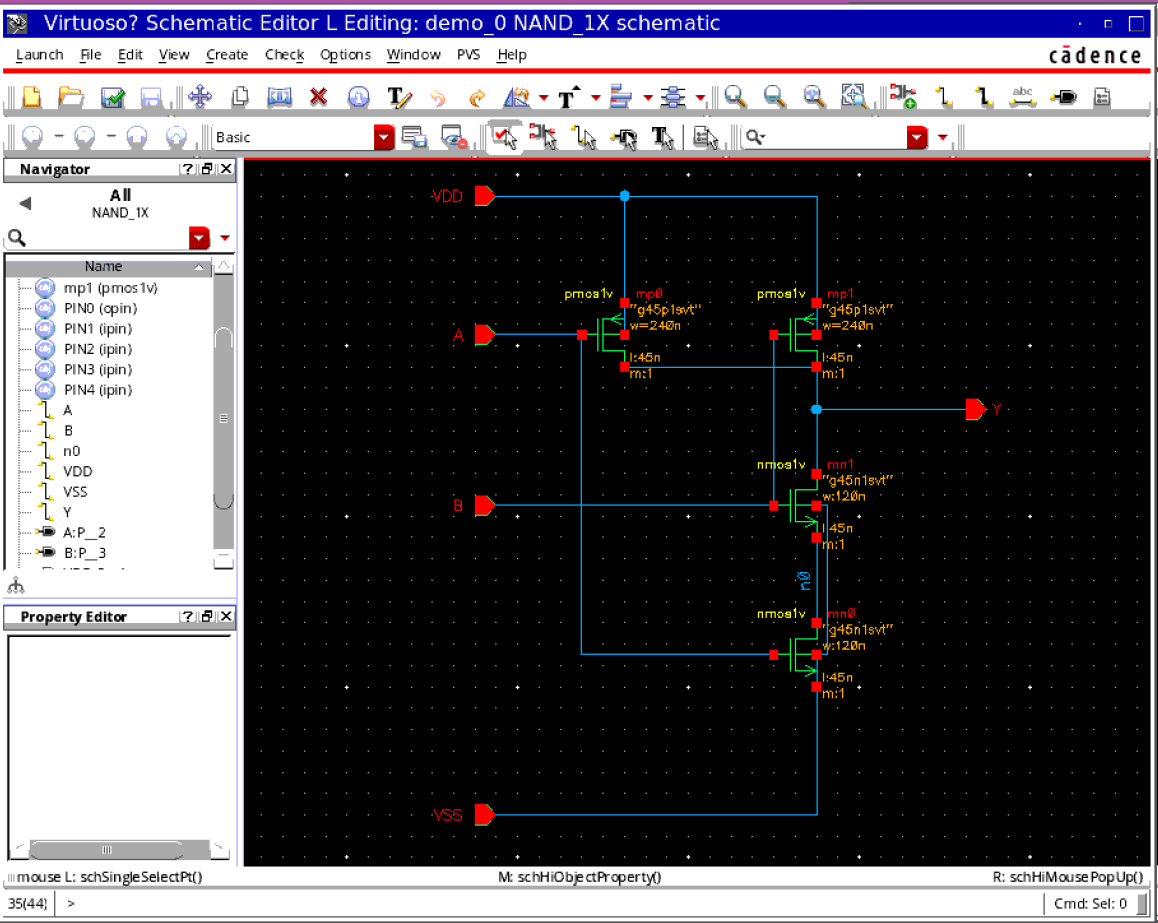
* Design an inverter schematic with WNMOS = 120nm and WPMOS = 240nm. This is INV\_1X.

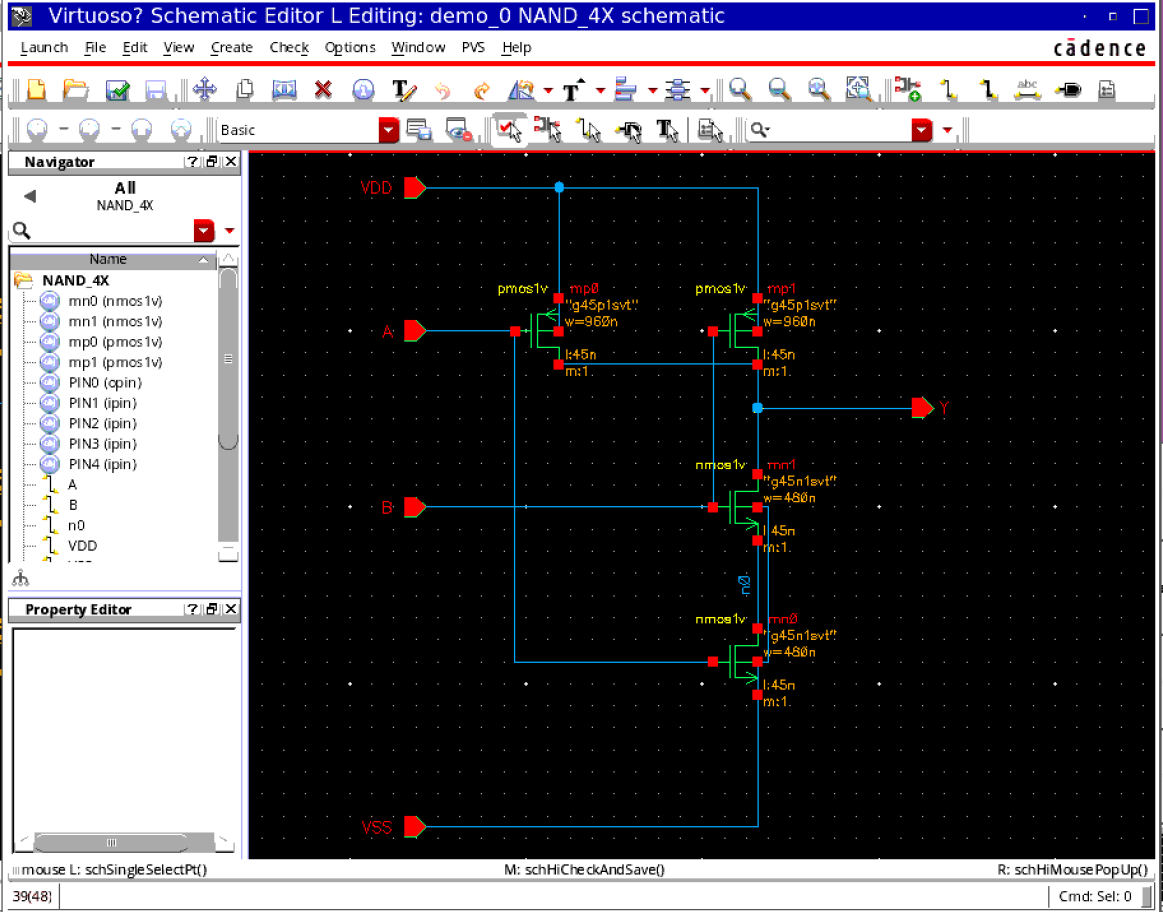


* Design another inverter with both NMOS and PMOS 4 times as big as INV\_1X. This is INV\_4X.



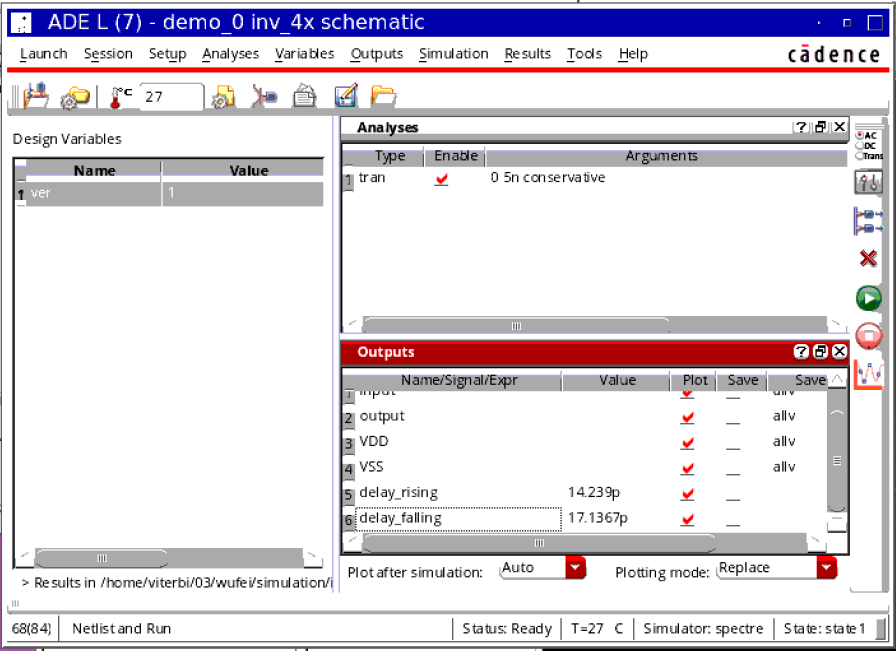
* Design NAND2\_1X, NAND2\_4X, NOR2\_1X and NOR2\_4X.





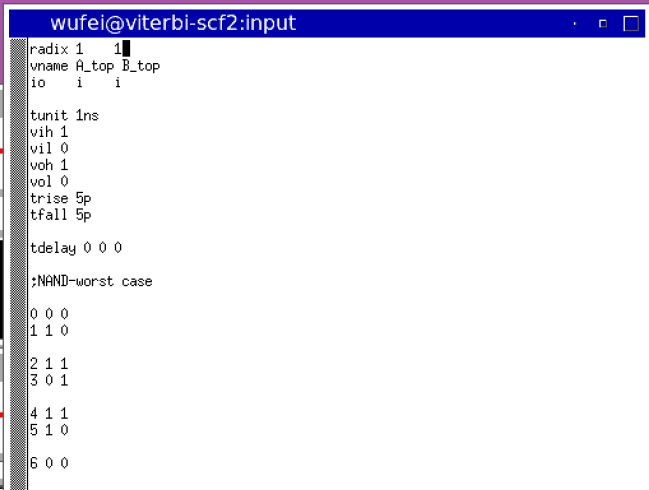
In each case, size the transistors so that the worst case propagation delays are equal to the corresponding inverter (e.g. τPLH and τPHL for NOR2\_4X should be equal to those of INV\_4X). Remember to check different cases to find the worst case delay.

Detecting the delay of inv\_4x show like following:

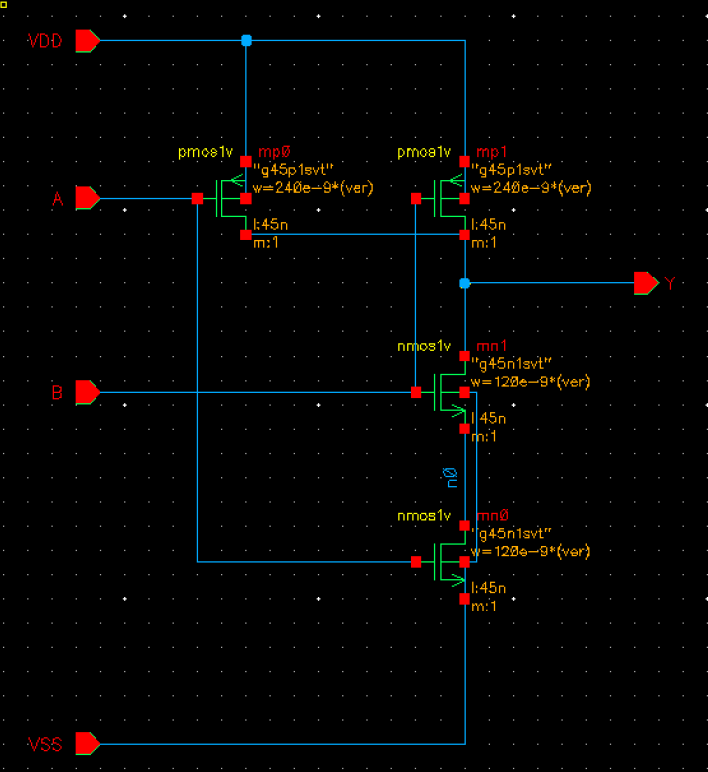


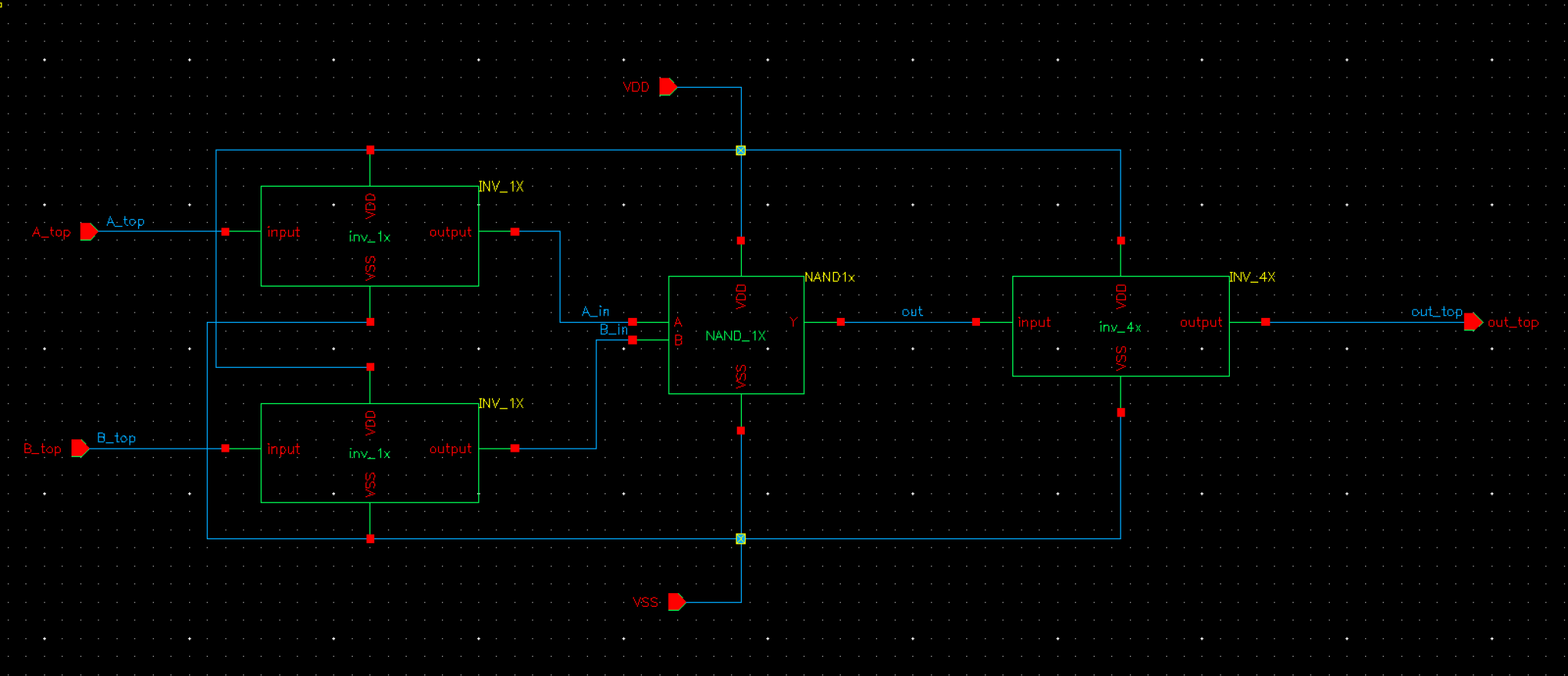
Theoretically, in the worst situation, there is only one PMOS to drive the output and one NMOS to drive the output, so we set the size of the MOS 2 times to the INV4x to get the close delay time required:

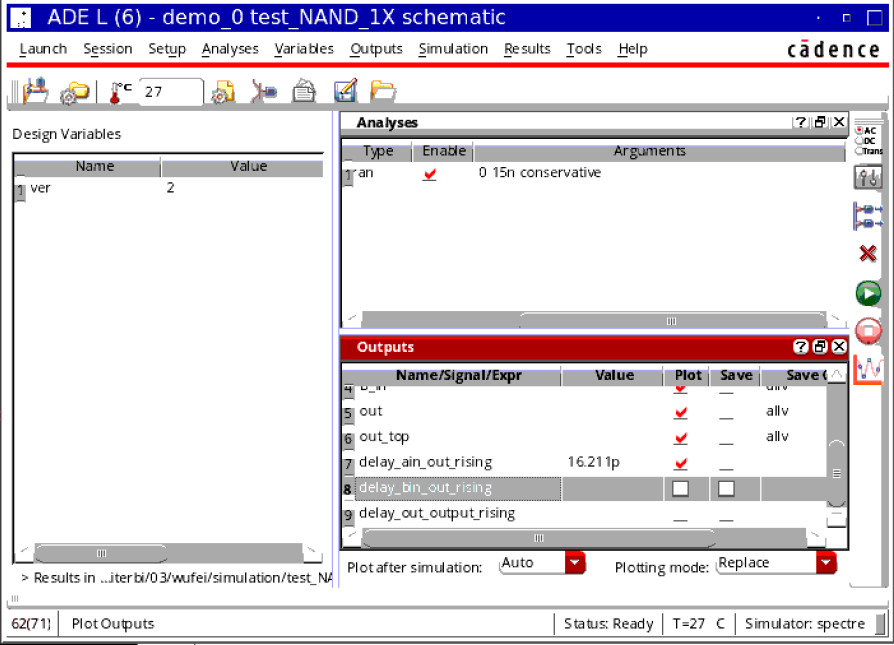
For NAND the worst situation should be ab00->ab01/ab10

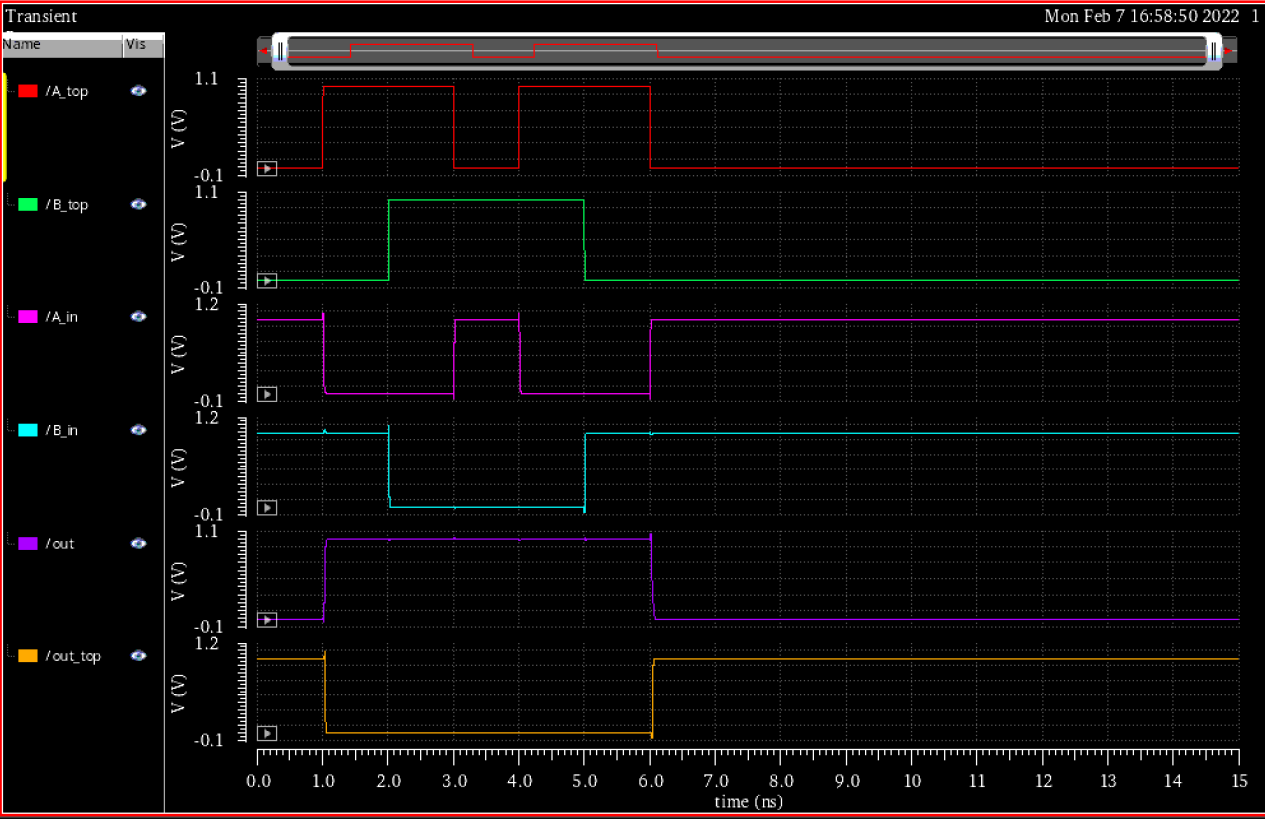


NAND1x:

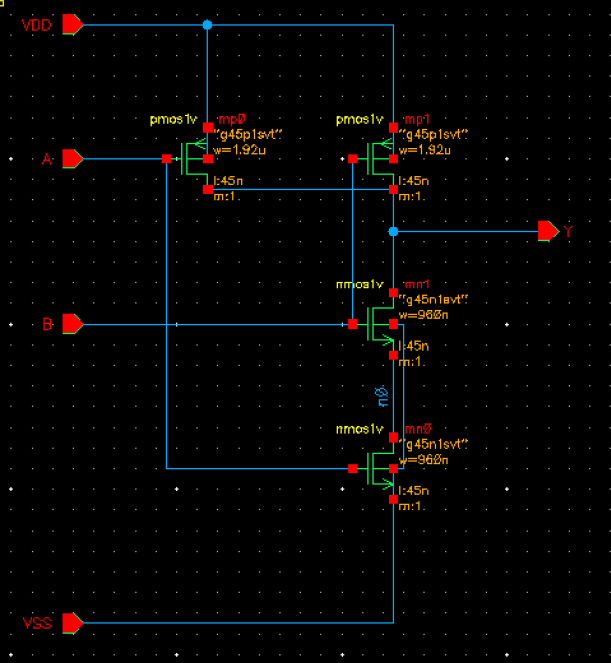


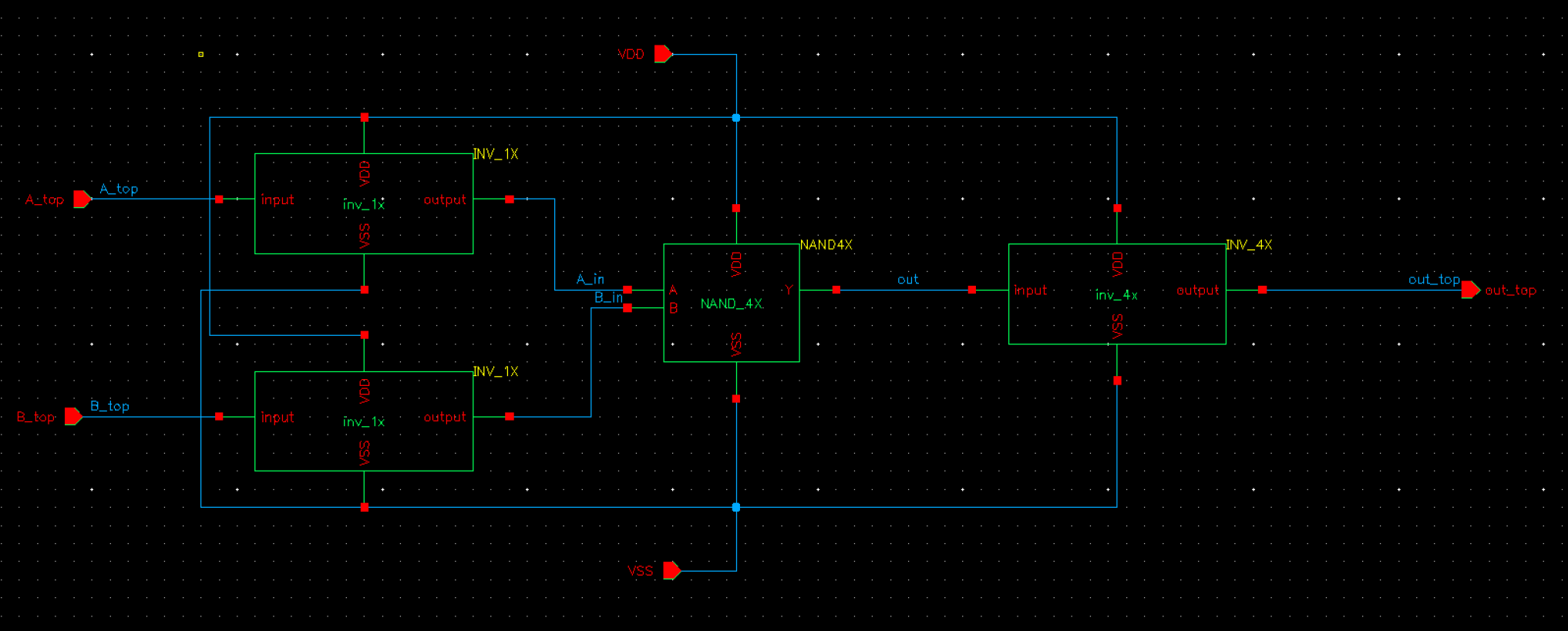






NAND4x:

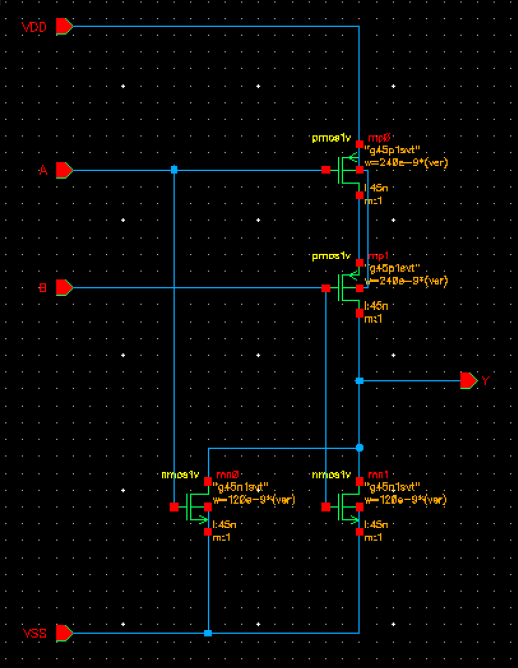


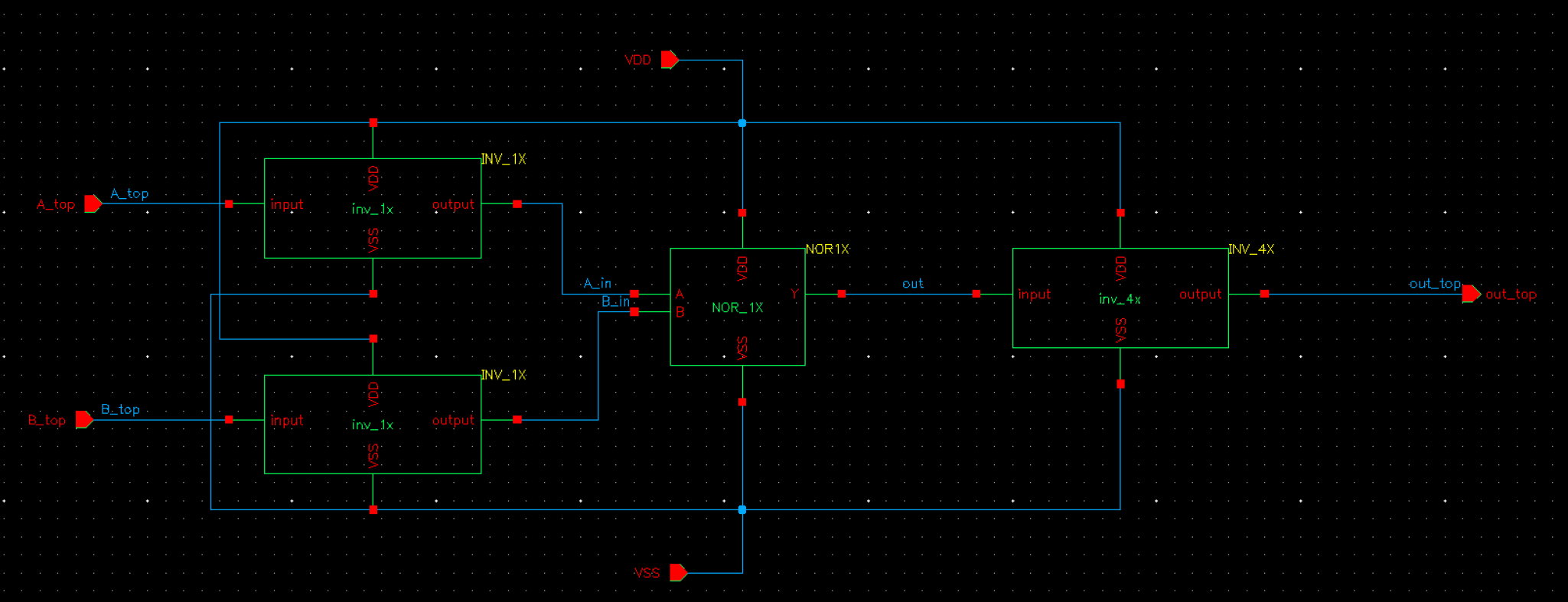


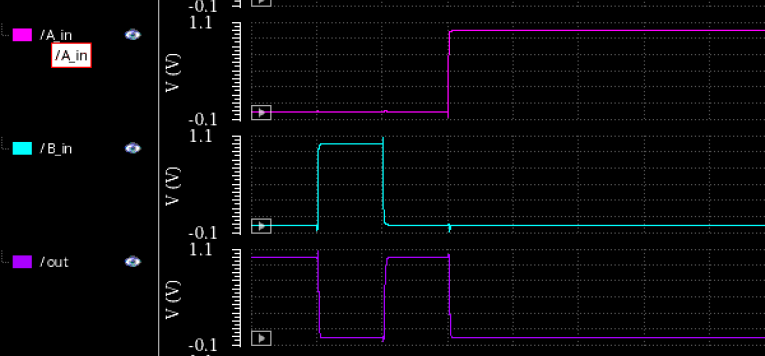


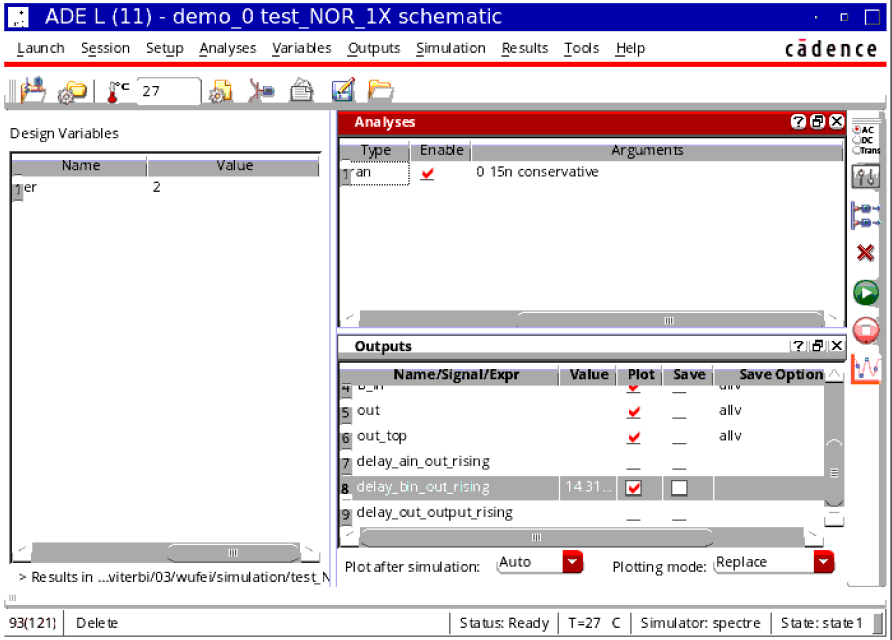
NOR1x



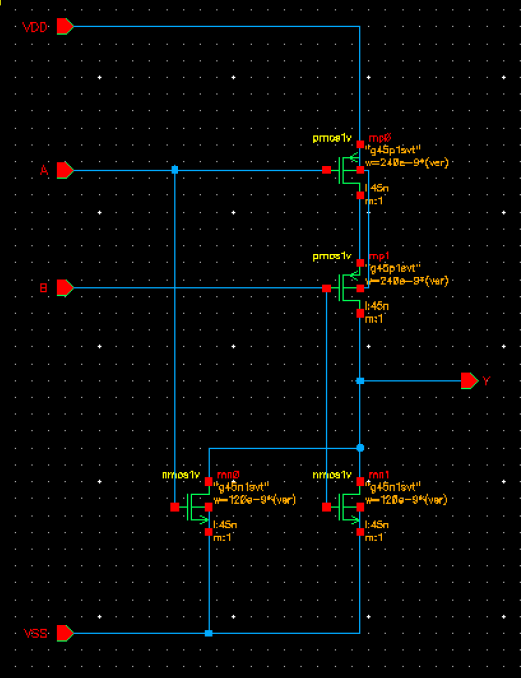


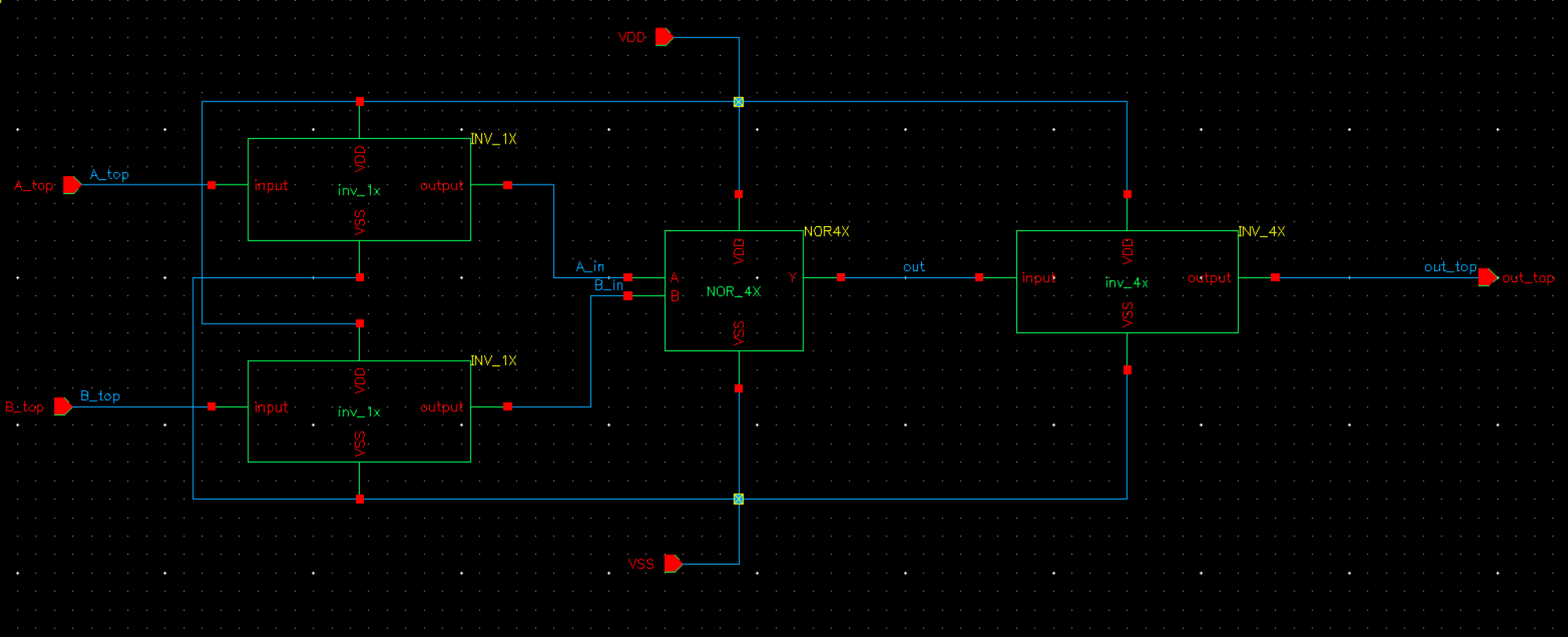


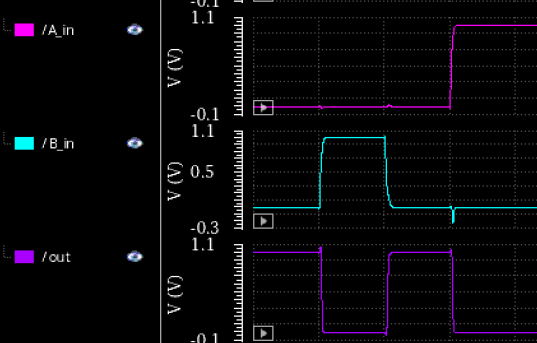


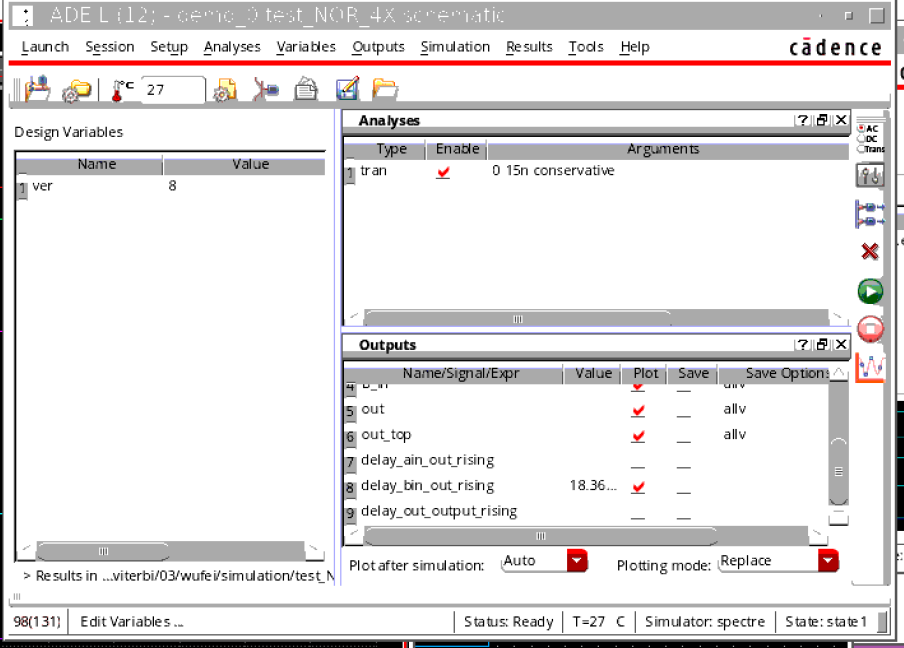


NOR4x







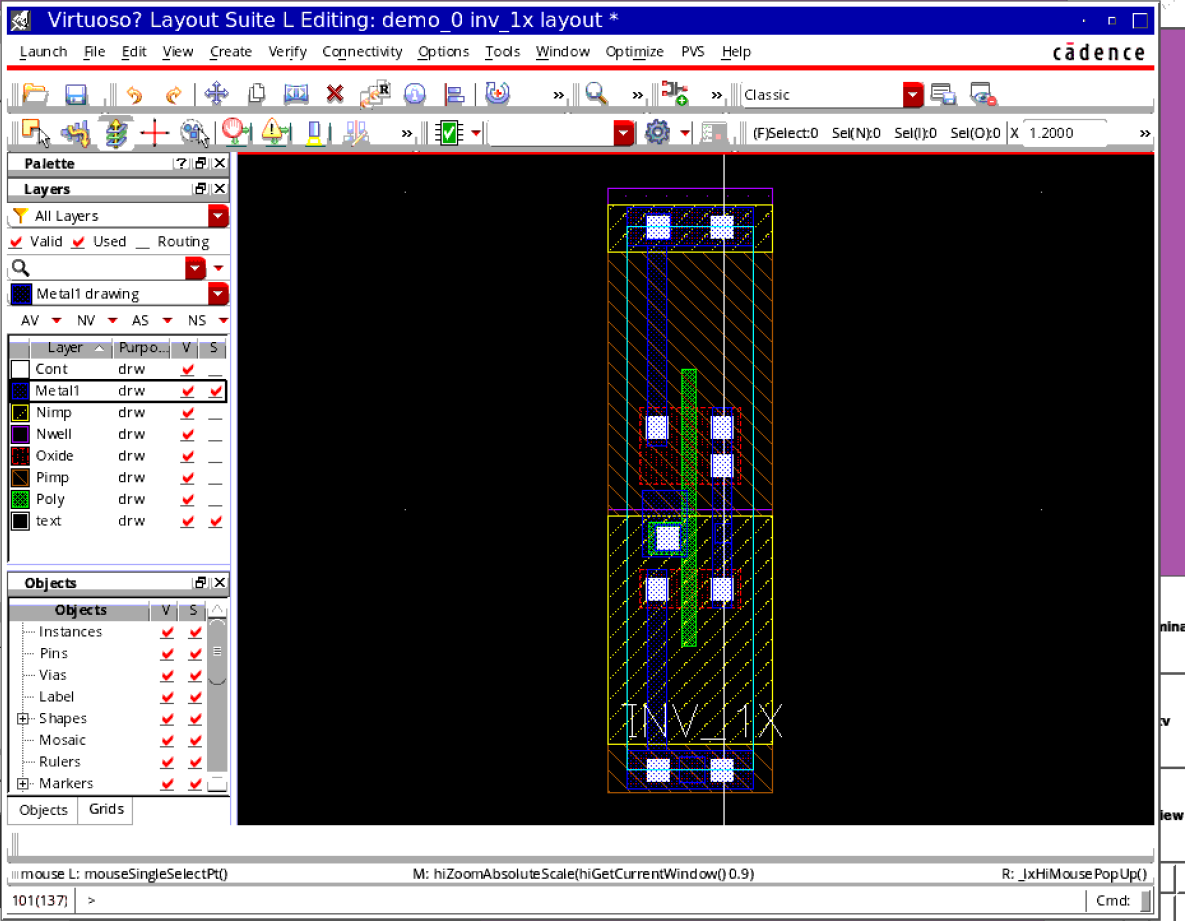


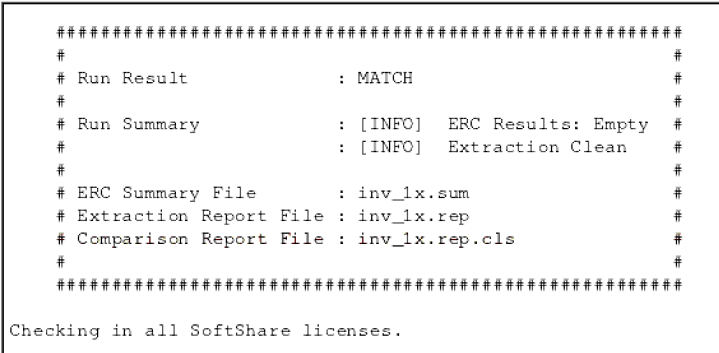
# Step4/Step3

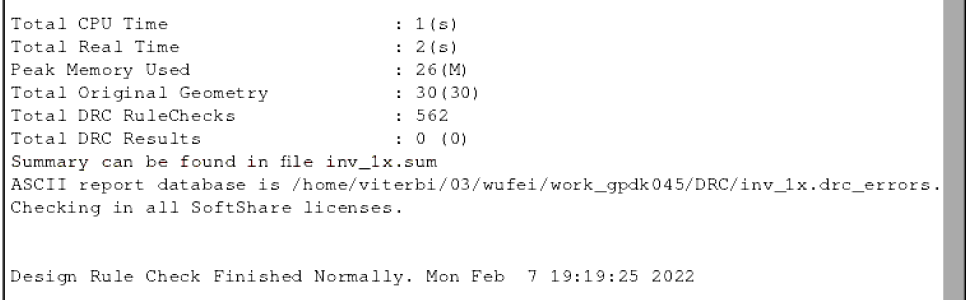
Layout design:

* Draw layouts for all the 6 gates and their delay measurement testbenches (i.e. INV\_1X connected to inputs and INV\_4X to outputs).
* Perform DRC and LVS checks with the respective schematics.
* Find the rising and falling propagation delays. You’ll find they are different from the schematic. Think about the reason.
* Repeat Step 3 functional verification for the layouts.

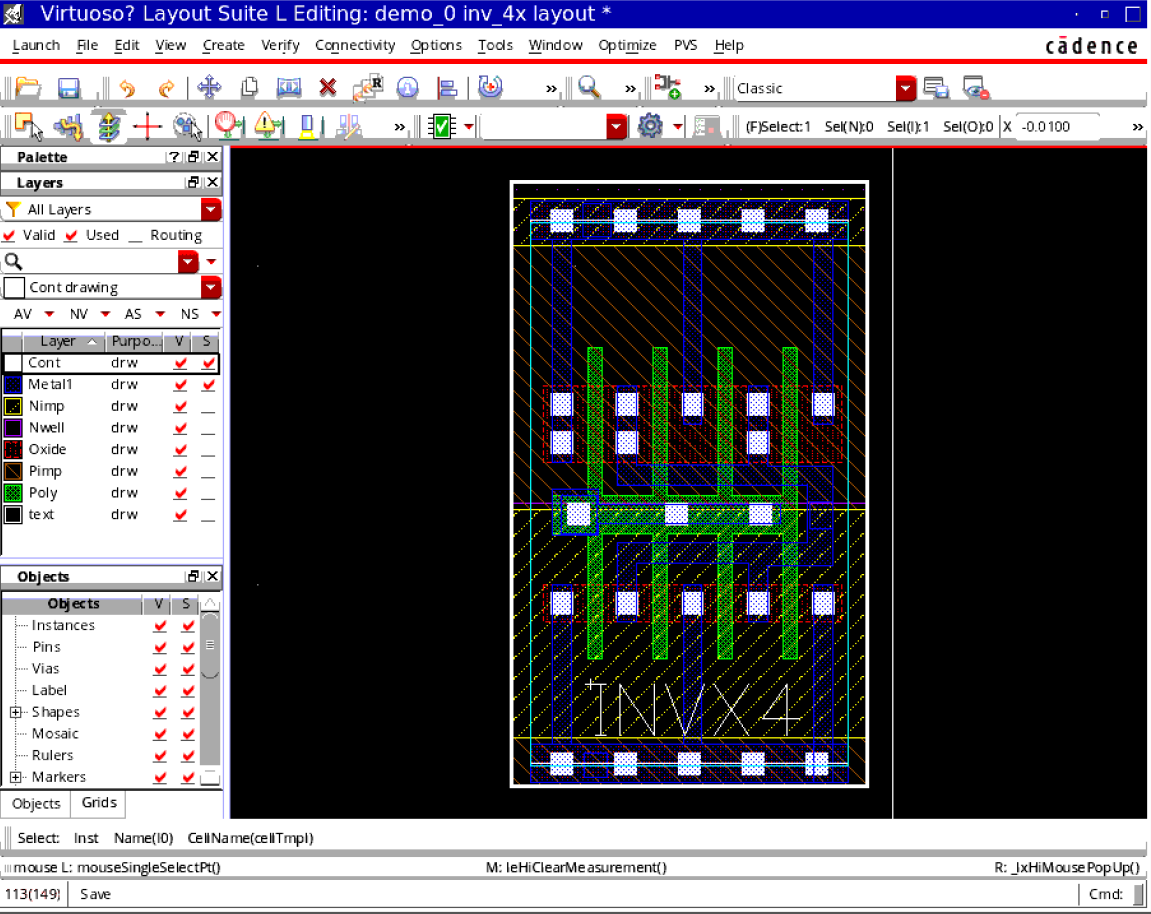
## INV1X

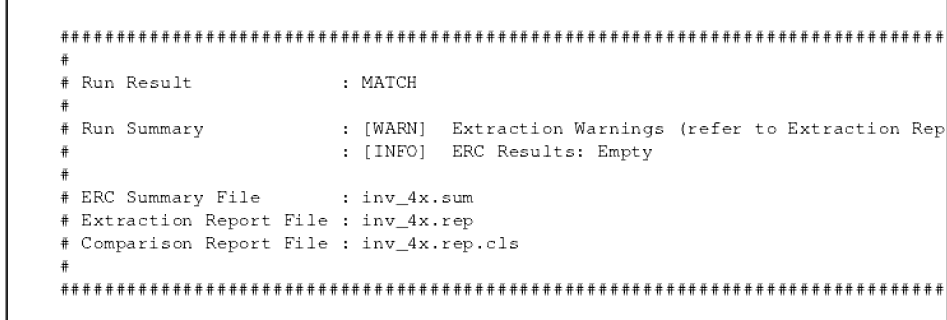


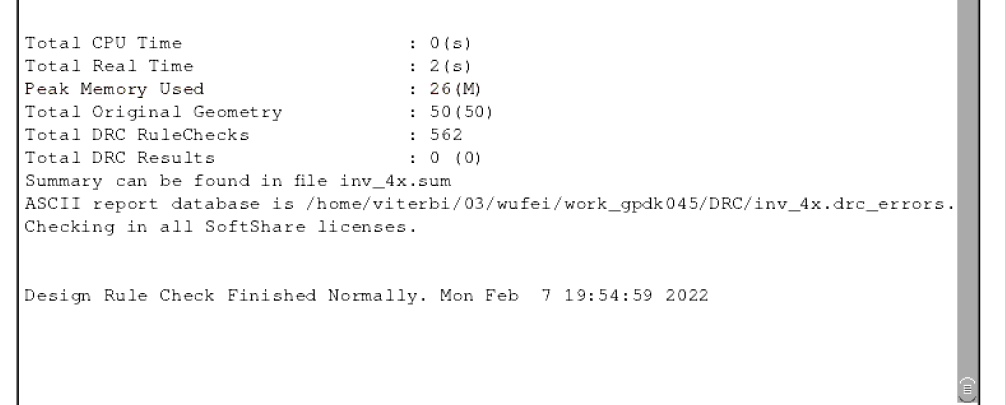




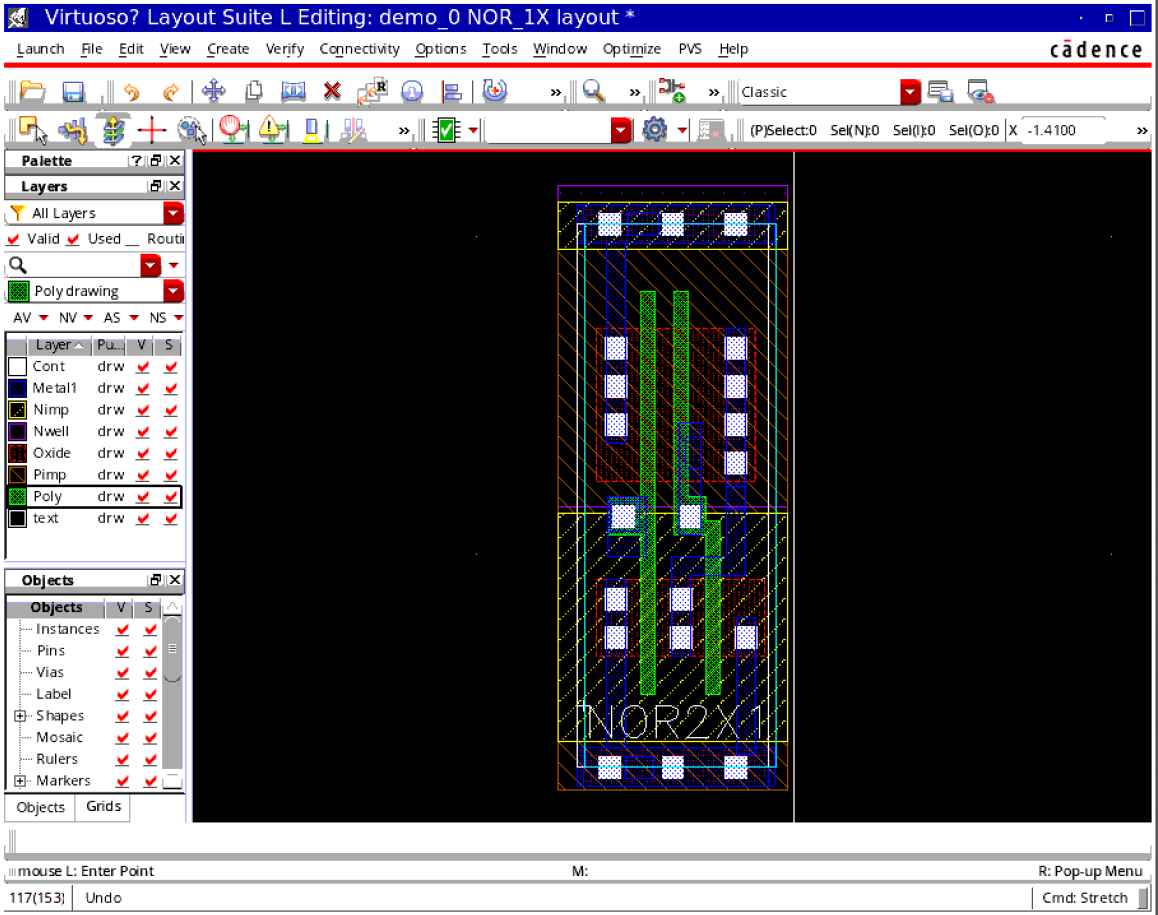
## INV4X

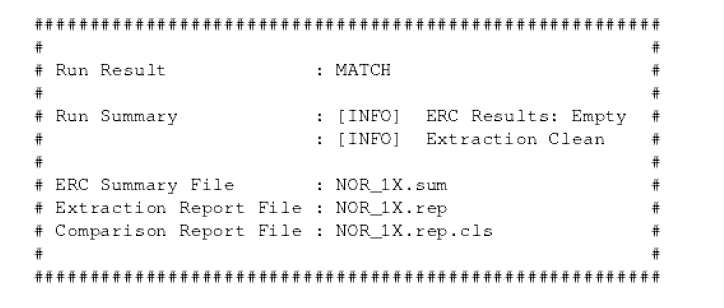


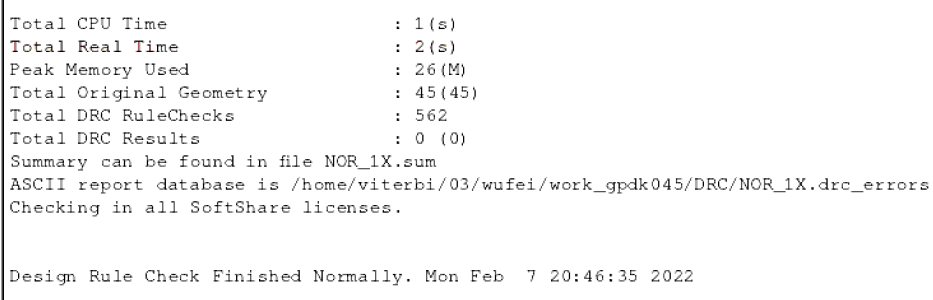


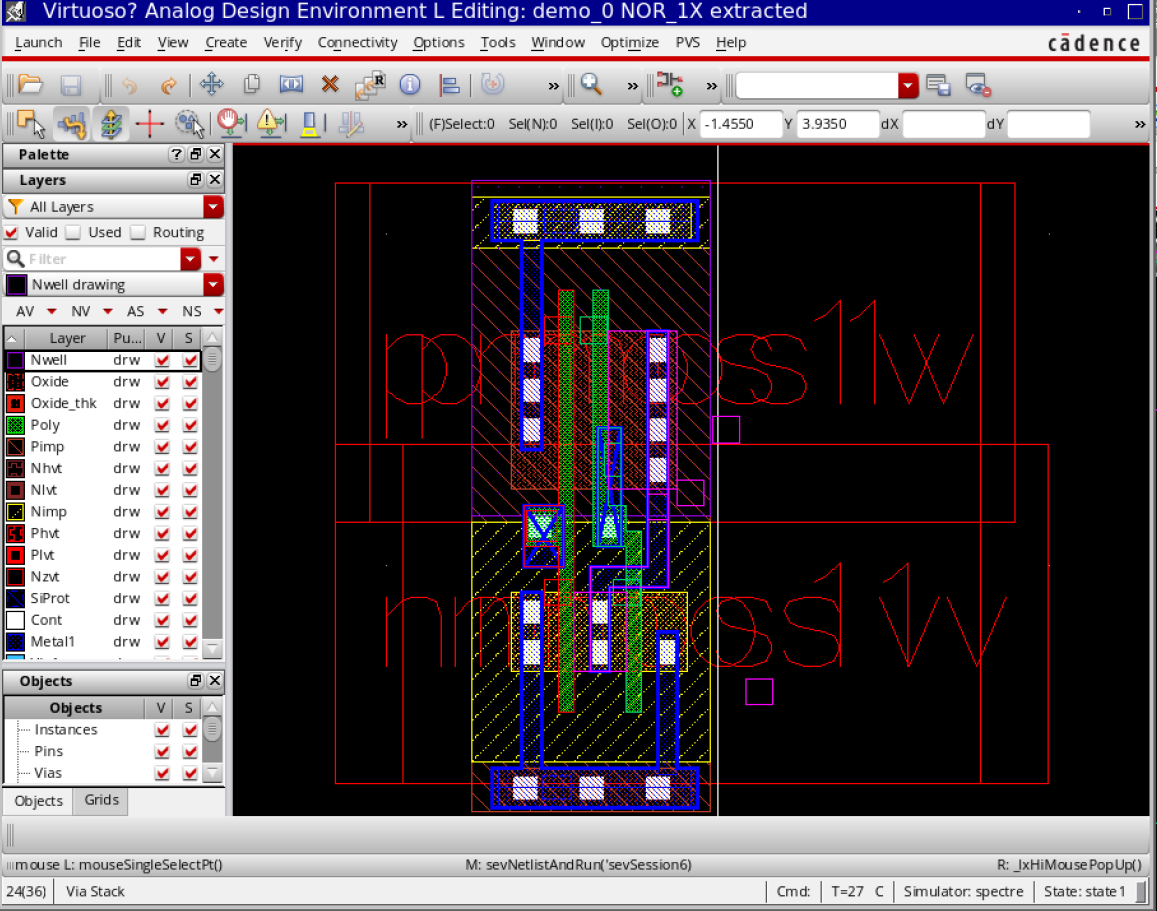


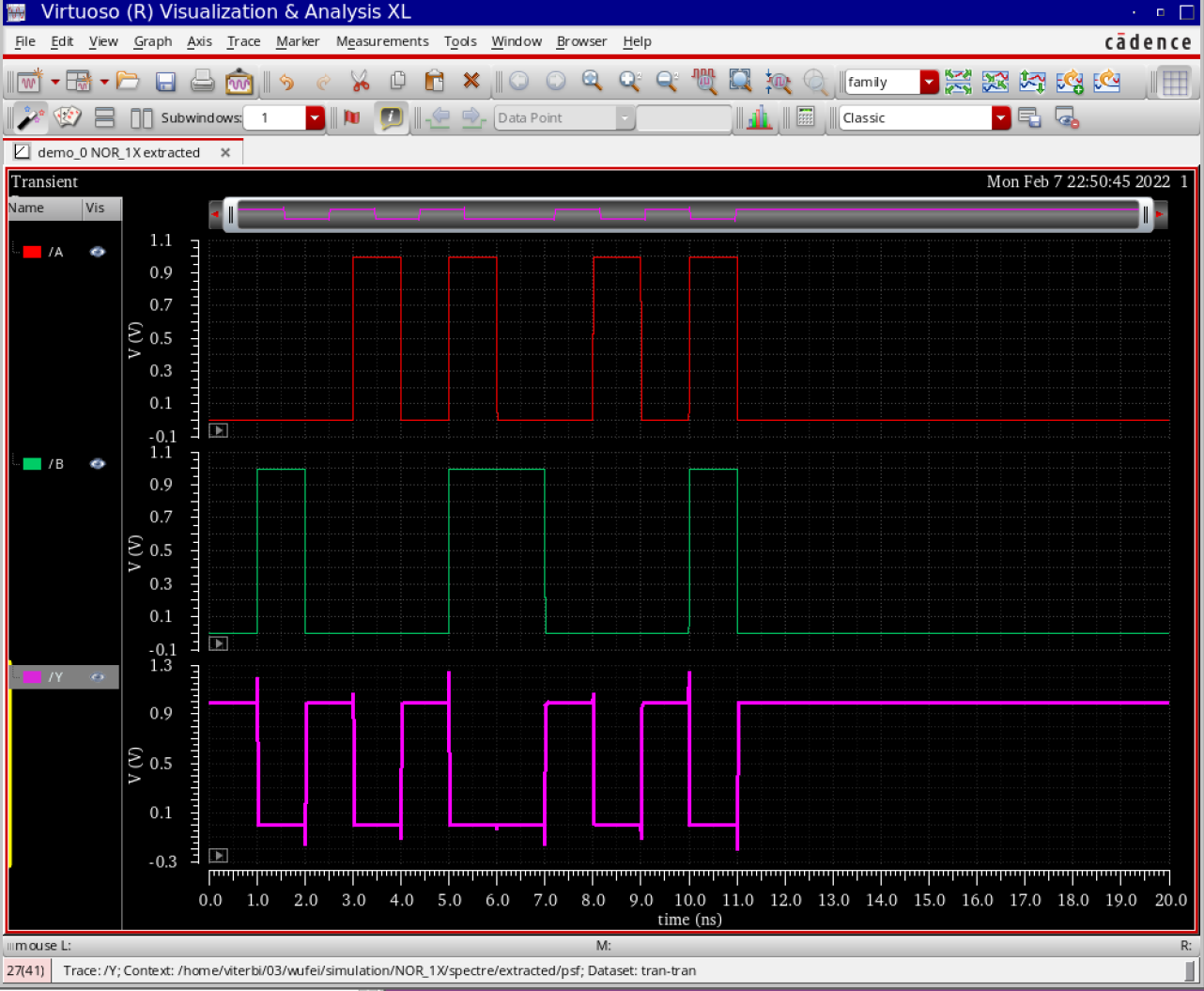
## NOR1X



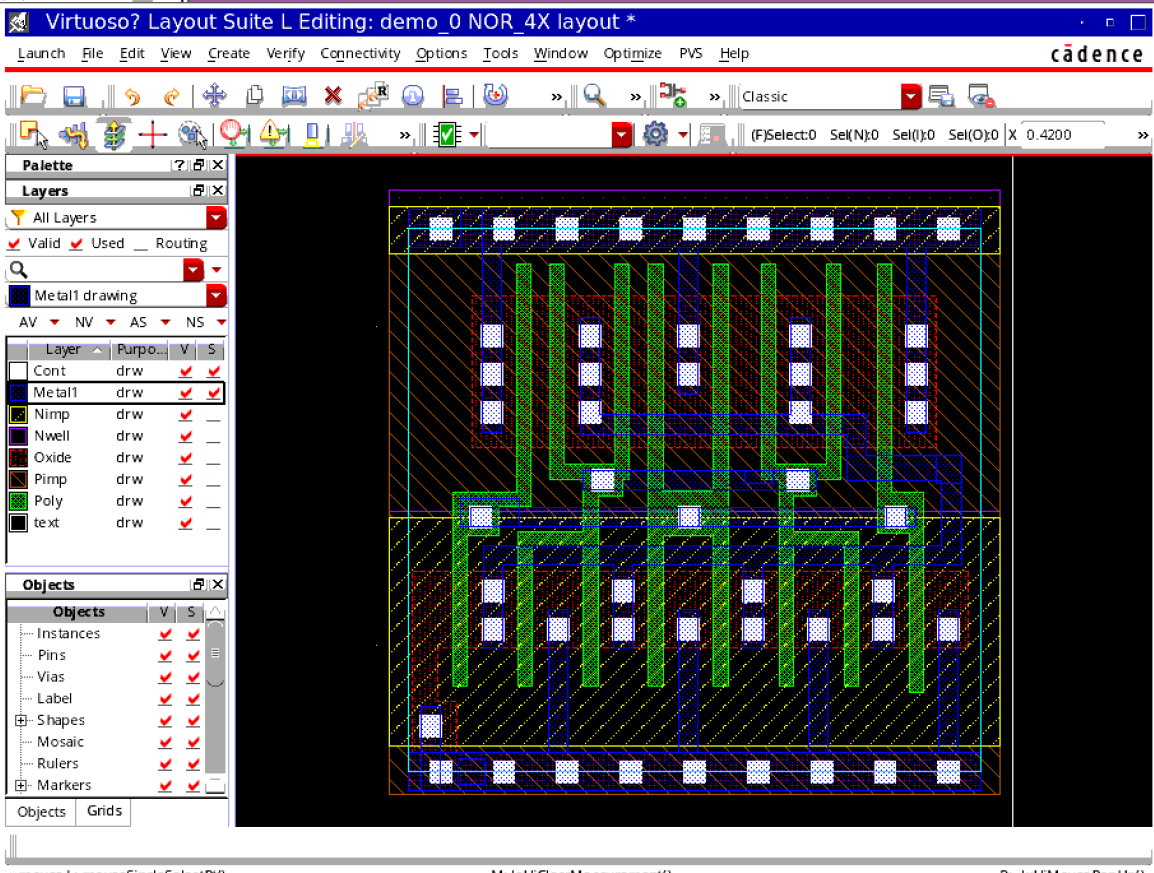


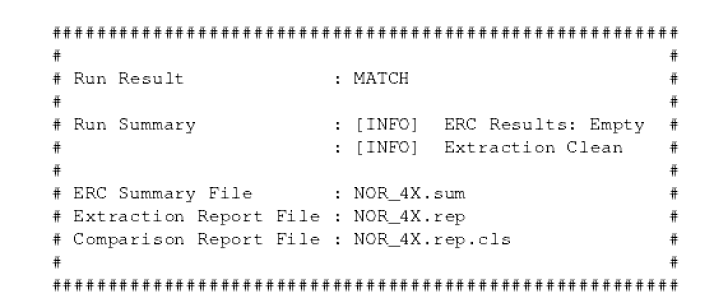


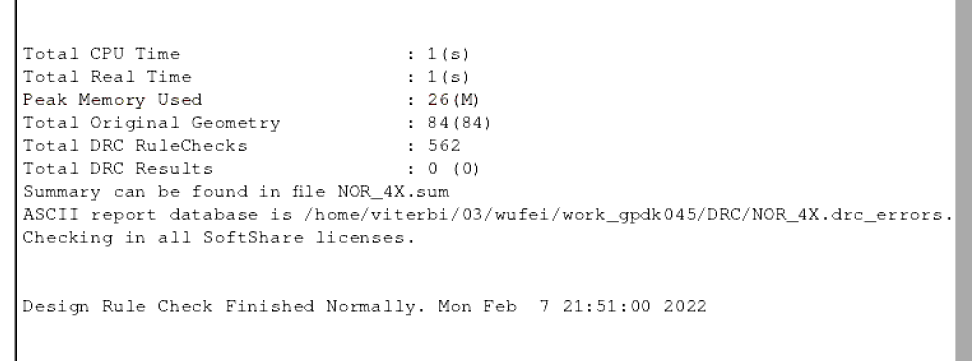


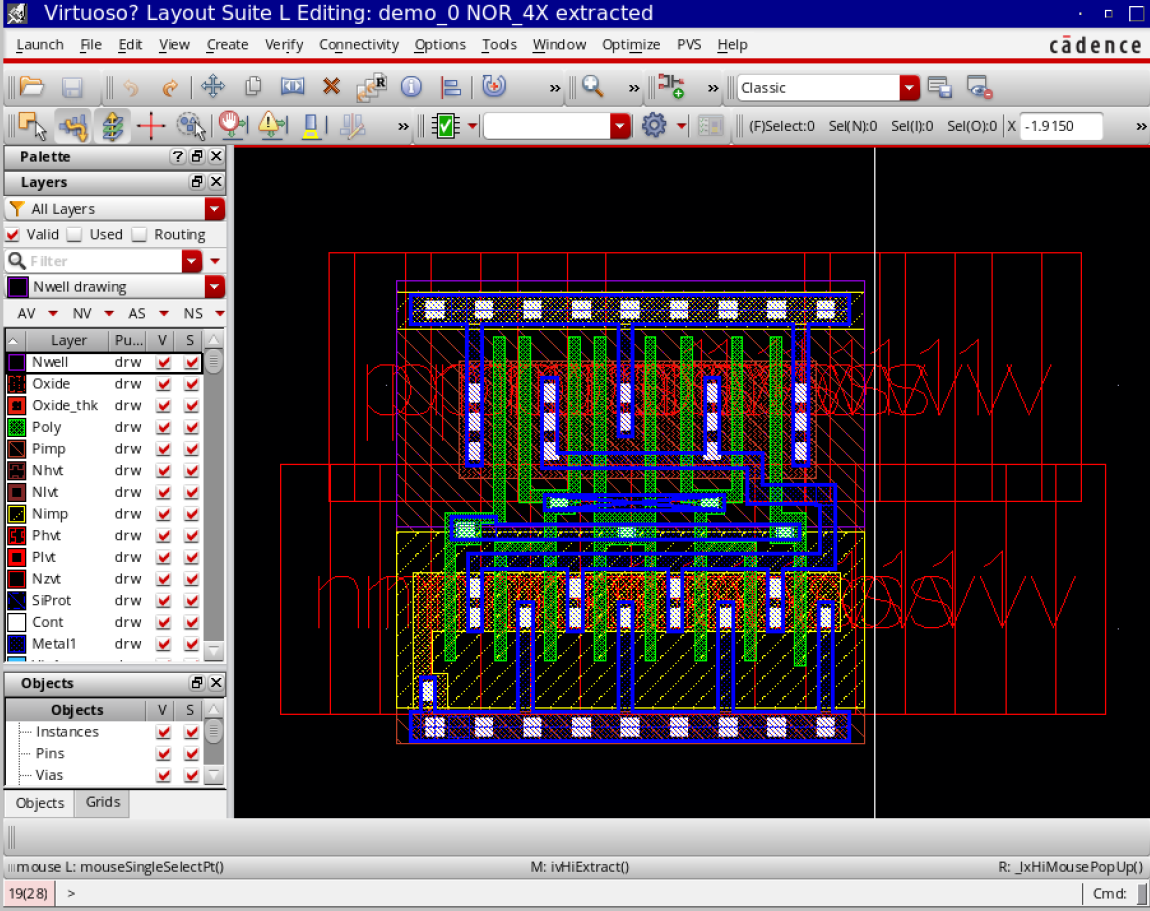


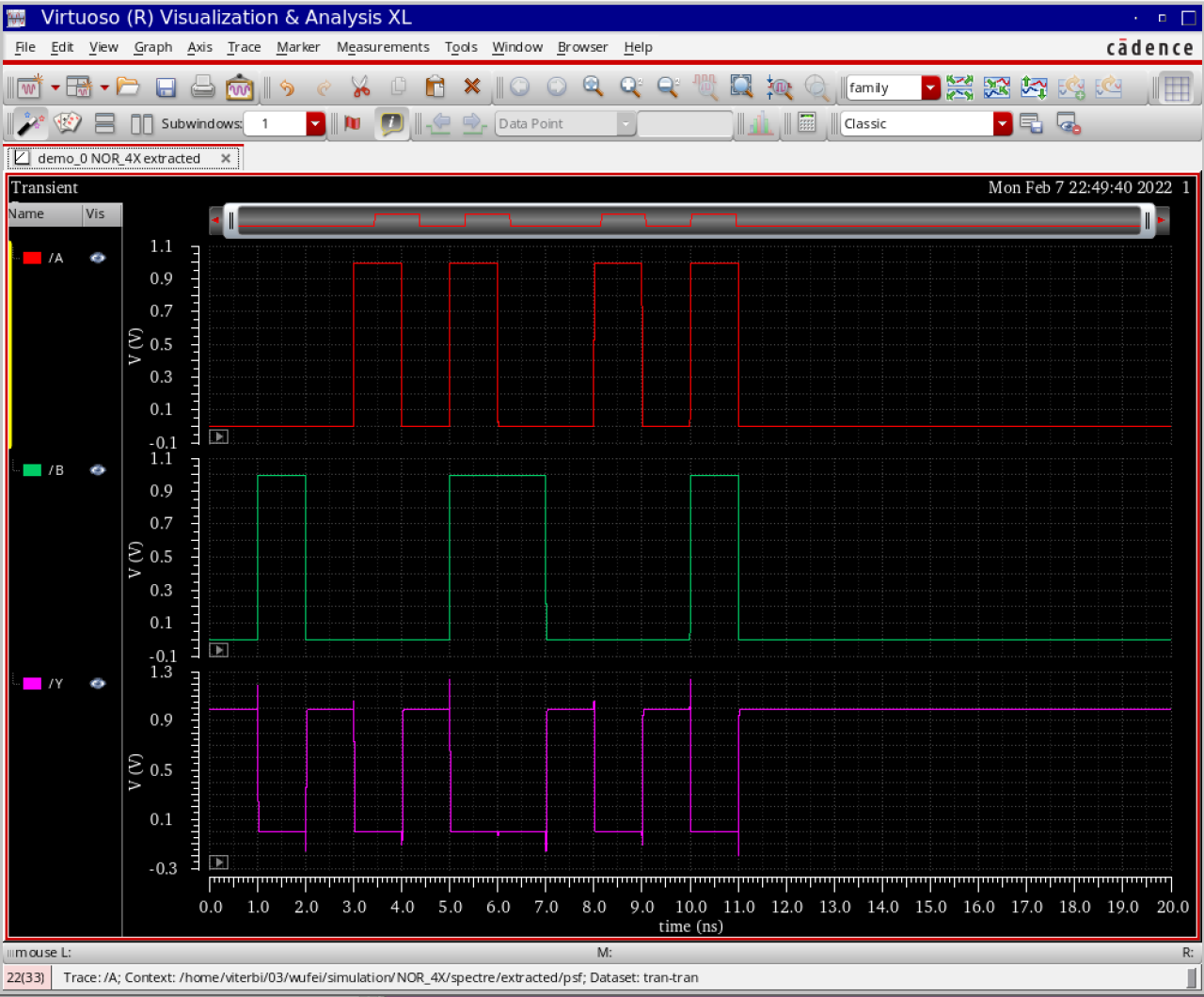
## NOR4X



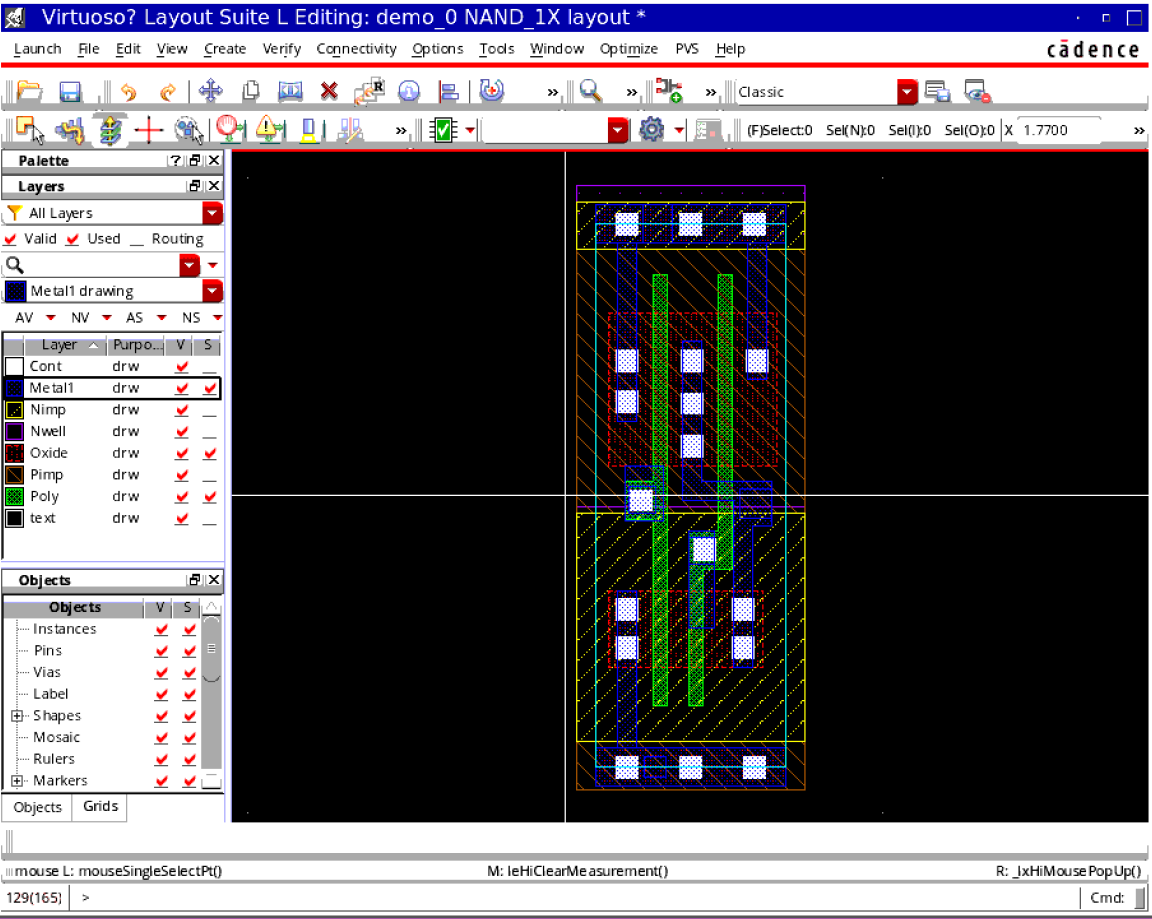


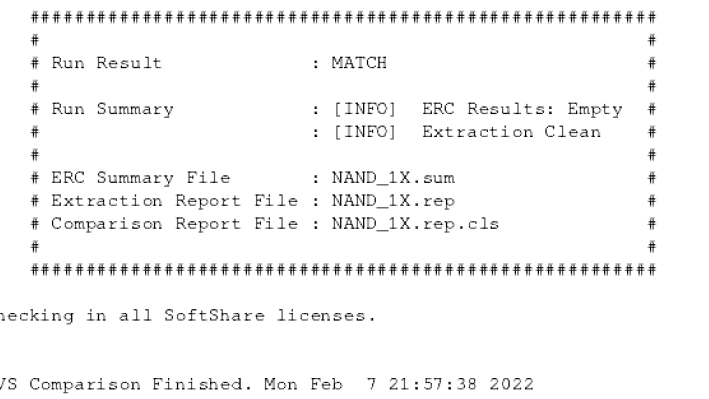


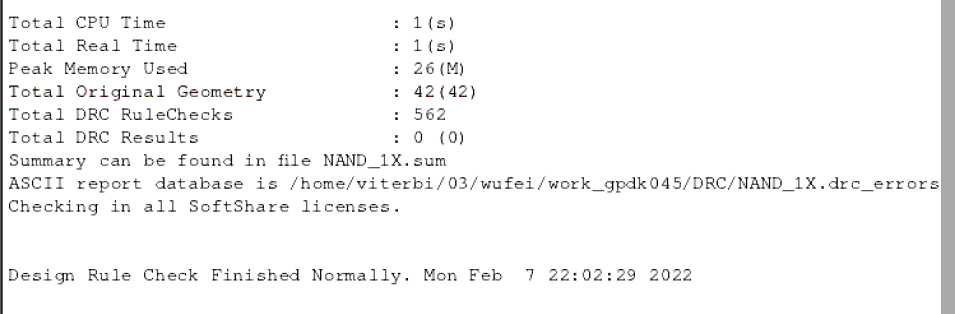


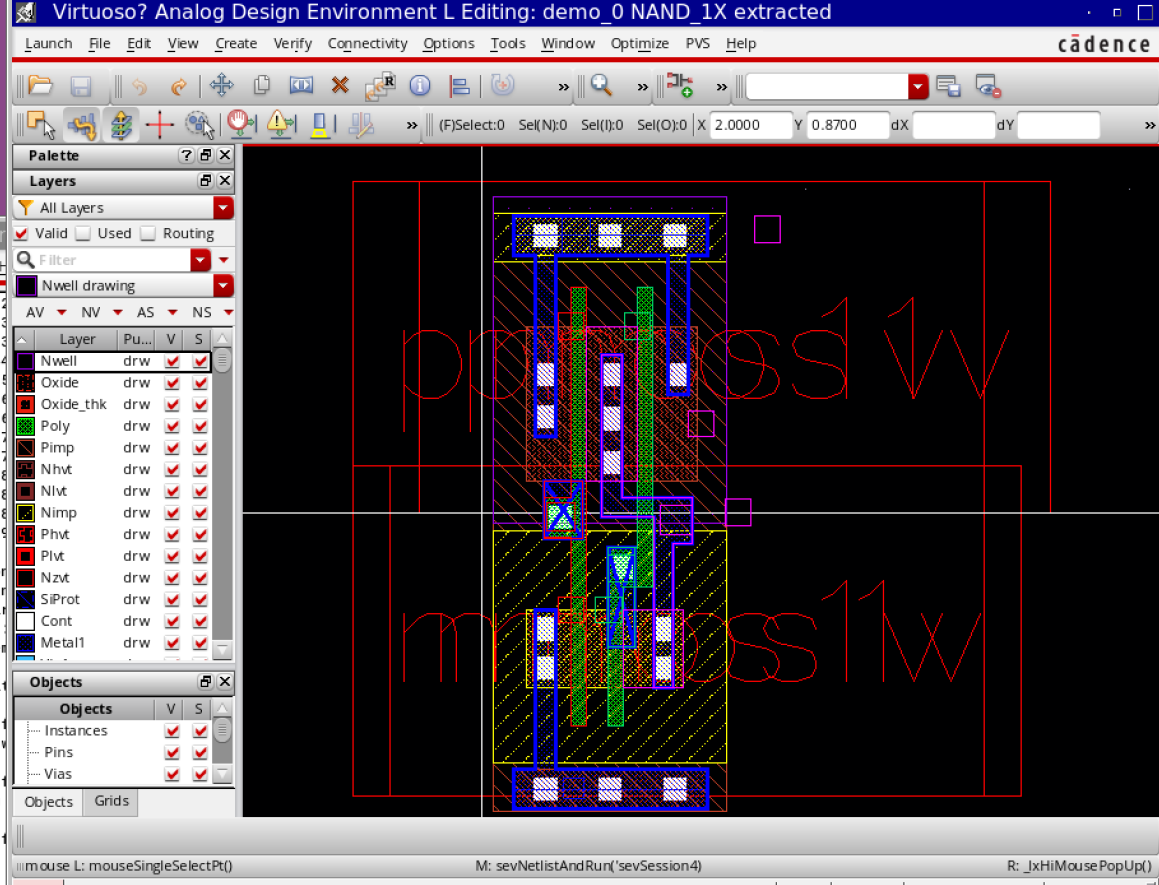


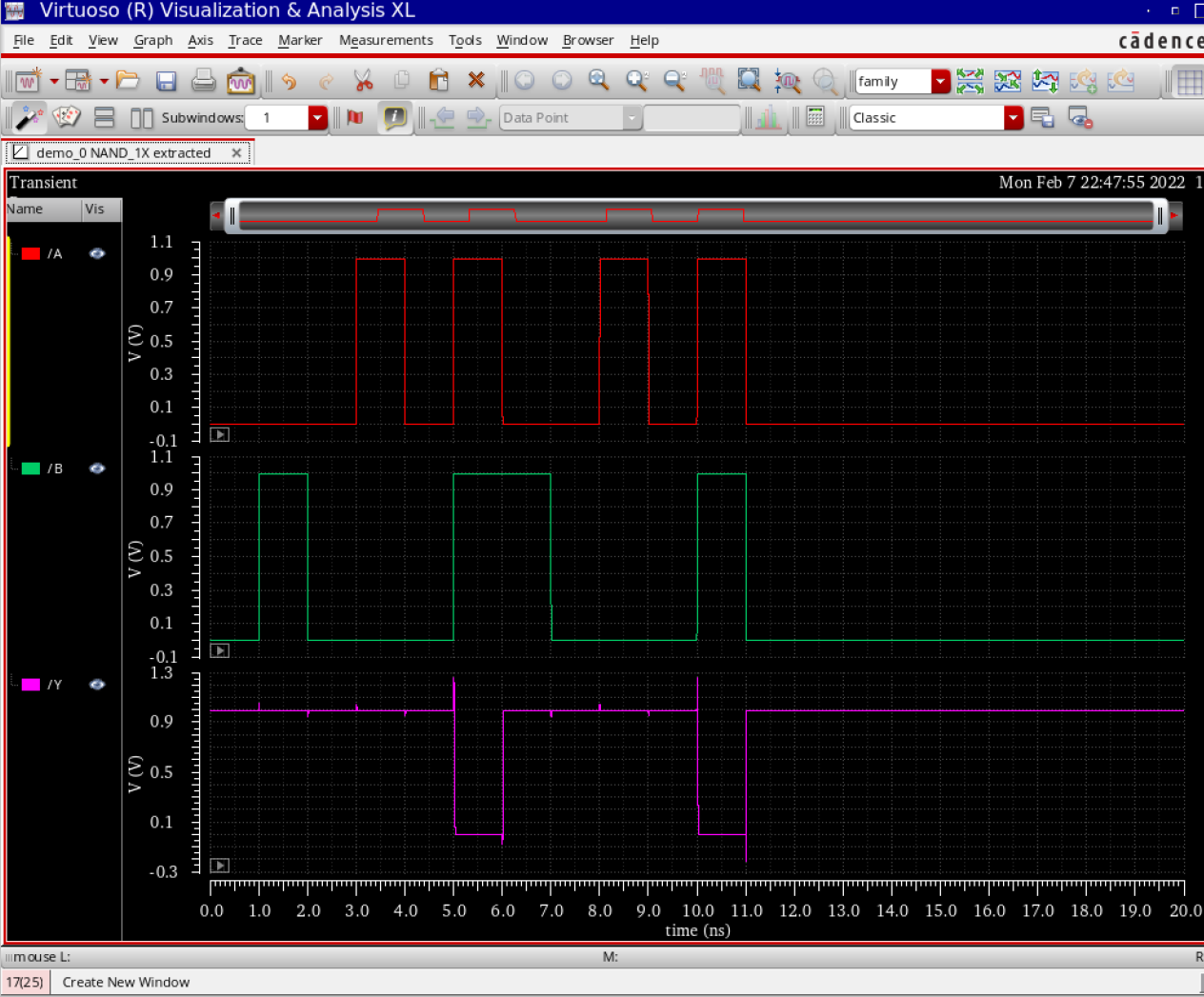
## NAND1X











## NAND4X

