Lab3

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Document ref			
Version			
Release date			
Author	Wu Fei		
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Distribution List	[Distribution list]		
Approved by	Name	Signature	Date

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Spring 2022

EE 477

Revision History

Date	Version List of changes	Author + Signature

C A T A L O G

1 Motivation

The delay of **RCAs** (Ripple Carry Adders) increases linearly as the number of inputs grows. One of the faster adders is the CSA (Carry Select Adder) which uses parallelism to increase speed with higher area costs. You will design (the layout) of an 8-bit CSA.

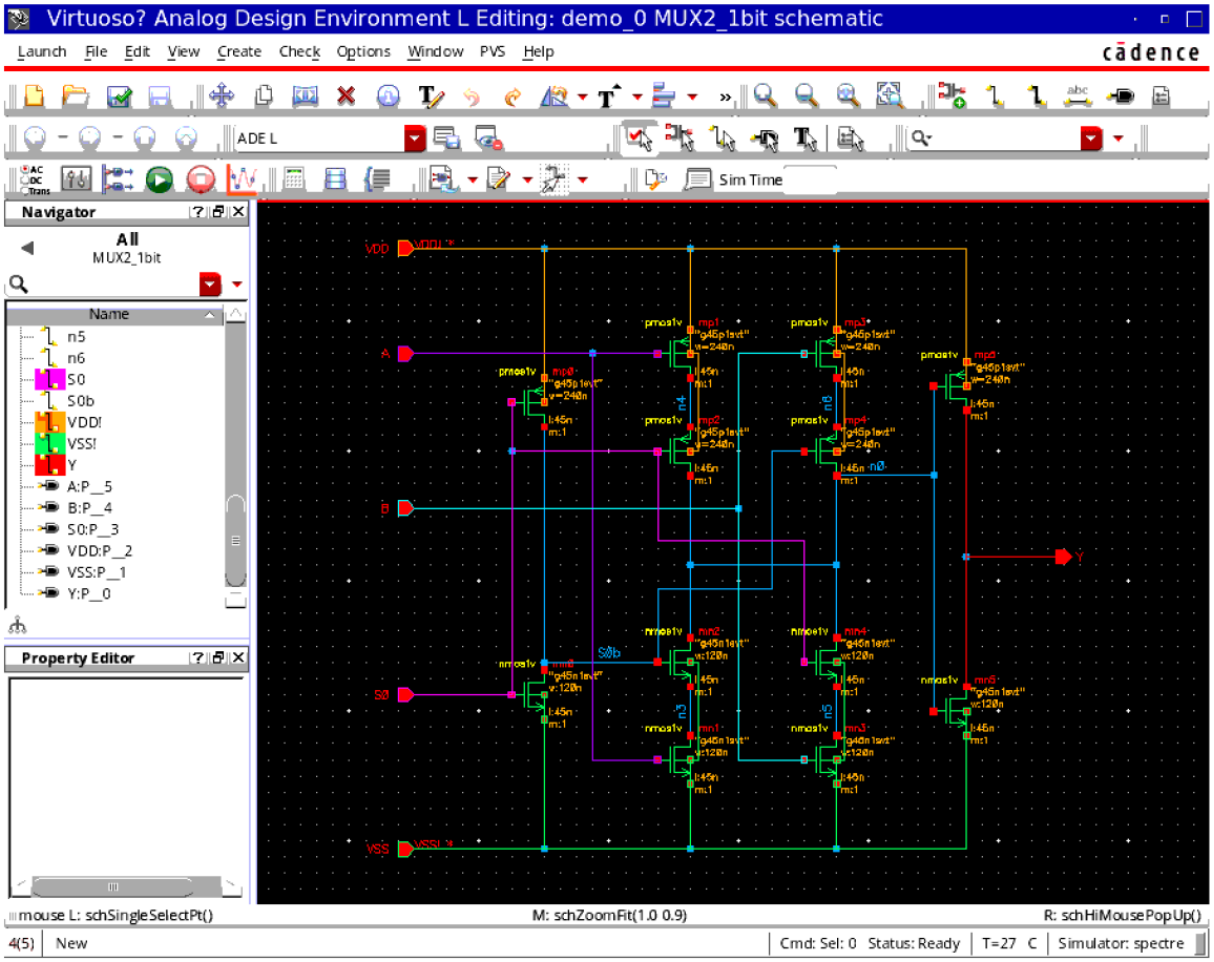
- Use **rise and fall time for all input stimuli = 10ps** (Note that it is NOT 100)
- For functionality waveforms, please write what the inputs and expected outputs are for each case. Example: Inputs are A=11111111 (255 in decimal), B=10000000 (128 in decimal), C0=0, expected outputs are C8=1, S=01111111. Then show the 9 output waveforms only.
- The input transition you chose for worst case delay of the CSA.
- Average delays for C8 for schematic and extracted.

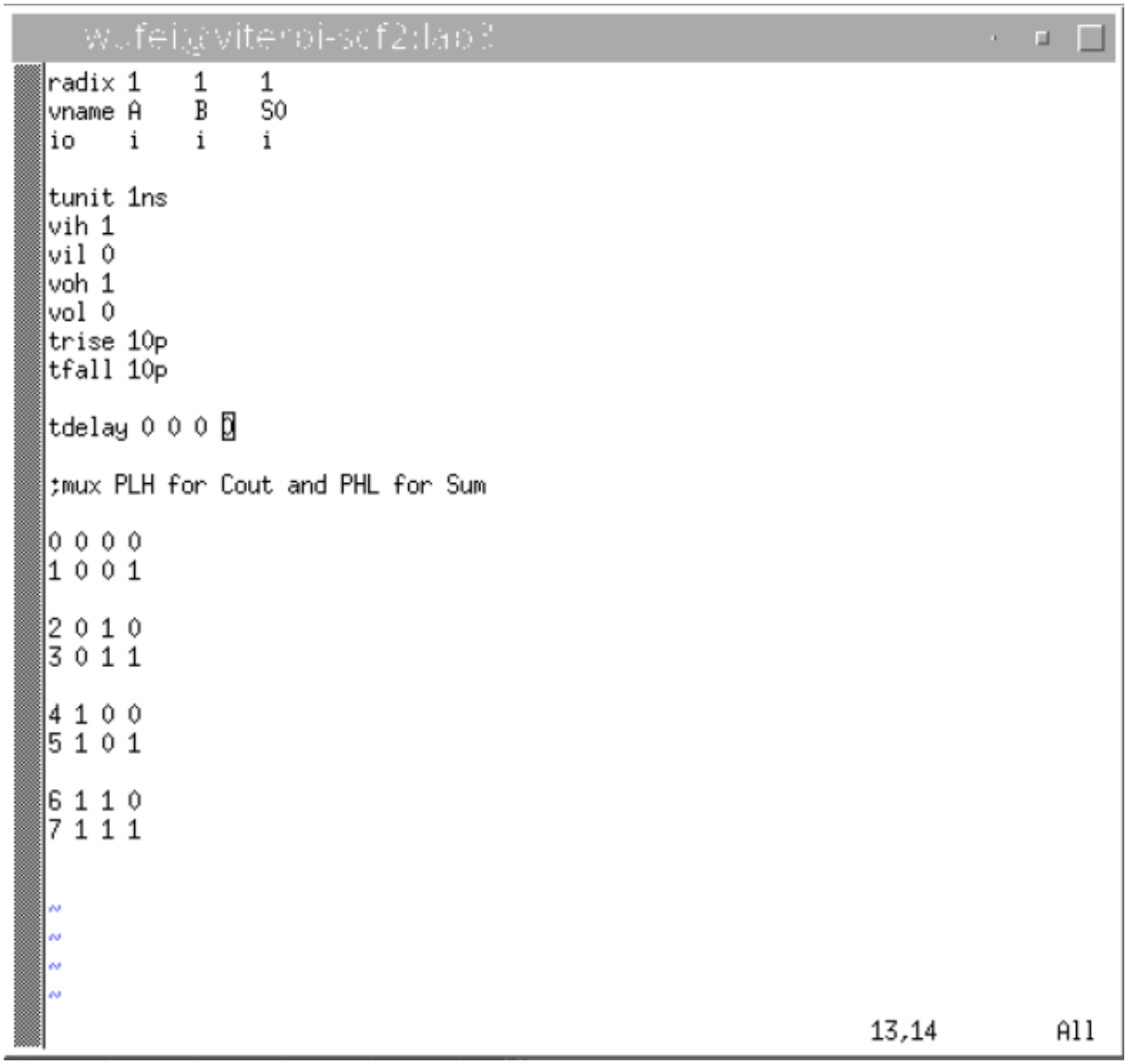
2 MUX design

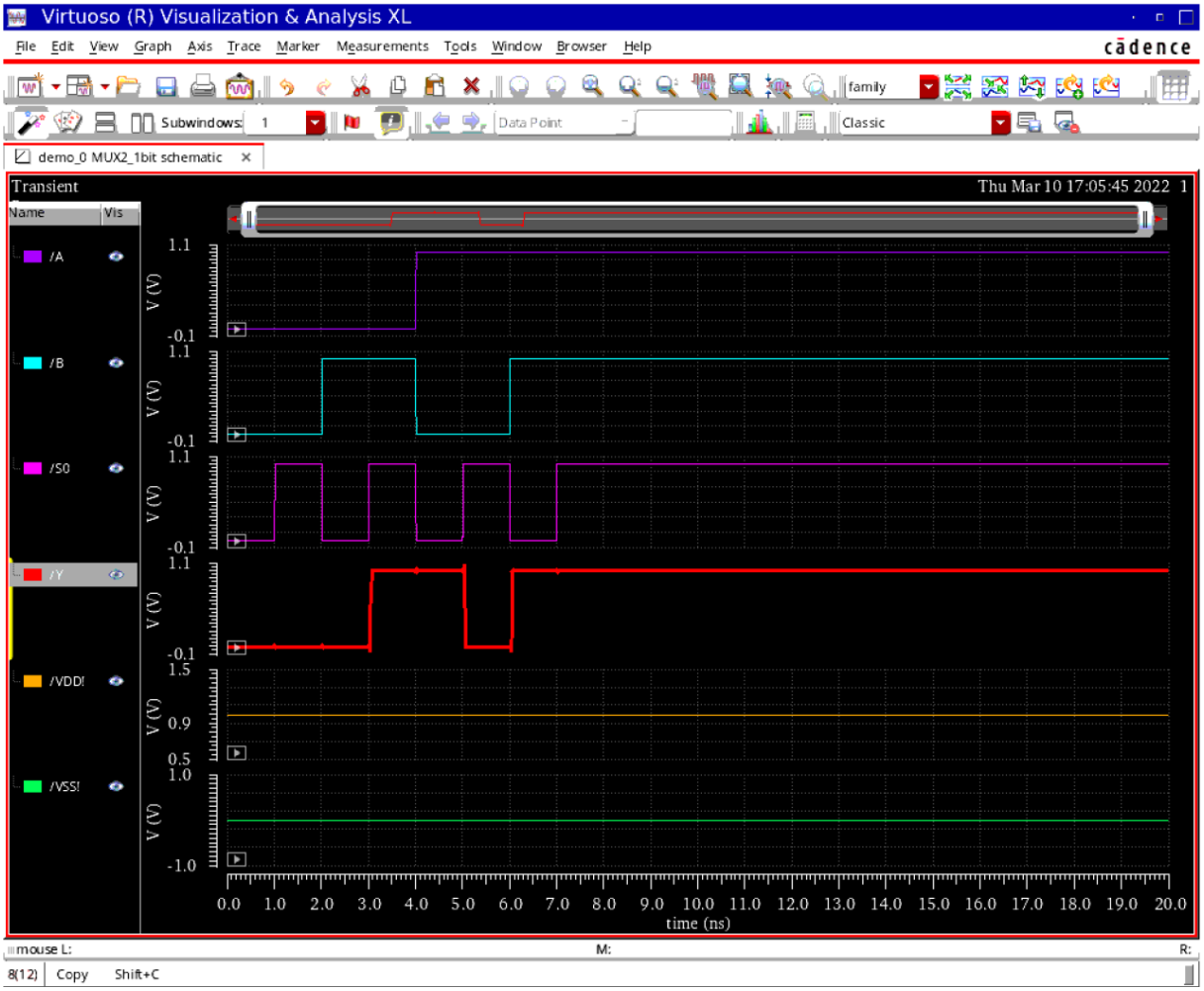
- An N-bit wide, M-to-1 multiplexer (MUX) has M inputs each of which is N-bits. It selects one of them to pass to output (which has N bits). Selection is done using log2M select bits which are inputs.
- ~~Design a 4-bit wide 2-to-1 MUX schematic. It will have 2 sets of inputs, each of which is 4 bits. It will also have a single select bit input and a 4-bit output.~~
- Design a 2-bit wide 2-to-1 MUX schematic. It will have 2 sets of inputs, each of which is 2 bits. It will also have a single select bit input and a 2-bit output. You only need 2 bit muxes in the CSA design.
- Draw the schematic and layout and verify the functionality

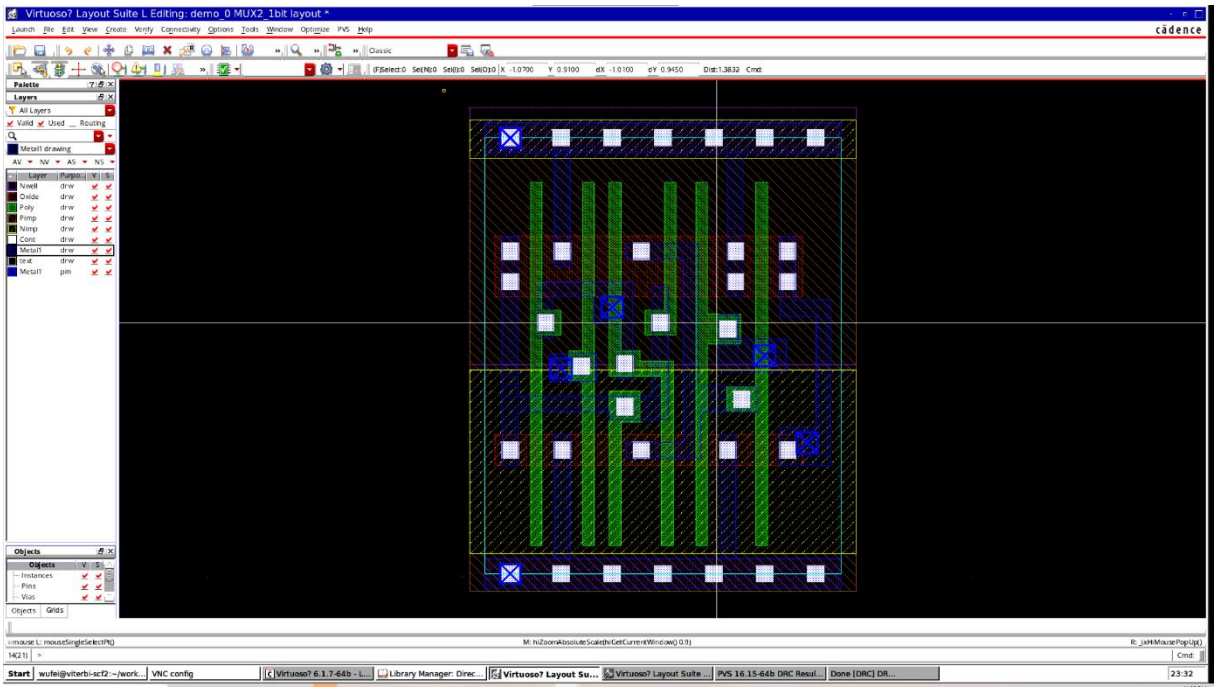
2.1 1bit mux2

Schematic

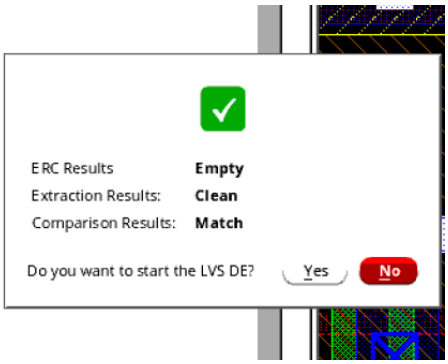



w.feigviterbi-scf2:lab3
radix 1 1 1
vname A B S0
io i i i
tunit 1ns
vih 1
vil 0
voh 1
vol 0
trise 10p
tfall 10p
tdelay 0 0 0 0
;mux PLH for Cout and PHL for Sum
0 0 0 0
1 0 0 1
2 0 1 0
3 0 1 1
4 1 0 0
5 1 0 1
6 1 1 0
7 1 1 1
13,14 All


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
demo_0 MUX2_1bit schematic
Transient
Thu Mar 10 17:05:45 2022
Name
Vis
/A
/B
/S0
/Y
/VDD!
/VSS!
V (V)
time (ns)
mouse L:
M:
R:
Copy
Shift+C


Virtuoso? Layout Suite L Editing: demo_0 MUX2_1bit layout *
cadence

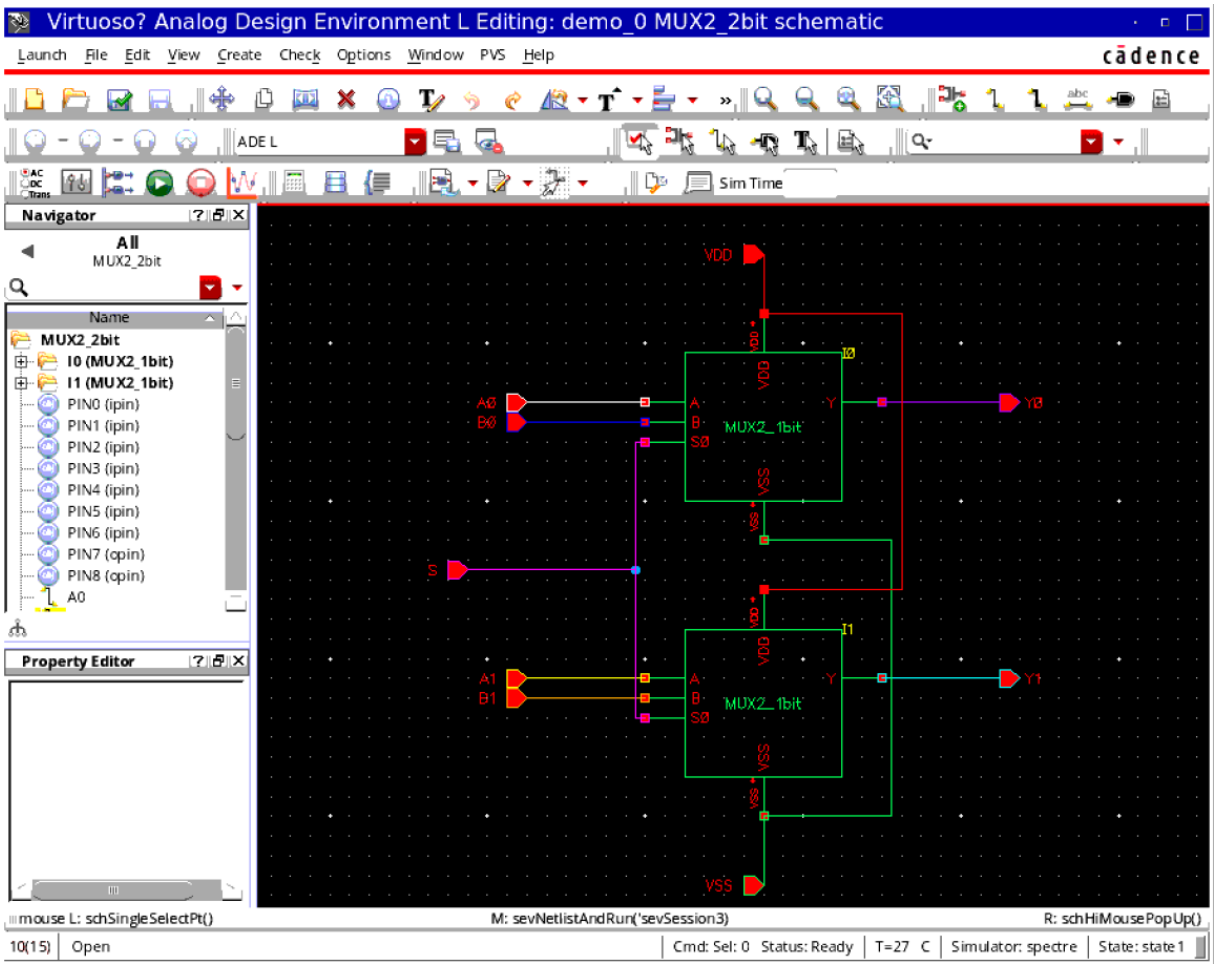
```
#########################################################
#                                                       #
# Run Result              : MATCH                       #
#                                                       #
# Run Summary             : [INFO]  ERC Results: Empty  #
#                         : [INFO]  Extraction Clean    #
#                                                       #
# ERC Summary File        : MUX2_1bit.sum               #
# Extraction Report File  : MUX2_1bit.rep               #
# Comparison Report File  : MUX2_1bit.rep.cls           #
#                                                       #
#########################################################
```

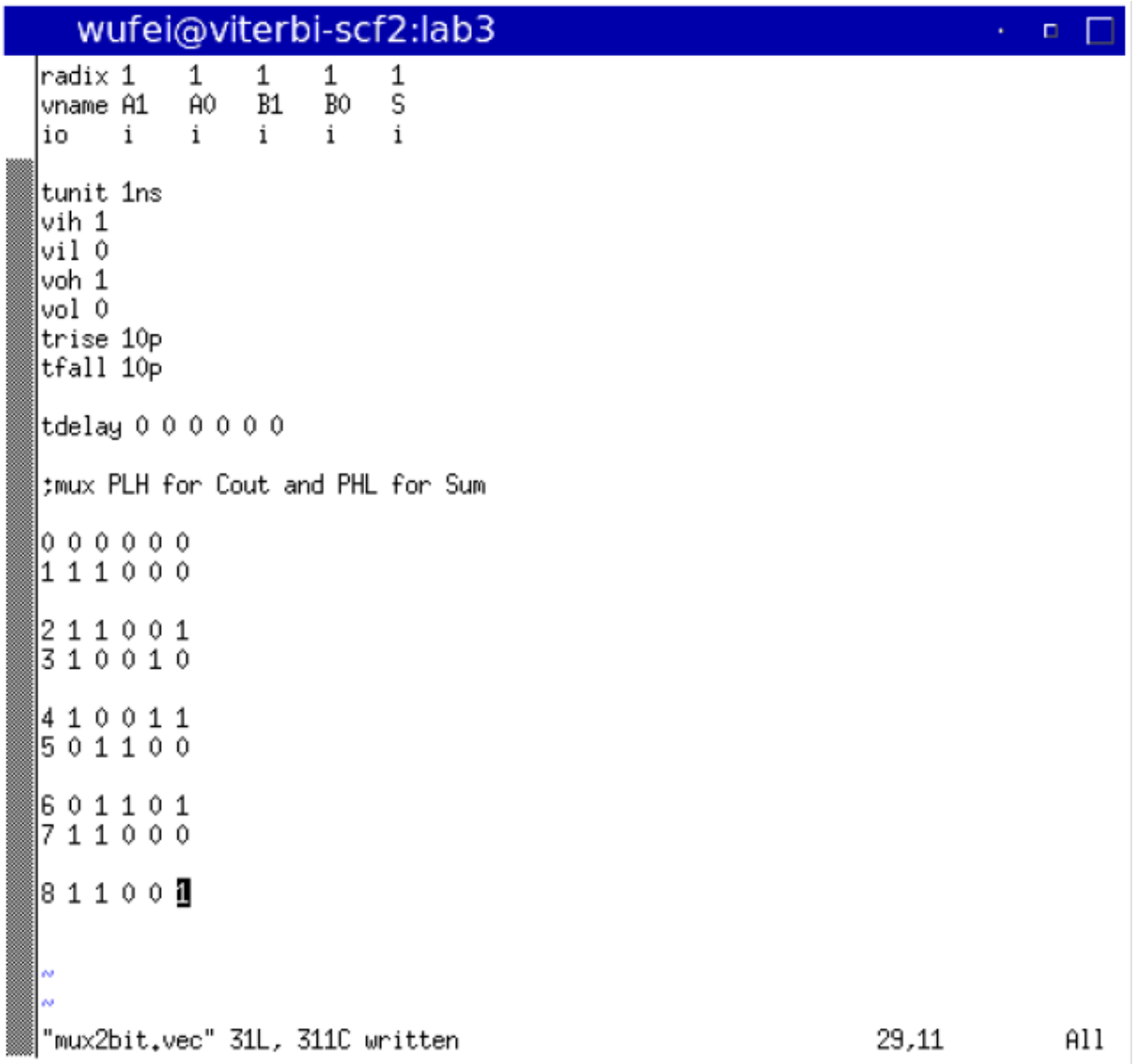


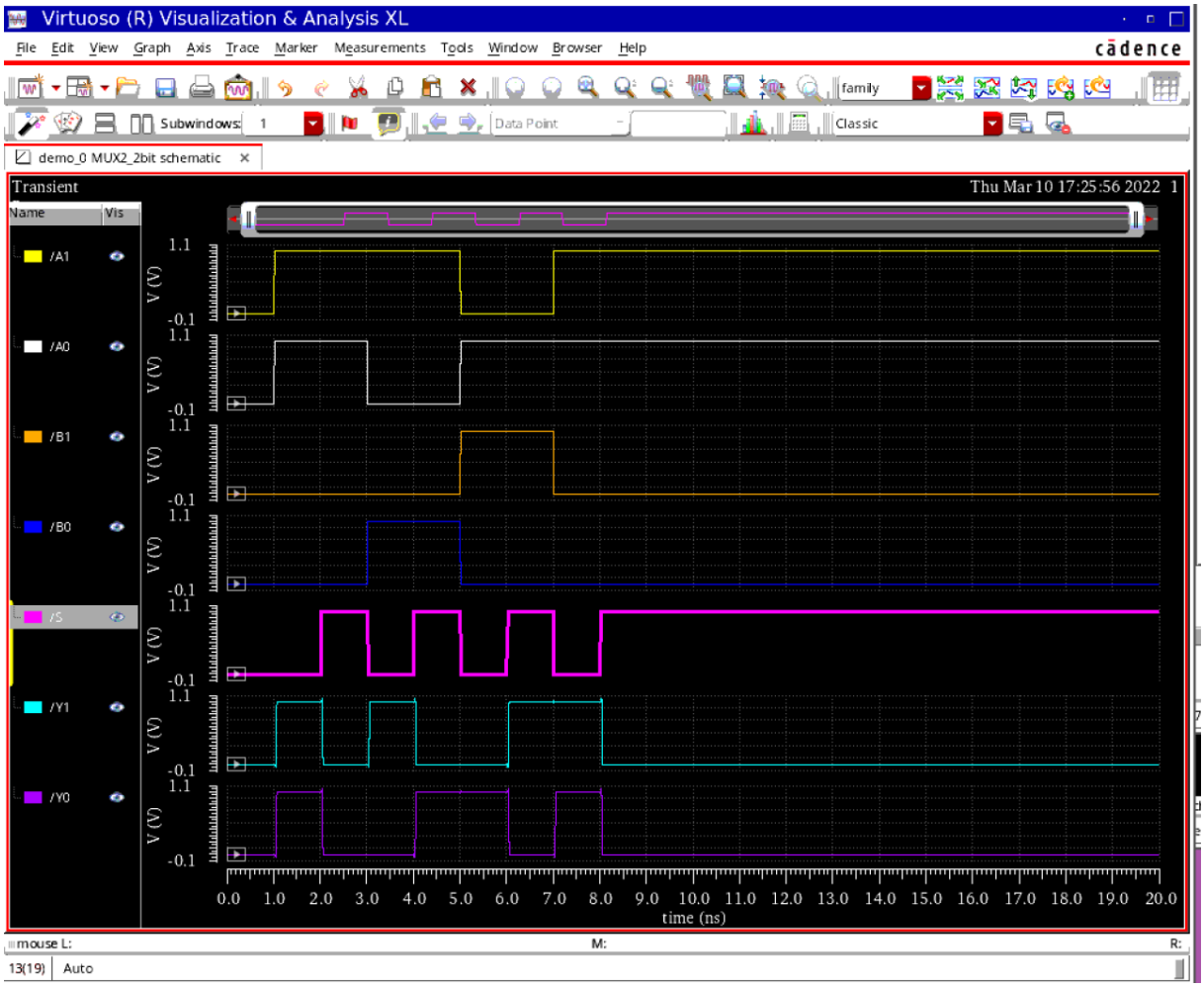

```
Total CPU Time                    : 1(s)
Total Real Time                   : 1(s)
Peak Memory Used                  : 26(M)
Total Original Geometry           : 71(71)
Total DRC RuleChecks              : 562
Total DRC Results                 : 0 (0)
Summary can be found in file MUX2_1bit.sum
ASCII report database is /home/viterbi/03/wufei/work_gpdk045/DRC/MUX2_1bit.drc_erro
Checking in all SoftShare licenses.


Design Rule Check Finished Normally. Thu Mar 10 23:31:23 2022
```

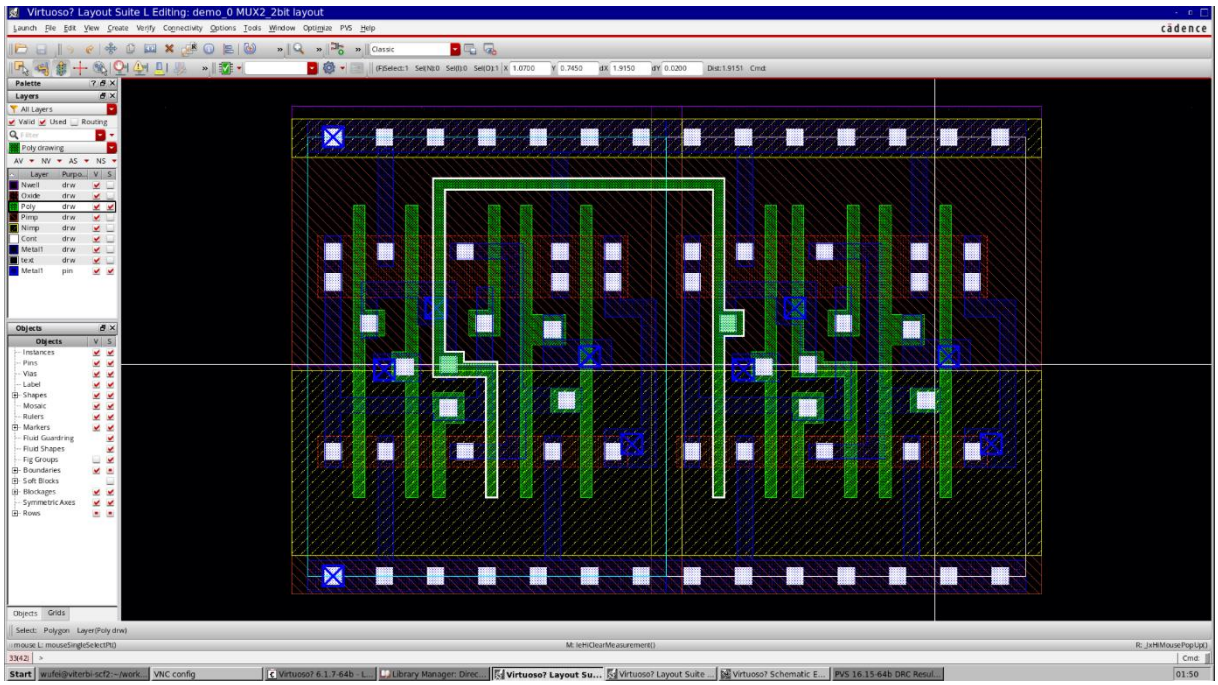
2.2 2bits mux

Schematic


Virtuoso? Analog Design Environment L Editing: demo_0 MUX2_2bit schematic
Launch File Edit View Create Check Options Window PVS Help
cadence
ADE L
Sim Time
Navigator
All
MUX2_2bit
Name
MUX2_2bit
I0 (MUX2_1bit)
I1 (MUX2_1bit)
PIN0 (ipin)
PIN1 (ipin)
PIN2 (ipin)
PIN3 (ipin)
PIN4 (ipin)
PIN5 (ipin)
PIN6 (ipin)
PIN7 (opin)
PIN8 (opin)
A0
Property Editor
VDD
A0
B0
S
A1
B1
I0
I1
A
B
S0
Y
MUX2_1bit
VSS
Y0
Y1
mouse L: schSingleSelectPt()
M: sevNetlistAndRun('sevSession3)
R: schHiMousePopUp()
10(15)
Open
Cmd: Sel: 0 Status: Ready
T=27 C
Simulator: spectre
State: state1

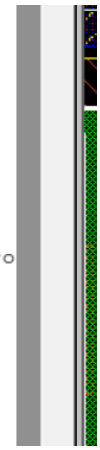

wufei@viterbi-scf2:lab3
radix 1 1 1 1 1
vname A1 A0 B1 B0 S
io i i i i i
tunit 1ns
vih 1
vil 0
voh 1
vol 0
trise 10p
tfall 10p
tdelay 0 0 0 0 0 0
;mux PLH for Cout and PHL for Sum
0 0 0 0 0 0
1 1 1 0 0 0
2 1 1 0 0 1
3 1 0 0 1 0
4 1 0 0 1 1
5 0 1 1 0 0
6 0 1 1 0 1
7 1 1 0 0 0
8 1 1 0 0 1
"mux2bit.vec" 31L, 311C written
29,11
All


Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
cadence
Subwindows: 1
Data Point
Classic
demo_0 MUX2_2bit schematic
Transient
Thu Mar 10 17:25:56 2022
Name
Vis
/A1
/A0
/B1
/B0
/S
/Y1
/Y0
V (V)
1.1
-0.1
0.0 1.0 2.0 3.0 4.0 5.0 6.0 7.0 8.0 9.0 10.0 11.0 12.0 13.0 14.0 15.0 16.0 17.0 18.0 19.0 20.0
time (ns)
mouse L:
M:
R:
13(19)
Auto


Virtuoso? Layout Suite L Editing: demo_0 MUX2_2bit layout
cadence

```
    ############################################################
    #                                                          #
    # Run Result              : MATCH                          #
    #                                                          #
    # Run Summary             : [INFO]  ERC Results: Empty     #
    #                         : [INFO]  Extraction Clean       #
    #                                                          #
    # ERC Summary File        : MUX2_2bit.sum                  #
    # Extraction Report File  : MUX2_2bit.rep                  #
    # Comparison Report File  : MUX2_2bit.rep.cls               #
    #                                                          #
    ############################################################

Checking in all SoftShare licenses.


PVS Comparison Finished. Fri Mar 11 01:48:05 2022
```

```
Total CPU Time                  : 0(s)
Total Real Time                 : 1(s)
Peak Memory Used                : 26(M)
Total Original Geometry         : 112(135)
Total DRC RuleChecks            : 562
Total DRC Results               : 0 (0)
Summary can be found in file MUX2_2bit.sum
ASCII report database is /home/viterbi/03/wufei/work_gpdk045/DRC/MUX2_2bit.drc_erro
Checking in all SoftShare licenses.


Design Rule Check Finished Normally. Fri Mar 11 01:50:41 2022
```

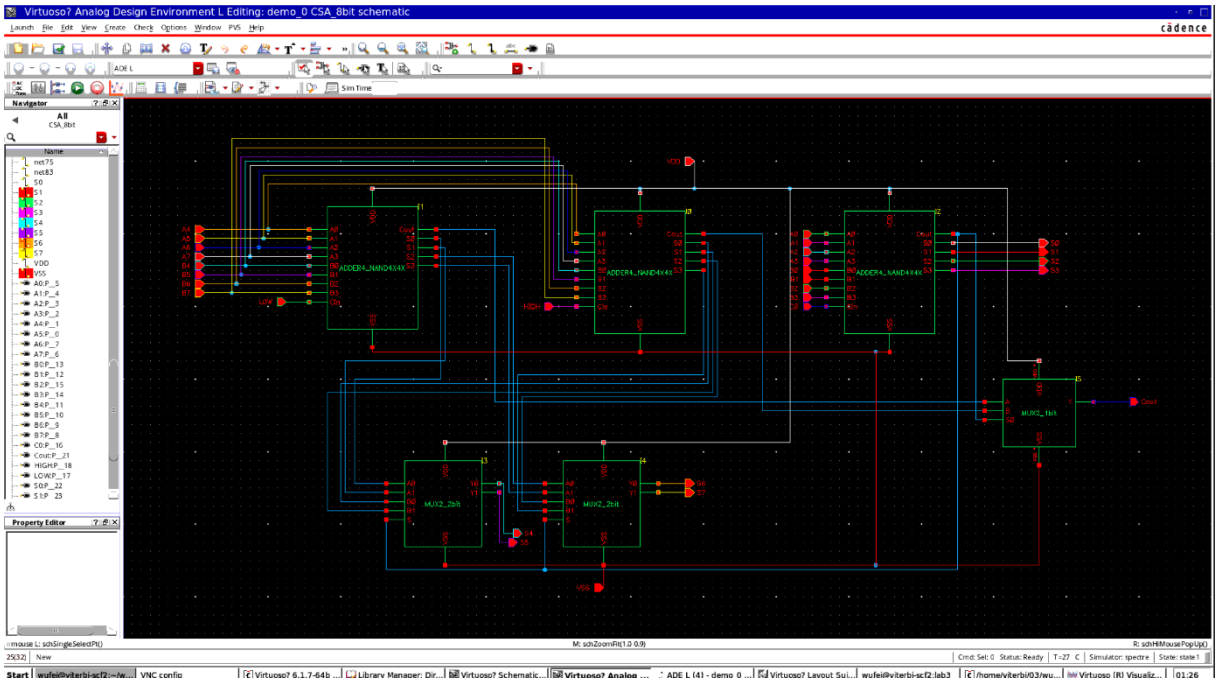


3 8_bit carry select adder design

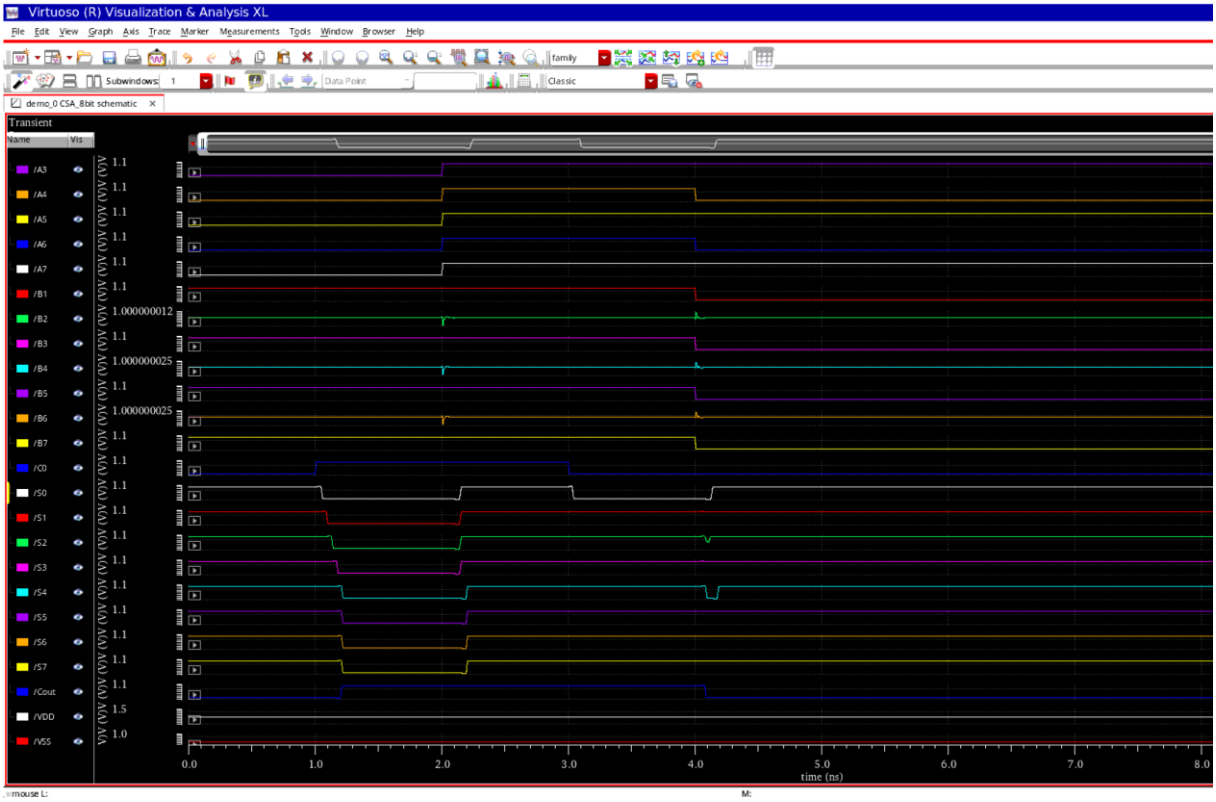
- A CSA computes the outputs for the later stages, i.e., the one processing the higher significant bits, for two cases of input carry as 1 and also as 0, both, while the earlier stages work on the addition of lower significant bits. By the time, the actual carry bit is calculated by the earlier stages, the higher stages are also done and all it takes to produce the complete result is to use the multiplexer to pass the correct results.
- You may choose any of the circuit recommendations presented during lecture and discussion classes.
- You are welcome to use your 4-bit RCA of lab2 as part of this lab.
- Do a functionality test. Use at least 3 different combinations for <a[8:1],b[8:1],c0>.
- Build a delay measurement circuit. All inputs <a[8:1],b[8:1],c0> should be applied through INV_1X. Connect an INV_4X for each output (i.e., <c8,s[8:1]>).</c8,s[8:1]></a[8:1],b[8:1],c0></a[8:1],b[8:1],c0>
- Find an input transition which results in worst case delay for output C8. Repeat for S8.
- For this input transition, measure the average delay.
- Draw the layout for the 8-bit CSA.
- Draw layout for the delay measurement circuit and measure average delay of C8 on the extracted view using the same worst case input transition.

3.1 CSA_8bit

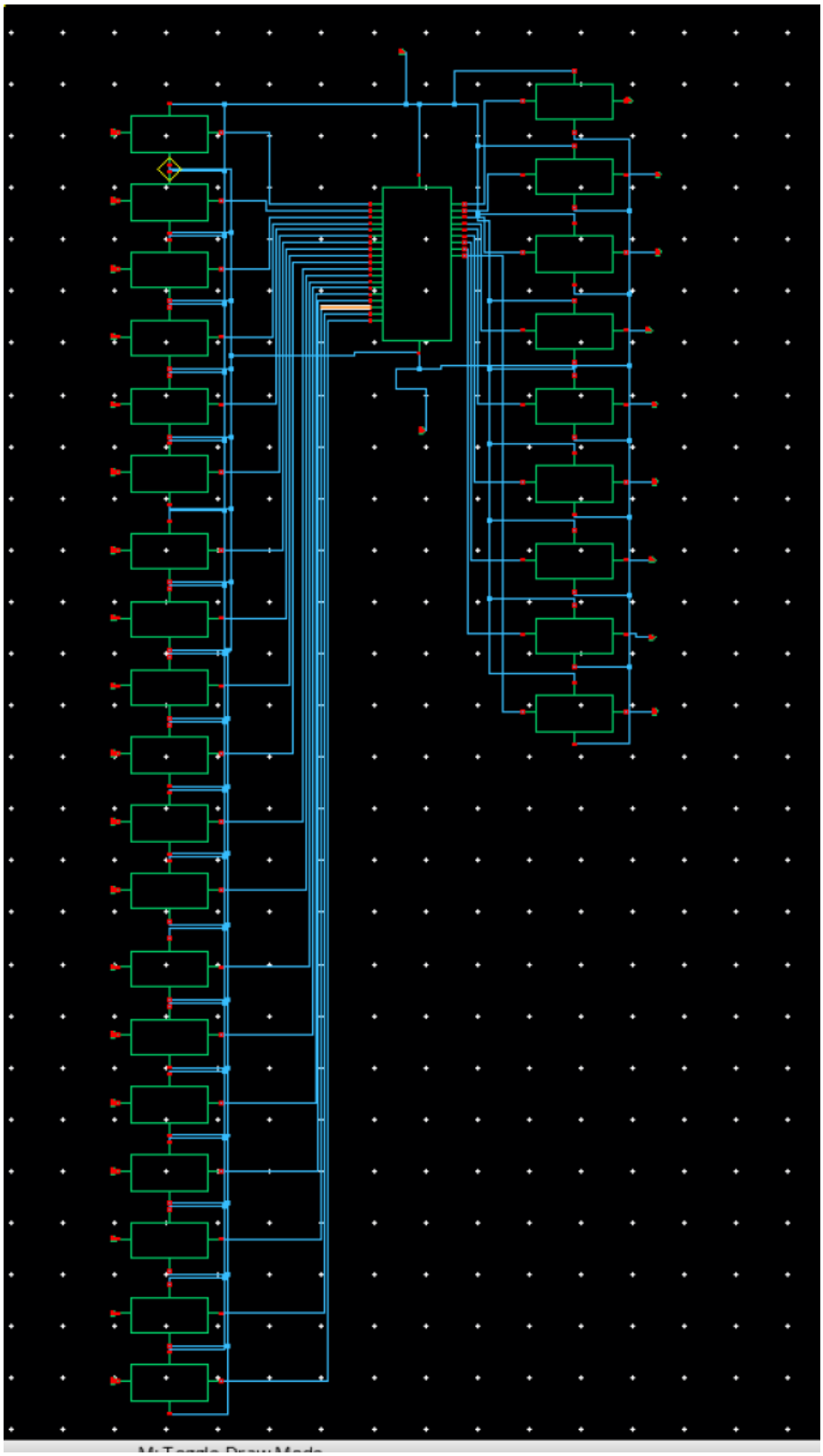
3.1.1 SCH

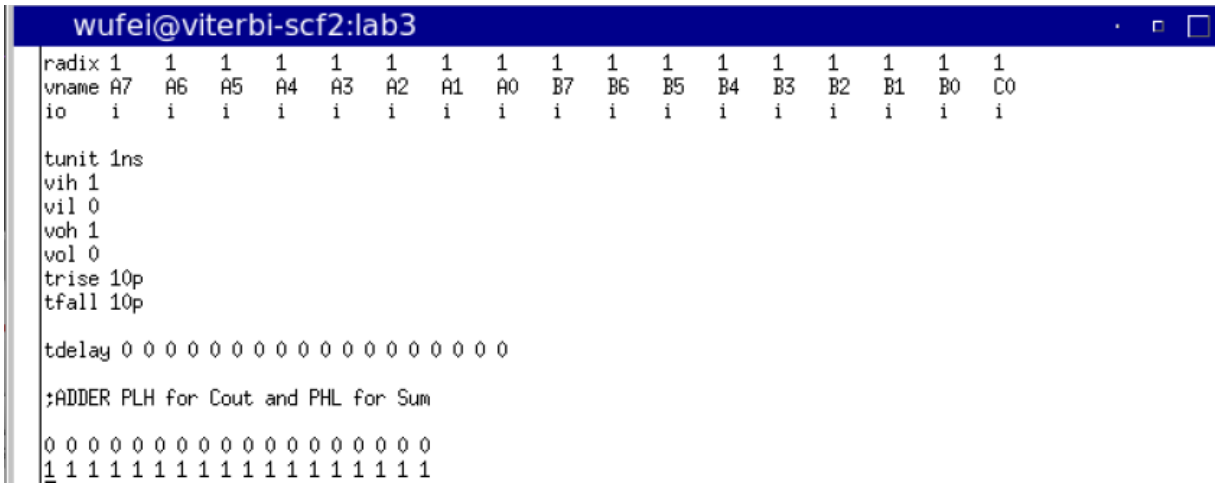


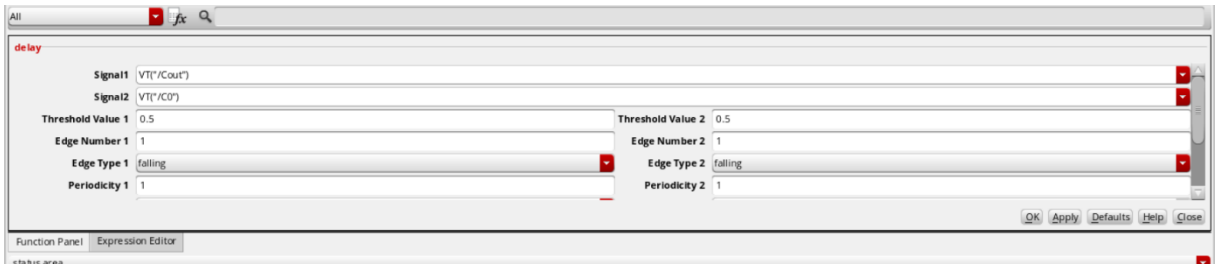

```
radix 1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1    1
vname A7   A6   A5   A4   A3   A2   A1   A0   B7   B6   B5   B4   B3   B2   B1   B0   C0
io    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i    i

tunit 1ns
vih 1
vil 0
voh 1
vol 0
trise 10p
tfall 10p

tdelay 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0

;ADDER PLH for Cout and PHL for Sum

0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 0
1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1

2 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
3 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0

4 1 0 1 0 1 0 1 0 0 1 0 1 0 1 0 1 0
```

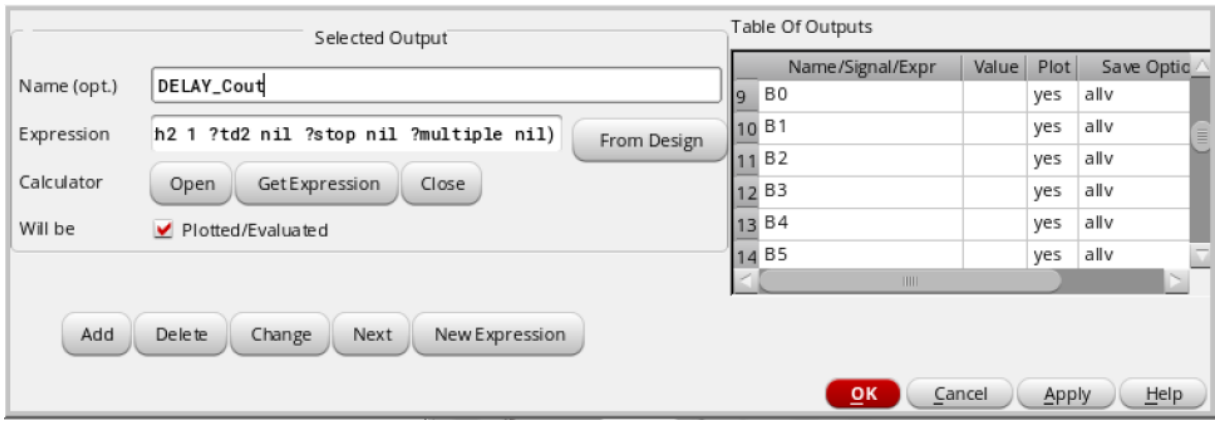

Virtuoso (R) Visualization & Analysis XL
File Edit View Graph Axis Trace Marker Measurements Tools Window Browser Help
demo_0 CSA_8bit schematic
Transient
/A3
/A4
/A5
/A6
/A7
/B1
/B2
/B3
/B4
/B5
/B6
/B7
/CI
/S0
/S1
/S2
/S3
/S4
/S5
/S6
/S7
/Cout
/VDD
/VSS
1.000000012
1.000000025
1.000000025
0.0
1.0
2.0
3.0
4.0
5.0
6.0
7.0
8.0
time (ns)

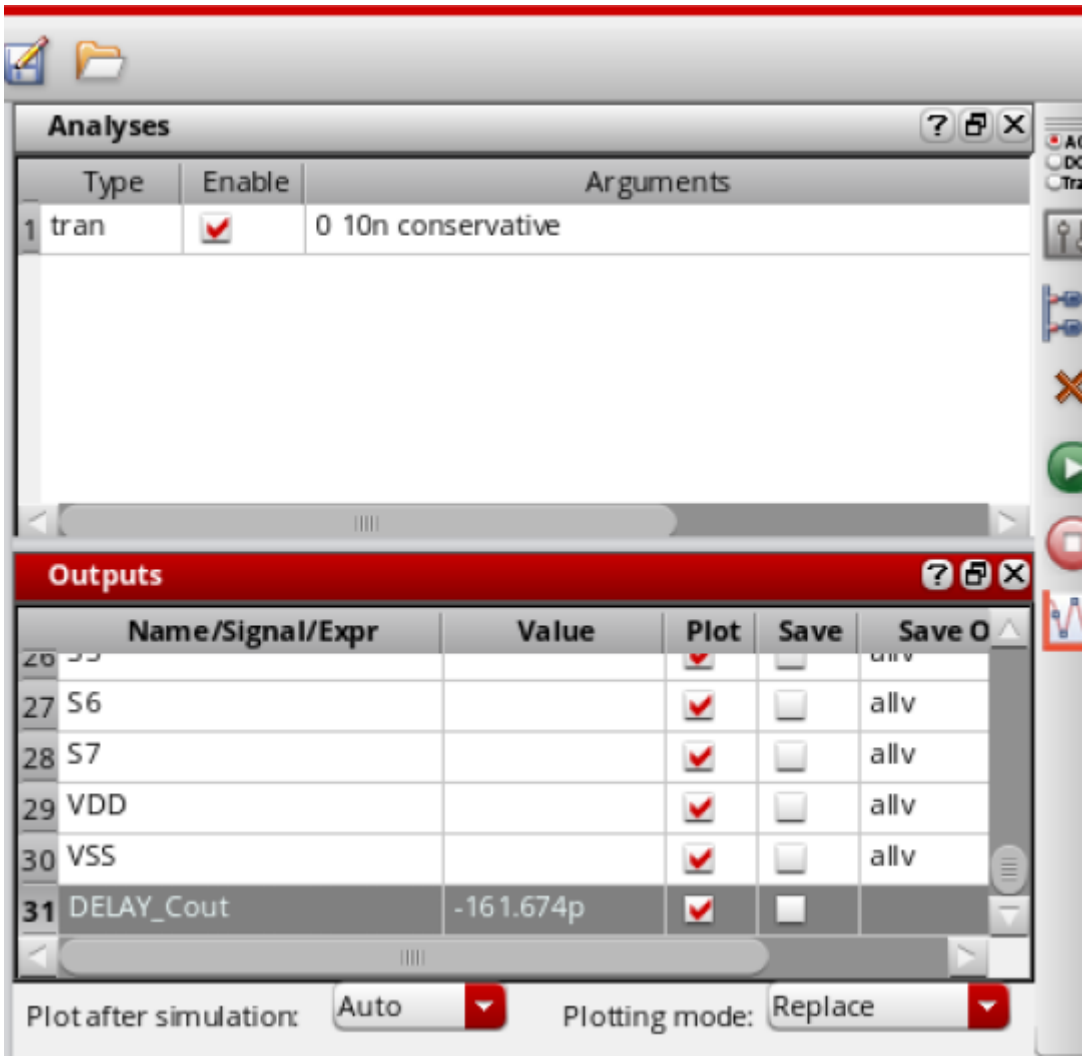
3.2 TEST



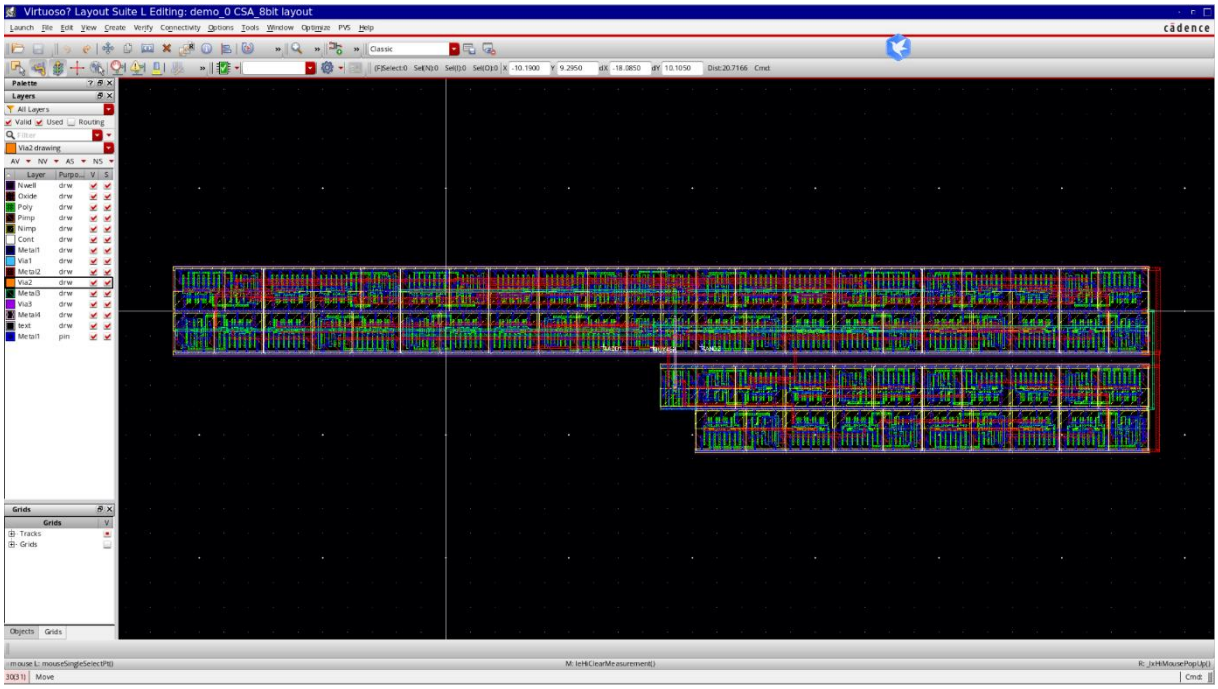

wufei@viterbi-scf2:lab3
radix 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1
vname A7 A6 A5 A4 A3 A2 A1 A0 B7 B6 B5 B4 B3 B2 B1 B0 C0
io i i i i i i i i i i i i i i i i i
tunit 1ns
vih 1
vil 0
voh 1
vol 0
trise 10p
tfall 10p
tdelay 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
;ADDER PLH for Cout and PHL for Sum
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1


All
delay
Signal1 VT("/Cout")
Signal2 VT("/C0")
Threshold Value 1 0.5
Edge Number 1 1
Edge Type 1 falling
Periodicity 1 1
Threshold Value 2 0.5
Edge Number 2 1
Edge Type 2 falling
Periodicity 2 1
OK Apply Defaults Help Close
Function Panel Expression Editor


Selected Output
Name (opt.) DELAY_Cout
Expression h2 1 ?td2 nil ?stop nil ?multiple nil)
From Design
Calculator Open Get Expression Close
Will be Plotted/Evaluated
Table Of Outputs
Name/Signal/Expr Value Plot Save Optic
9 B0 yes allv
10 B1 yes allv
11 B2 yes allv
12 B3 yes allv
13 B4 yes allv
14 B5 yes allv
Add Delete Change Next New Expression
OK Cancel Apply Help


Analyses
Type
Enable
Arguments
1
tran
0 10n conservative
Outputs
Name/Signal/Expr
Value
Plot
Save
Save O
27
S6
allv
28
S7
allv
29
VDD
allv
30
VSS
allv
31
DELAY_Cout
-161.674p
Plot after simulation:
Auto
Plotting mode:
Replace

3.3 LAYOUT




```
#################################################################
#                                                               #
# Run Result              : MATCH                               #
#                                                               #
# Run Summary             : [INFO]  ERC Results: Empty          #
#                           : [INFO]  Extraction Clean          #
#                                                               #
# ERC Summary File        : CSA_8bit.sum                        #
# Extraction Report File  : CSA_8bit.rep                        #
# Comparison Report File  : CSA_8bit.rep.cls                    #
#                                                               #
#################################################################
```

```
Total CPU Time                  : 2(s)
Total Real Time                 : 2(s)
Peak Memory Used                : 114(M)
Total Original Geometry         : 3321(5105)
Total DRC RuleChecks            : 562
Total DRC Results               : 0 (0)
Summary can be found in file CSA_8bit.sum
ASCII report database is /home/viterbi/03/wufei/work_gpdk045/DRC/CSA_8bit.drc_error
Checking in all SoftShare licenses.
```