Cadence Virtuoso Tutorial

version 6.2

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Cadence Virtuoso Setup

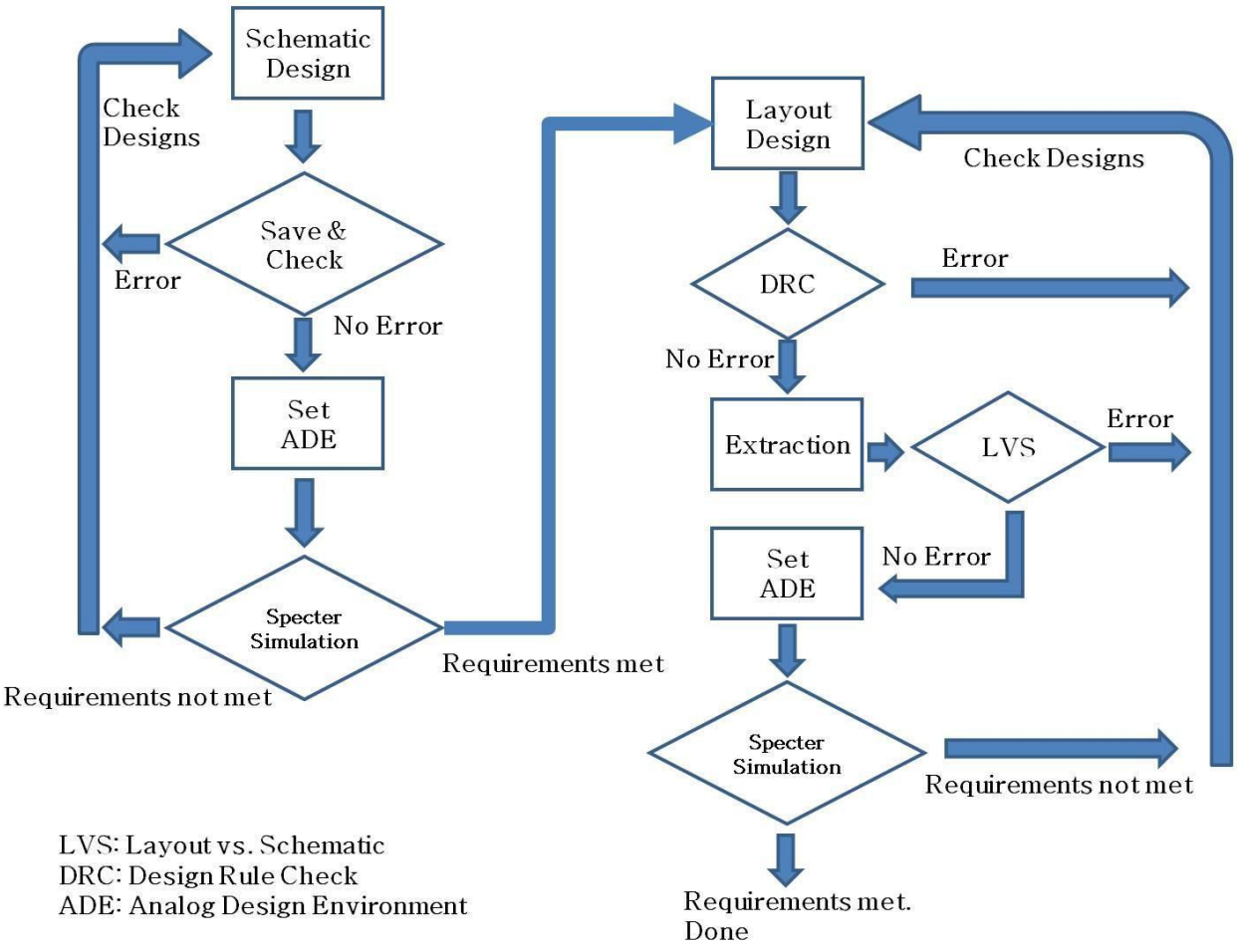
A. Please use the steps (in the Cadence Virtuoso Setup Guide, which is separately provided) to be able to run Virtuoso on your account.

B. Type **virtuoso &** at the command prompt. The “&” is for background execution, it is useful when we want to keep the command prompt in the same console.

Basic Design Flow

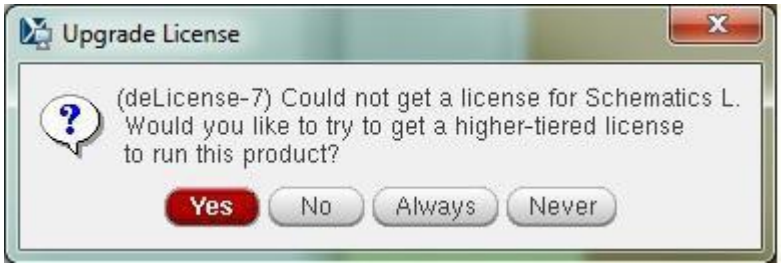
1. Overall design flow

Following flow chart shows overall design flow.

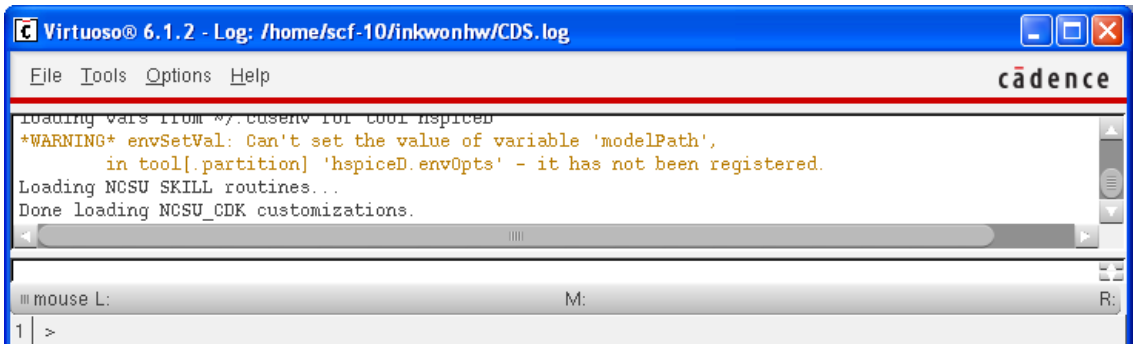


2. Create Library

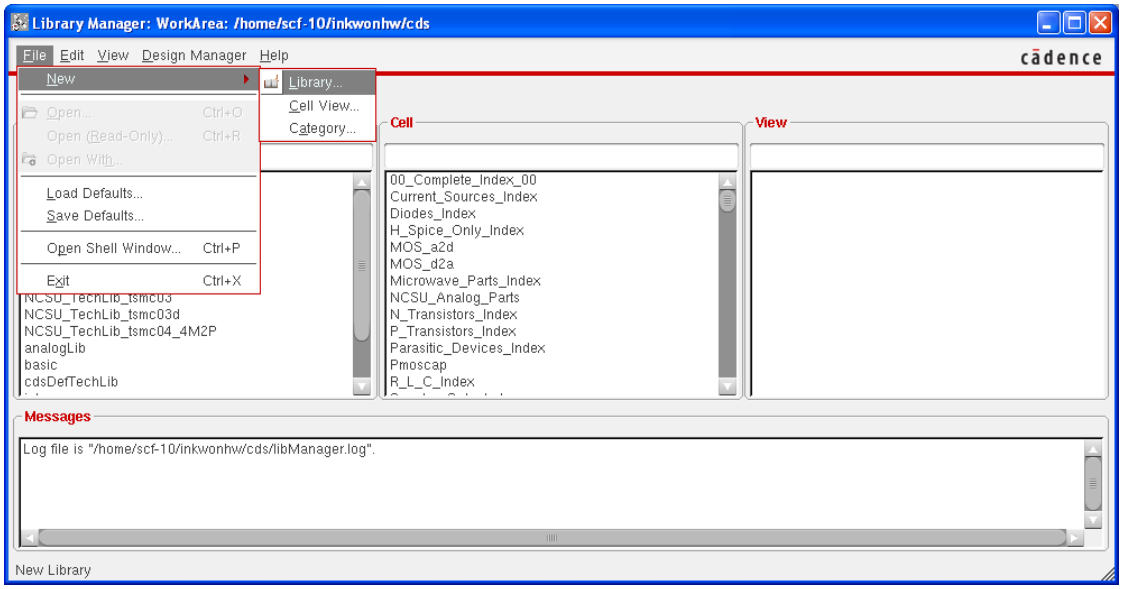
For prompt to access for higher tiered license, click “always”.



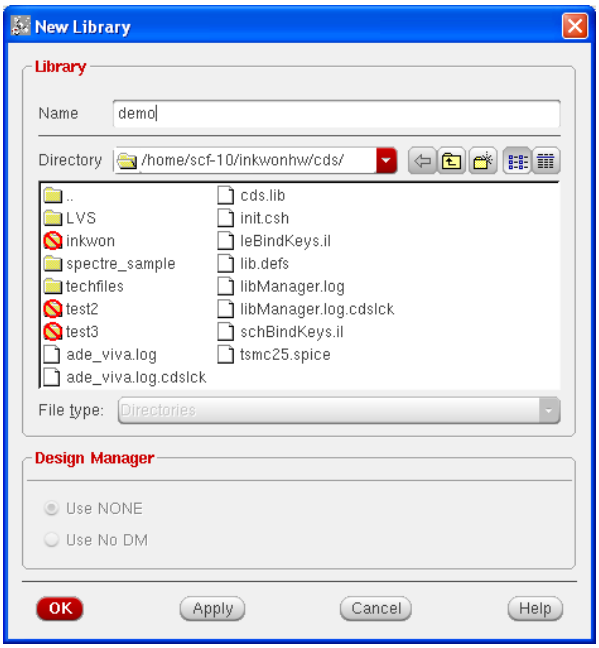
A. Tools → Library Manager

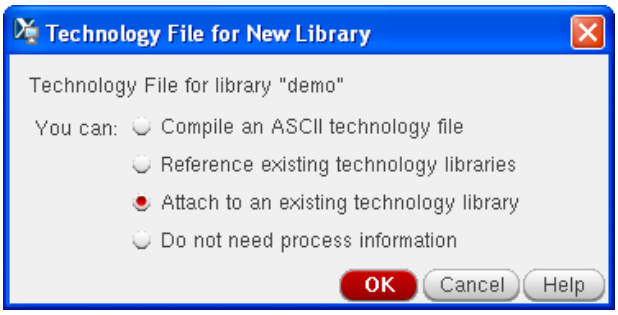


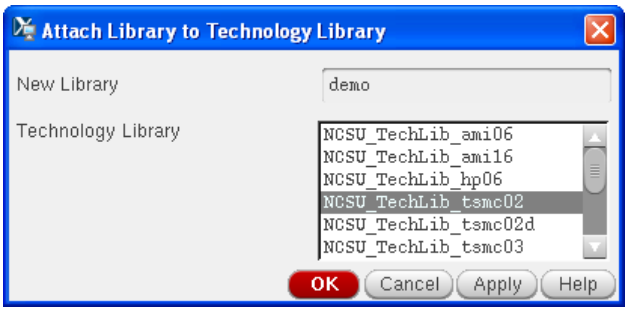
B. File → New → Library



C. Give a name and attach it to a technology library



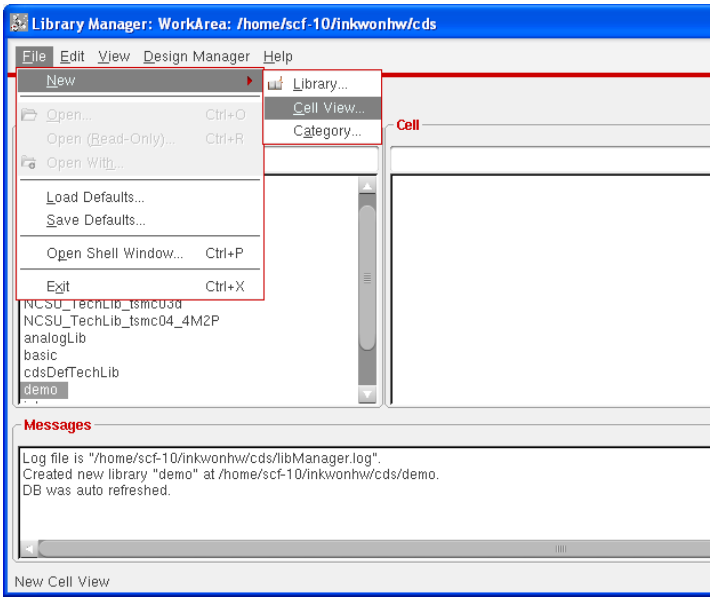


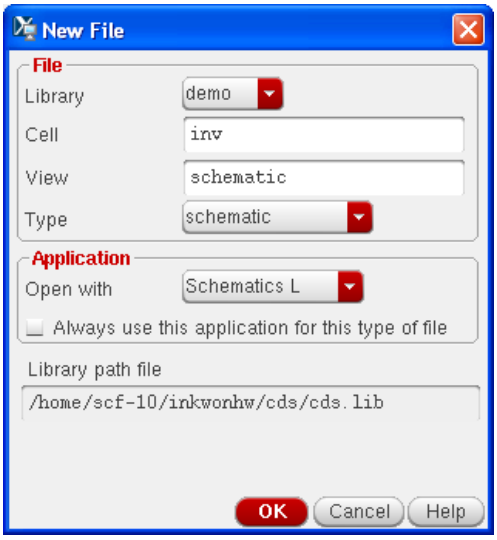


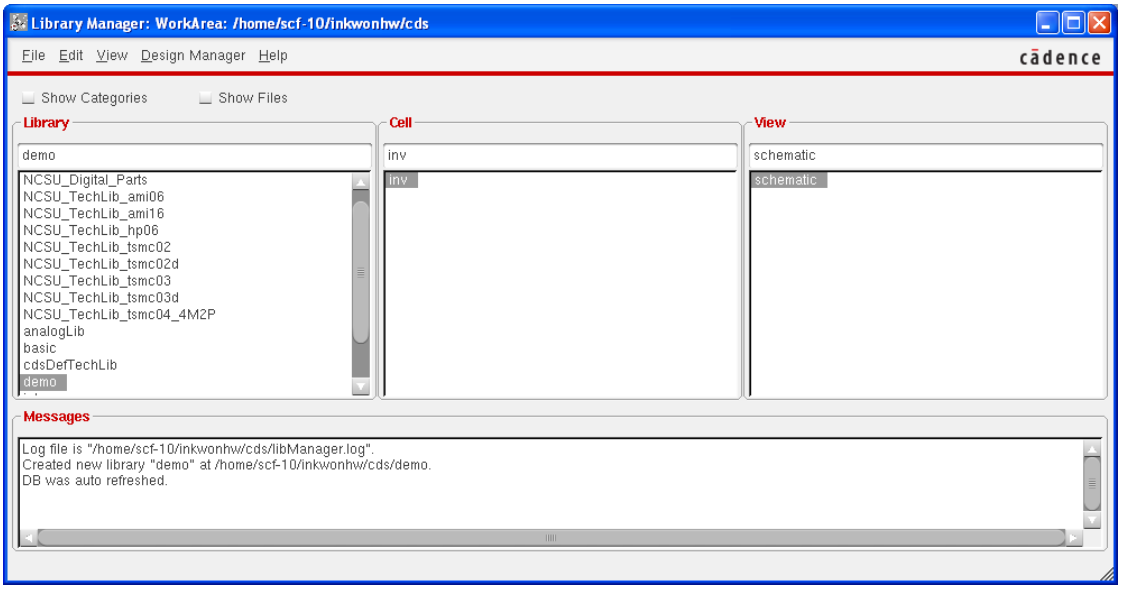
3. Schematic

A. Create a cell view

select the library just created, File->new





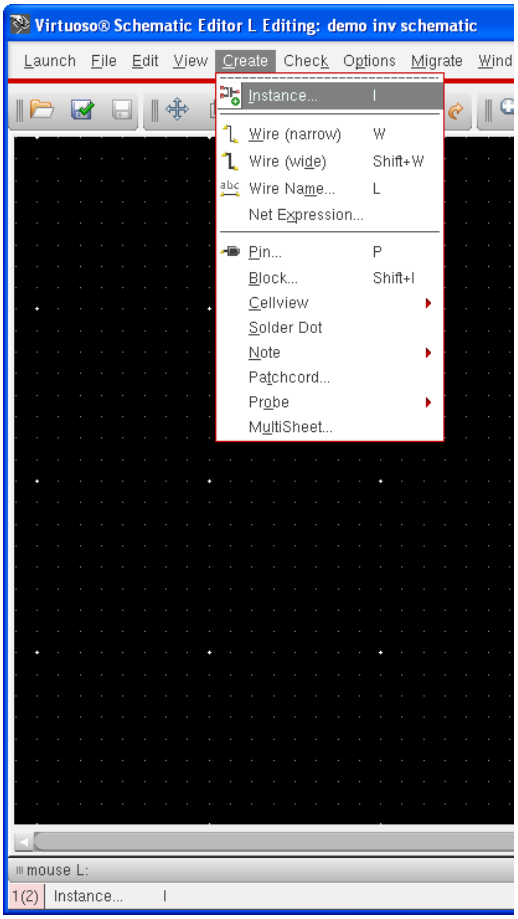


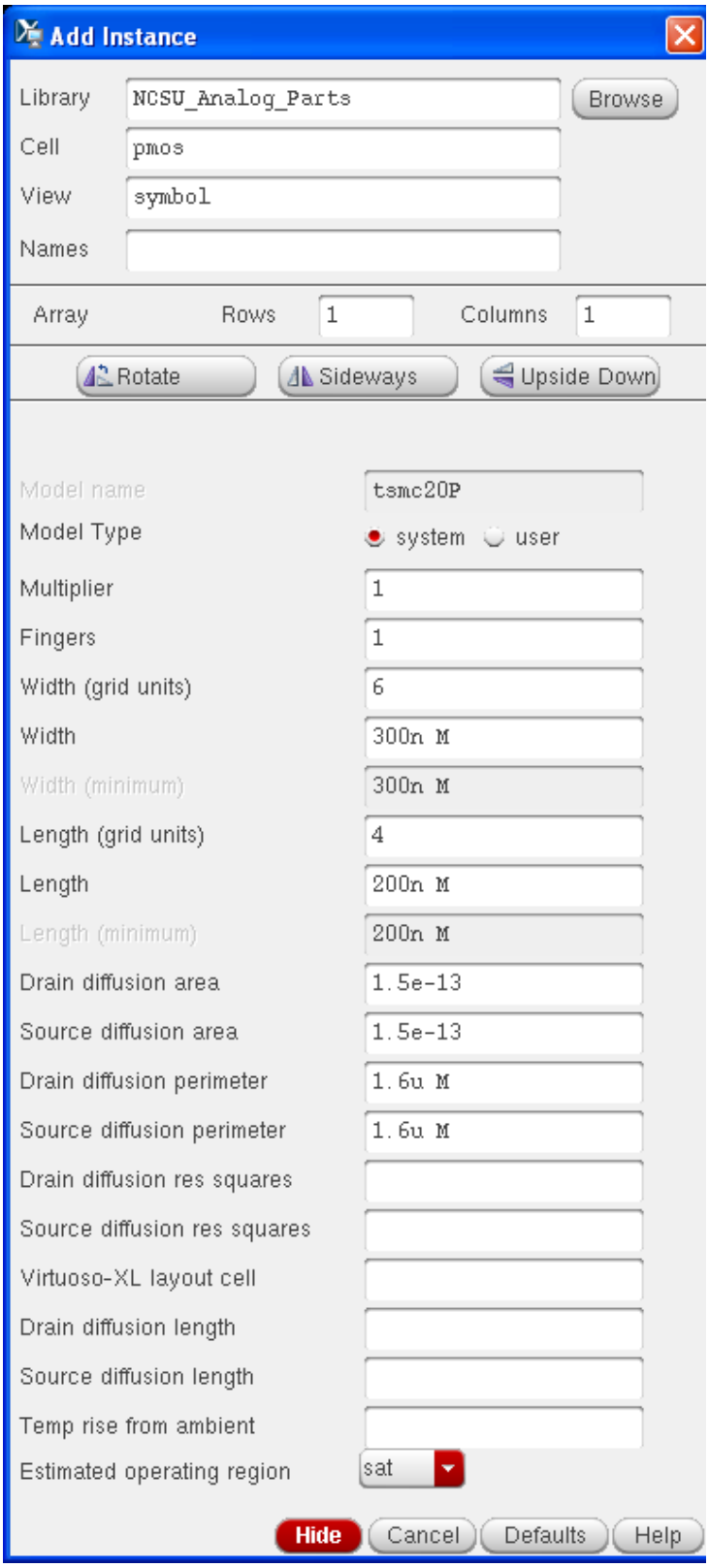
B. Draw a schematic

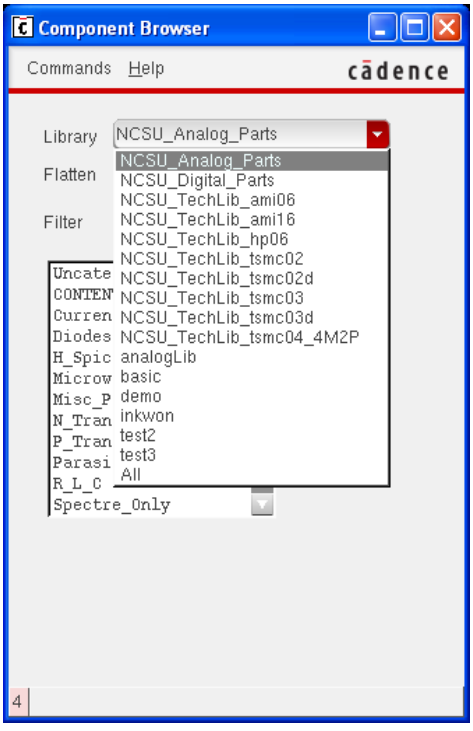
i. Add instances – pmos

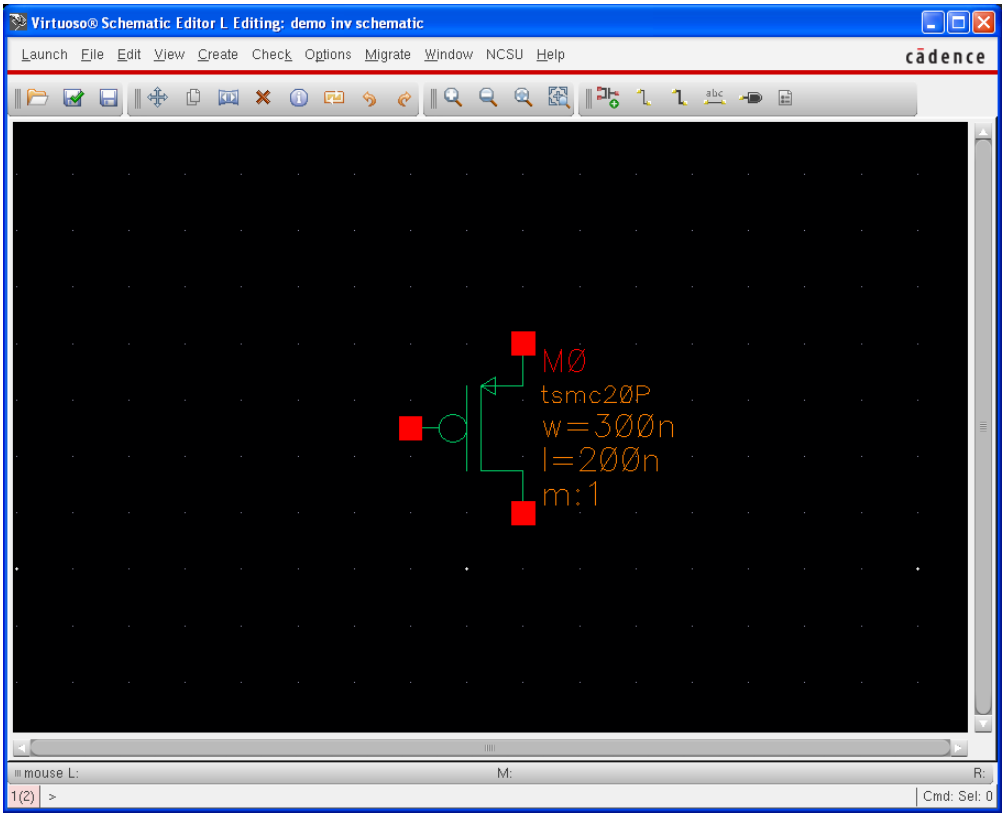
You can modify Width of transistors. Don‟t modify length unless you have a special purpose.

You should select a NCSU_Analog_Parts library.

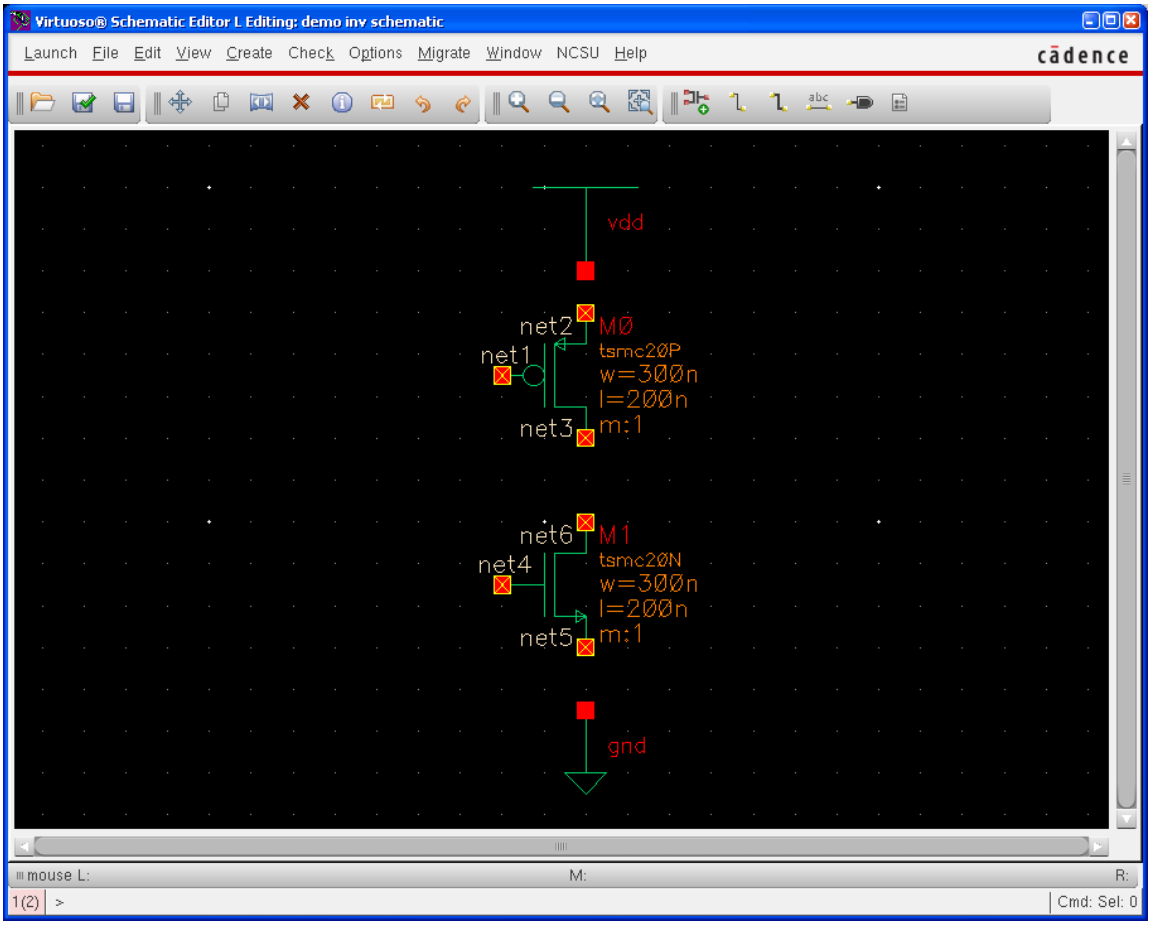




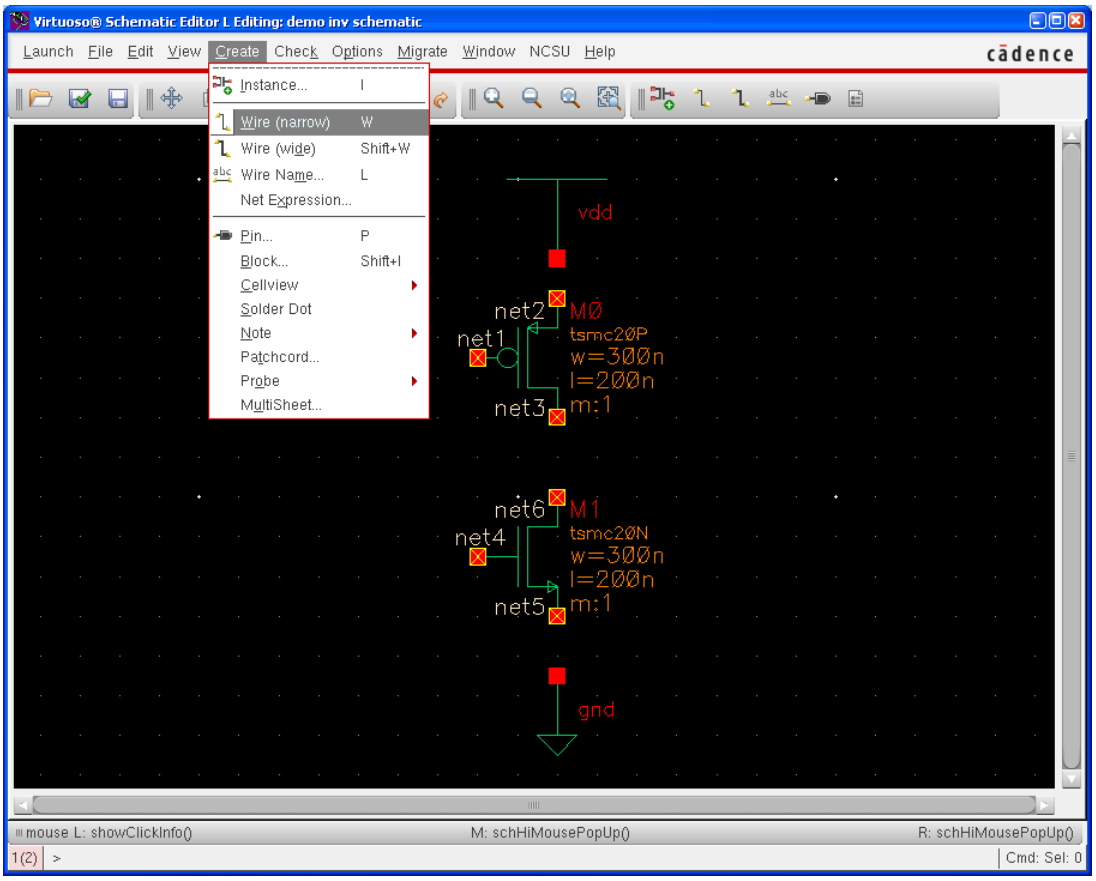


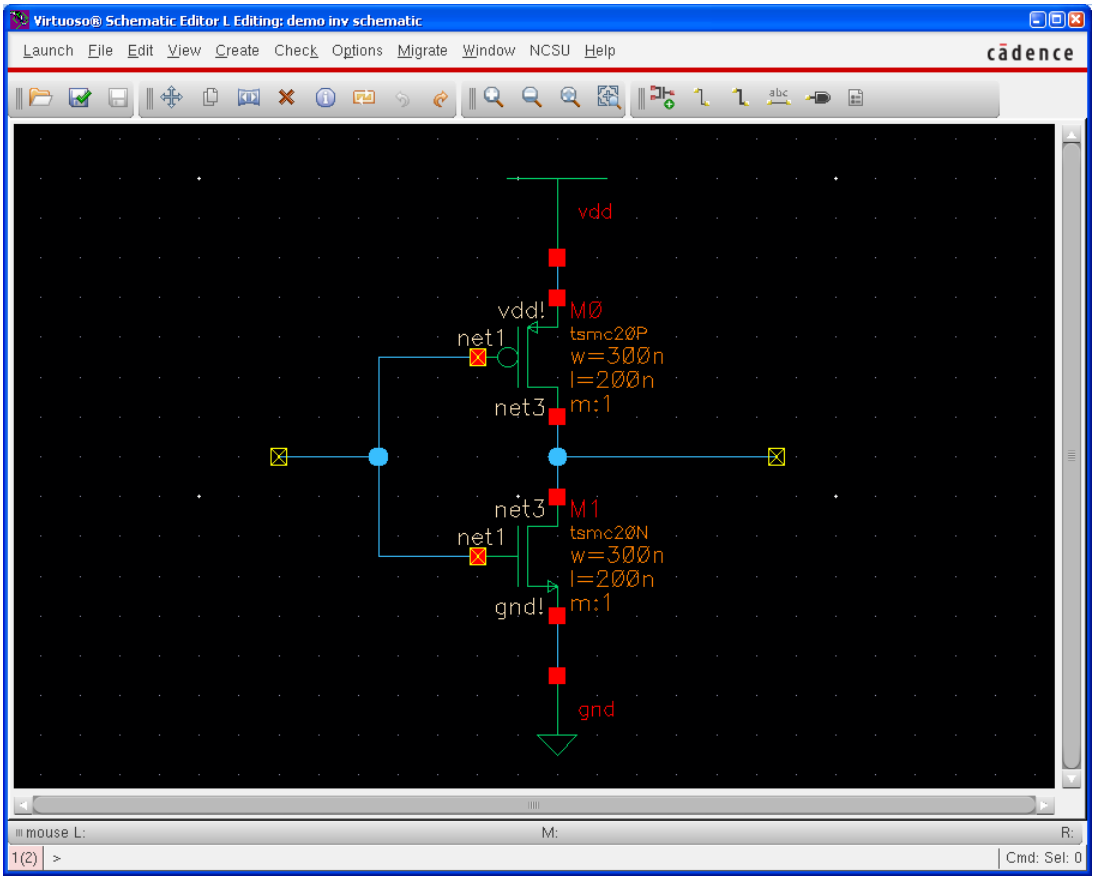


ii. Add instances – nmos, vdd, and gnd

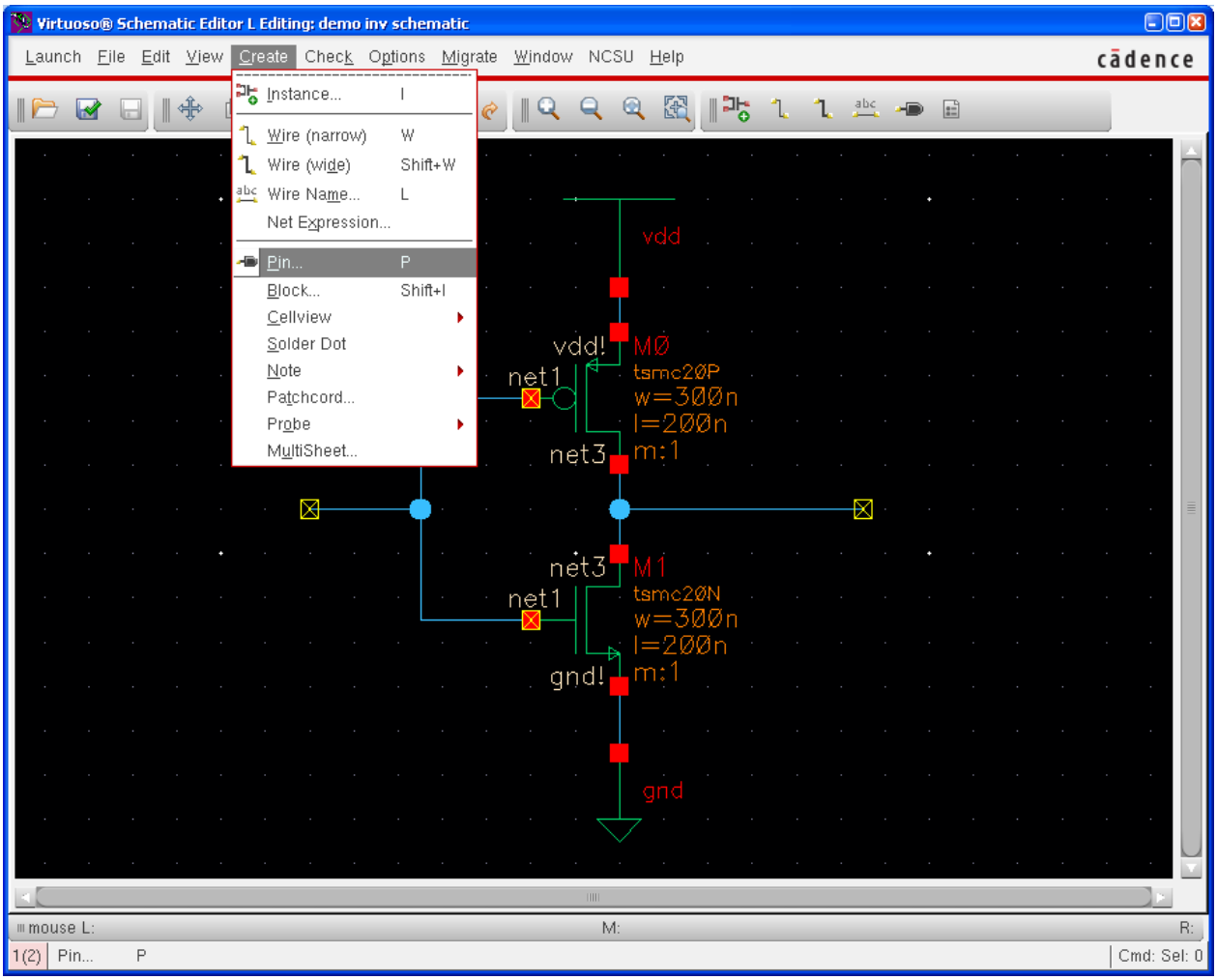


iii. Add wires: Create → Wire

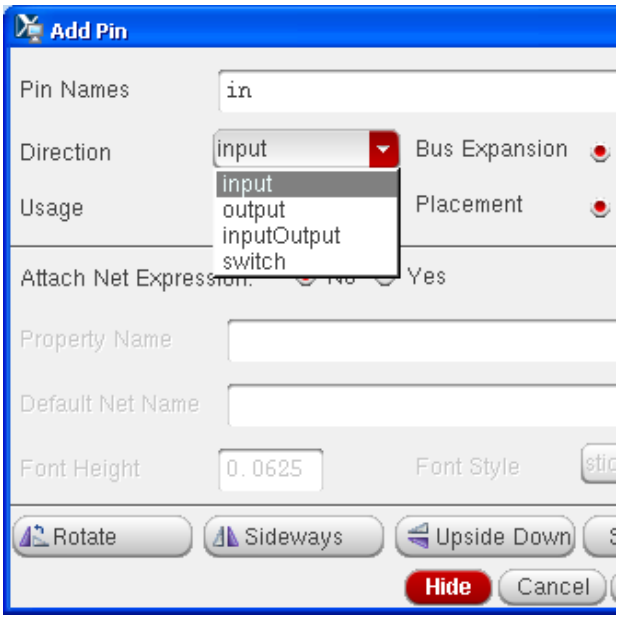


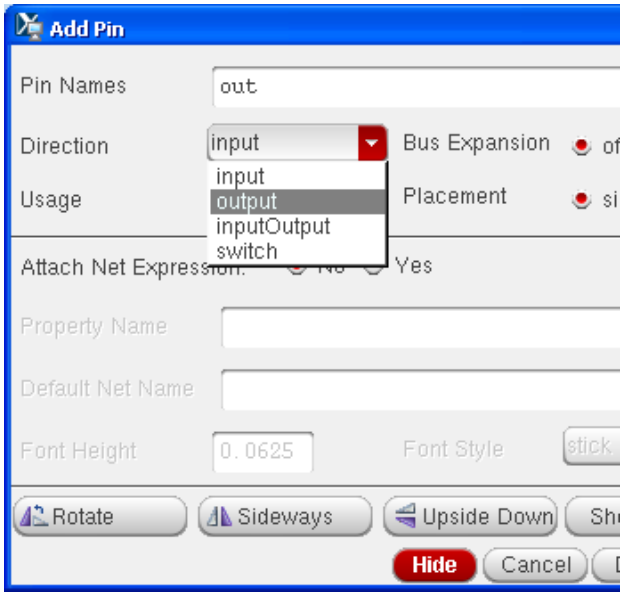


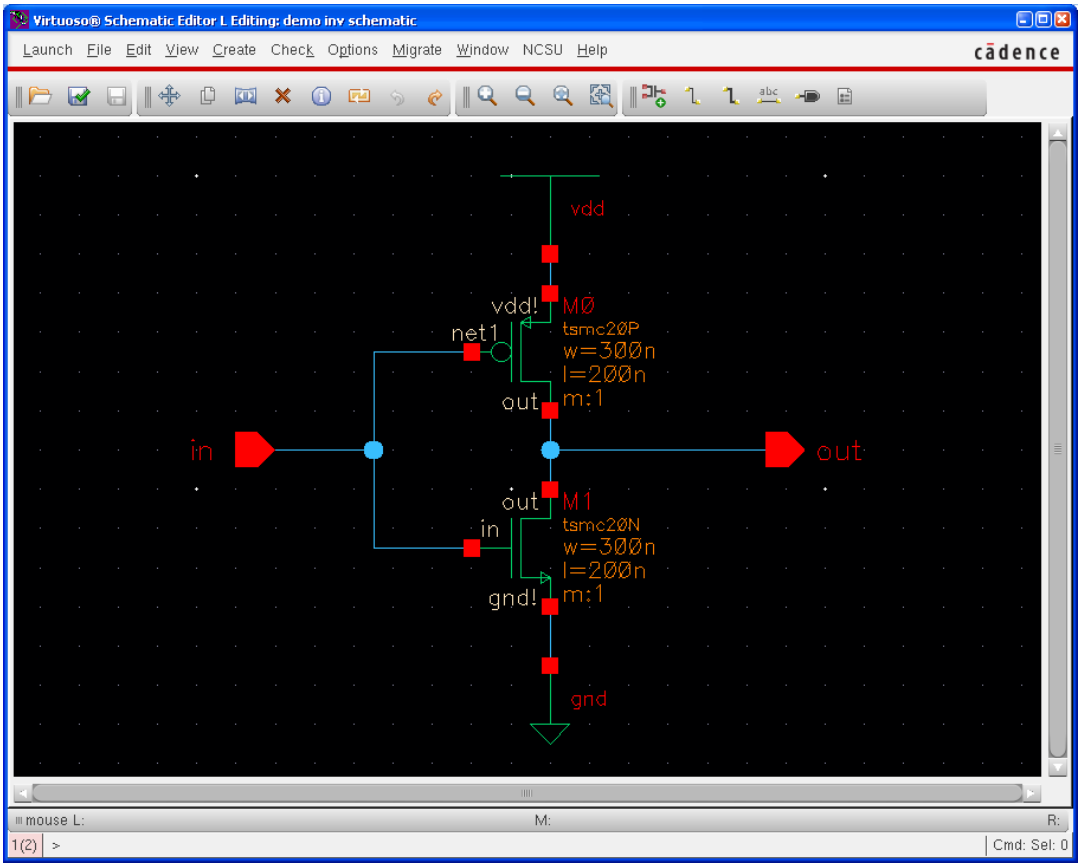
iv. Add pins: Create → Pin



We have for different types of direction. For schematics, we only use two types, input and output. InputOutput type is for supply changes, and it is necessary only for layout. We will discuss about this later.





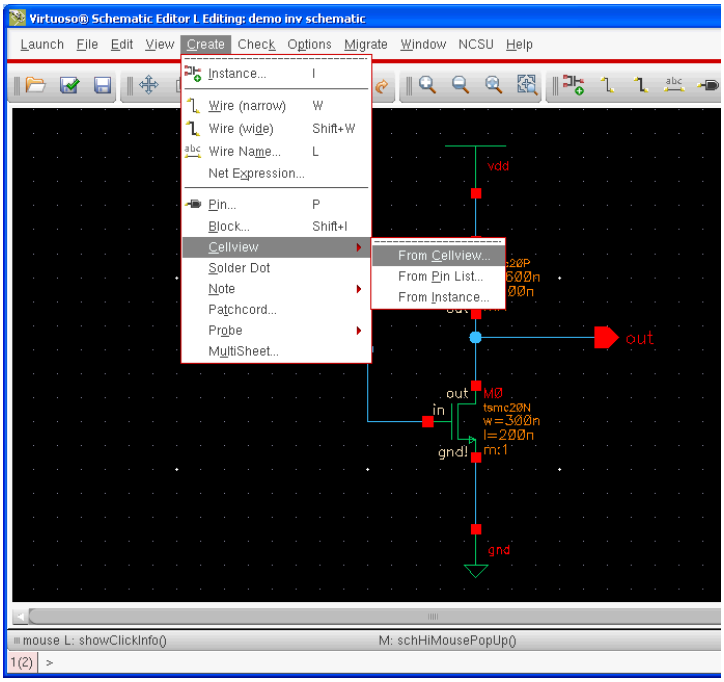


Check and save →  to make sure there are no errors.

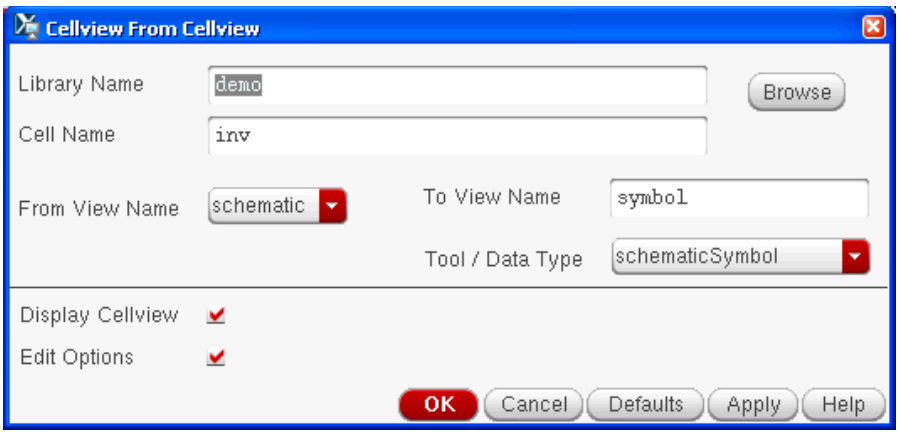
Now, we completed a schematic design.

C. Create a symbol (Optional)

For hierarchical design, we may need to make symbols of designed circuits.



Create → CellView → From Cellview


Cellview From Cellview
Library Name
demo
Browse
Cell Name
inv
From View Name
schematic
To View Name
symbol
Tool / Data Type
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Display Cellview
Edit Options
OK
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Defaults
Apply
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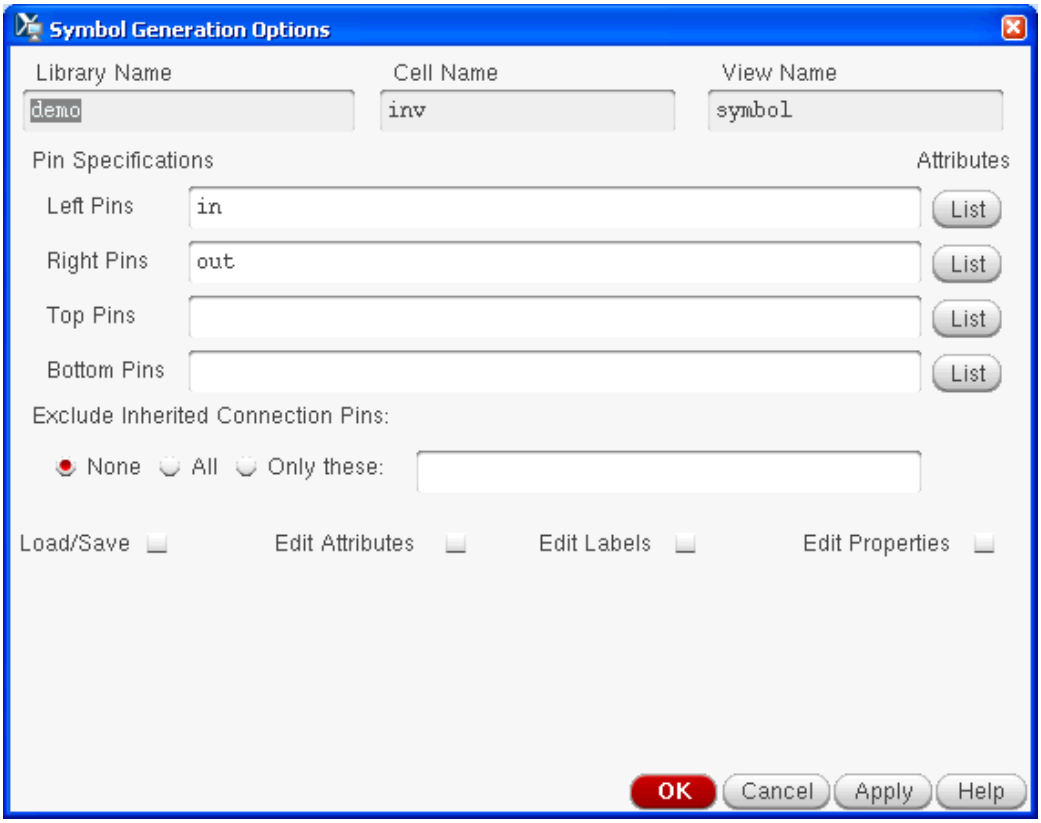
Symbol Generation Options
Library Name
Cell Name
View Name
demo
inv
symbol
Pin Specifications
Attributes
Left Pins
in
List
Right Pins
out
List
Top Pins
List
Bottom Pins
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Exclude Inherited Connection Pins:
None
All
Only these:
Load/Save
Edit Attributes
Edit Labels
Edit Properties
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Cancel
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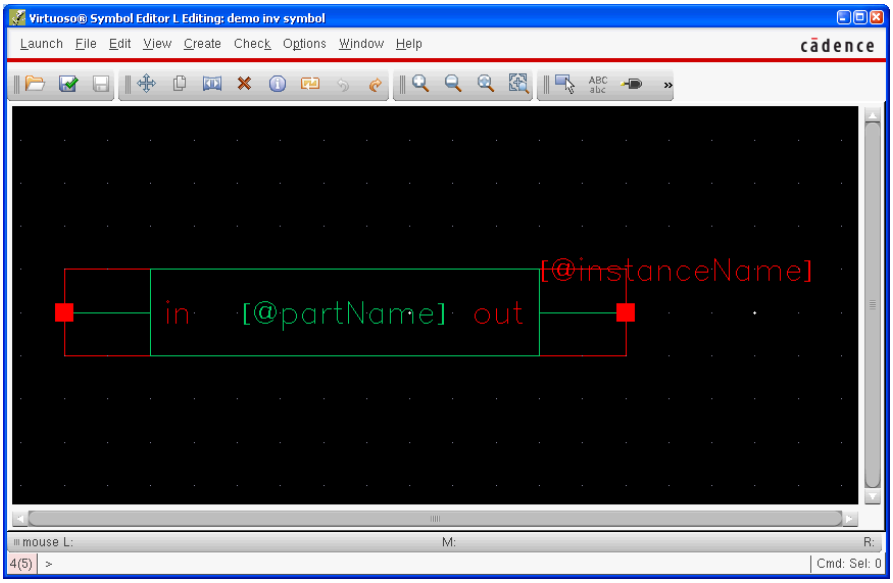
Help


Virtuoso® Symbol Editor L Editing: demo inv symbol
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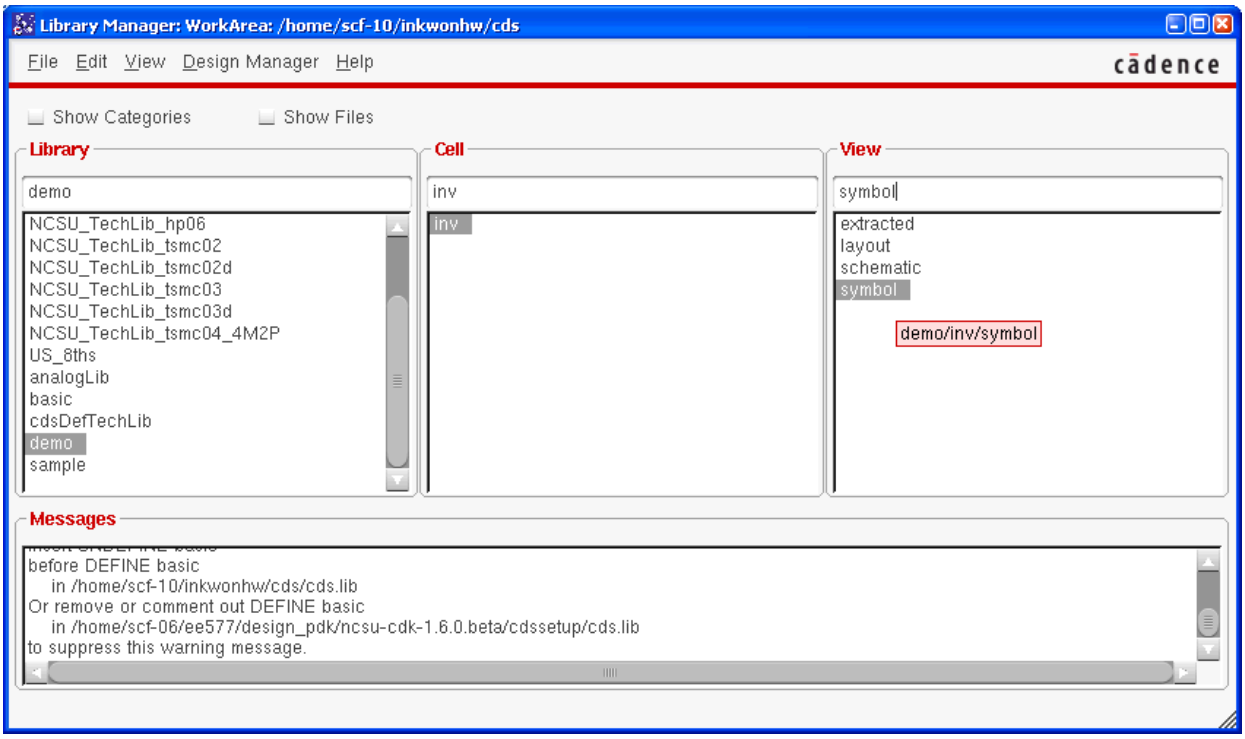


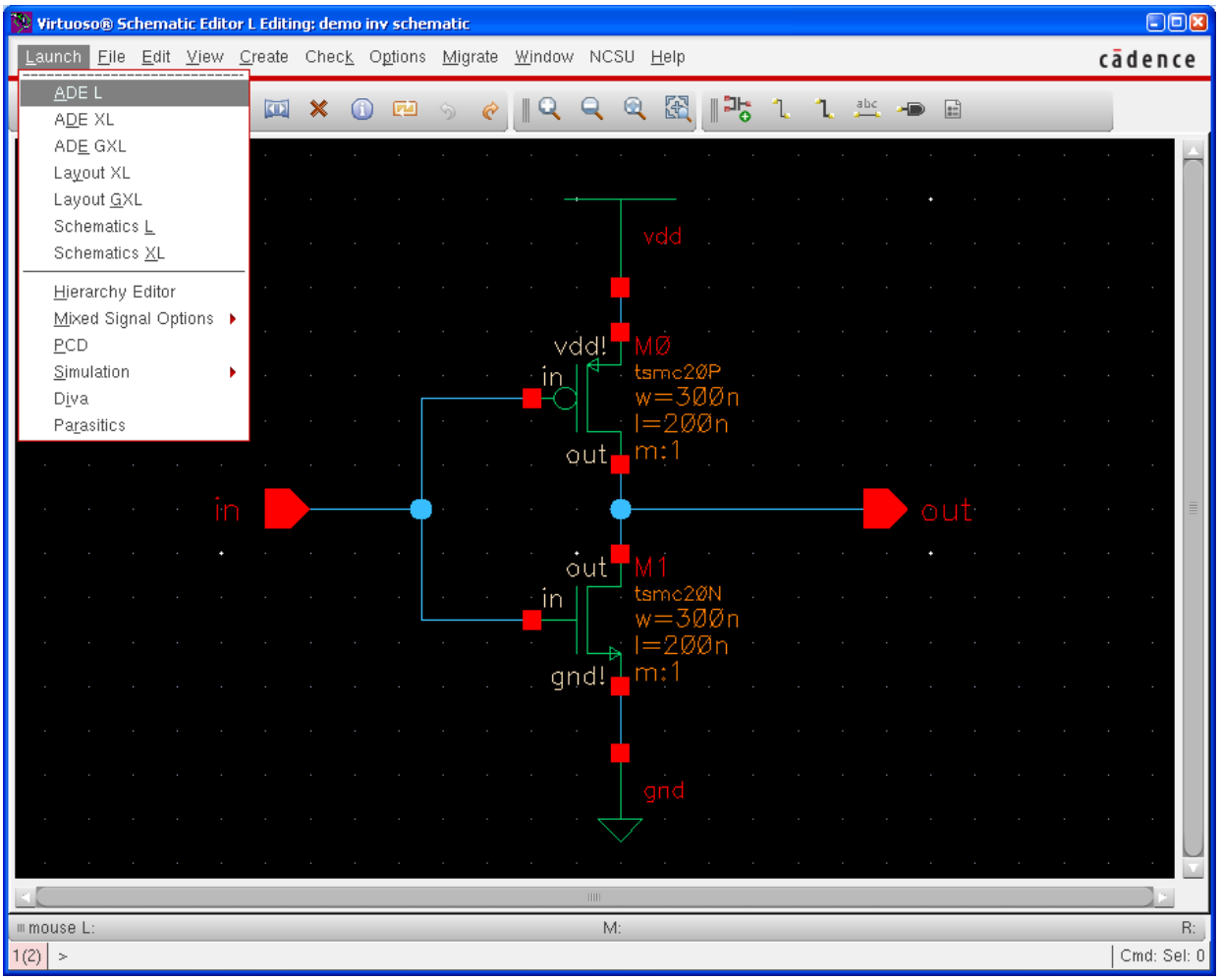
Remember that when you use more than one symbol in schematic, they all will have common Vdd and Gnd even if there are one Gnd and Vdd for each symbol (in the original design). To design with symbols in layout, you should make sure that all of the Vdd and Gnds are connected.

4. Run Spectre simulation (Transient analysis)

We will run spectre simulation. This section is for **both** schematics and layouts. I will show an example for a schematic. You can do the same thing for a layout.

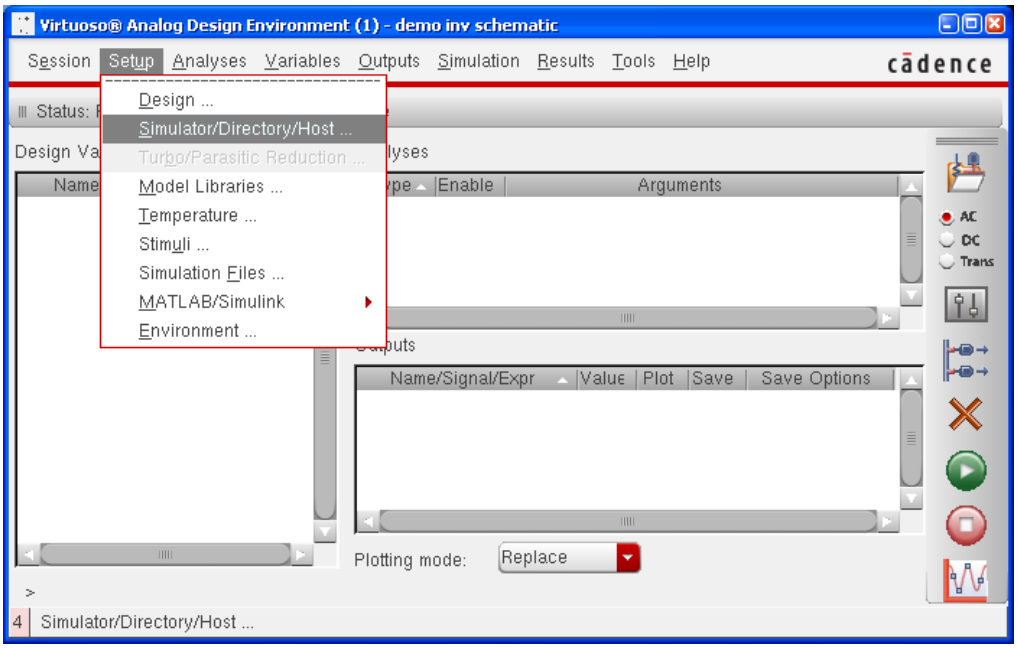
A. Launch ADE (Analog Design Environment) L

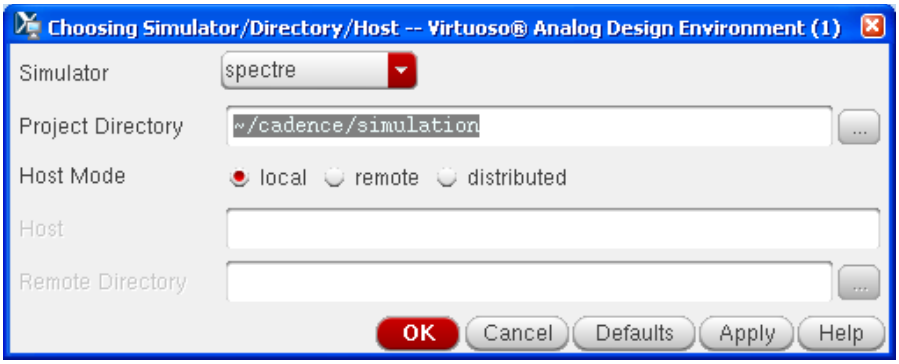
Launch → ADE L



B. Basic setup

Check if your simulator is spectre. You can modify project directory.

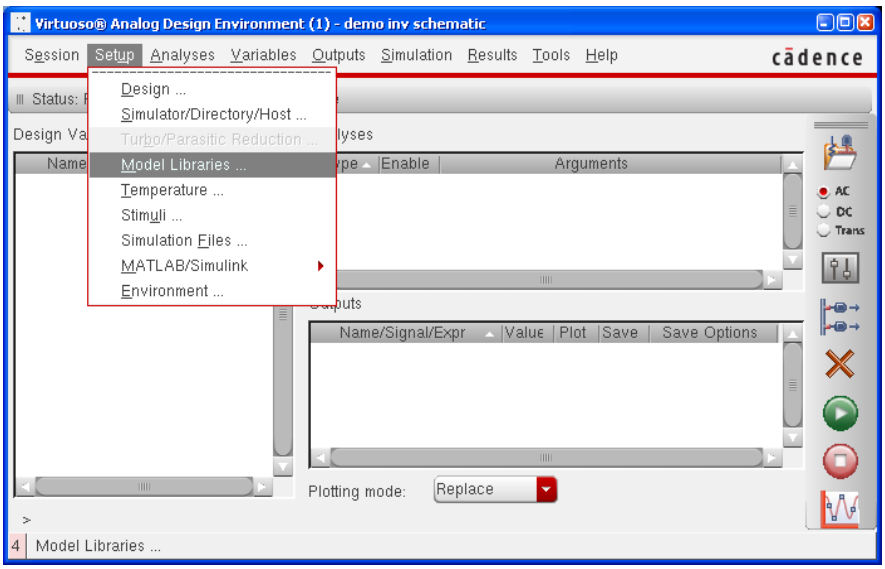


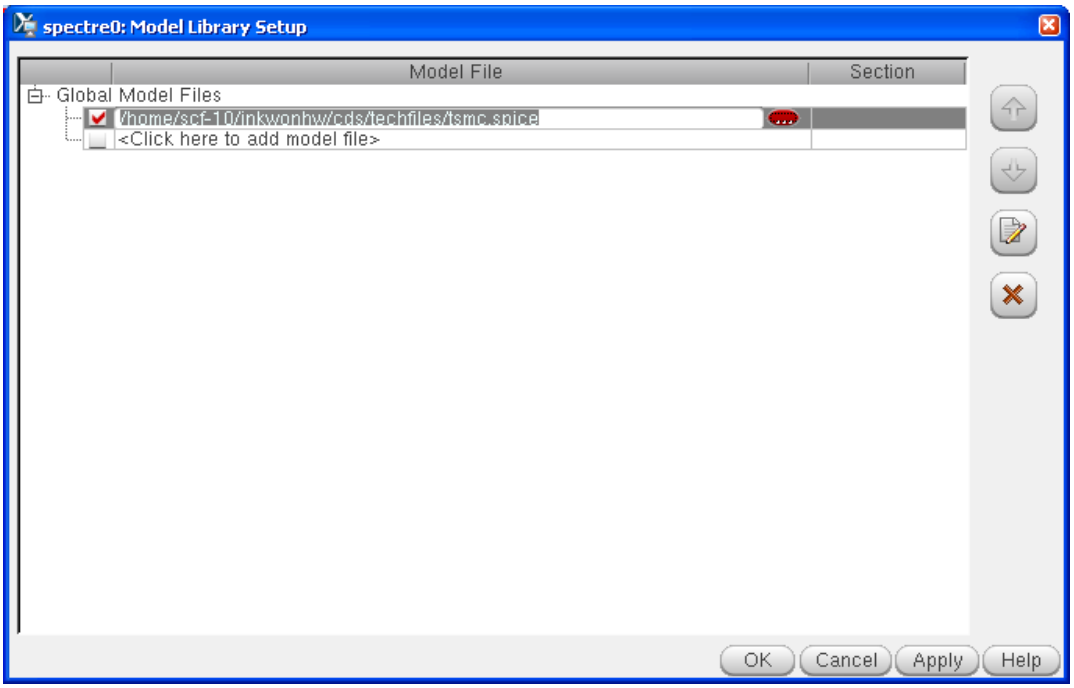


C. Model Libraries

You can download a library file at the DEN blackboard.

Put the tech file under /home/scf-10/your-user-name/cds/techfiles/

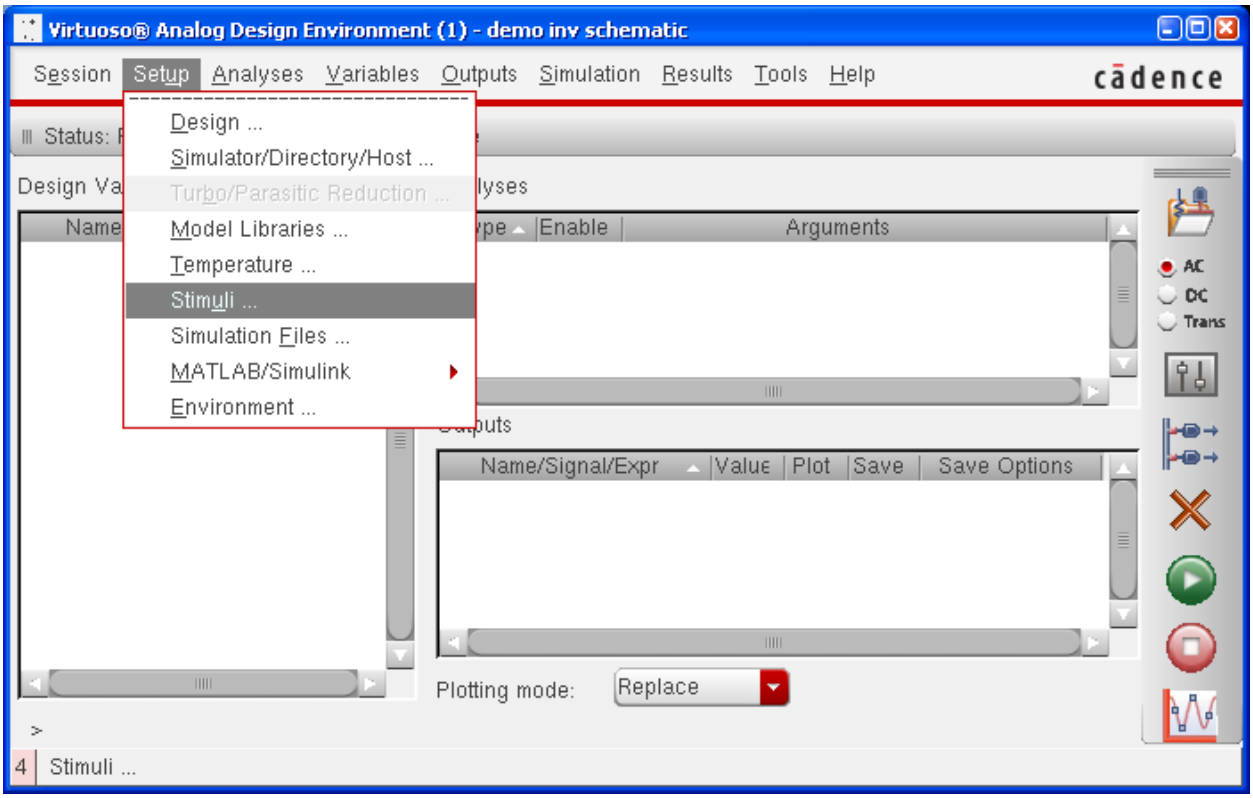

Virtuoso® Analog Design Environment (1) - demo inv schematic
Session
Setup
Analyses
Variables
Outputs
Simulation
Results
Tools
Help
cadence
Design ...
Simulator/Directory/Host ...
Turbo/Parasitic Reduction ...
Model Libraries ...
Temperature ...
Stimuli ...
Simulation Files ...
MATLAB/Simulink
Environment ...
Enable
Arguments
AC
DC
Trans
Name/Signal/Expr
Value
Plot
Save
Save Options
Plotting mode:
Replace
4
Model Libraries ...



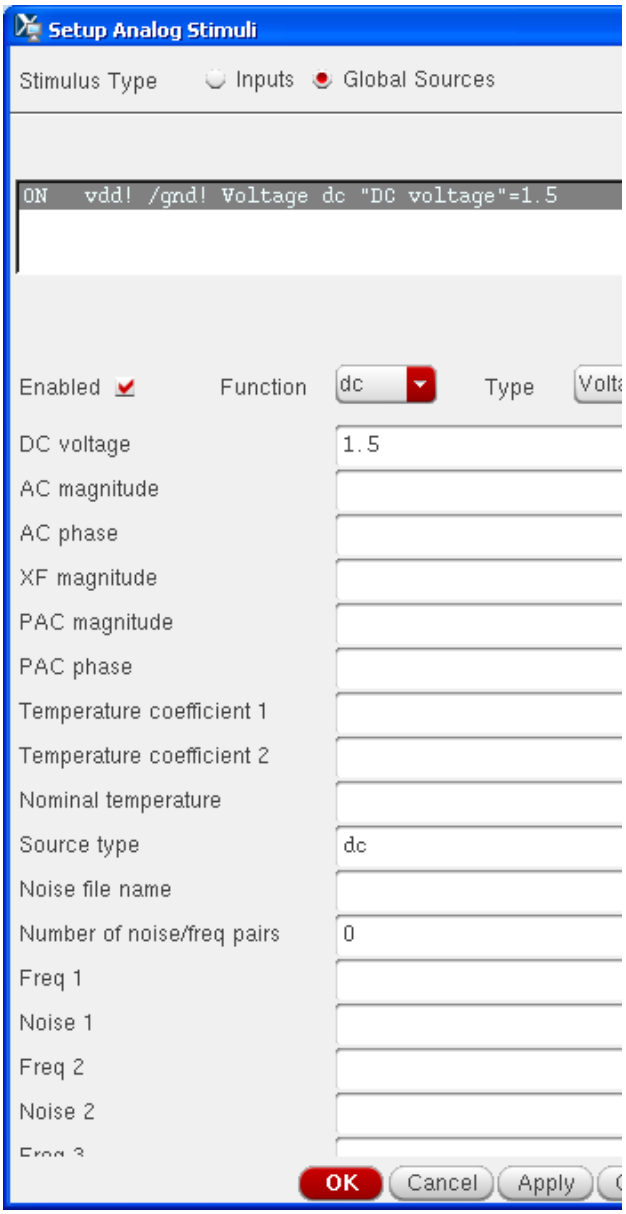
Please only use the provided tsmc file because some tsmc files does not work correctly.

D. Stimuli

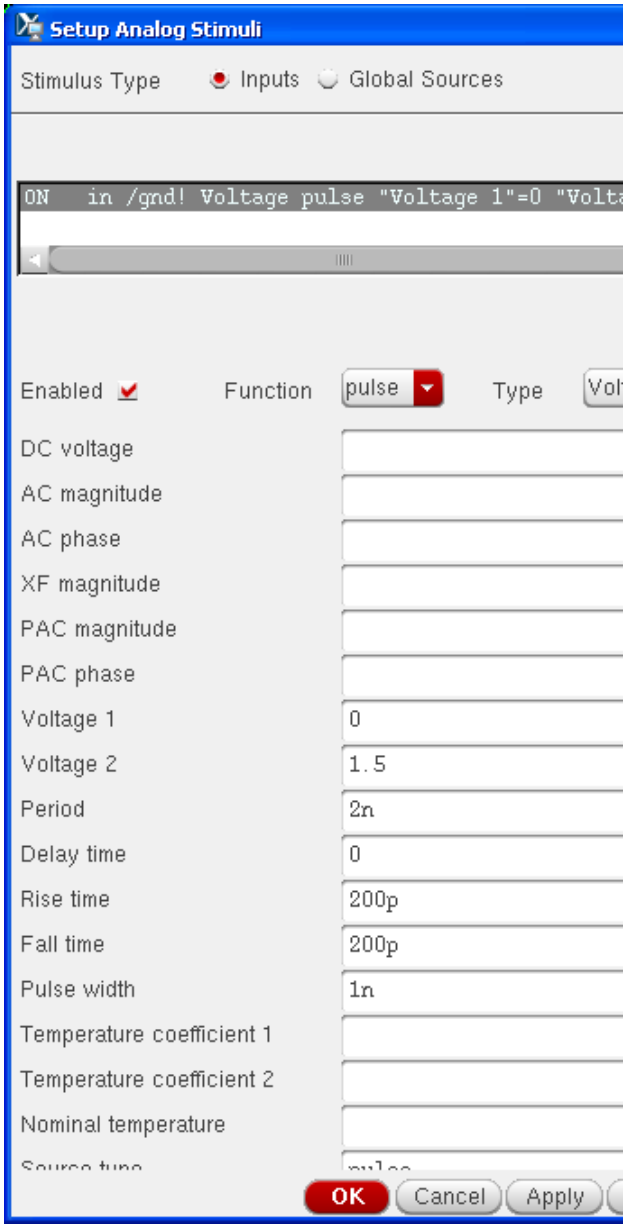
Define input signals include supply nets (for layout, vdd! and gnd! are under inputs and both should be enabled.)



Global sources



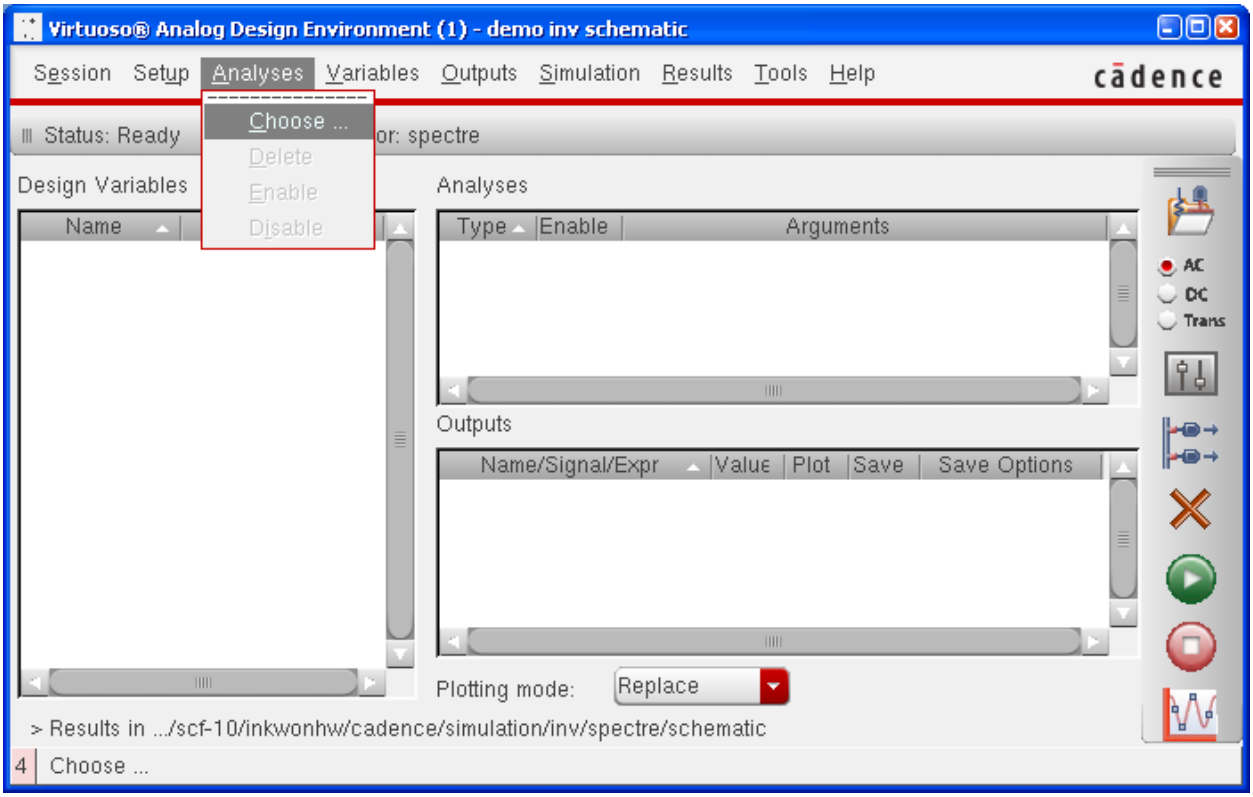
Input (change)



Remember to check Enabled button and then press OK or APPLY otherwise you will lose the configured numbers.

E. Choose a type of analysis - transient

You can choose „dc“ if you want to do dc analysis



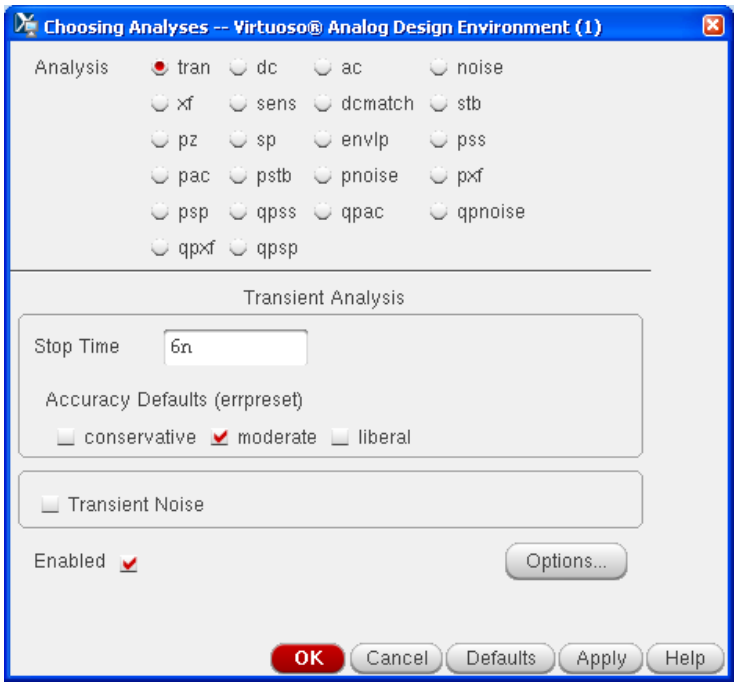
A. Choose tran

B. Give Stop time which means how long you want to simulate

C. Select moderate as accuracy defaults

D. Do not check Transient Noise

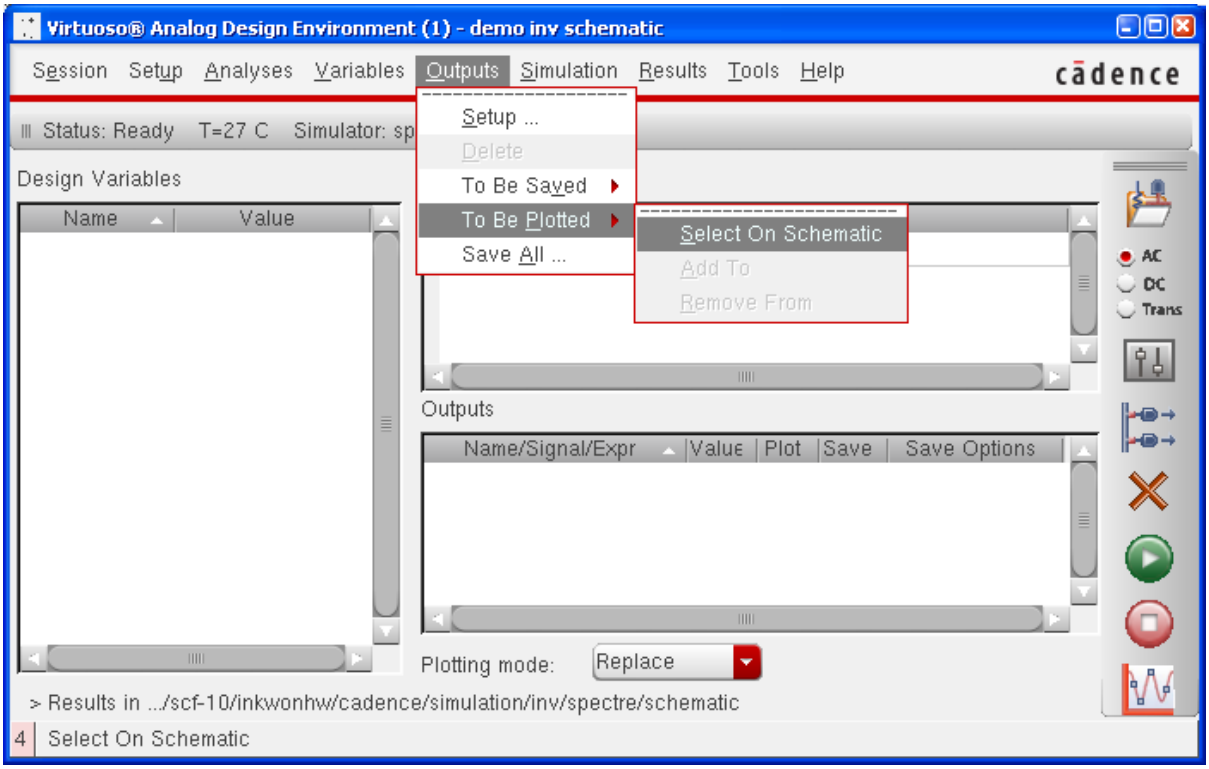
E. Check Enabled



F. Select signals to plot

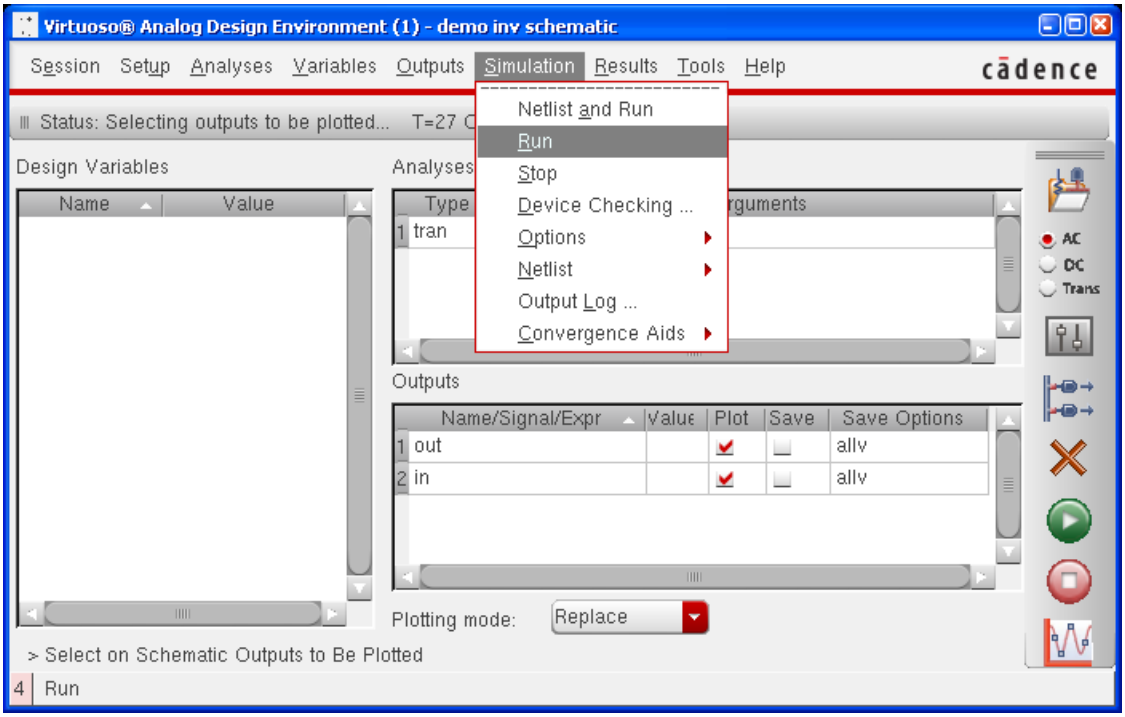
Outputs → To Be Plotted → Select On Schematic

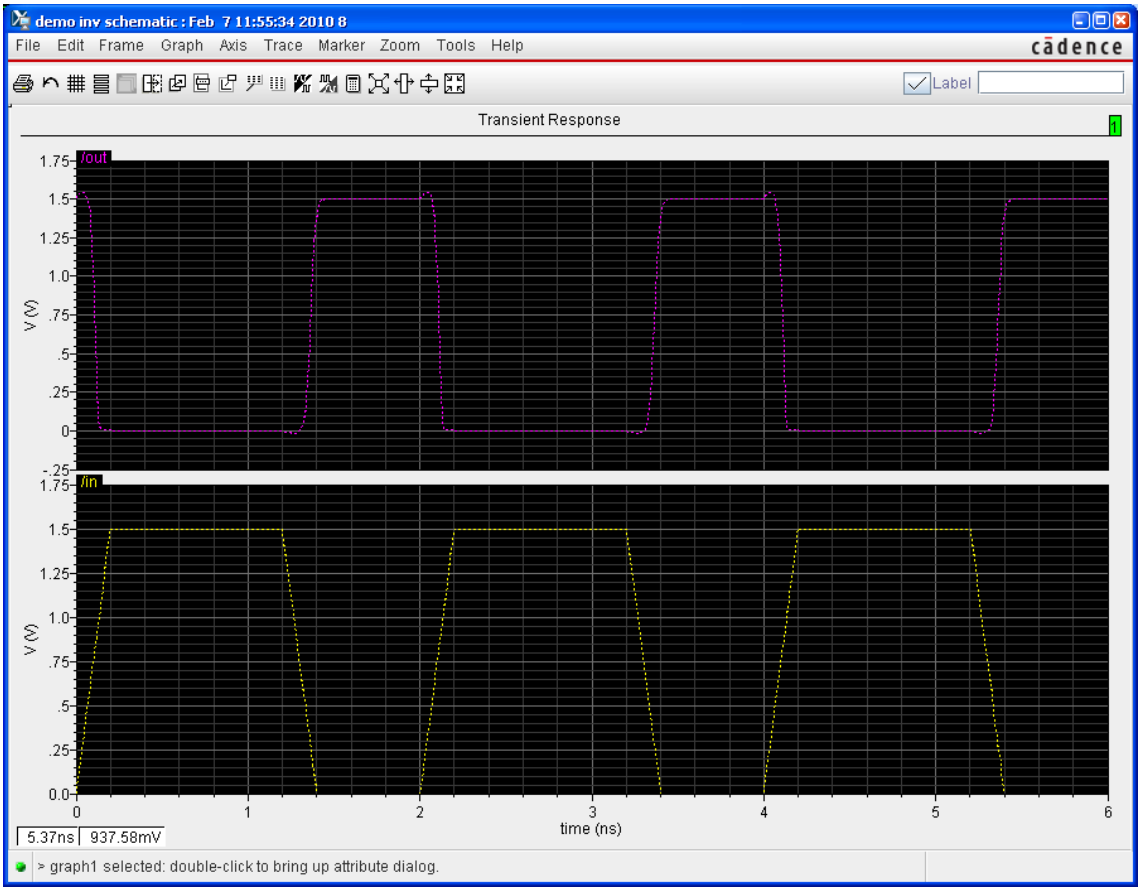
Click a signal (Pin) on a schematic/extracted. In Extracted try to use pins for signal that you need in the simulation because it is hard to select a net in the extracted view.



G. Run simulation

Simulation → Run



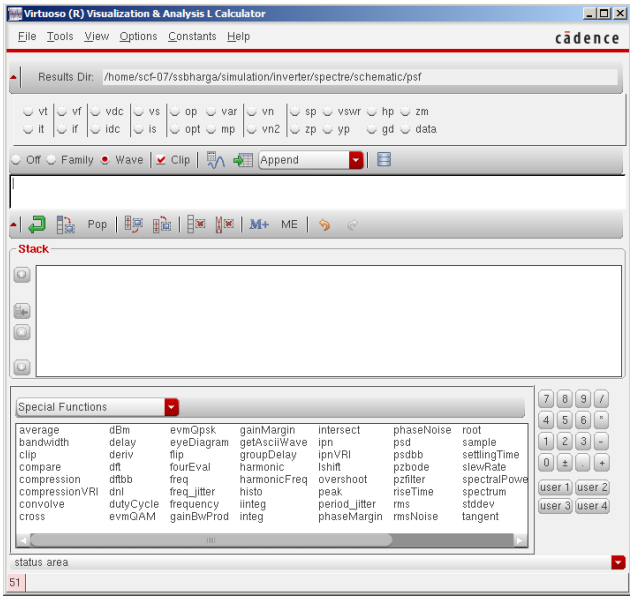


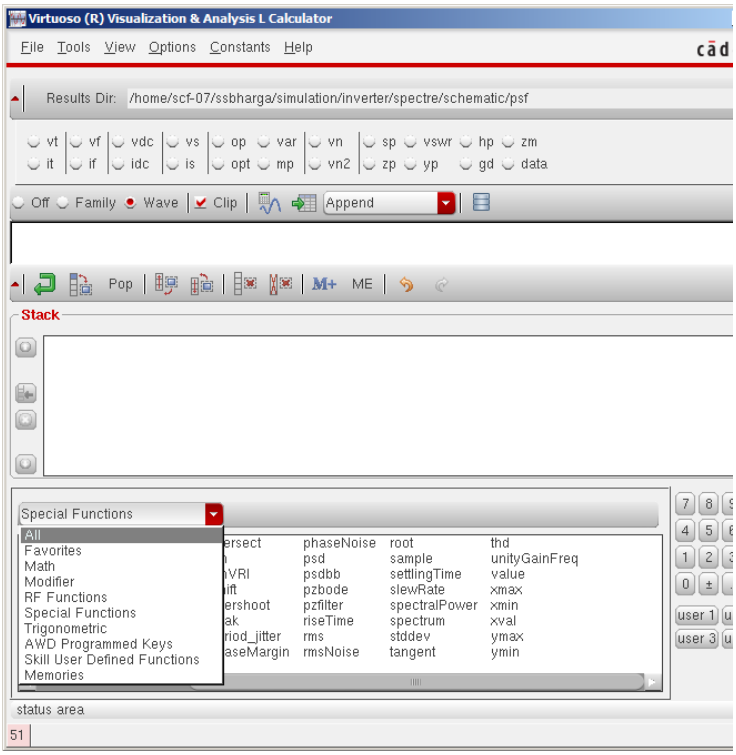
If you see a waveform like above picture, you followed every step properly.
Good job!.

H. Measurement

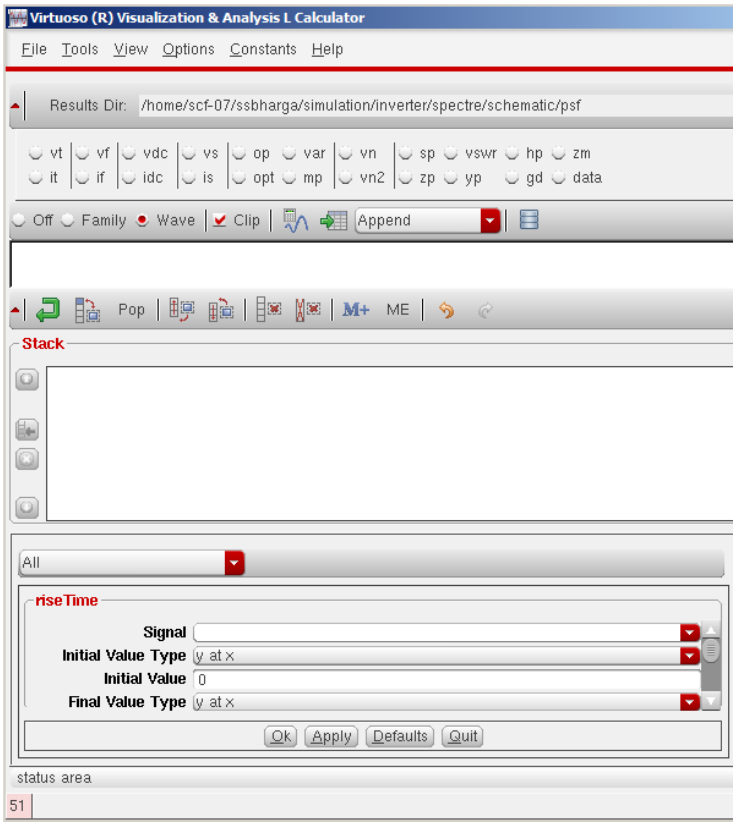
The following steps describe the measurement of rise time. Using similar steps other parameters of delay, fall time can be estimated.

Invoke the calculator  or tools-> calculator , select the Wave radio button:

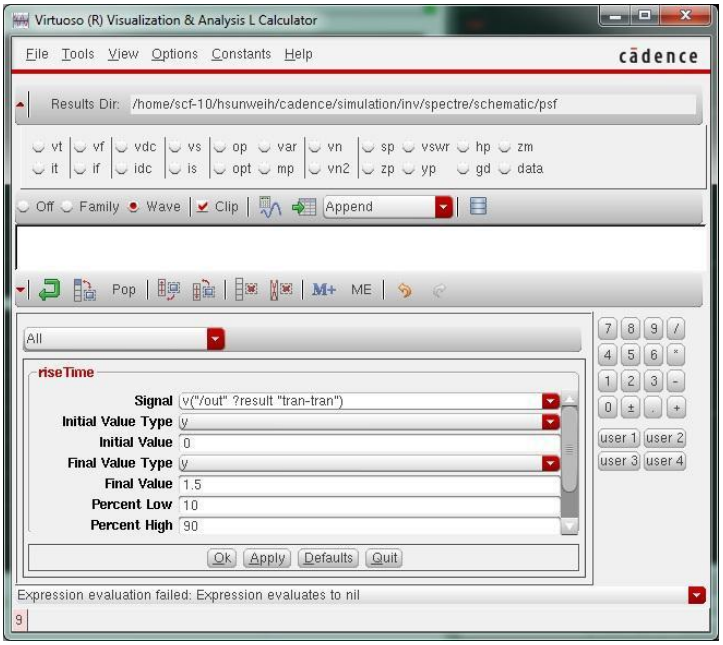




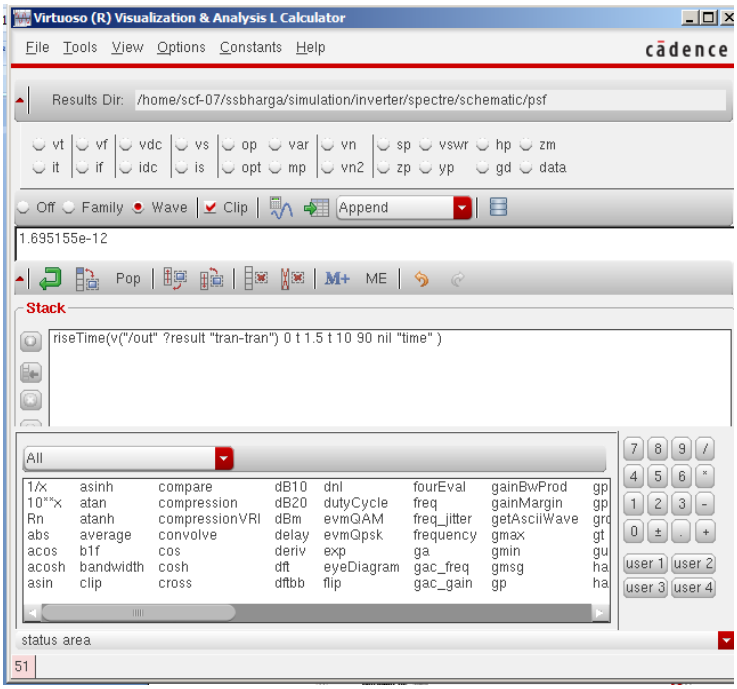
In the functions window – choose "all"



Select the rise time option



Select the signal from the waveform window whose rise time needs to be determined and click “OK”:



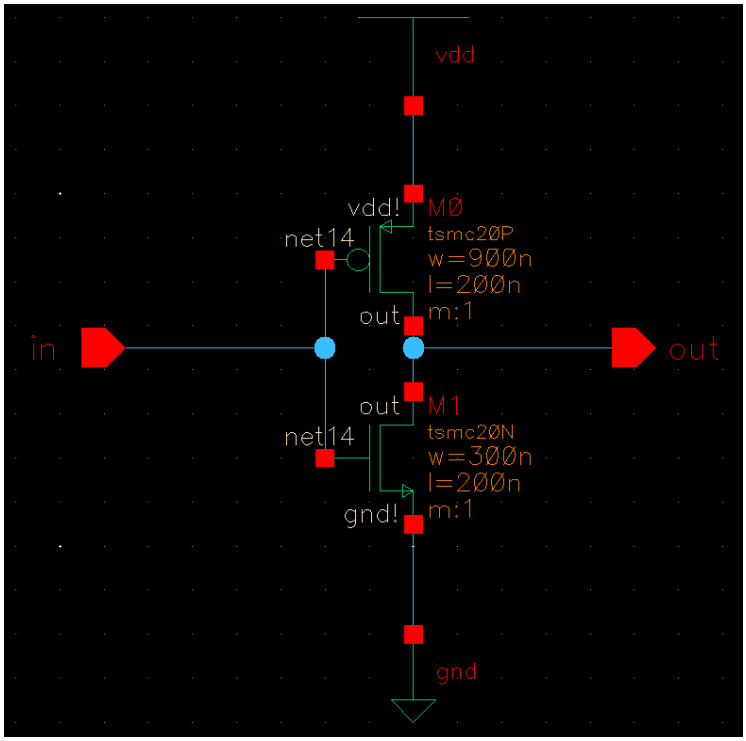
Click the evaluate buffer →  to display results as follows

You can also select a signal from calculator for example cos(Vin) as one of the plotted signals and you can see the results whenever you run the simulation.

Remember to save the simulation setup to use it later. You can do so by clicking on **Session → Save State** in the ADE (Analog Design Environment) window. Next time you want to simulate the same cell, you can reload your configuration by clicking on **Session → Load State**.

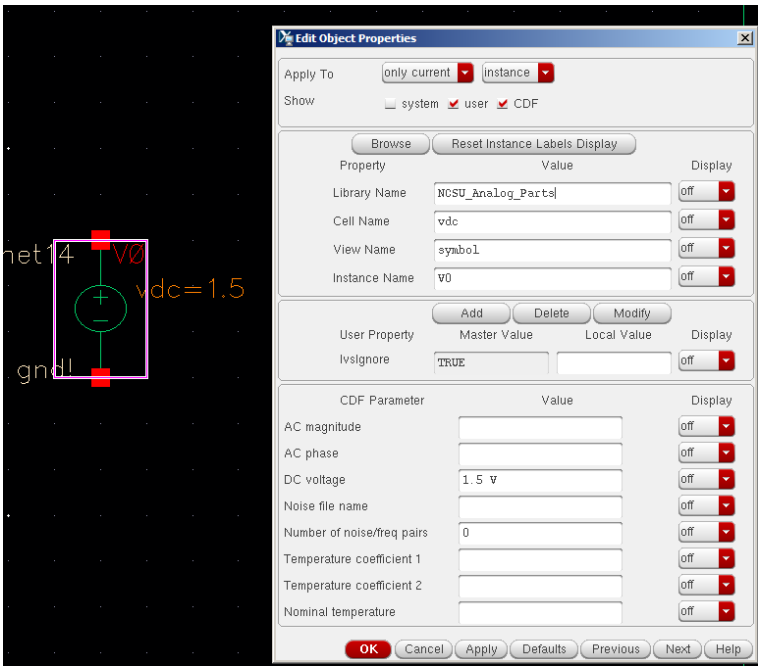
5. Run Spectre simulation (DC analysis)

The following inverter schematic is already created



A. Voltage Source

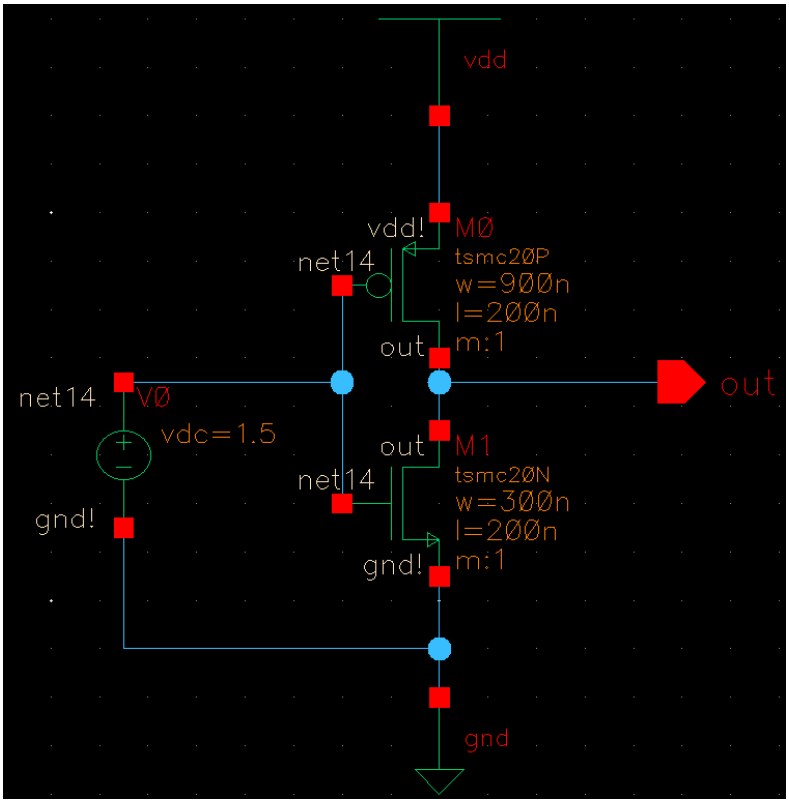
For DC analysis , the input pin “in” must be altered. The following are the steps to alter the pin “in” : Create→instance→NCSU analog parts→Voltage_sources select Vdc



The DC voltage must be set to 1.5V as shown.

B. Replace Input Pin

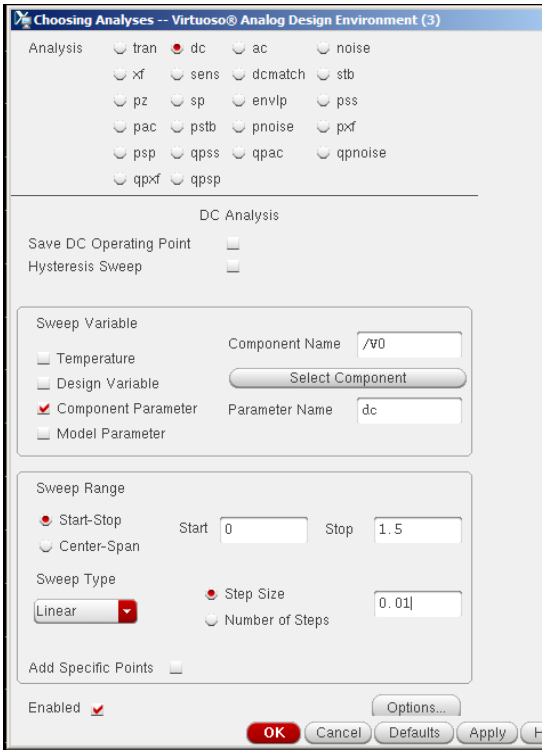
The Input pin “in” must be replaced with the above voltage source as shown below



Check and Save (make sure you get no errors)

C. Choosing Analyses

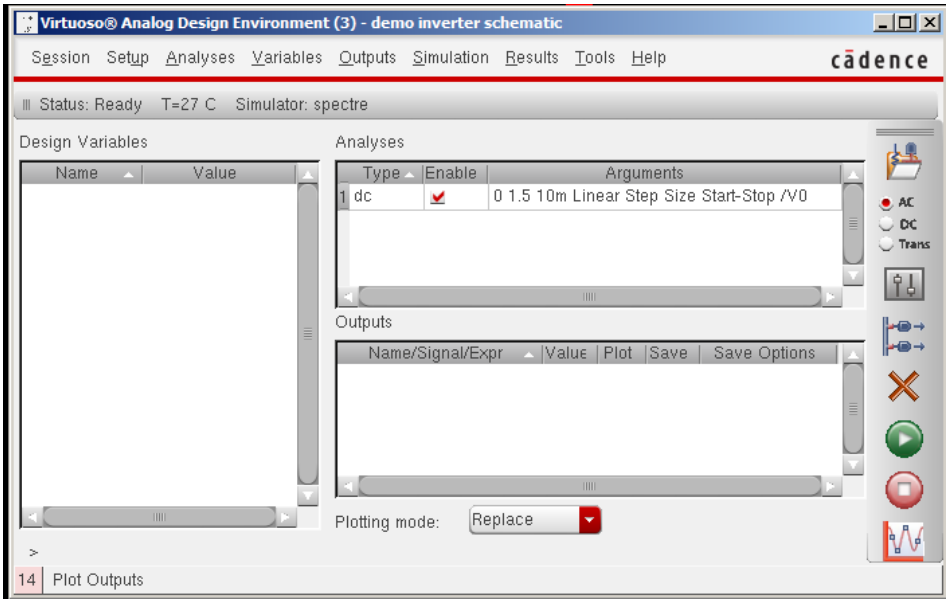
Launch ADE L, repeat steps A to D in section 3 of „Basic Design Flow“ except that there is no “in” input signal this time.



Go to Analyses → Choose dc

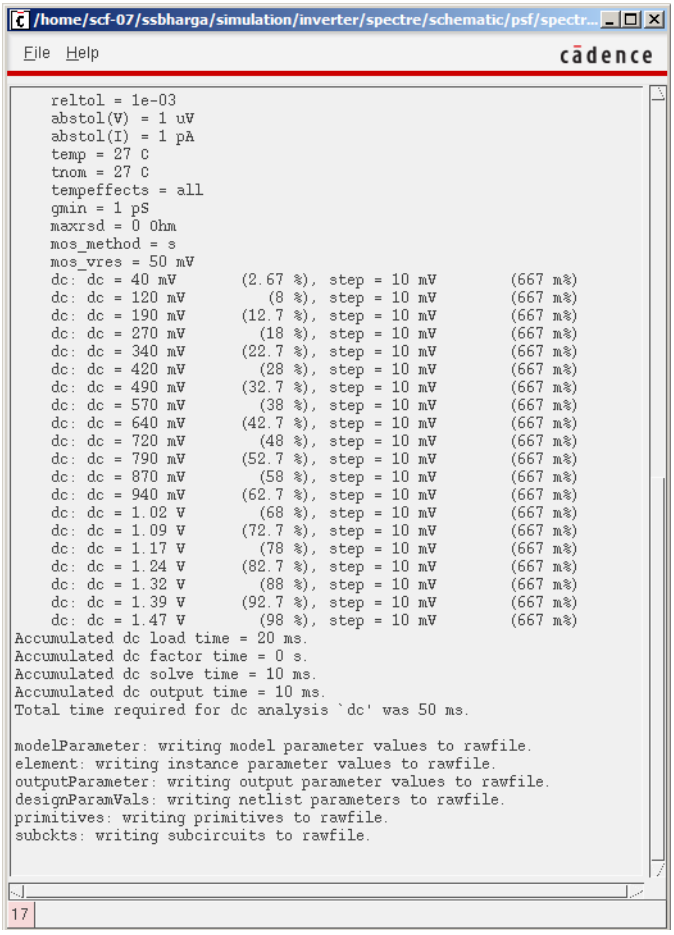
Choose „Component Parameter“,
Select Component, then the voltage source in the schematic, then choose 0 as Start, 1.5 as Stop and 0.01 as step .

Make sure that there are no other analyses selected apart from DC

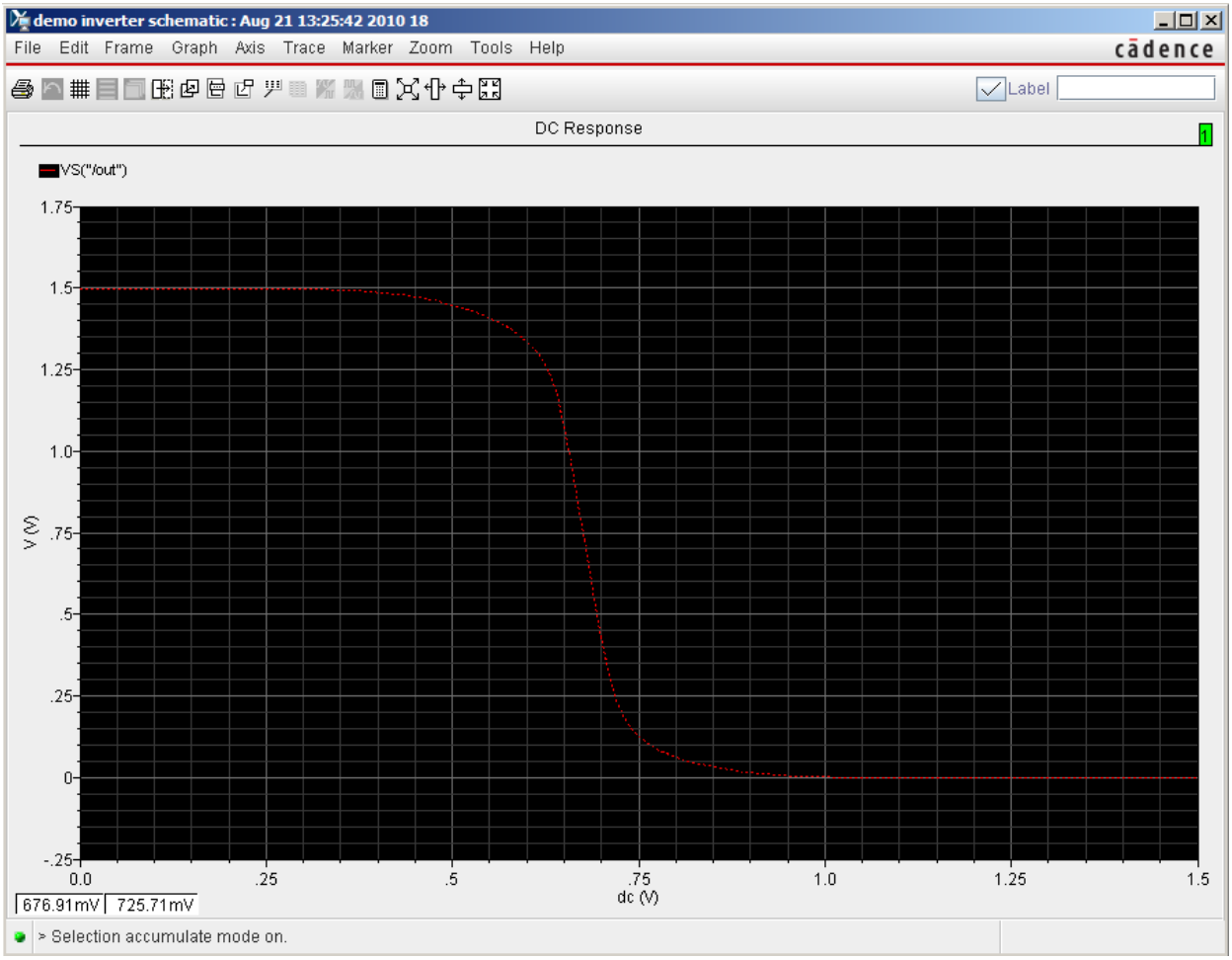


D. Run Simulation

Do simulations→netlist and run. On successful completion we get the following



Now, go to the results→Direct plot→DC. Click on the output pin “out” on the schematic and ESC key to get the following VTC

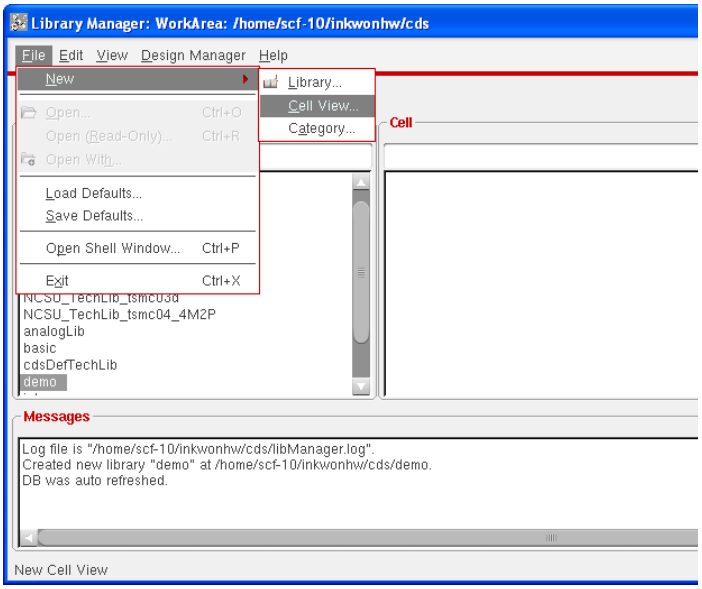


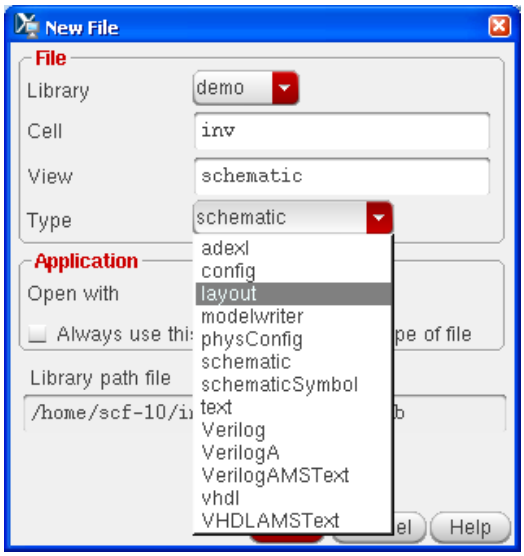
6. Layout

It‟s time to draw layout. Schematics are for verifying your design very roughly. They don‟t consider physical features like parasitic capacitances. After determining your design variables by schematics, you need to draw layouts.

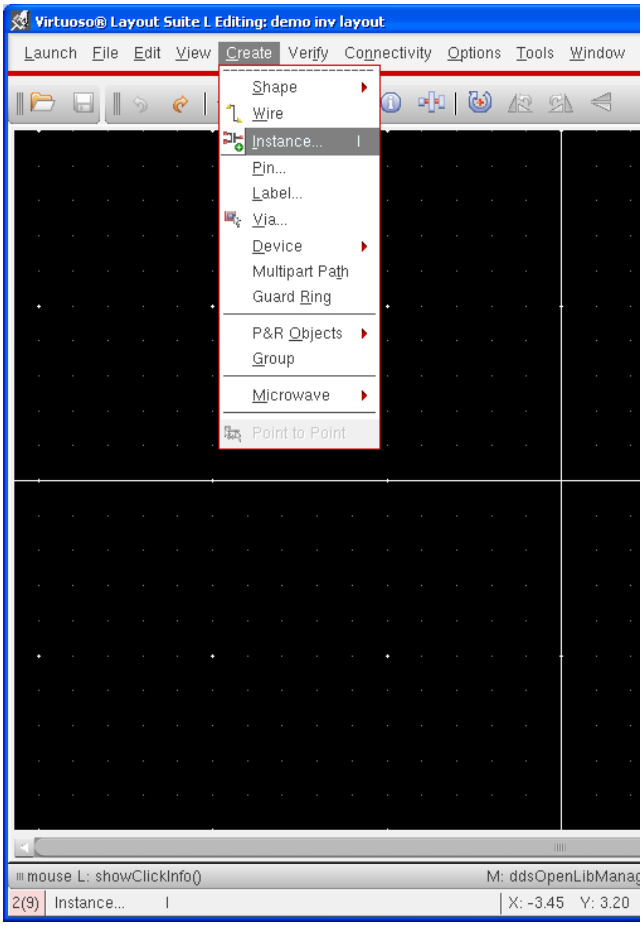
Design flow of layouts is very similar to one of schematics, but it has additional step which is LVS check. It is for check if your layout is identical to the schematic or not. Hence, this step is very important. If your logic doesn‟t pass this step, you may lose significant points for that.

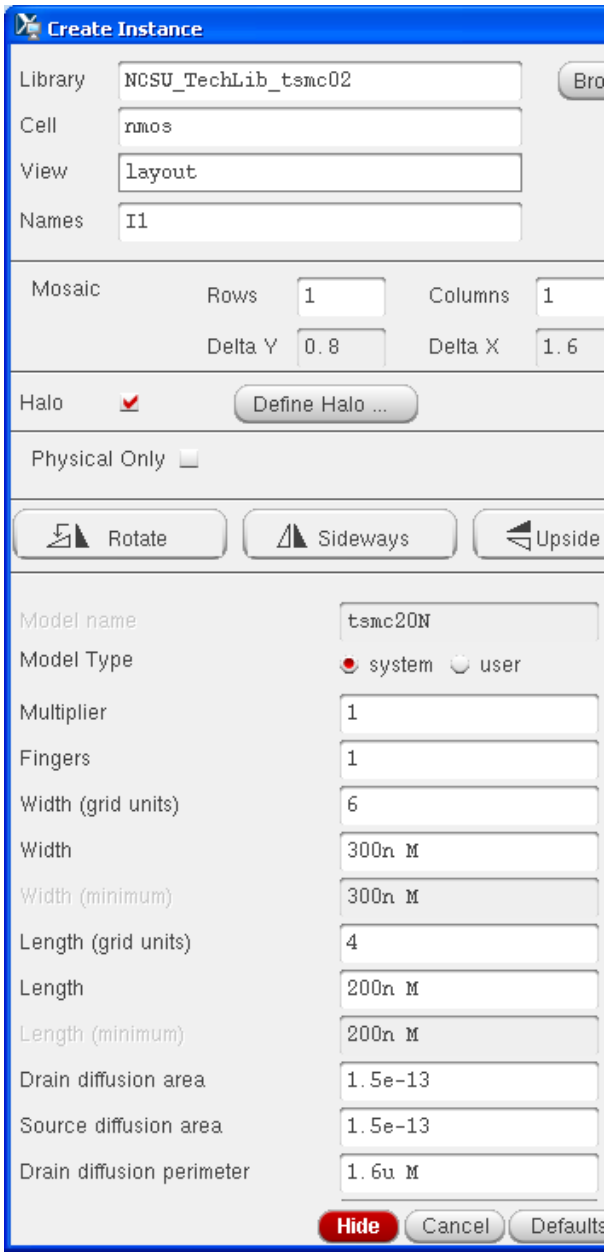
A. Create a layout

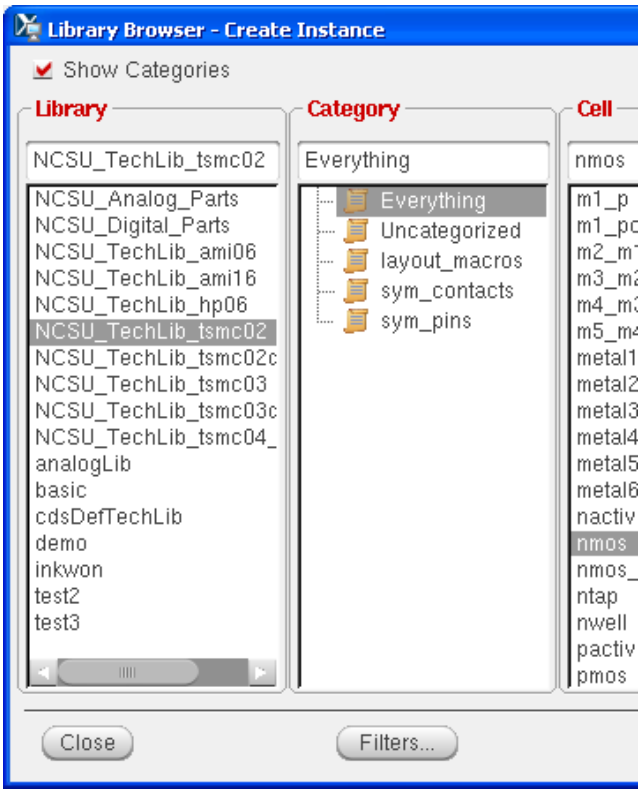




B. Add an instance - nmos

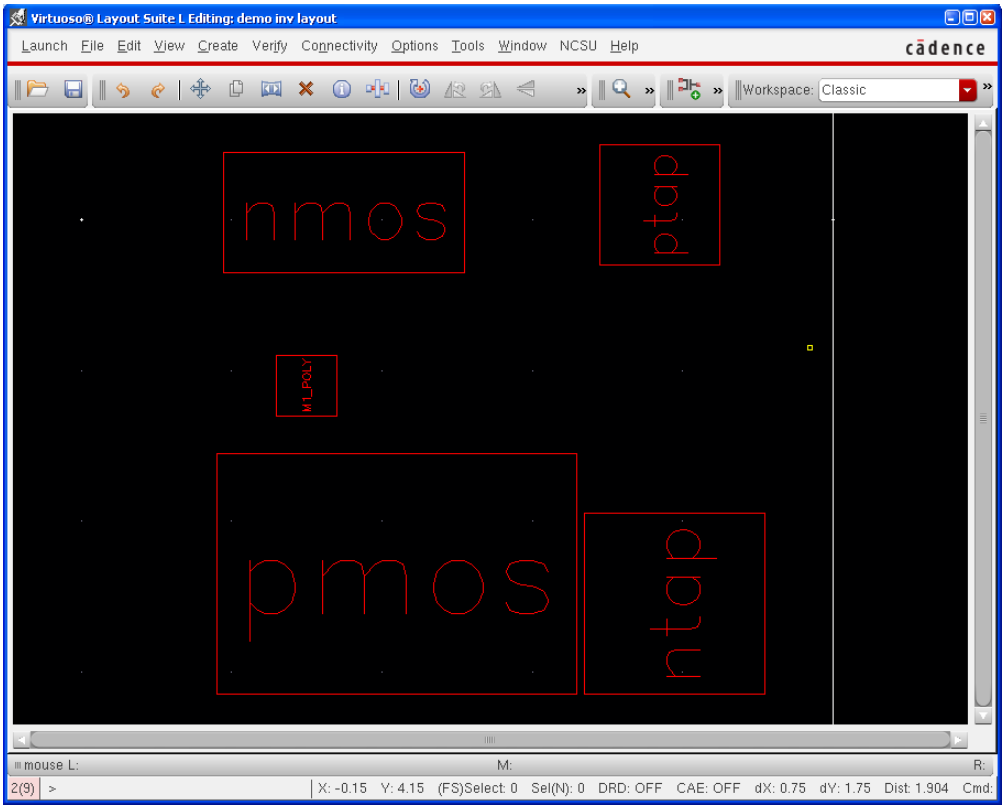




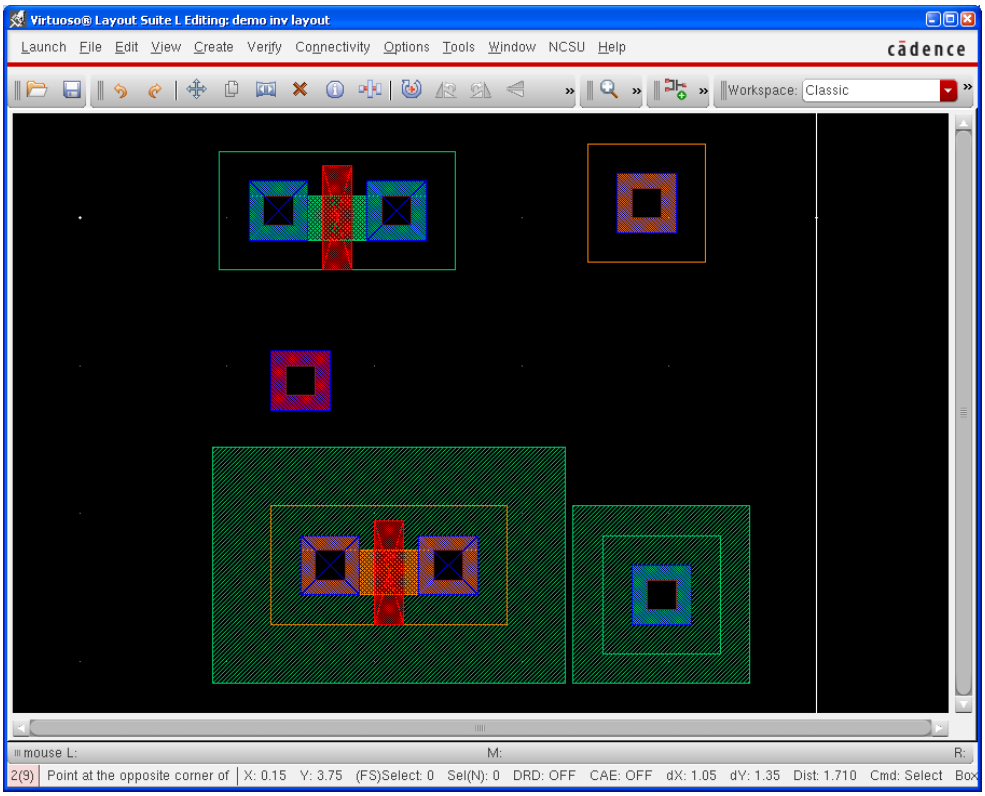


You can modify width of transistors.

C. Add more instances – pmos, ptap, ntap, and m1_ploy



You can select alternate view of a layout. Try „Shift + f“ and „Ctrl + f“.

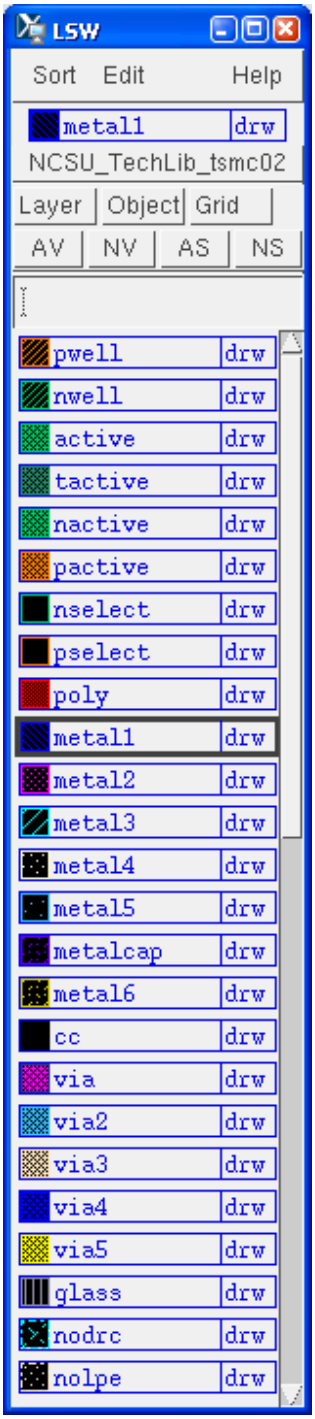


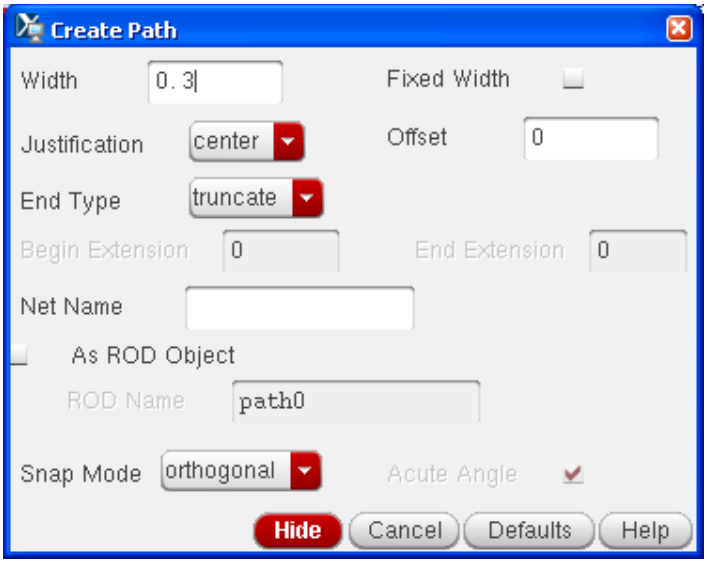
D. Draw metal1

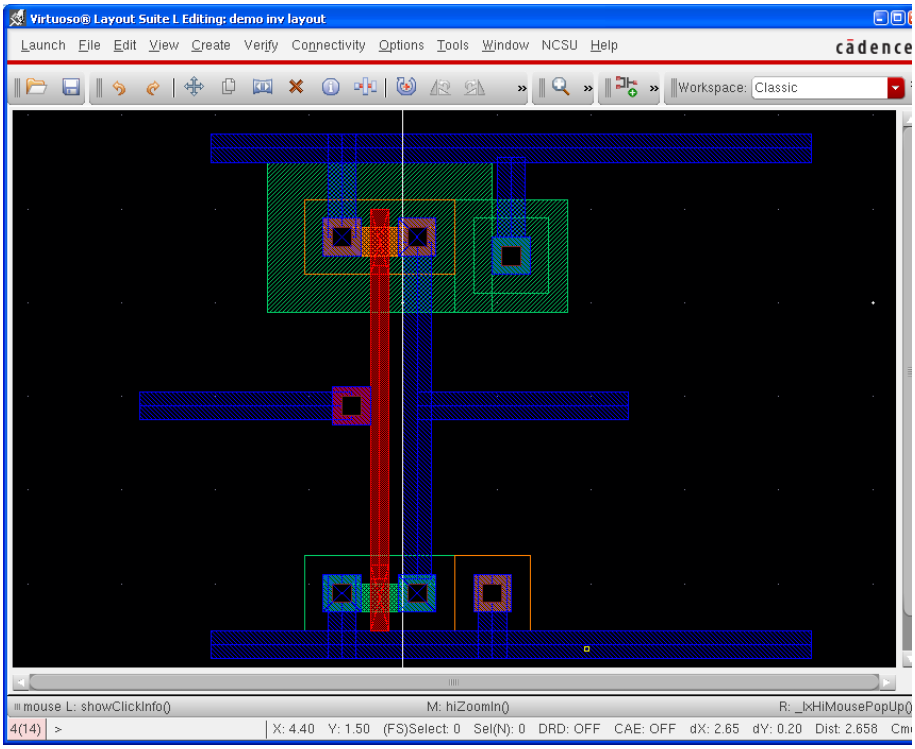
There are few ways for drawing metal, but I recommend you use „path". It's quite convenience than others.

Create → Shape → Path

First of all, you should select metal1 on LSW window. Default width for metal1 is 0.3, which means 300nm (3 λ). You can draw metal layer simply by clicking



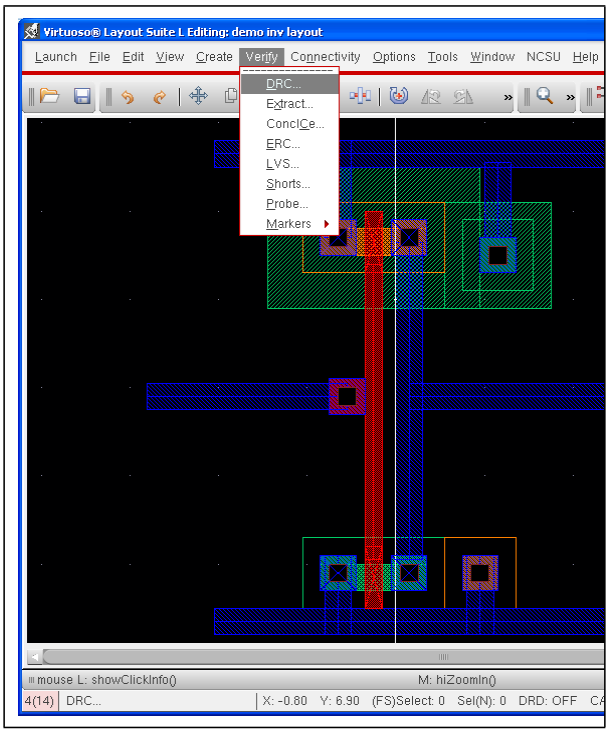


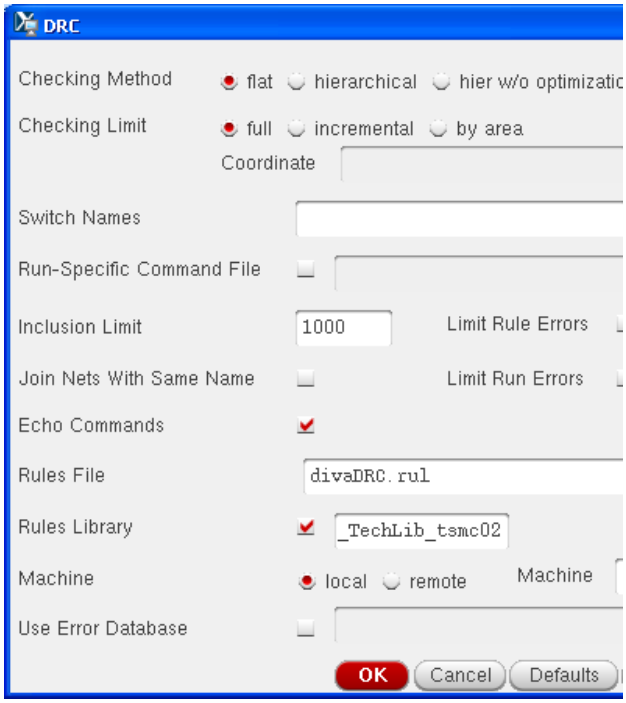


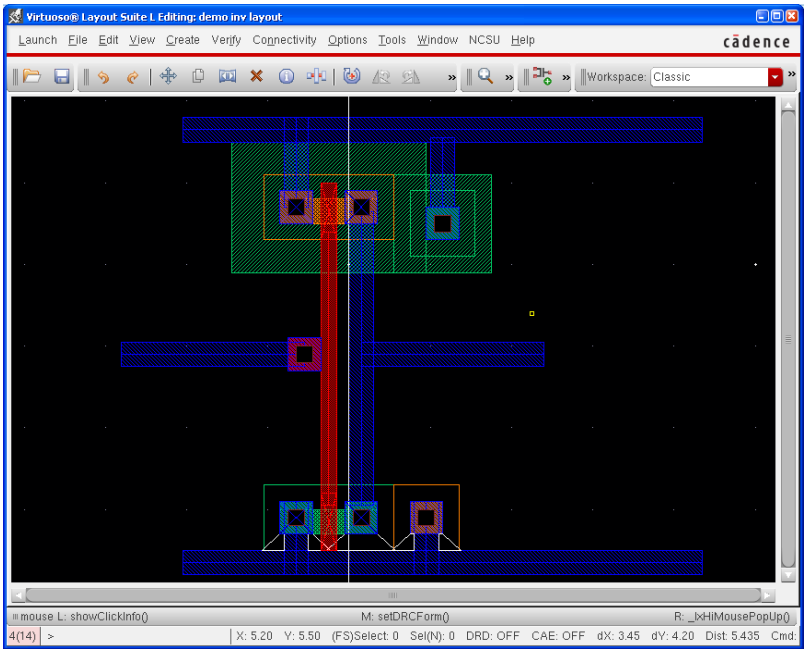
E. Run DRC

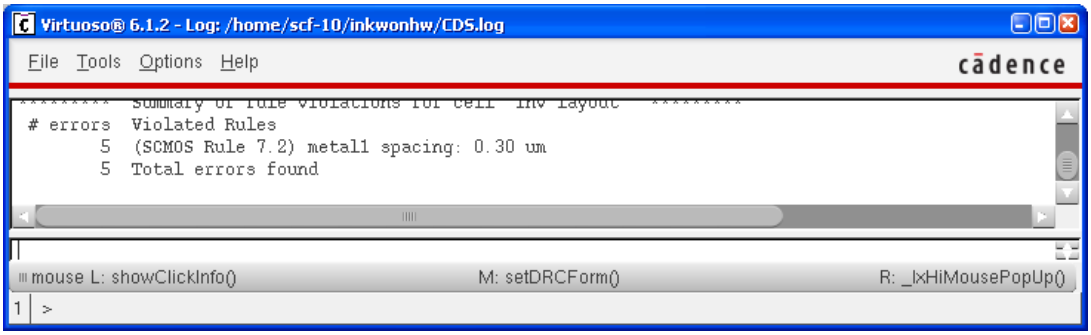
This step checks if your layout follows design rules.

Verify → DRC

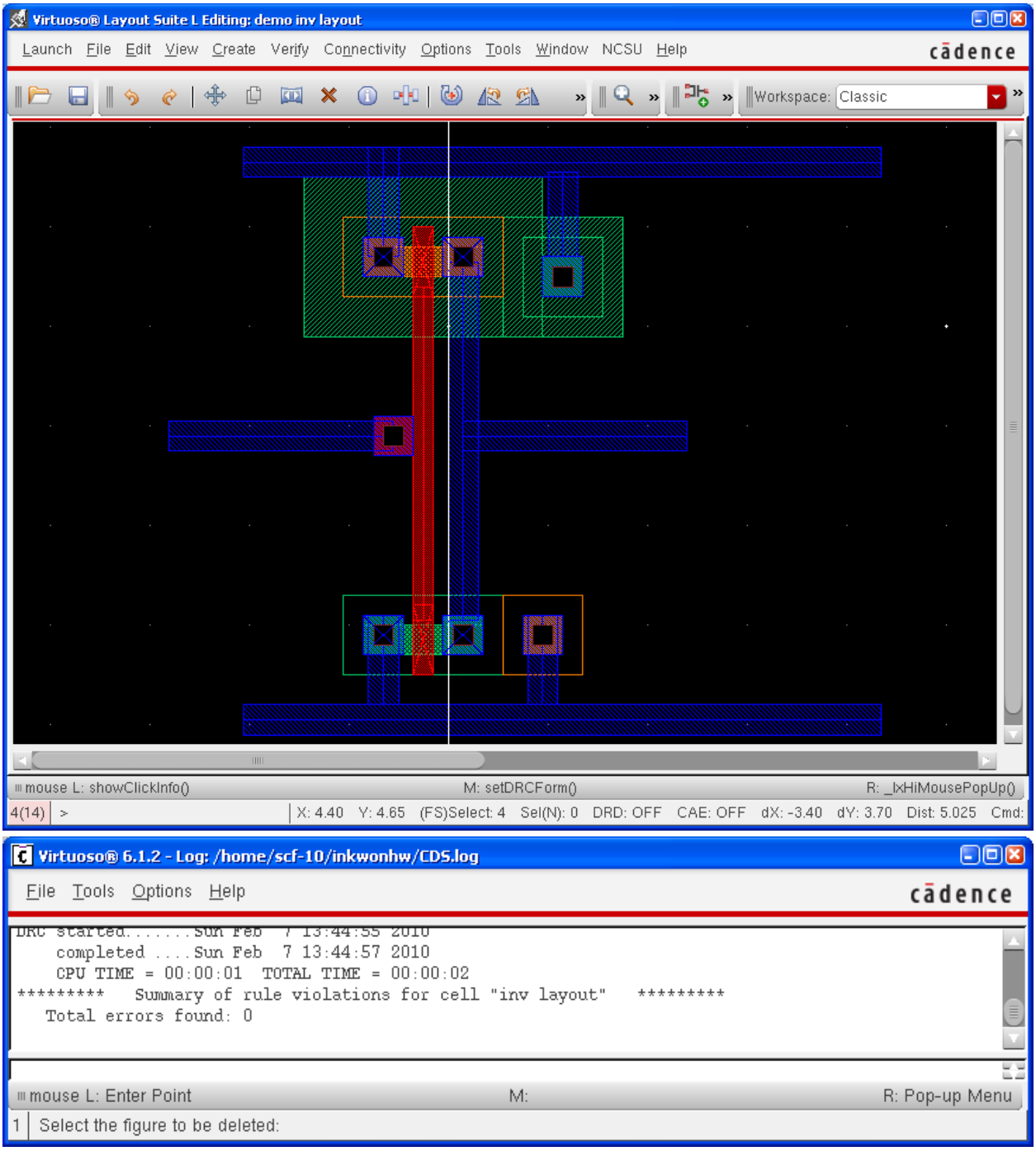








We have five errors. It is because a gnd metal layer is too close to an nmos transistor.
After modifying layout, run DRC again.

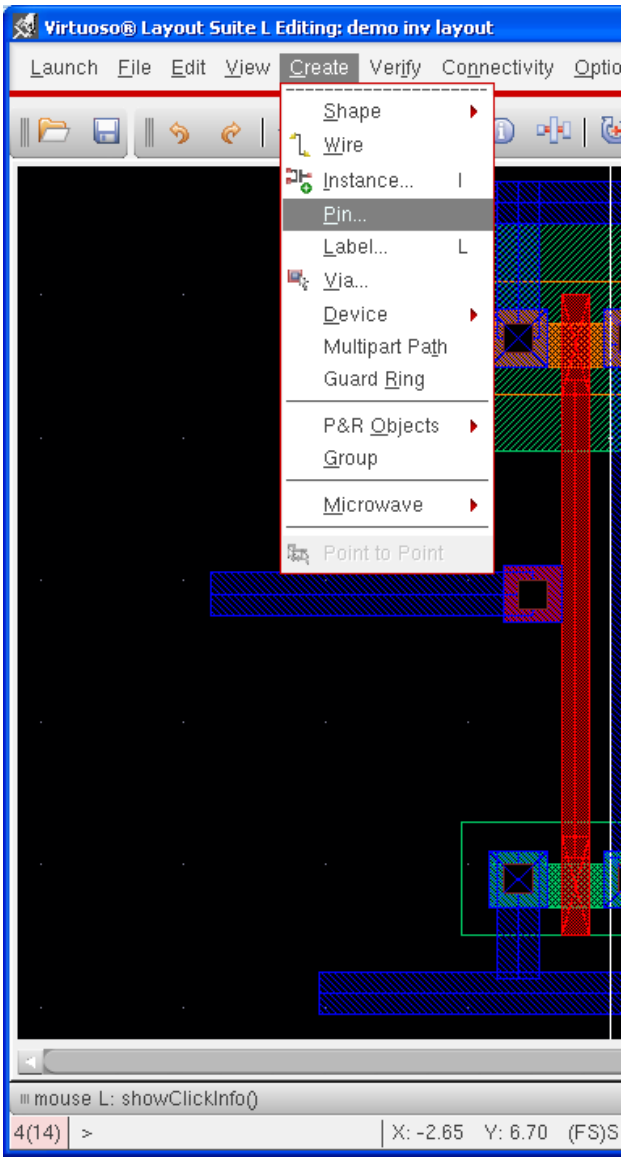


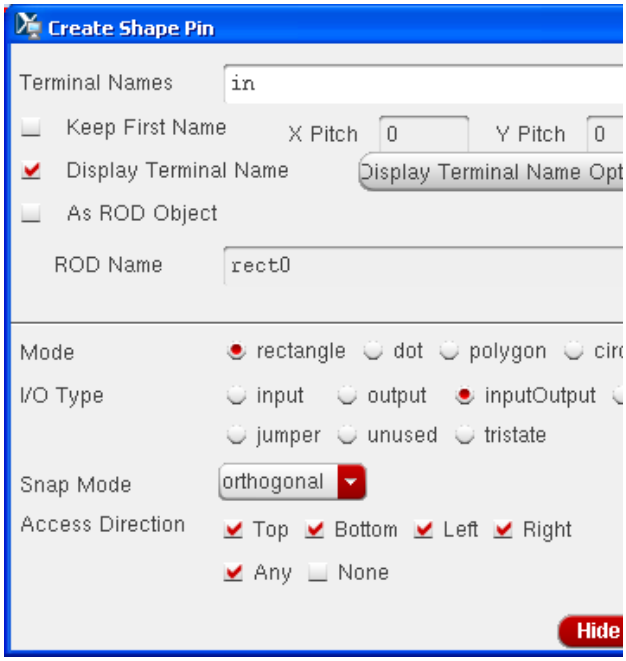
There is no error!!

F. Add pins

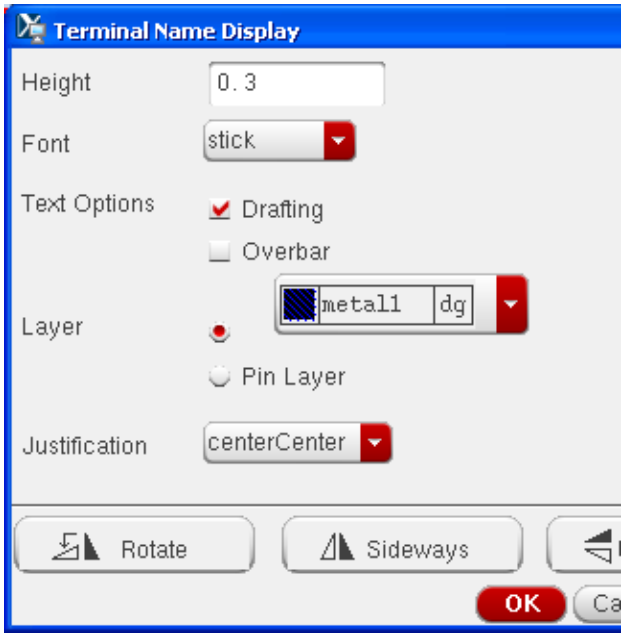
We had two pins on a schematic, which are „in“ and „out“. Pins are for assigning signals to physical device, so we assign voltage level of gnd and vdd by using pins. Hence, we have 4 pins for the layout, which are „in“, „out“, „gnd!“, and „vdd!“.

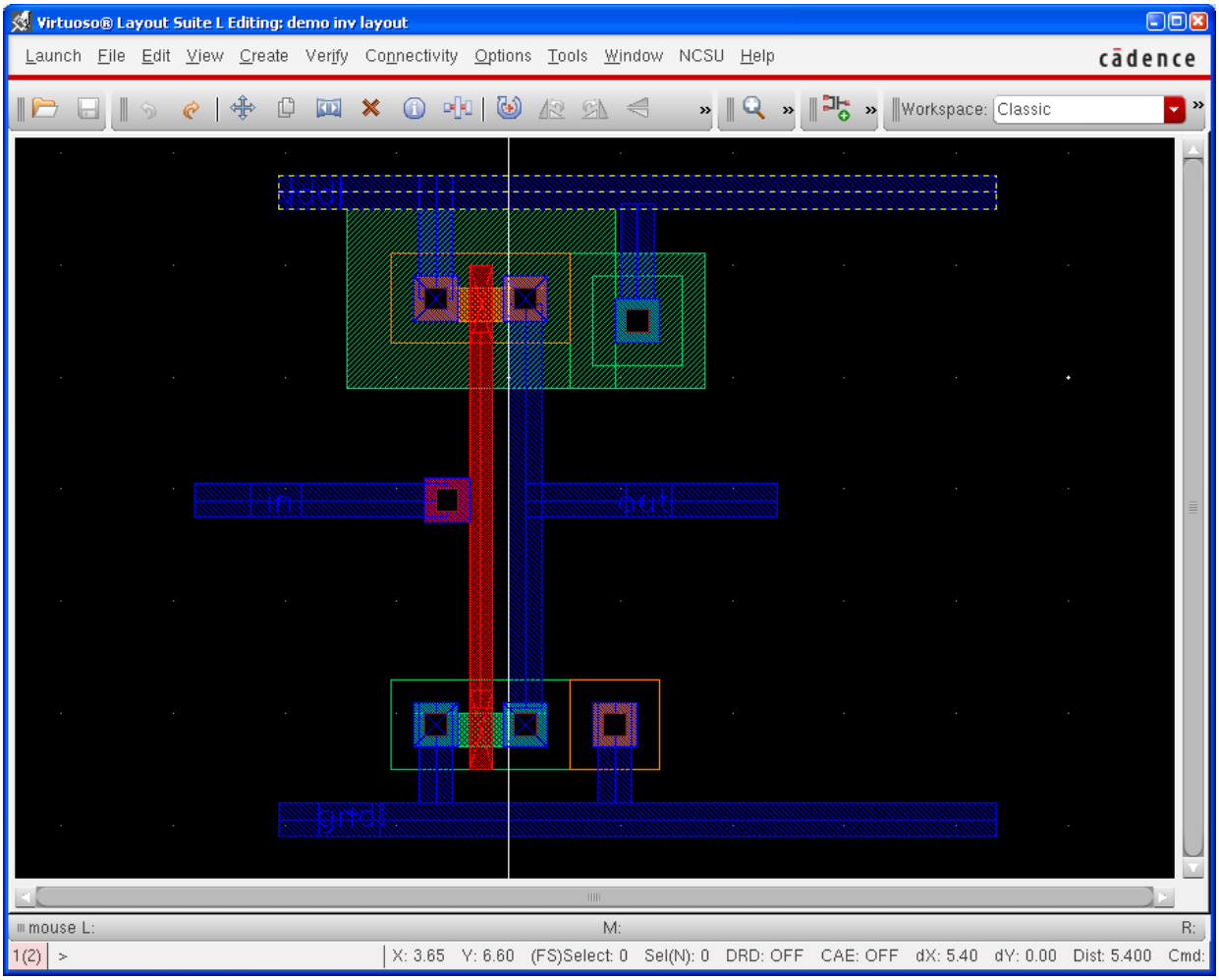
Create → Pin





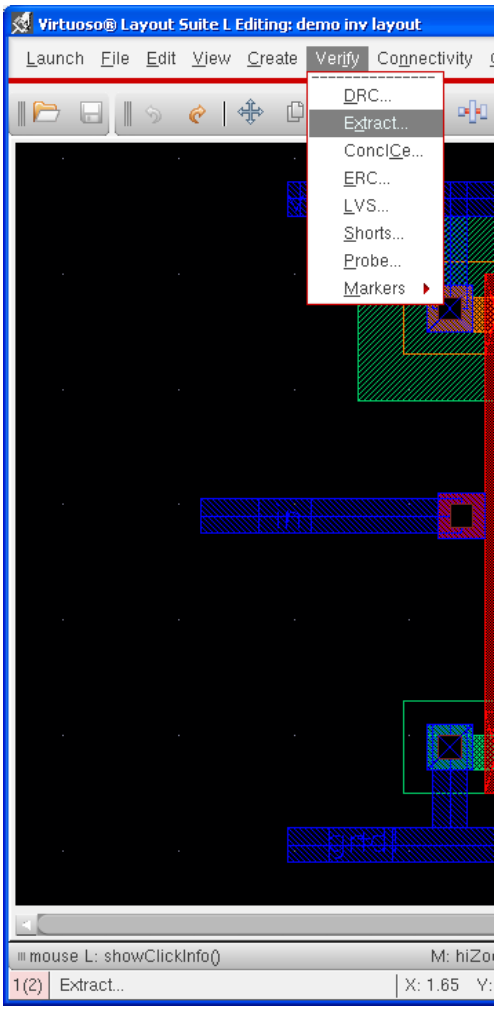
Check „Display Terminal Name“ if you want to see pin name on the layout.
Click „Display Terminal Option

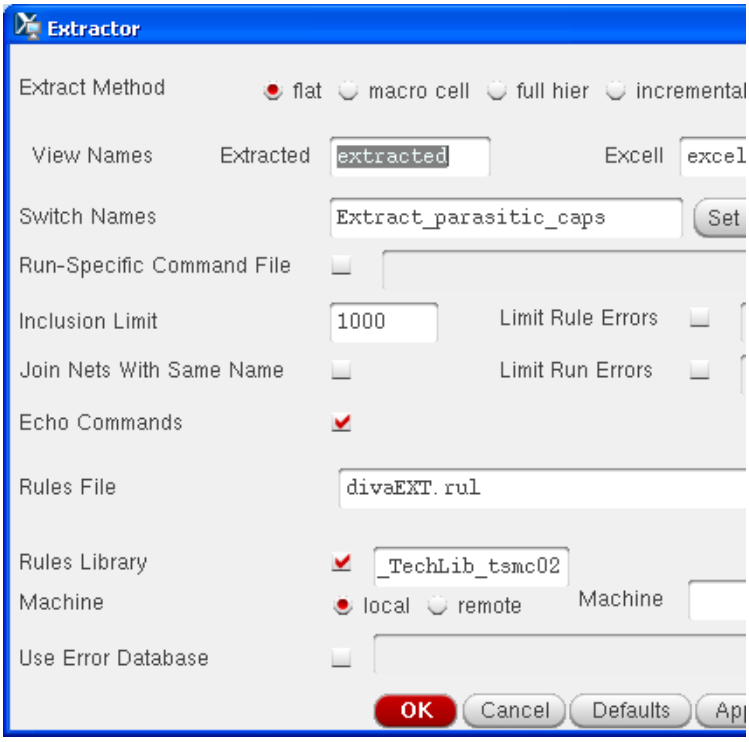



Virtuoso® Layout Suite L Editing: demo inv layout
Launch File Edit View Create Verify Connectivity Options Tools Window NCSU Help
cadence
Workspace: Classic
mouse L:
M:
R:
1(2)
X: 3.65 Y: 6.60 (FS)Select: 0 Sel(N): 0 DRD: OFF CAE: OFF dX: 5.40 dY: 0.00 Dist: 5.400 Cmd:

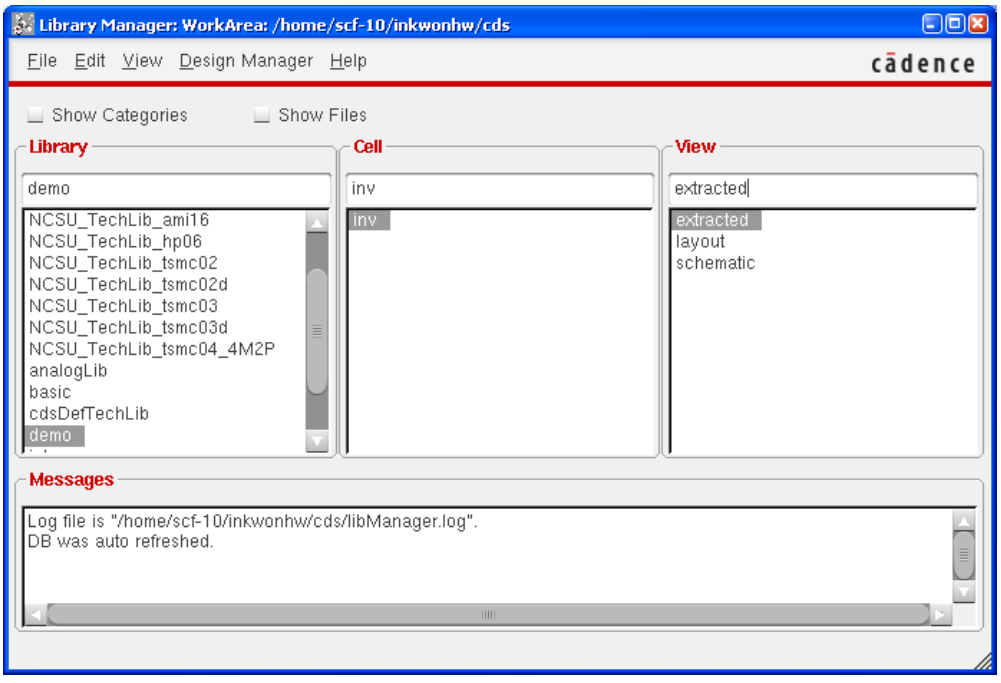
G. Extract

A layout is just a picture. If you need to run simulation using the layout, you should convert it to the other format. It is done by extracting. It‟s something like compiling a code.





Select „Extract_parastic_cap‟ as a switch name, otherwise your extracted design won‟t have parasitic capacitances.

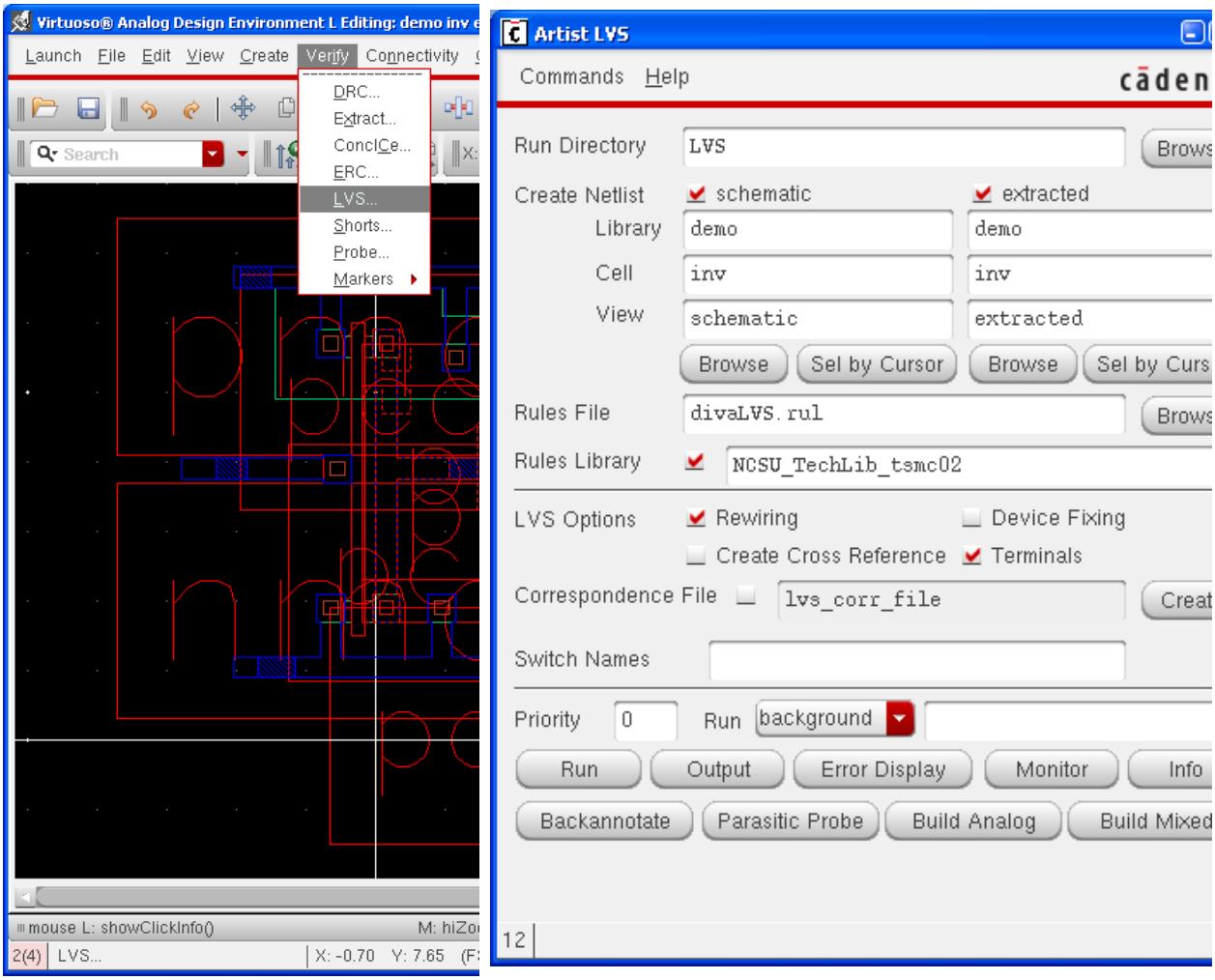


H. Run LVS

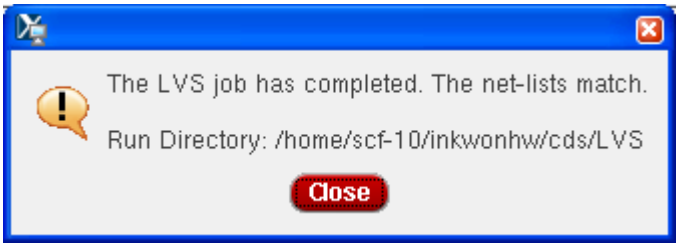
As I mentioned before, this step is very important for your grading. More complicated design, more time will be required for debugging LVS.

Verify → LVS

Keep in mind. You **SHOULD** compare your schematic with **EXTRACTED**.



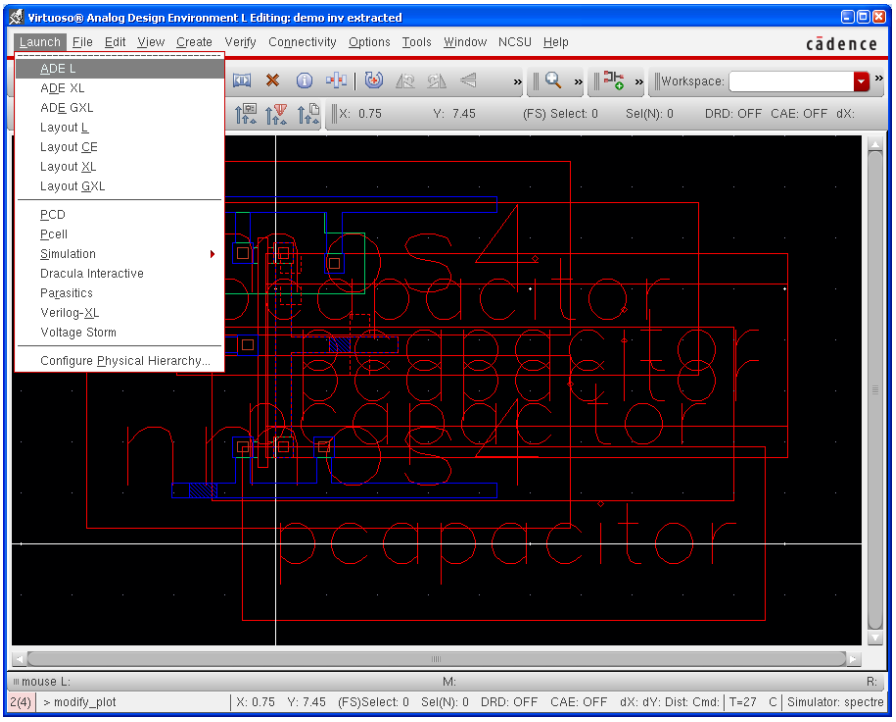
I hope all of you will see the following window.

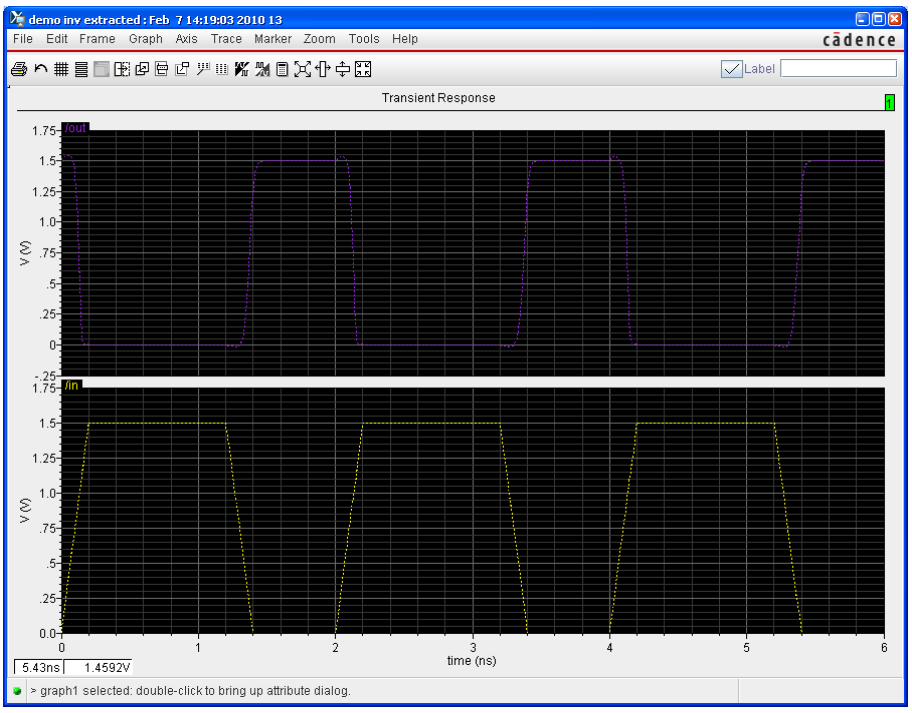


If there are errors, you can check the results by clicking „Output“ button. „Error Display“ also might be helpful.

I. Run Spectre simulation

It is same as schematics. Please follow the instructions for the schematics.





Congratulations!!

You followed all steps I prepared. Let‟s do the same thing for more complicated designs.

*Some useful information

Useful Links:

http://www.edaboard.com/
http://www.eda.ncsu.edu/wiki/NCSU_EDA_Wiki
http://www.cadence.com/community/forums/