Additional Cadence Virtuoso Guide

Based on Cadence GPDK 45nm Technology

EE 577 A

University of Southern California

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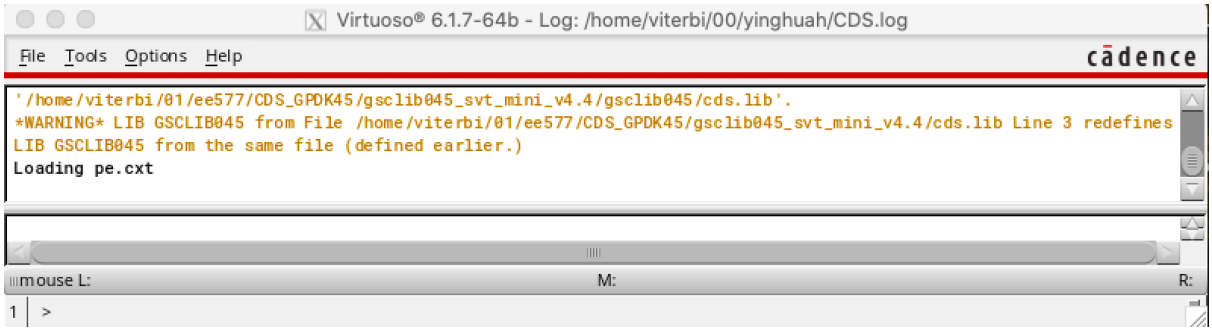
1. Download Three Setup files:

- `setup_cds_gpdk045.sh`
- `setup_ee477_ee577a_v2001b.csh`

upload them to **viterbi-scf1.usc.edu** or **viterbi-scf2.usc.edu** node.

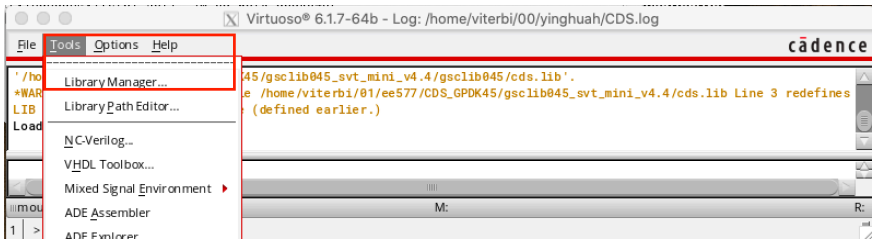
2. Install new environment for cadence virtuoso:

- Run the script setup_cds_gpdk045.sh on scf1 or scf2 servers. Once it is done, you will find a new folder called "work_gpdk045" (This step only needs to be done once).
  - **`sh setup_cds_gpdk045.sh`**
- Source **`setup_ee477_ee577a_v2001b.csh`** file (This step is needed every time you log into the server).
  - **`source setup_ee477_ee577a_v2001b.csh`**
- Go to 'work_gpdk045' directory and open your Cadence Virtuoso software
  - **`cd work_gpdk045`**
  - **`virtuoso &`**
- You will see the following window.

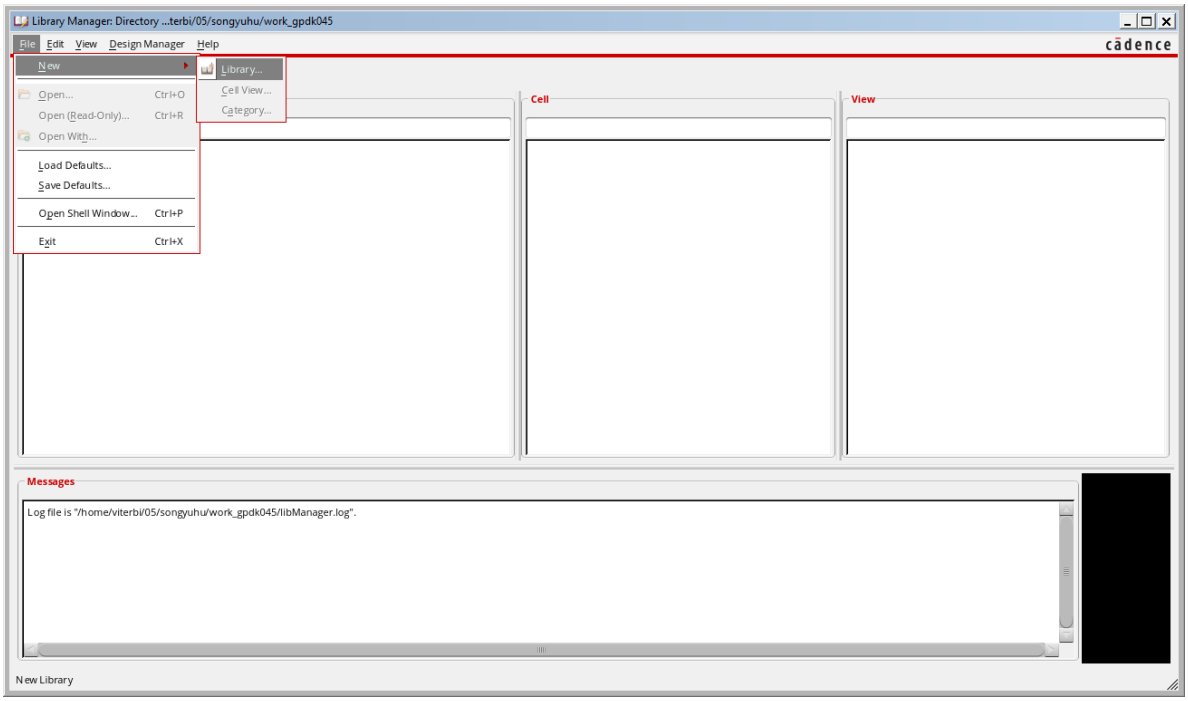


3. Schematic design:

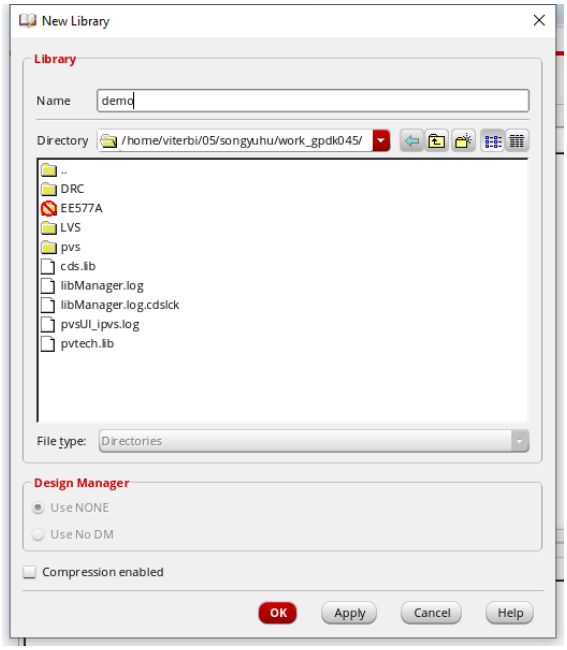
- Open the library manager by **Tools -> Library Manager**



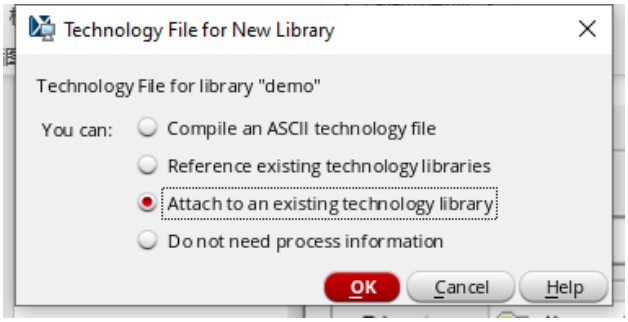
- Create your library by **File -> New -> Library**



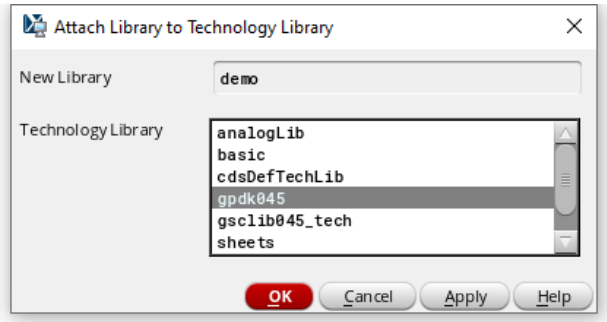
- Name your library and click “OK”



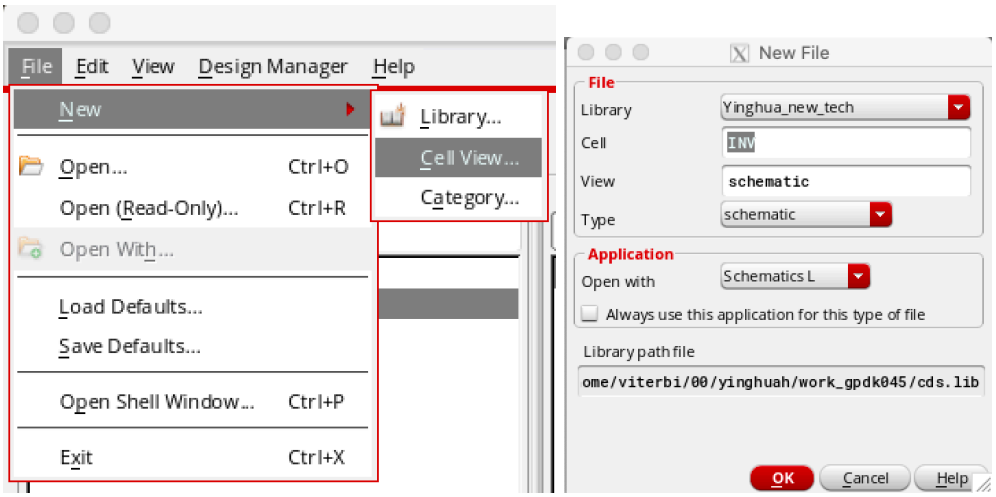
- “Attach to an existing technology library” and click “OK”.

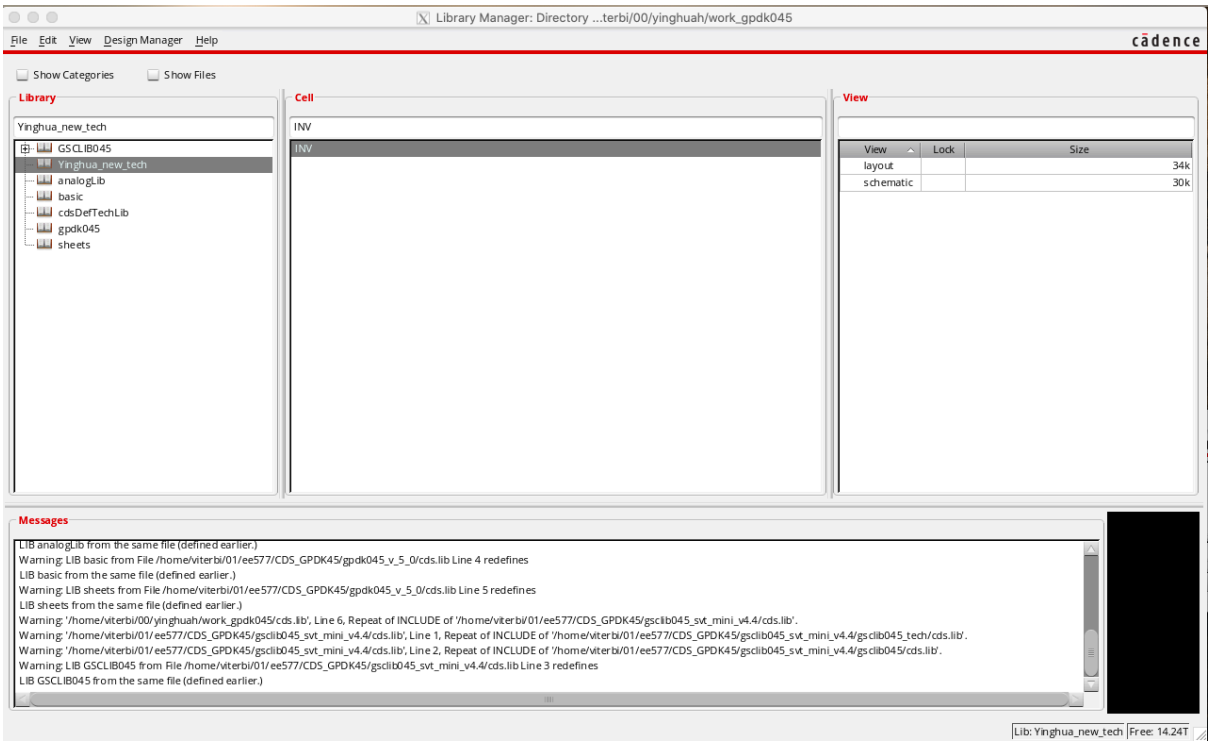


- Choose “gpdk045” and click “OK”.



- Create a new cell view



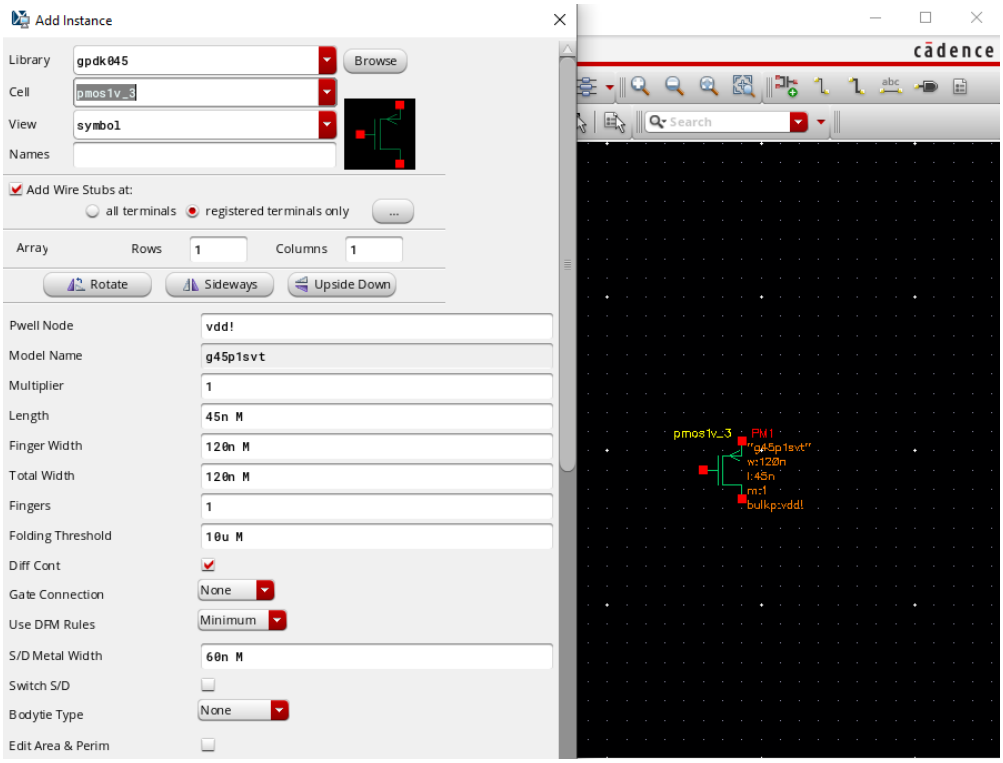


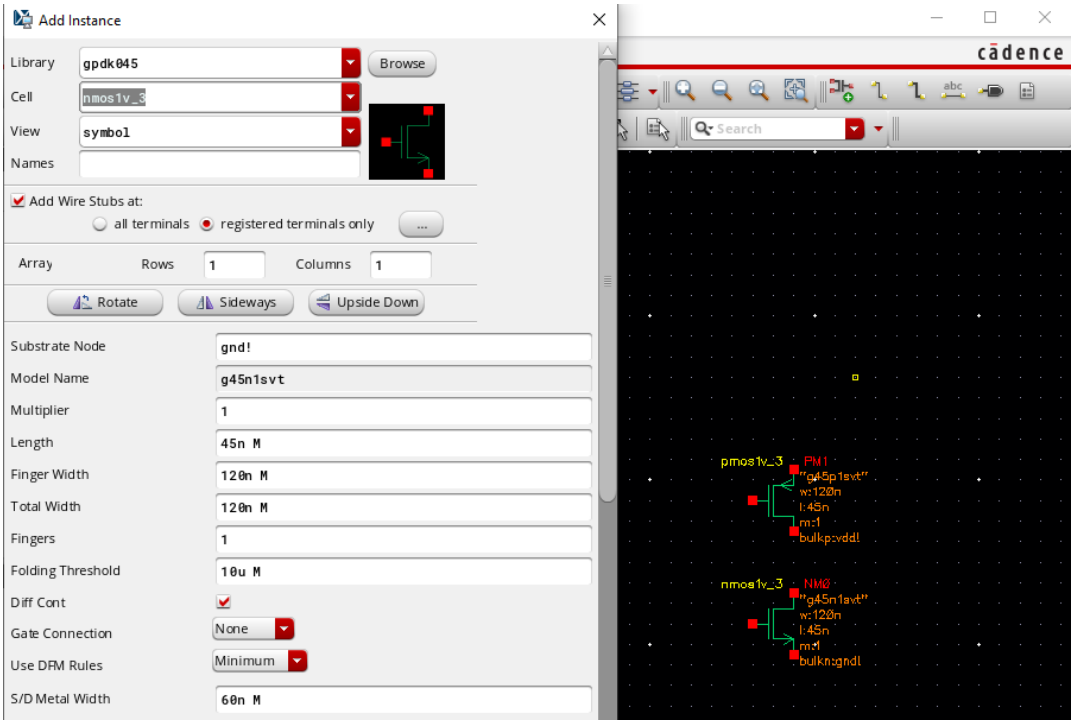
- Click the cell and draw the schematic

- Add instance – Create -> Instance

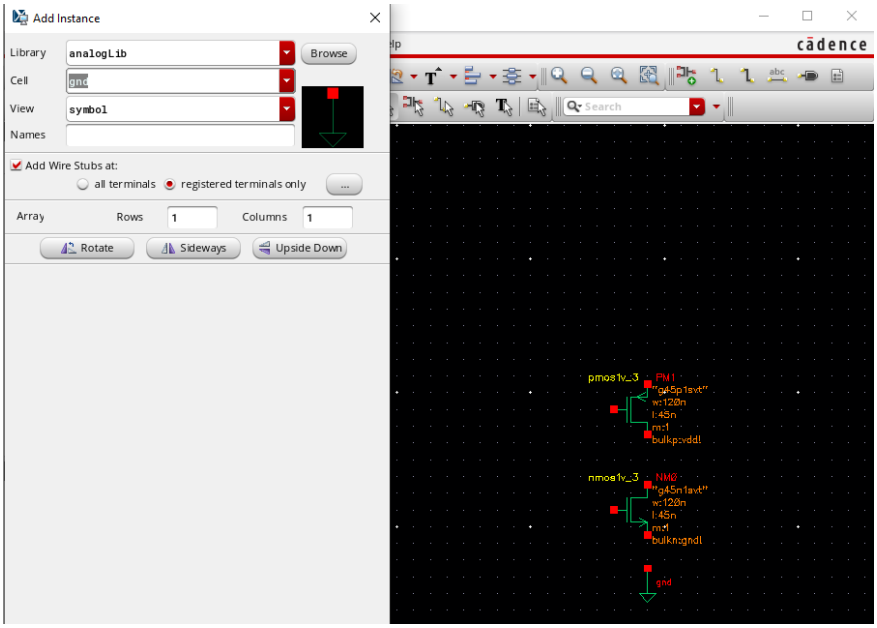
You should select the **gpdk045** library and use **pmos1v_3** or **nmos1v_3** to draw Pmos and Nmos.

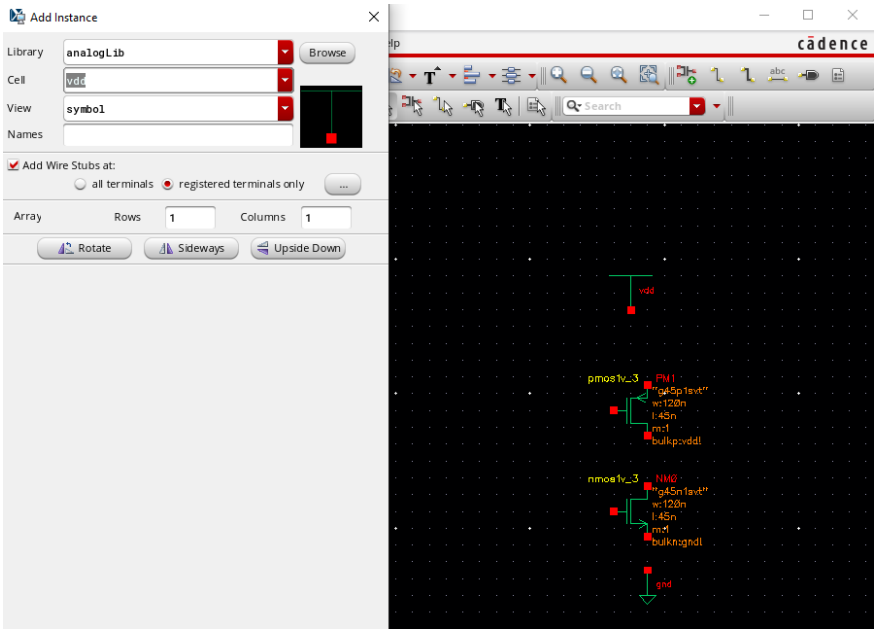
You can modify Width of transistors by changing **Finger Width or Fingers as shown below**.



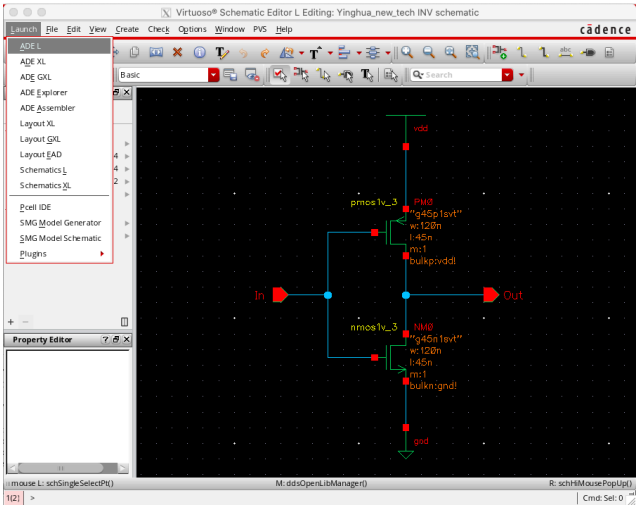


VDD and GND are in a different library called **analogLib**.



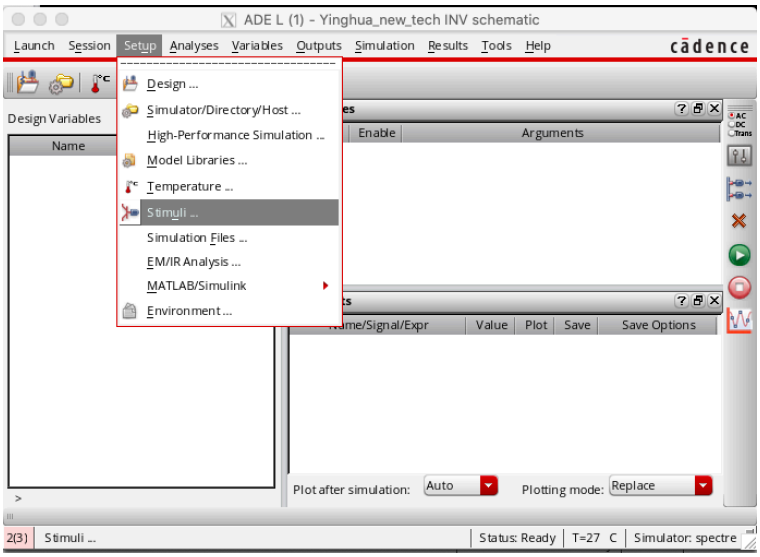


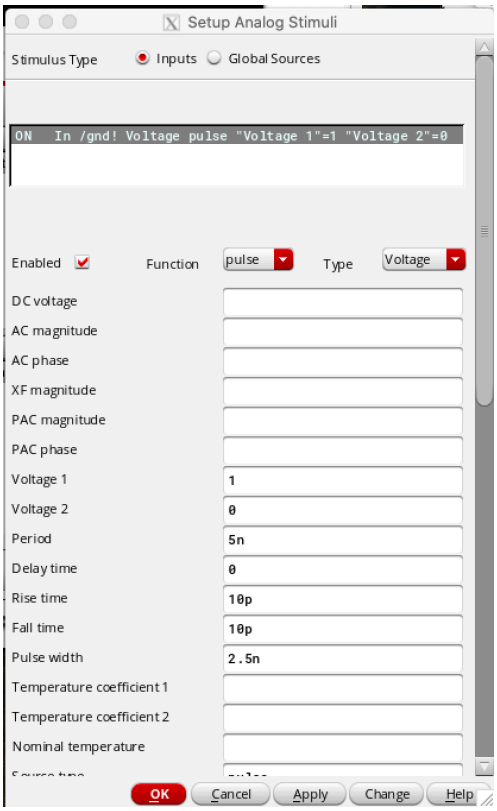
- Run the simulation. **Launch -> ADE L**

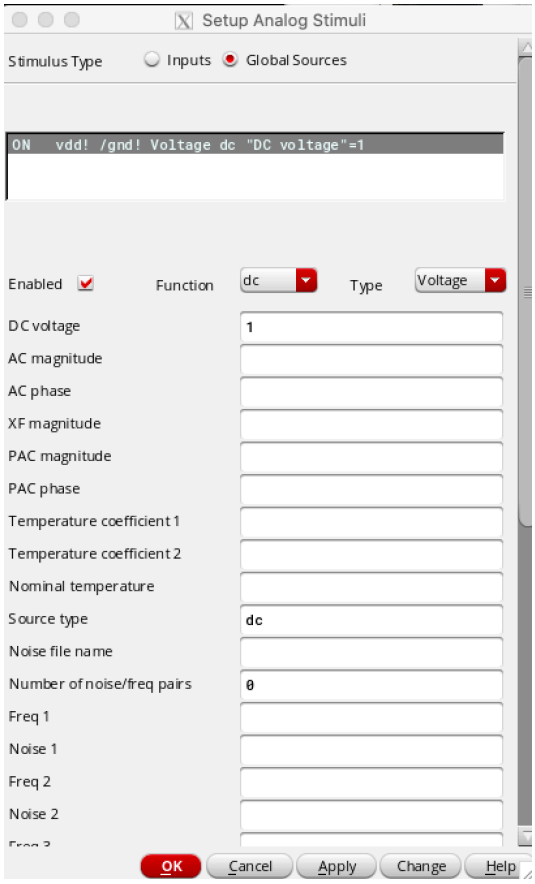


- Set Stimuli for input ports and Vdd. In this example, we set “In” as a step waveform.

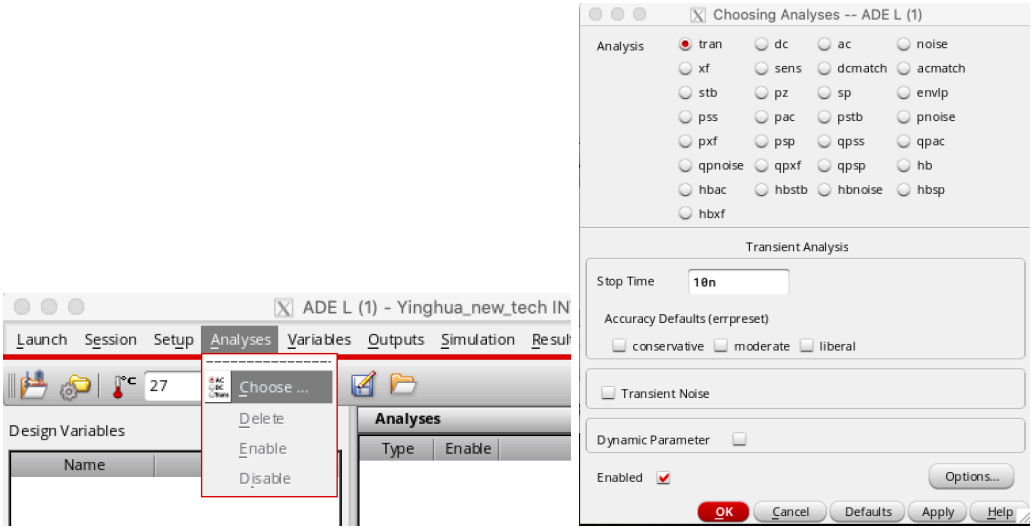
  NOTE: In 45 nm, Vdd = 1V



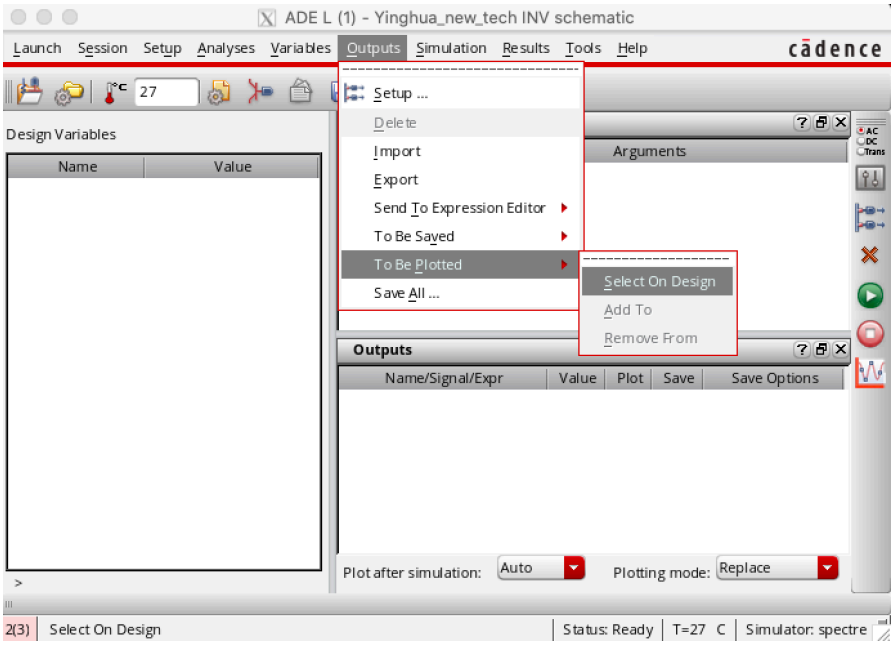




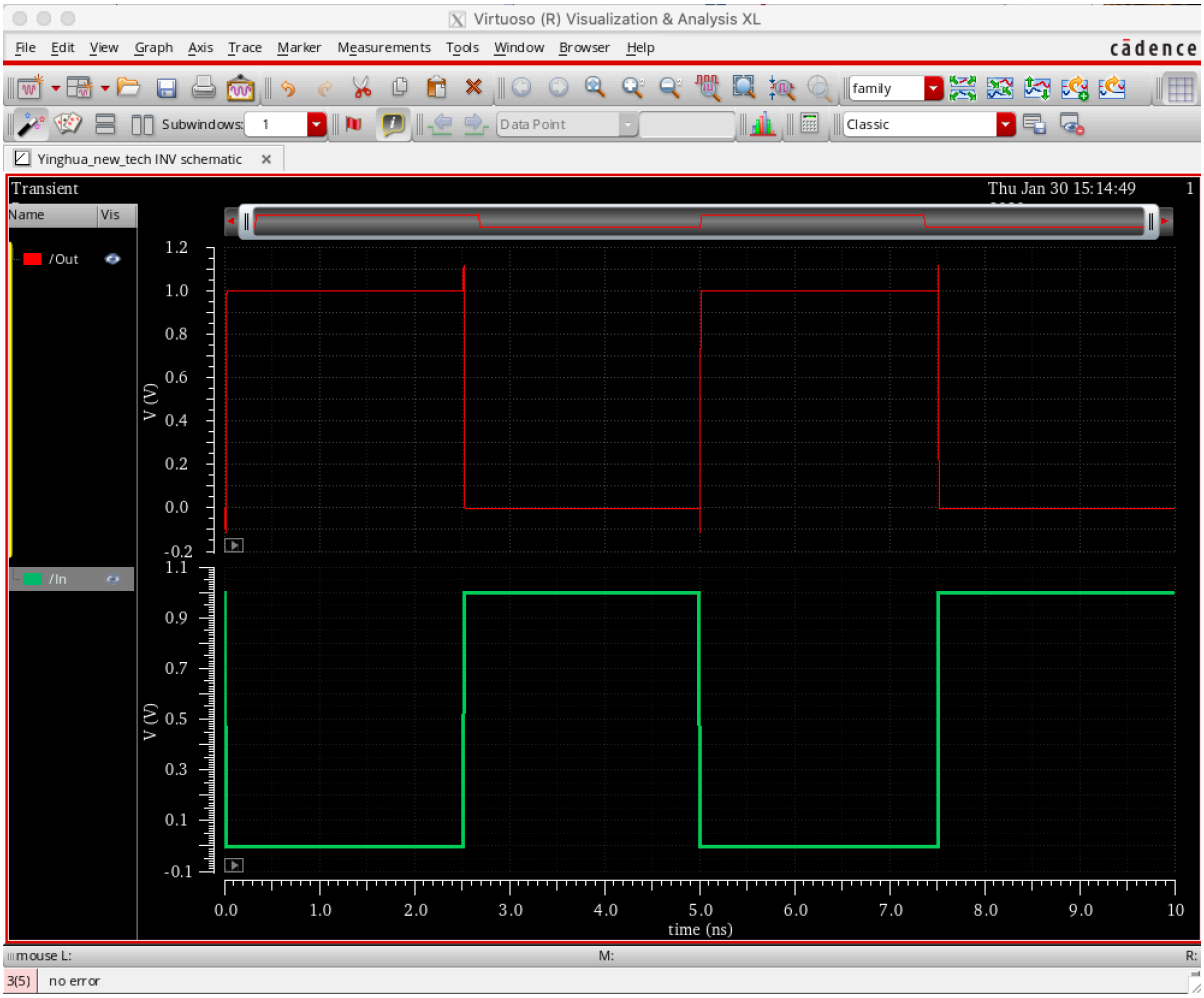
- Select Simulation type and enable it.



- Select nodes to be observed.

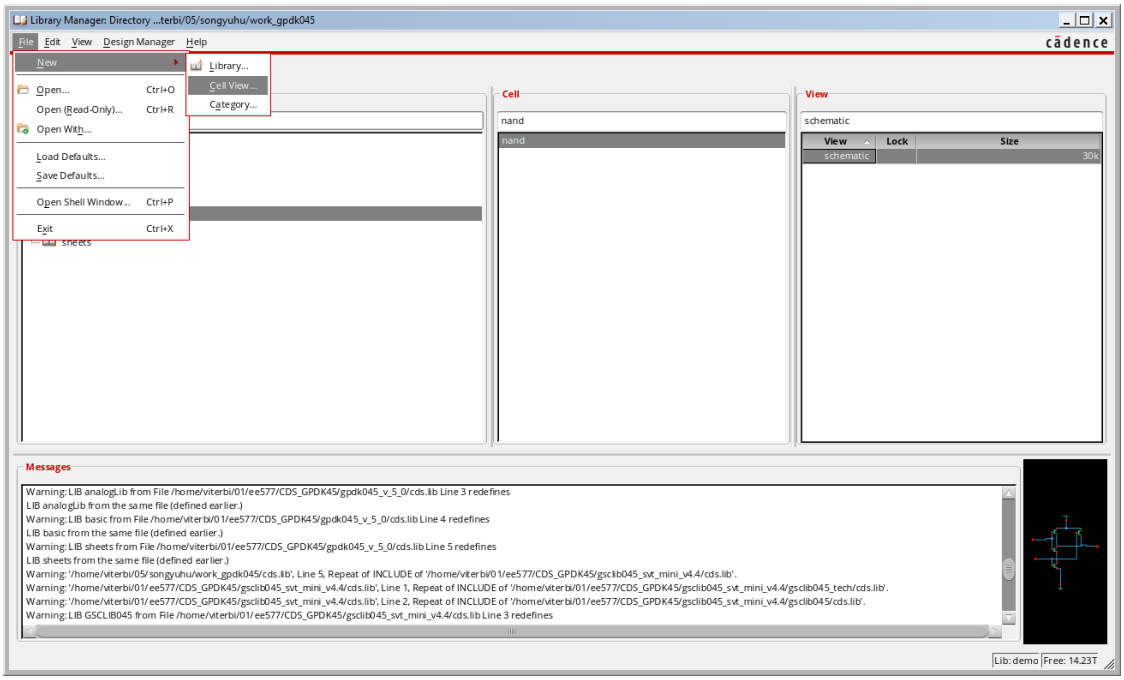


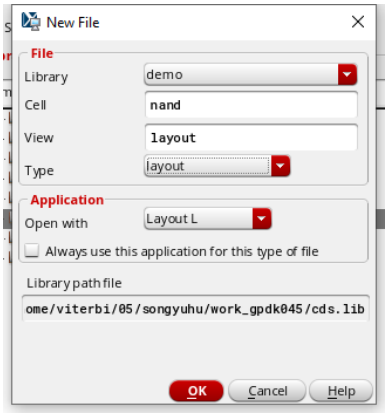
Run simulation by clicking the greed button on the right.



4. Layout design

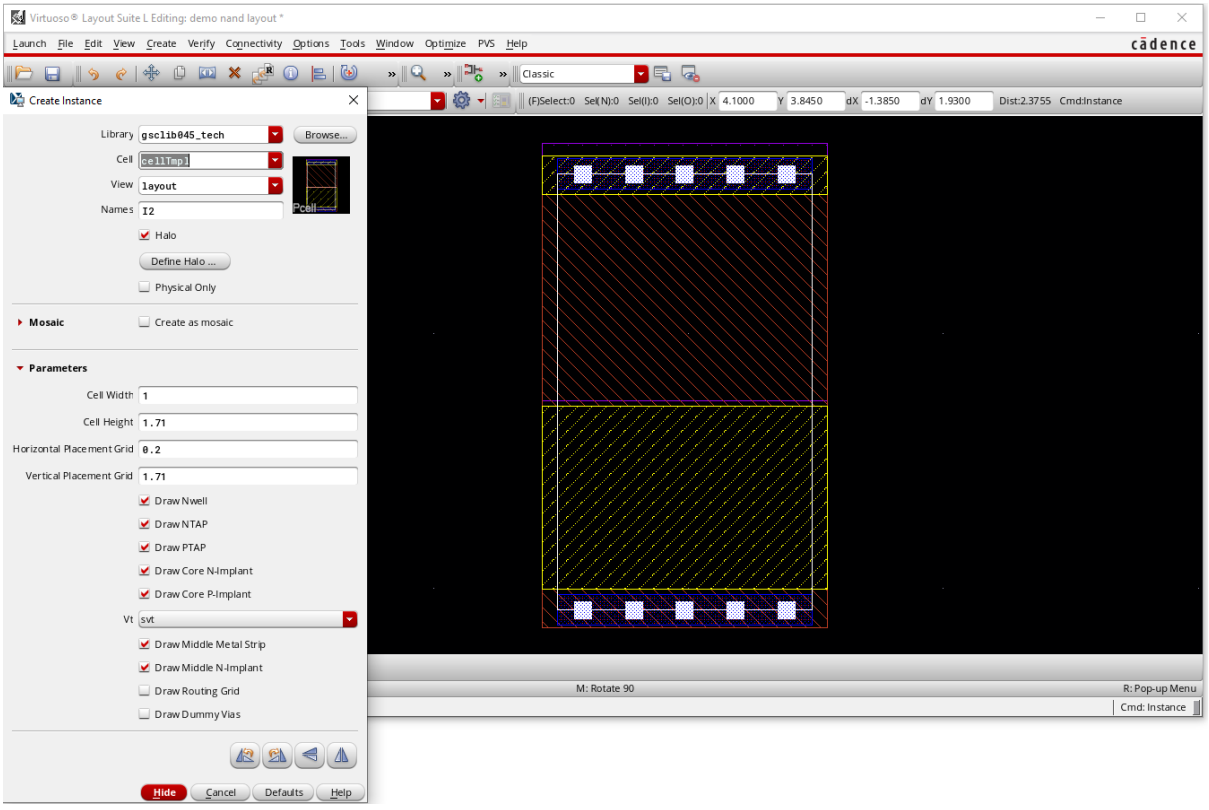
- Create a new Cell View for layout



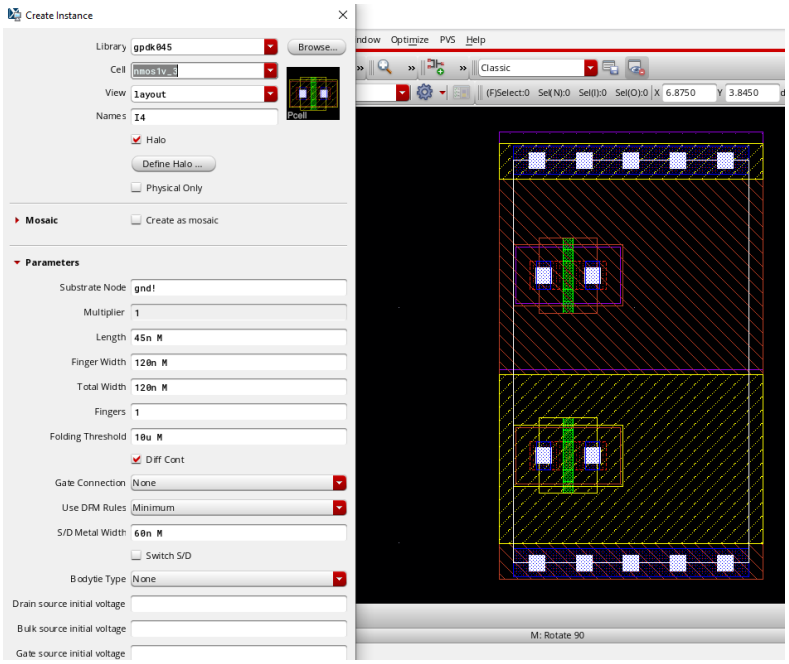


- Create -> instance
- Firstly, create cell template for your design. It is in the **gsclib045_tech** library. You can change the width or height for your cell template.

  NOTE: For most of the cases, we recommend you keep the default cell height and only change the cell width. In some rare cases where the width MOS device is extremely large, you may adjust the cell height.

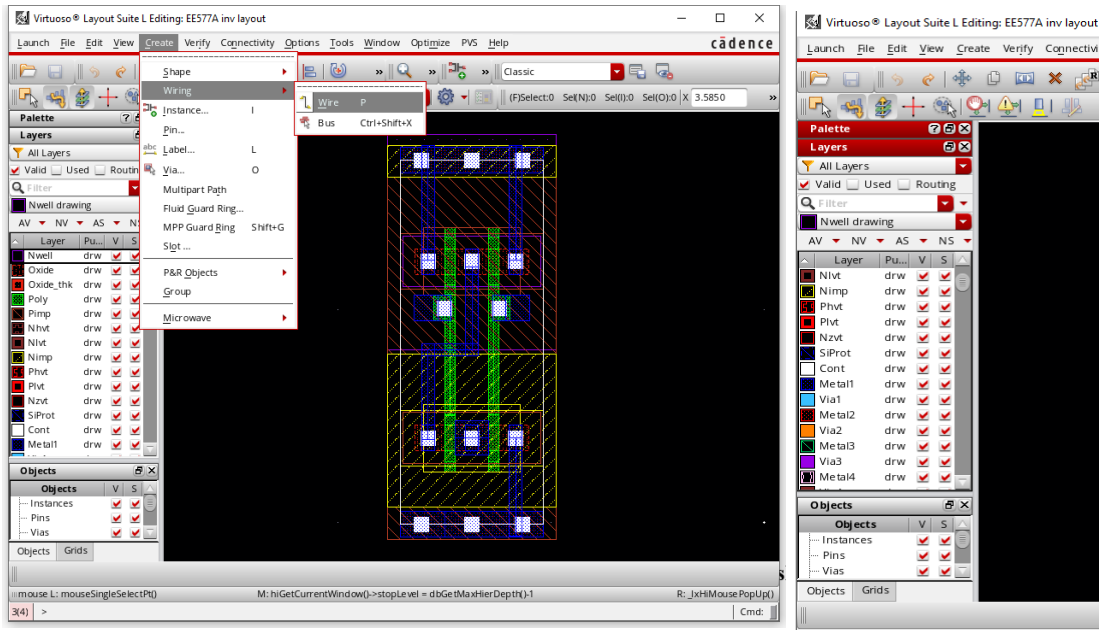


- You should select the **gpdk045** library and use **pmos1v_3** or **nmos1v_3** to draw Pmos and Nmos.
- You can modify Width of transistors by changing **Finger Width or Fingers as shown below**.



- Create->Wiring->Wire

  Use wire to connect every component. Make sure the logic for layout design is same as the logic for your schematic design. You can choose different layers to draw your wire.



- Create->Via

  If you want to connect different layers, you need create Via to connect them.

  For example, we create a via for Metal 1 to Poly.

  Tips: if you want to connect Metal 5 to Metal 1, you need create all of Vias between them.

- Create->Pin

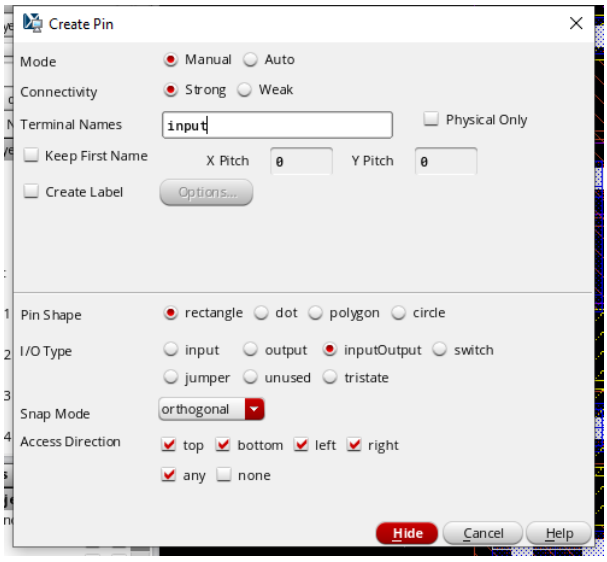
  You need create all of pins in your schematic by doing this step.

  For input, select I/O type to ‘input’.

  For output, select I/O type to ‘output’.

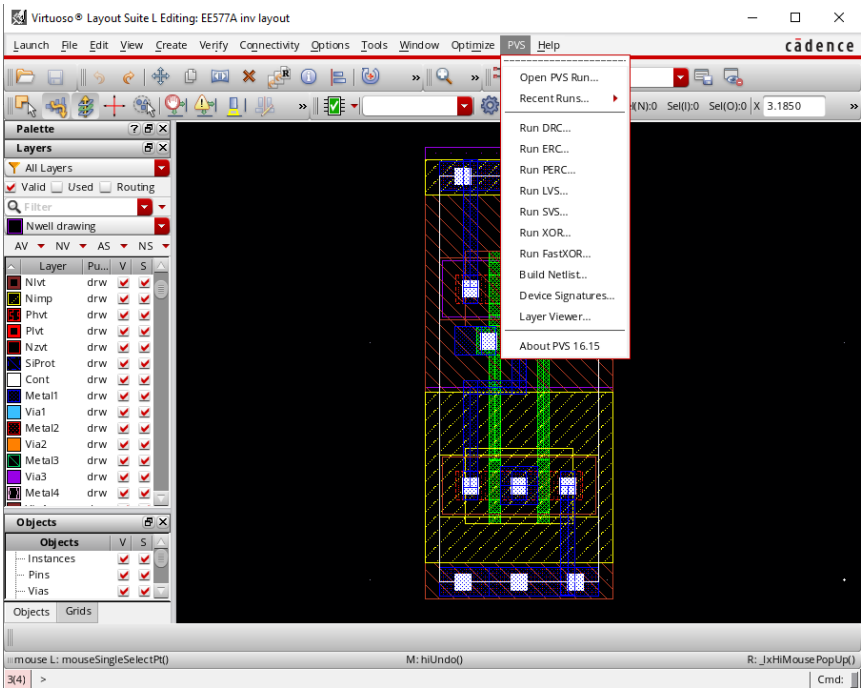
  For GND and VDD, select I/O type to ‘input output’.

  You can also choose the different layers to draw the pins.

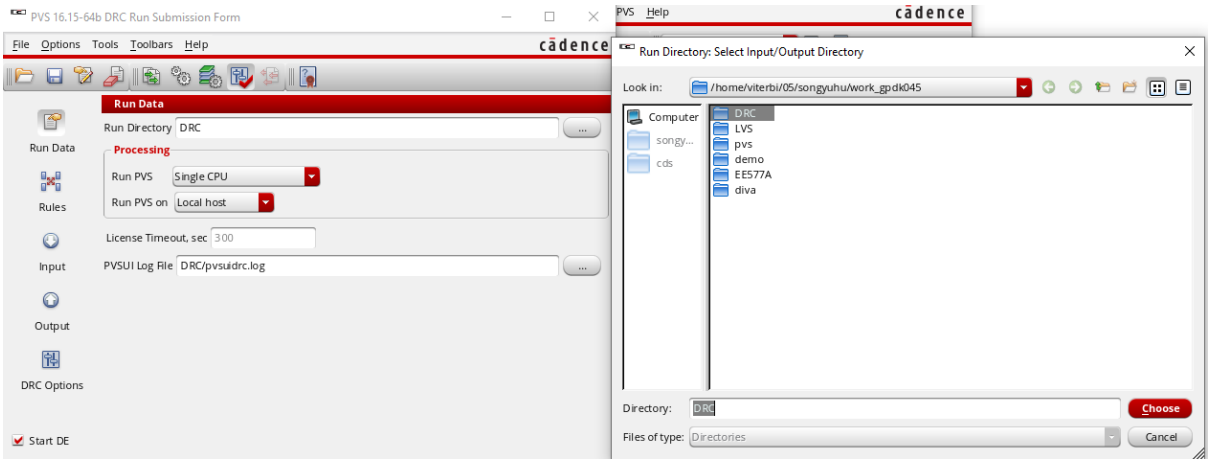


- Make sure that all your components are in the cell template. You can change the width or height of cell template to meet this requirement.
- Run DRC (Design Rules Check)

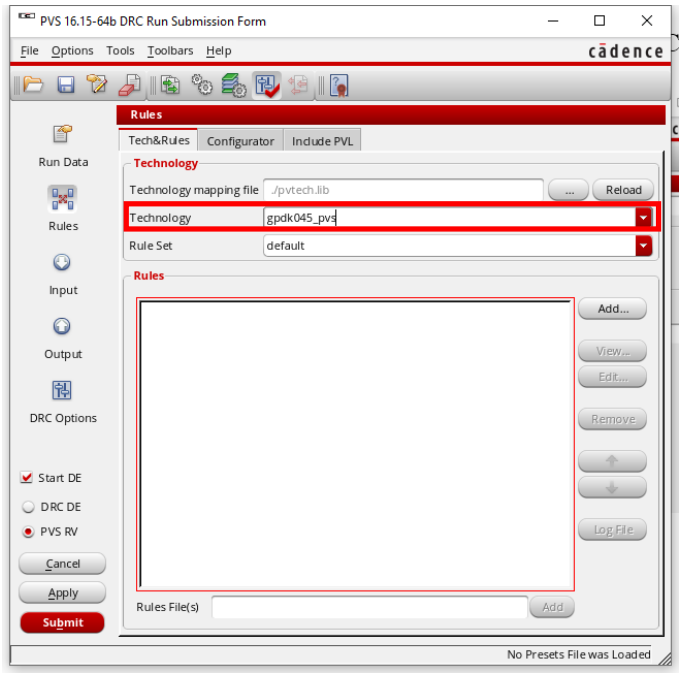
- PVS -> Run DRC



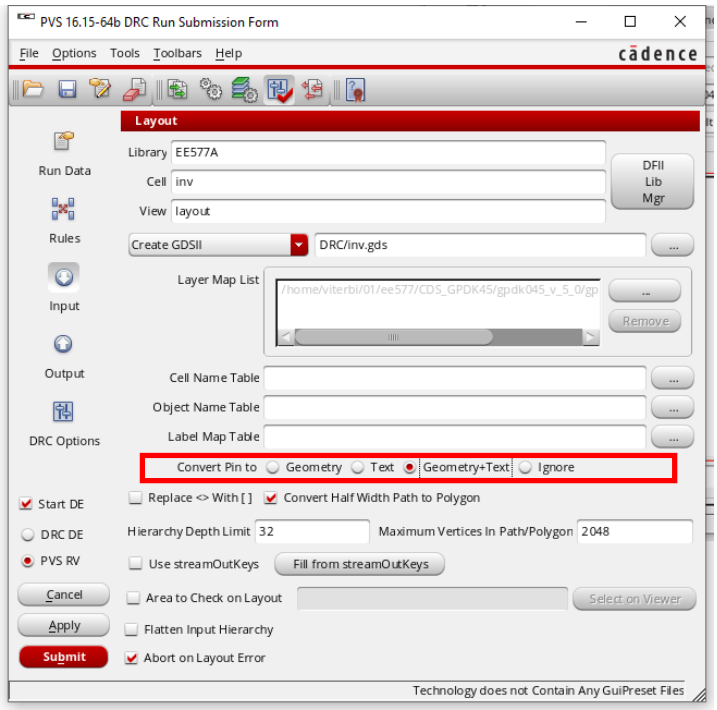
- Run data -> Choose Run Directory as ‘DRC’



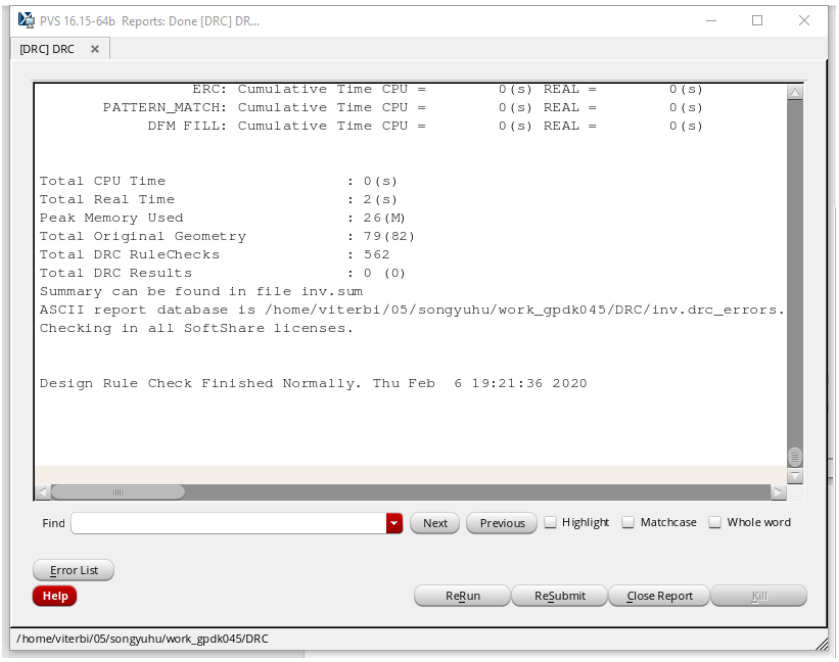
- Rules -> choose Technology as gpdk045_pvs

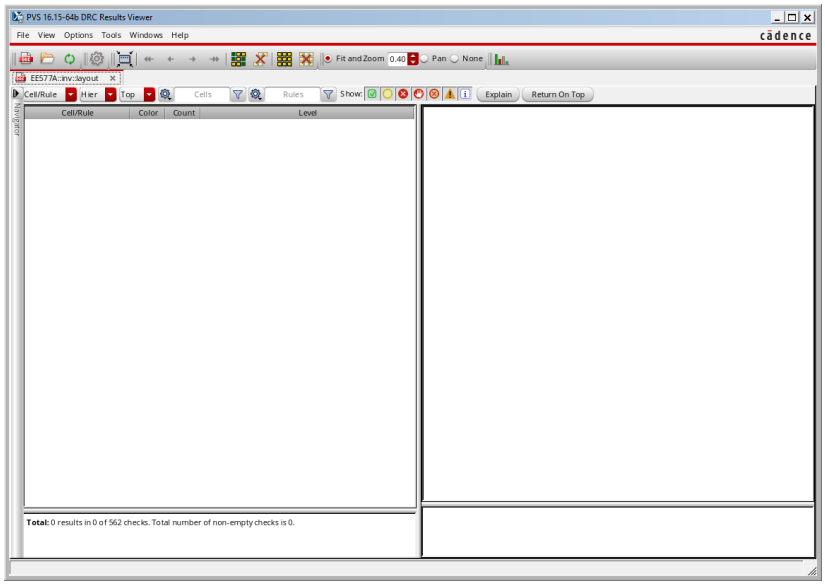


- Input -> choose ‘Convert Pin to’ as ‘Geometry + Text’
- You can check whether you run the correct Library, Cell and View

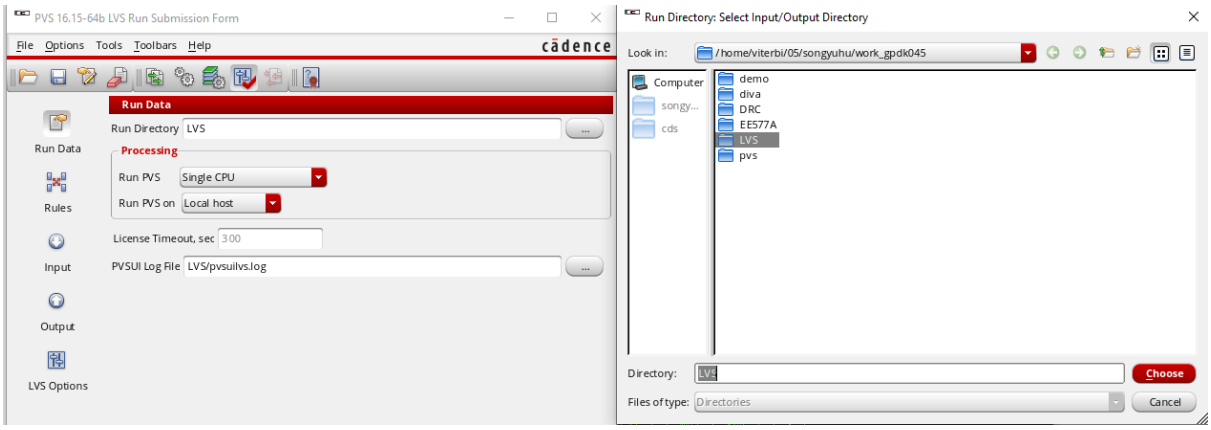


- Click ‘Submit’
- You can see if you have errors in the DRC and see some details about it.
- After you correct your errors and save the design, you can click ‘ReRun’ to run it again.

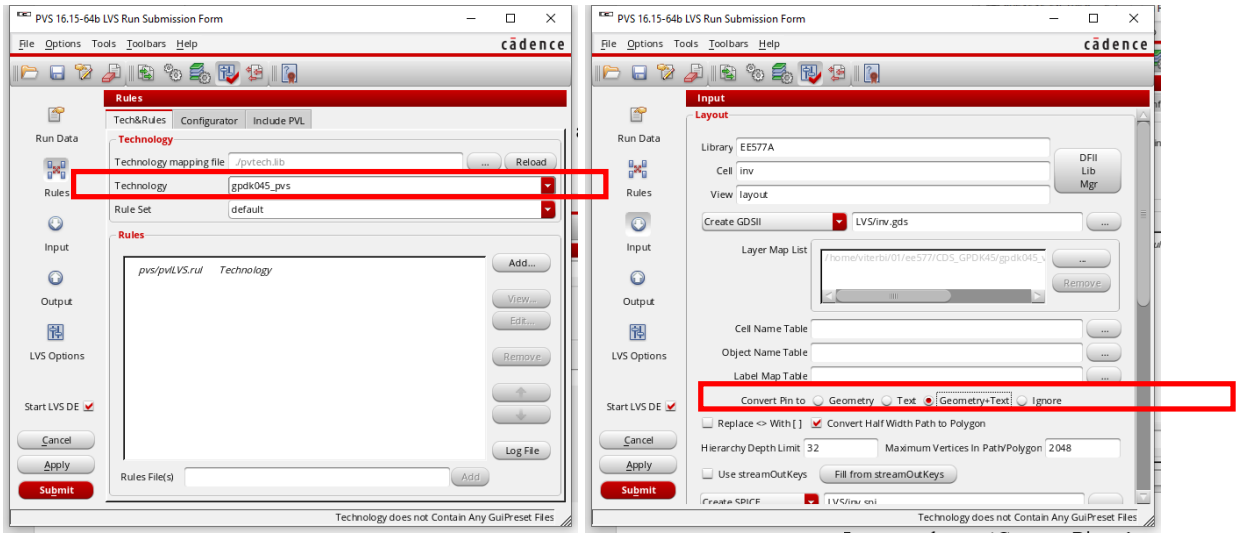




- Run LVS (Layout VS Schematic)
- PVS -> Run ~~DRC~~ LVS
- Run data -> Choose Run Directory as ‘LVS’

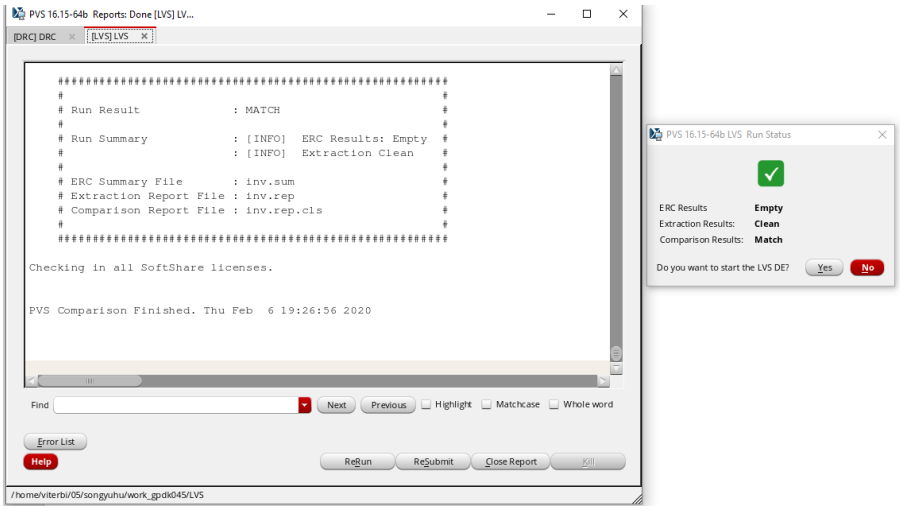


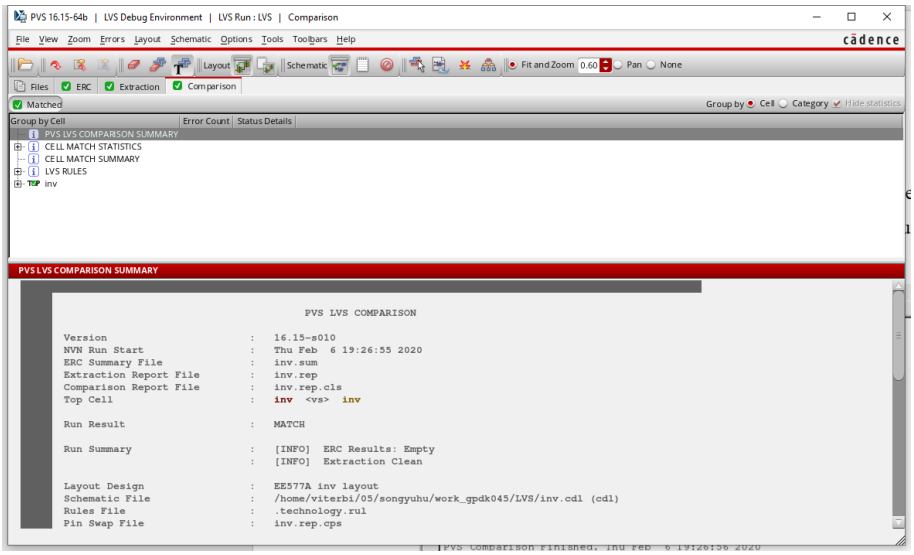
- Rules -> choose Technology as gpdk045_pvs



- Input -> choose ‘Convert Pin to’ as ‘Geometry + Text’
- You can check whether you run the correct Library, Cell and View

- Click ‘Submit’
- You can see if you have errors in the LVS and see some details about it.
- When you correct your errors, you can click ‘ReRun’ to run it again.



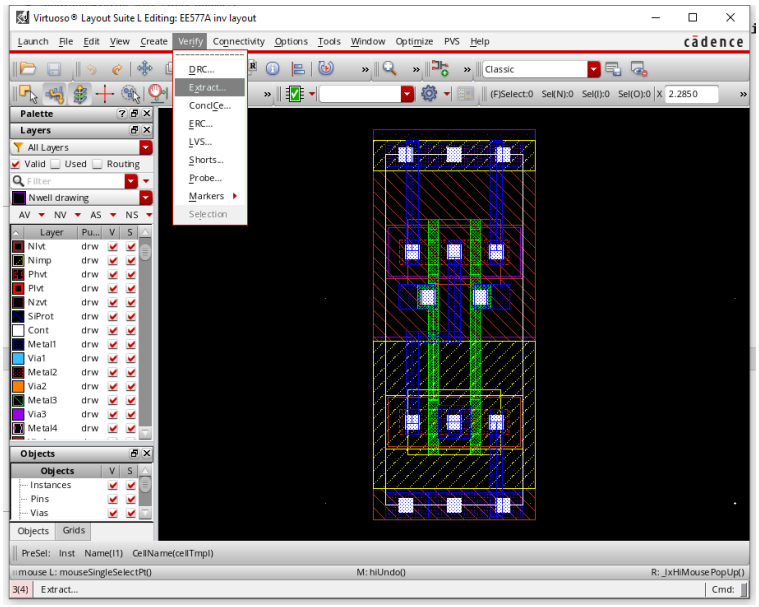


- Run simulation for layout design
- When you have the correct DRC and LVS for your layout design, you can start to simulate your layout design by extracting it firstly.
- Firstly, you need copy diva folder to ‘work_gpdk045’ by typing the command below in your home directory. (You only need to perform this step once)

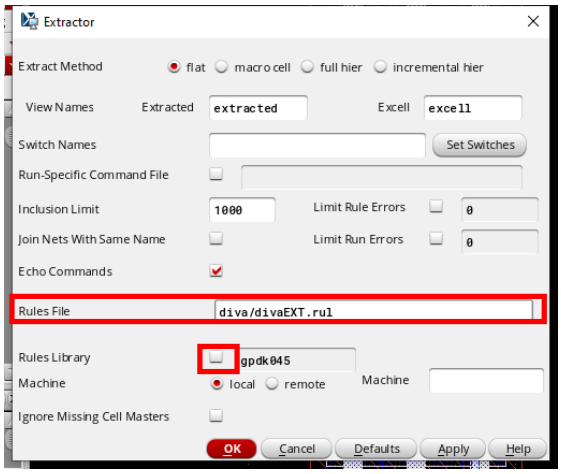
```
cp -r ~ee577/CDS_GPDK45/gpdk045_v_5_0/diva ~/work_gpdk045/
```

```
[yinghuah@viterbi-scf2 ~]$ cp -r ~ee577/CDS_GPDK45/gpdk045_v_5_0/diva ~/work_gpd
k045/
```

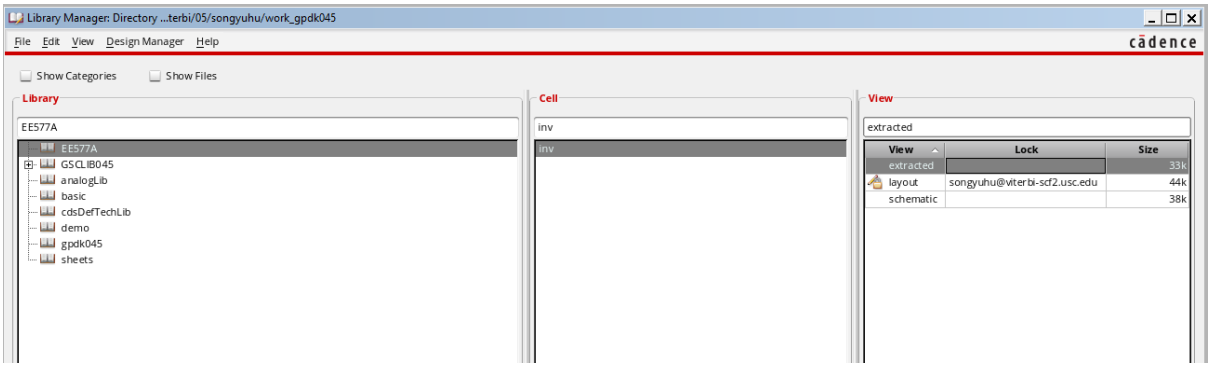
- Verify -> Extract



- In Rules File: ‘diva/divaEXT.rul’
- Deselect Rules Library
- Click ‘OK’



- You will see the extracted cell view in your library. Open it.



- Then you can run the simulation in the extracted file. The way to run the simulation is same as the method to run it in the schematic design.