|  |  |  |  |
| --- | --- | --- | --- |
| PHASE1 | | | |
| Project name |  | | |
| Document ref |  | | |
| Version | 1.0 | | |
| Release date | 20220403 | | |
| Author | Haoda Wang; Jason Yik; Wu Fei | | |
| Classification |  | | |
| Distribution List | phase1-W; phase2-H&J | | |
| Approved by | Name | Signature | Date |
|  |  |  |  |



**Ming Hsieh Department of Electrical Engineering**

**University of Southern California, Los Angeles, CA 90089**

**Spring 2022**

**EE 477**

Revision History

|  |  |  |  |
| --- | --- | --- | --- |
| **Date** | **Version** | **List of changes** | **Author + Signature** |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |

C A T A L O G

[1 Motivation 1](#_Toc99878203)

[2 Part 1: Multiplier 2](#_Toc99878204)

[3 Part 2: Divider 8](#_Toc99878205)

# Motivation

[Motivation](https://blackboard.usc.edu/webapps/blackboard/content/listContent.jsp?course_id=_294497_1&content_id=_8570577_1)

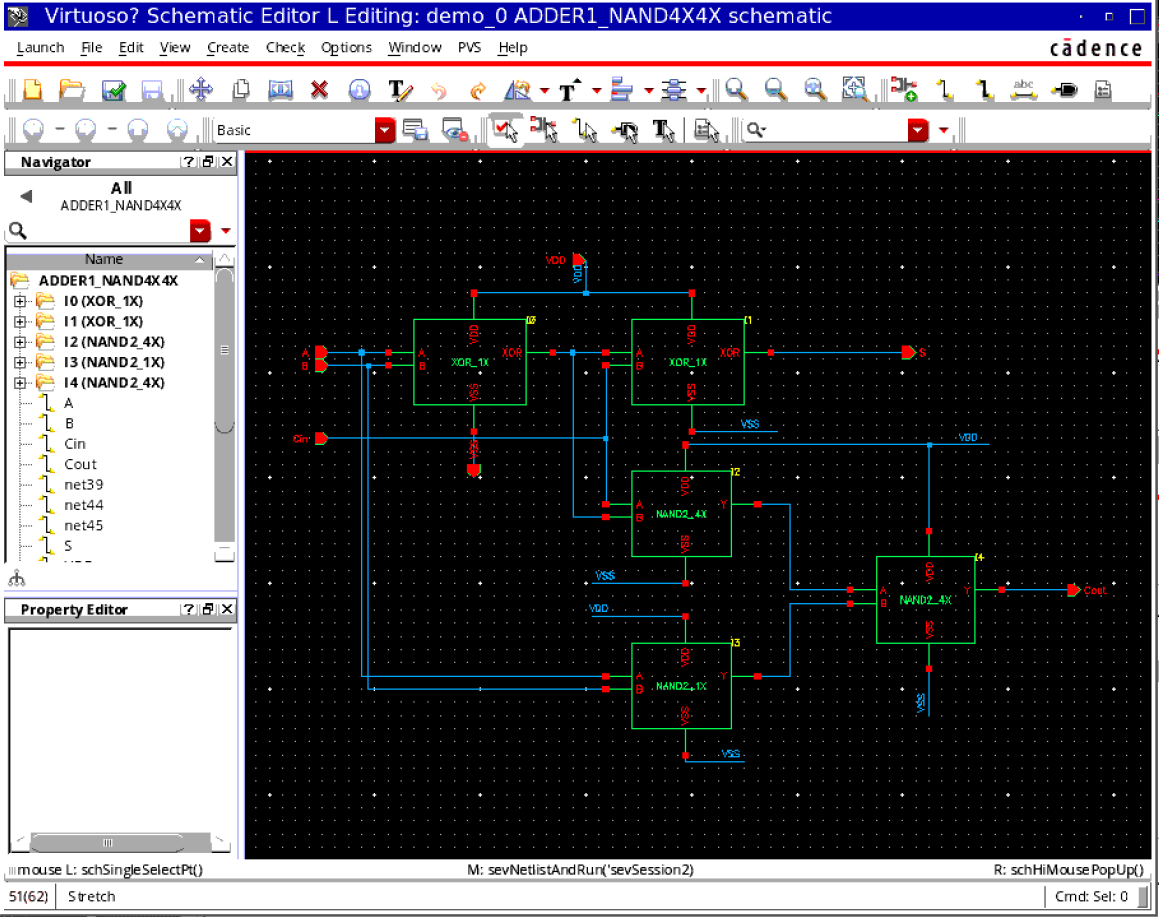
Multipliers and dividers are common arithmetic operations performed using the basic units adder and subtractor. For the final project, you will design a multiplier and divider to operate on 4-bit inputs.

# Part 1: Multiplier

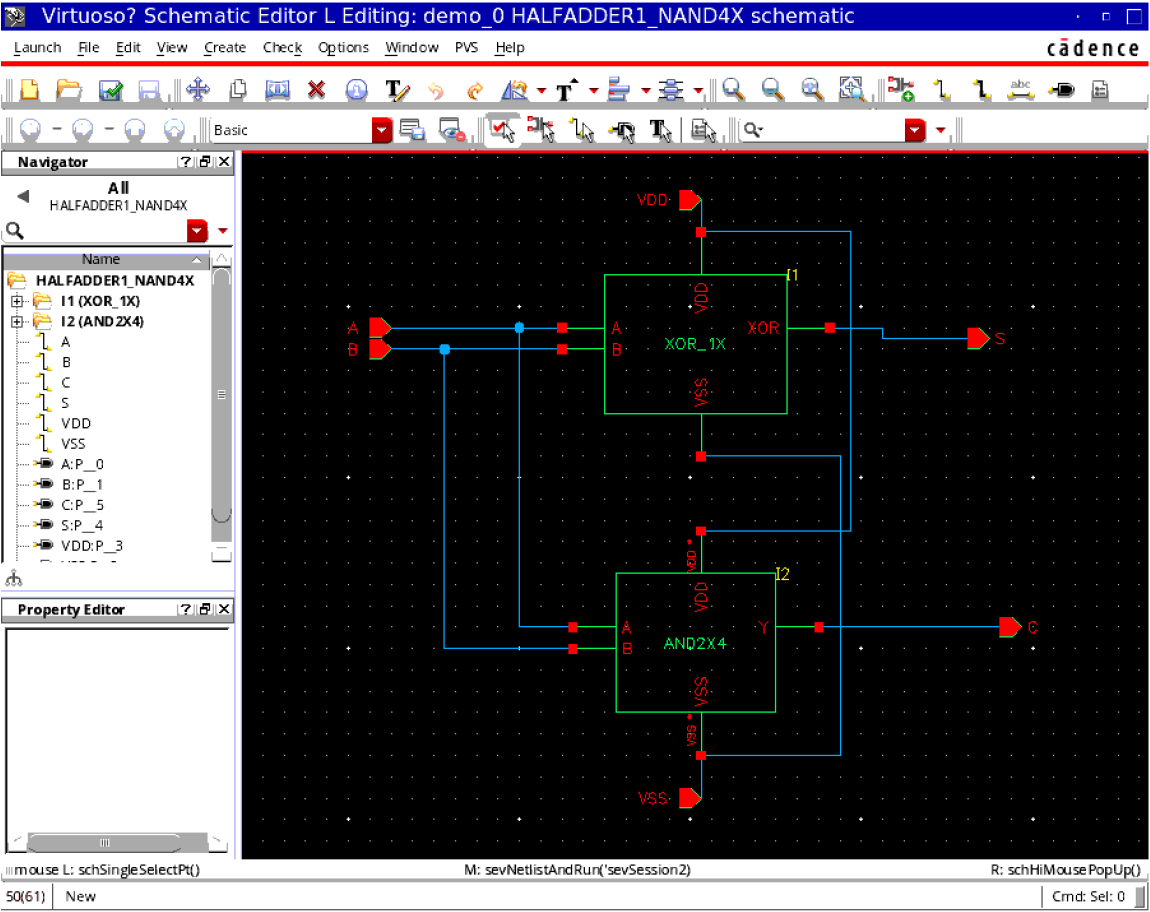
**Notes**:

Input A = {a3a2a1a0}, Input B = {b3b2b1b0}, Output product Z = {z7z6z5z4z3z2z1z0}

FA = Single bit Full Adder,



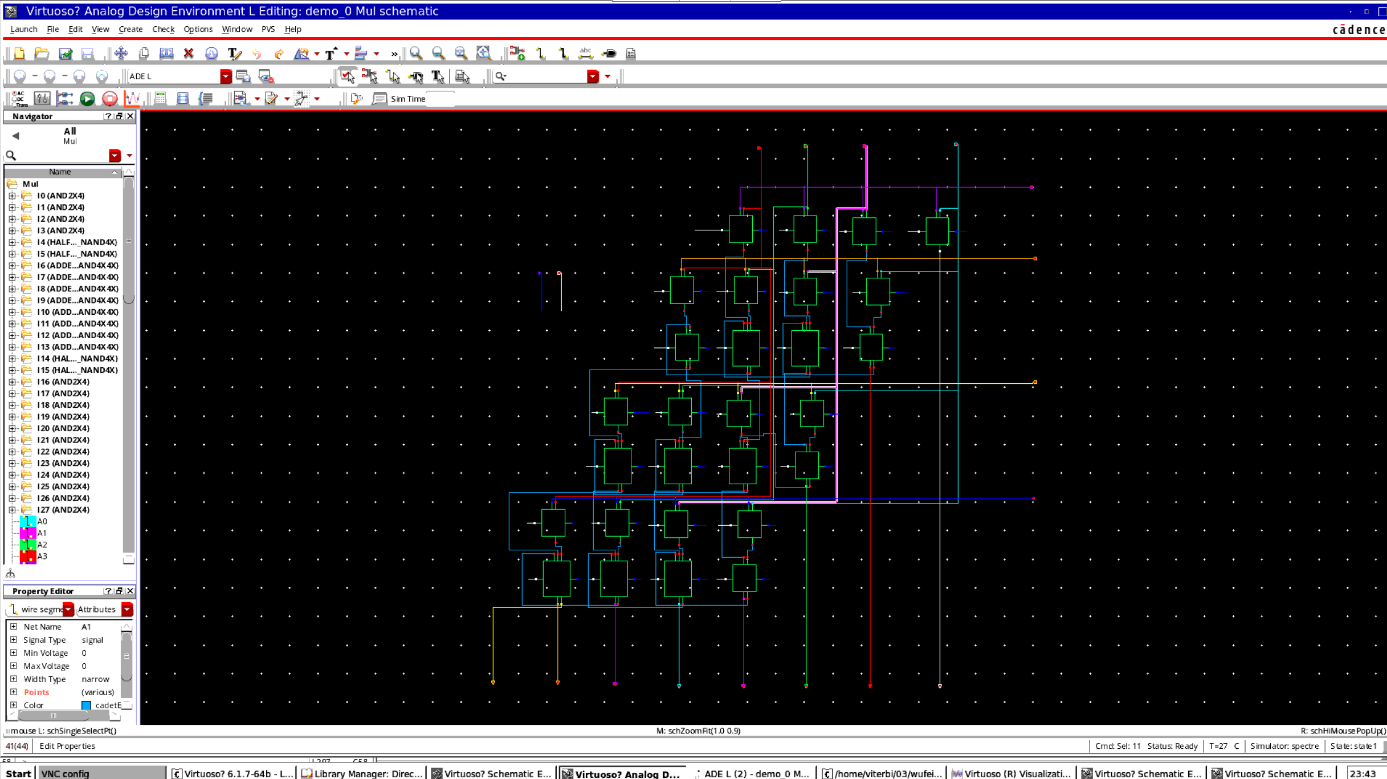
HA = Single bit Half Adder



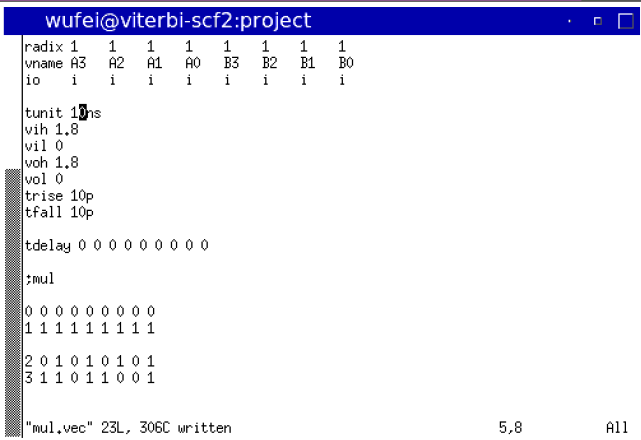
All blue-colored logic gates are 2-input AND

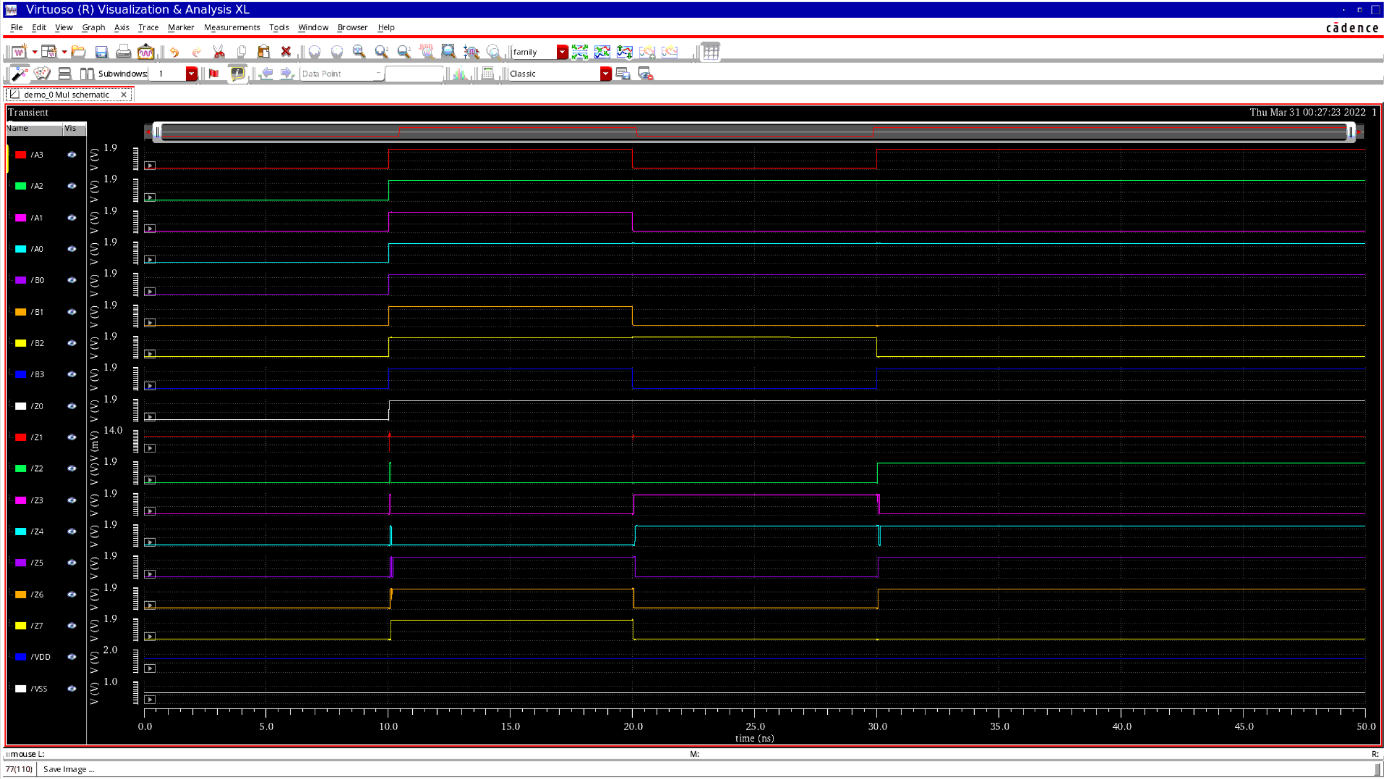
**Procedure**:

Design the schematic for the 4x4 multiplier as shown.



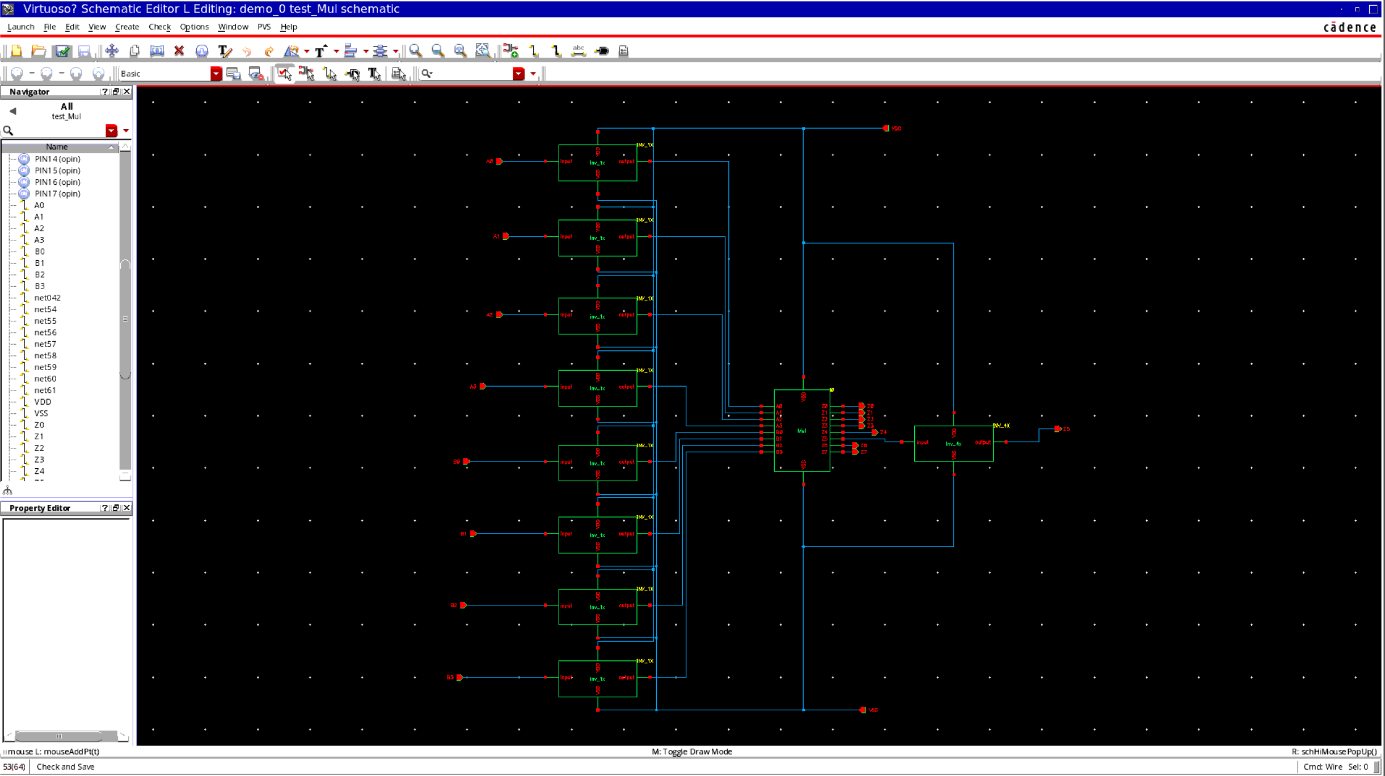
Do functionality verification using at least 3 input combinations.





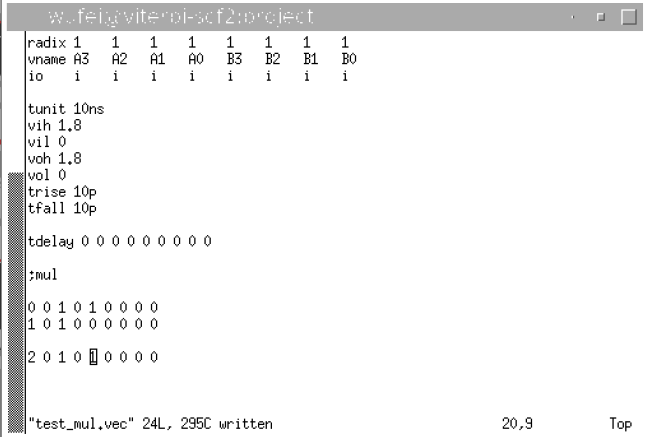
Design a delay measurement circuit where each input has inv\_1X preceding it.

Connect inv\_4X to output z5. Use this input transition:

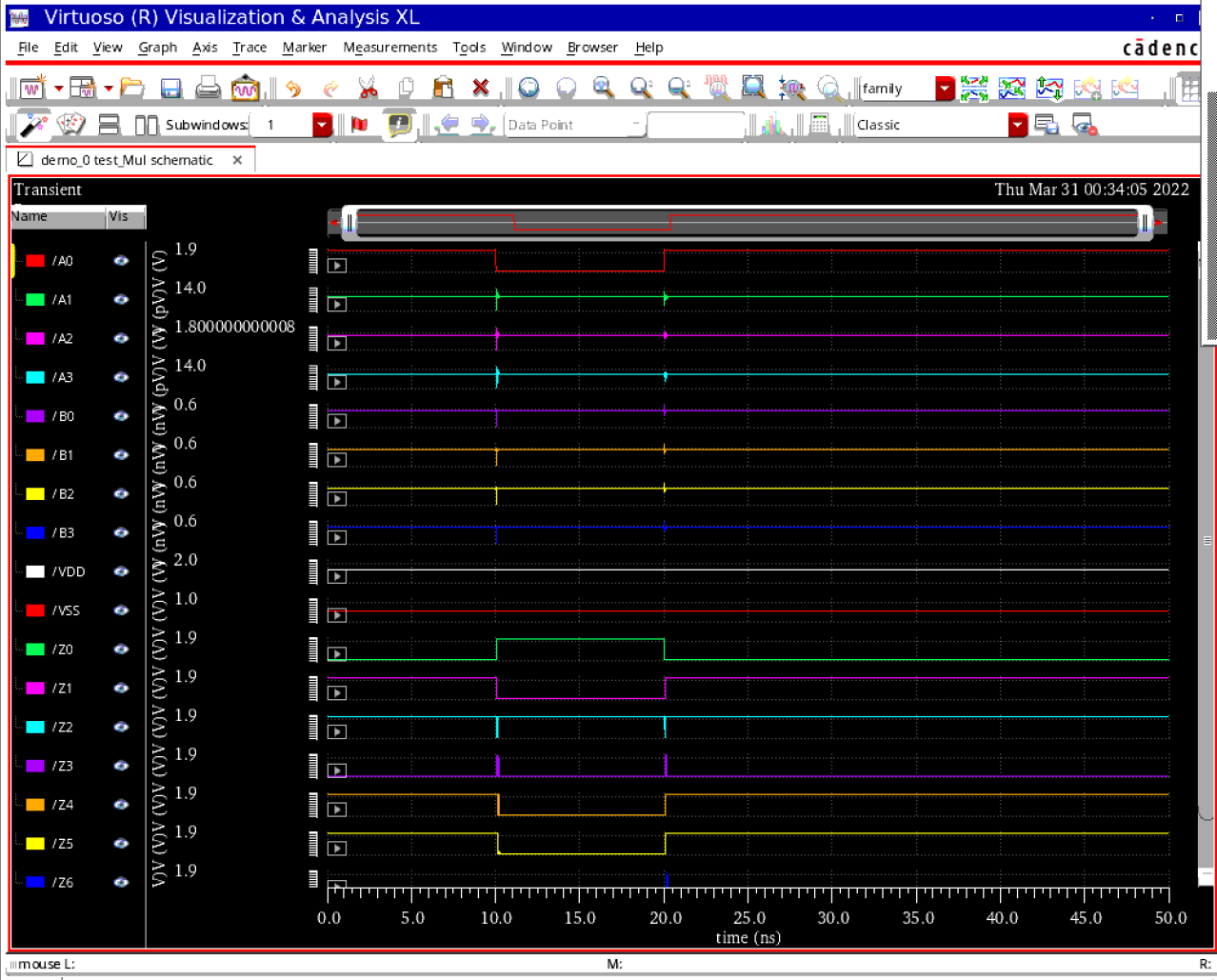


    b3,b2,b1,b0,a3,a2,a1 = 1 1 1 1 1 0 1 (fixed)

a0 goes from 0->1->0

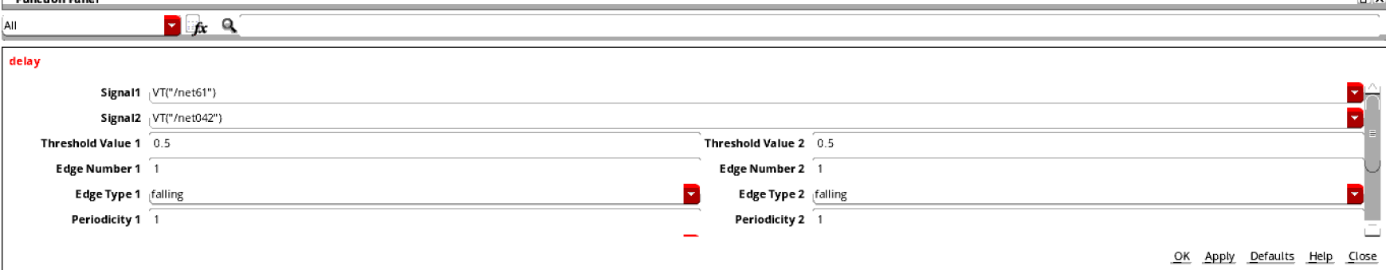


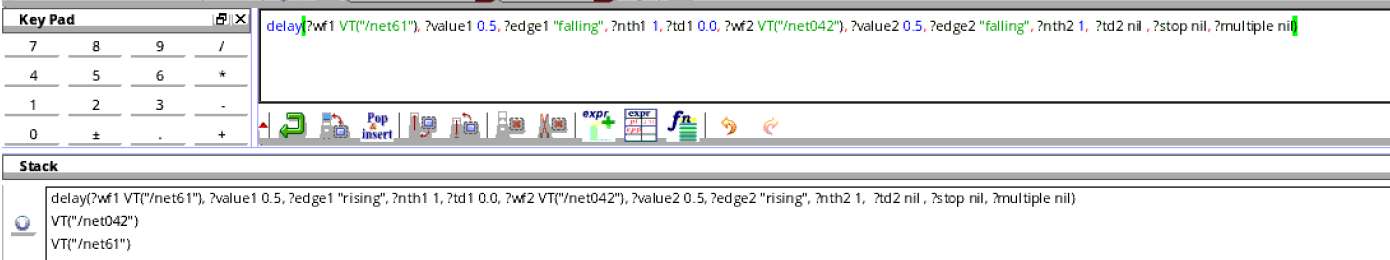
This will make z5 go from 0->1->0

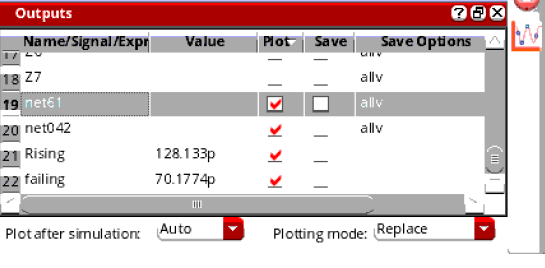




Measure the rising and falling propagation delay from a0 to z5

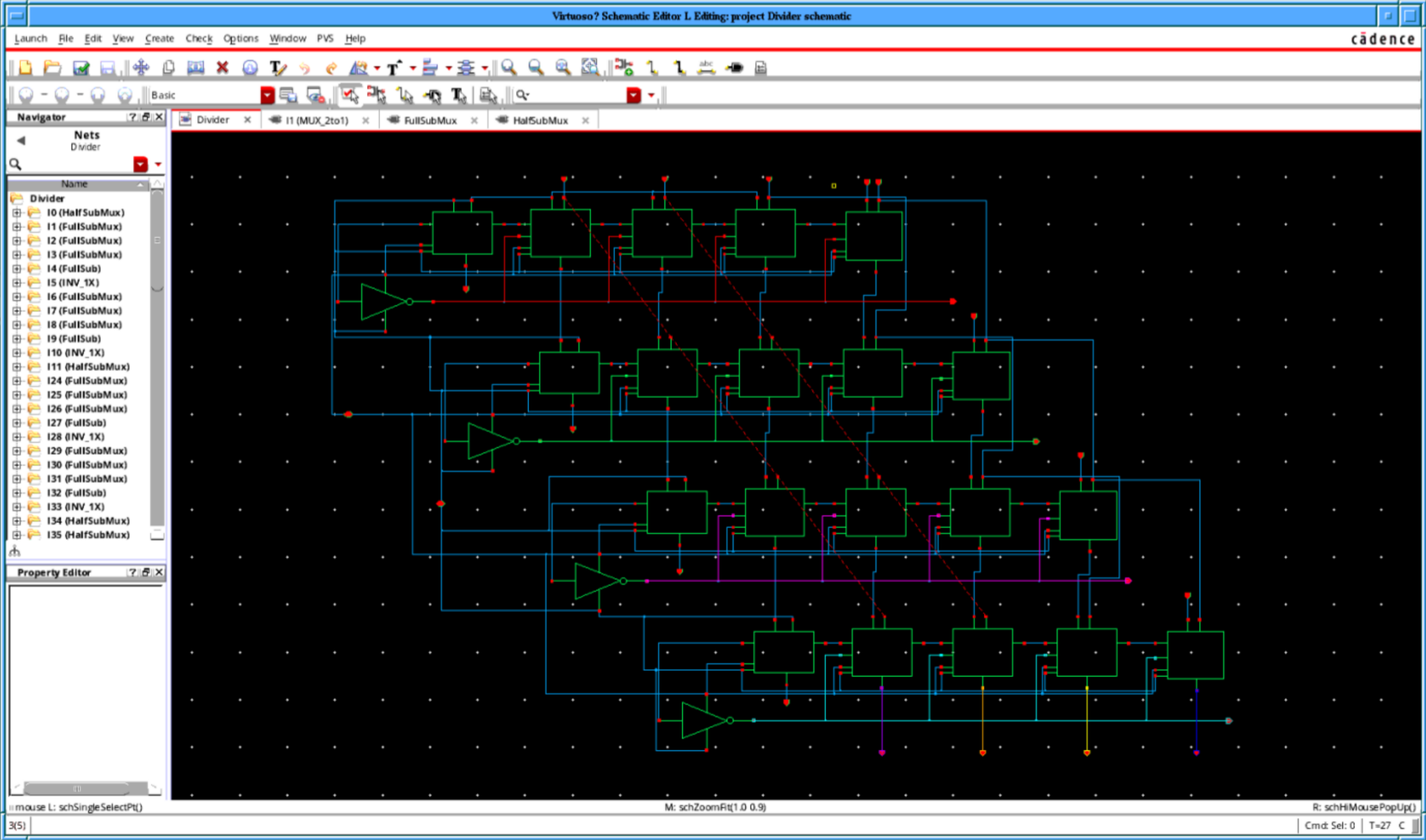




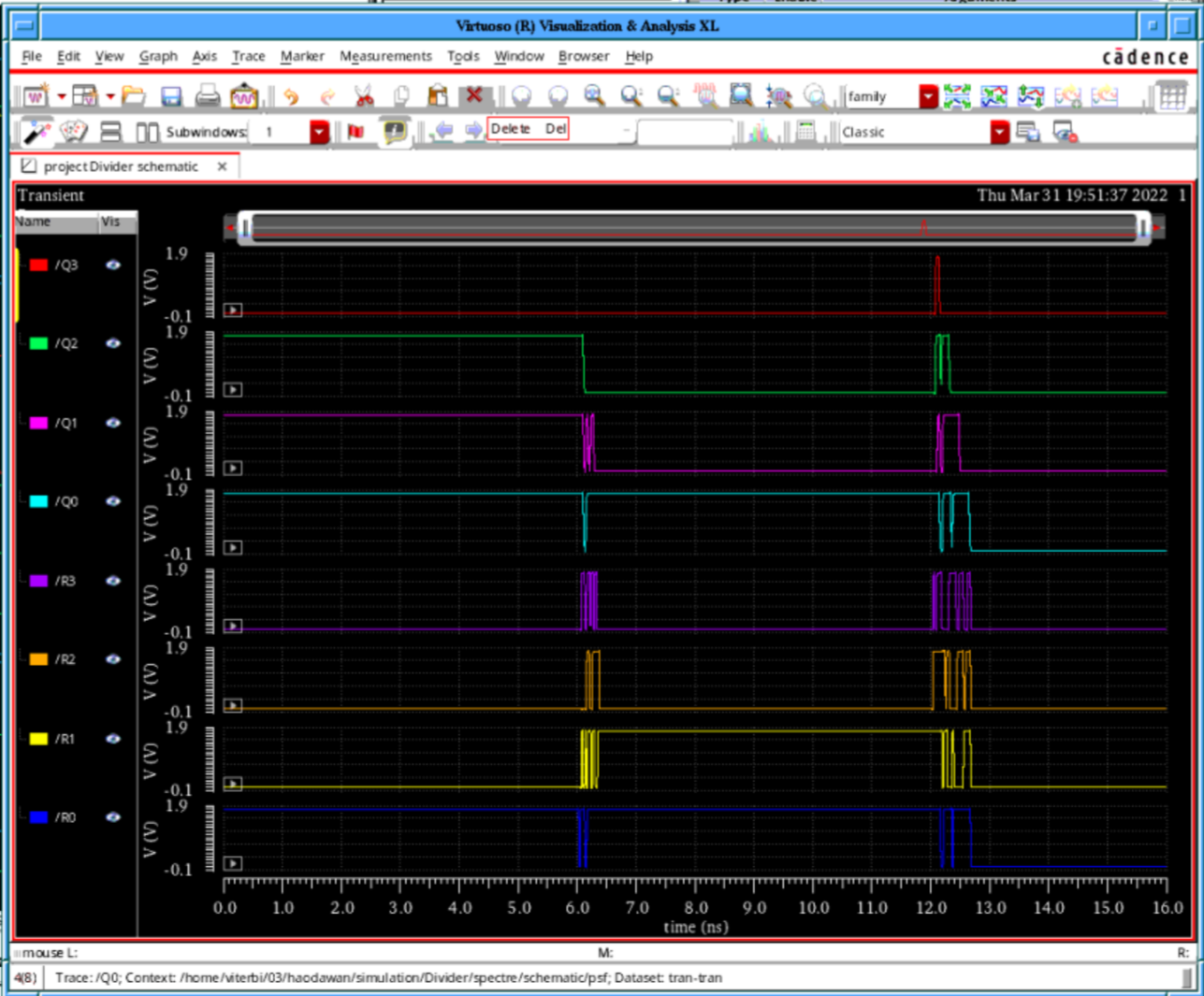


**Remember**: Given a and b values are inputs to the actual multiplier, so inputs to the preceding inverters should be the opposite.

# Part 2: Divider



Do functionality verification using at least 3 input combinations:



|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Test** | **D** | **d** | **Expected Q** | **Expected R** |
| 1 | 1111 | 0010 | 0111 | 0001 |
| 2 | 1000 | 0101 | 0001 | 0011 |
| 3 | 0000 | 0001 | 0000 | 0000 |