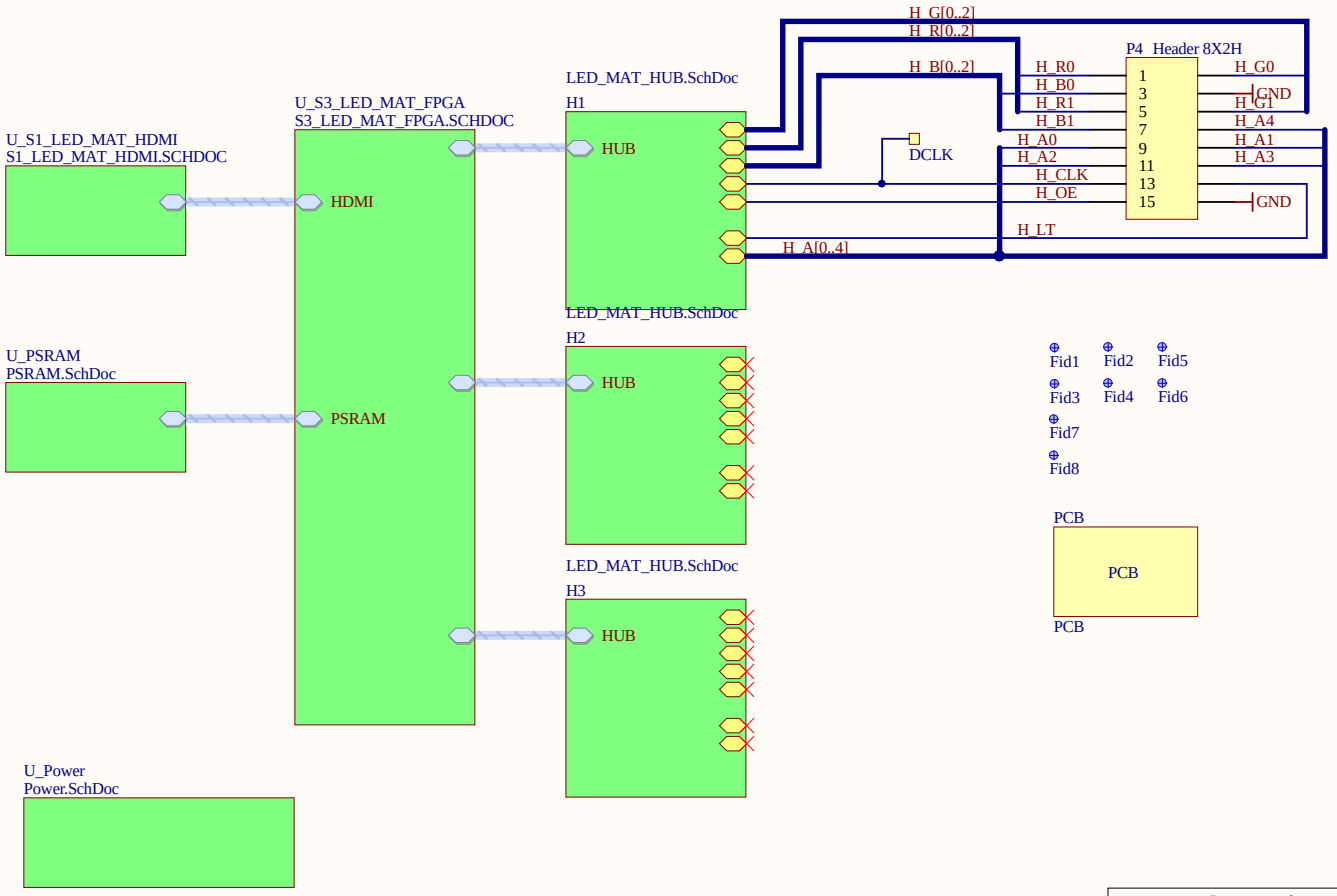
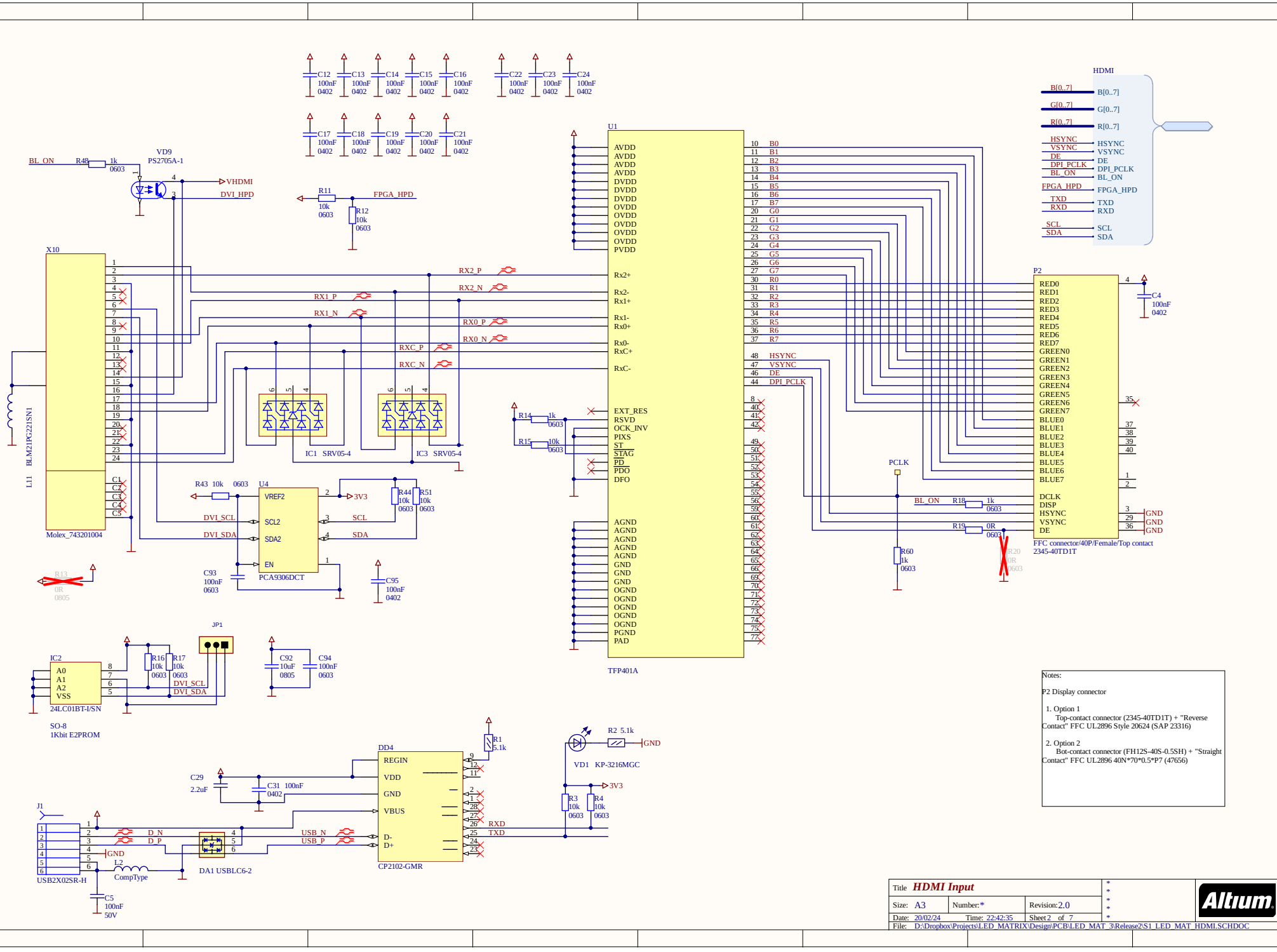
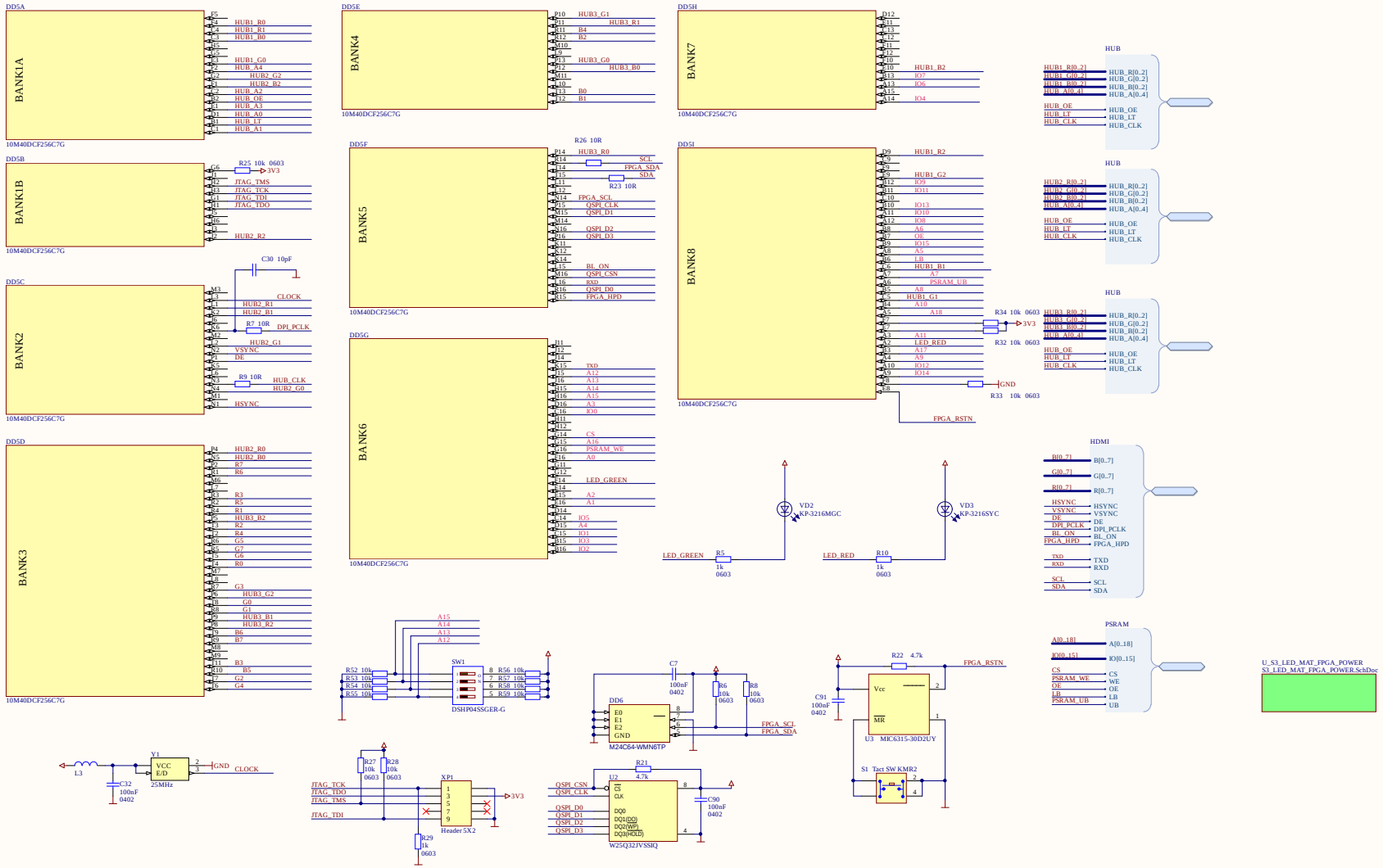


Title	***Top Connections***		
Size: A4	Number:	Revision:2.0	
Date: 20/02/24	Time: 22:42:35	Sheet 1 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\Top.SchDoc			


HDMI
B[0..7]
G[0..7]
R[0..7]
HSYNC
VSYNC
DE
DPI_PCLK
BL_ON
FPGA_HPD
TXD
RXD
SCL
SDA
U1
TFP401A
AVDD
DVDD
OVDD
PVDD
Rx2+
Rx2-
Rx1+
Rx1-
Rx0+
Rx0-
RxC+
RxC-
EXT_RES
RSVD
OCK_INV
PIXS
ST
STAG
PD
PDO
DFO
AGND
GND
OGND
PGND
PAD
B0
B1
B2
B3
B4
B5
B6
B7
G0
G1
G2
G3
G4
G5
G6
G7
R0
R1
R2
R3
R4
R5
R6
R7
HSYNC
VSYNC
DE
DPI_PCLK
P2
RED0
RED1
RED2
RED3
RED4
RED5
RED6
RED7
GREEN0
GREEN1
GREEN2
GREEN3
GREEN4
GREEN5
GREEN6
GREEN7
BLUE0
BLUE1
BLUE2
BLUE3
BLUE4
BLUE5
BLUE6
BLUE7
DCLK
DISP
HSYNC
VSYNC
DE
GND
FFC connector/40P/Female/Top contact
2345-40TD1T
C4 100nF 0402
PCLK
R60 1k 0603
BL_ON R18 1k 0603
R19 0R 0603
R20 0R 0603
C12 100nF 0402
C13 100nF 0402
C14 100nF 0402
C15 100nF 0402
C16 100nF 0402
C17 100nF 0402
C18 100nF 0402
C19 100nF 0402
C20 100nF 0402
C21 100nF 0402
C22 100nF 0402
C23 100nF 0402
C24 100nF 0402
BL_ON R48 1k 0603
VD9 PS2705A-1
VHDMI
DVI_HPD
R11 10k 0603
R12 10k 0603
FPGA_HPD
X10
Molex_743201004
L11 BLM21PG221SN1
RX2_P
RX2_N
RX1_P
RX1_N
RX0_P
RX0_N
RXC_P
RXC_N
IC1 SRV05-4
IC3 SRV05-4
R14 1k 0603
R15 10k 0603
R43 10k 0603
U4
PCA9306DCT
VREF2
SCL2
SDA2
EN
3V3
DVI_SCL
DVI_SDA
SCL
SDA
R44 10k 0603
R51 10k 0603
C93 100nF 0603
C95 100nF 0402
R13 0R 0805
JP1
IC2
24LC01BT-I/SN
SO-8
1Kbit E2PROM
A0
A1
A2
VSS
R16 10k 0603
R17 10k 0603
C92 10uF 0805
C94 100nF 0603
DD4
CP2102-GMR
REGIN
VDD
GND
VBUS
D-
D+
R1 5.1k
C29 2.2uF
C31 100nF 0402
VD1 KP-3216MGC
R2 5.1k
R3 10k 0603
R4 10k 0603
RXD
TXD
J1
USB2X02SR-H
D_N
D_P
USB_N
USB_P
DA1 USBLC6-2
L2
CompType
C5 100nF 50V
Notes:
P2 Display connector
1. Option 1
Top-contact connector (2345-40TD1T) + "Reverse Contact" FFC UL2896 Style 20624 (SAP 23316)
2. Option 2
Bot-contact connector (FH12S-40S-0.5SH) + "Straight Contact" FFC UL2896 40N*70*0.5*P7 (47656)
Title HDMI Input
Size: A3
Number: *
Revision: 2.0
Date: 20/02/24
Time: 22:42:35
Sheet 2 of 7
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\S1_LED_MAT_HDMI.SCHDOC
Altium


DD5A
BANK1A
10M40DCF256C7G
HUB1_R0
HUB1_R1
HUB1_B0
HUB1_G0
HUB_A4
HUB2_G2
HUB2_B2
HUB_A2
HUB_OE
HUB_A3
HUB_A0
HUB_LT
HUB_A1
DD5B
BANK1B
R25 10k 0603
3V3
JTAG_TMS
JTAG_TCK
JTAG_TDI
JTAG_TDO
HUB2_R2
DD5C
BANK2
C30 10pF
CLOCK
HUB2_R1
HUB2_B1
R7 10R
DPI_PCLK
HUB2_G1
VSYNC
DE
R9 10R
HUB_CLK
HUB2_G0
HSYNC
DD5D
BANK3
HUB2_R0
HUB2_B0
R7
R6
R3
R5
R1
HUB3_B2
R2
R4
G5
G7
G6
R0
G3
HUB3_G2
G0
G1
HUB3_B1
HUB3_R2
B6
B7
B3
B5
G2
G4
DD5E
BANK4
HUB3_G1
HUB3_R1
B4
B2
HUB3_G0
HUB3_B0
B0
B1
DD5F
BANK5
R26 10R
HUB3_R0
SCL
FPGA_SDA
SDA
R23 10R
FPGA_SCL
QSPI_CLK
QSPI_D1
QSPI_D2
QSPI_D3
BL_ON
QSPI_CSN
RXD
QSPI_D0
FPGA_HPD
DD5G
BANK6
TXD
A12
A13
A14
A15
A3
IO0
CS
A16
PSRAM_WE
A0
LED_GREEN
A2
A1
IO5
A4
IO1
IO3
IO2
DD5H
BANK7
HUB1_B2
IO7
IO6
IO4
DD5I
BANK8
HUB1_R2
IO9
HUB1_G2
IO11
IO13
IO10
IO8
A6
OE
IO15
A5
LB
HUB1_B1
A7
PSRAM_UB
A8
HUB1_G1
A10
A18
R34 10k 0603
R32 10k 0603
A11
LED_RED
A17
A9
IO12
IO14
R33 10k 0603
GND
FPGA_RSTN
HUB
HUB1_R[0..2]
HUB1_G[0..2]
HUB1_B[0..2]
HUB_A[0..4]
HUB_OE
HUB_LT
HUB_CLK
HUB2_R[0..2]
HUB2_G[0..2]
HUB2_B[0..2]
HUB3_R[0..2]
HUB3_G[0..2]
HUB3_B[0..2]
VD2
KP-3216MGC
LED_GREEN
R5
1k
0603
VD3
KP-3216SYC
LED_RED
R10
HDMI
R[0..7]
G[0..7]
B[0..7]
DE
DPI_PCLK
BL_ON
FPGA_HPD
TXD
RXD
SCL
SDA
HSYNC
VSYNC
PSRAM
A[0..18]
IO[0..15]
CS
PSRAM_WE
OE
LB
PSRAM_UB
U_S3_LED_MAT_FPGA_POWER
S3_LED_MAT_FPGA_POWER.SchDoc
SW1
DSHP04SSGER-G
R52 10k
R53 10k
R54 10k
R55 10k
R56 10k
R57 10k
R58 10k
R59 10k
A15
A14
A13
A12
DD6
M24C64-WMN6TP
E0
E1
E2
GND
C7
100nF
0402
R6
10k
0603
R8
10k
0603
FPGA_SCL
FPGA_SDA
R22 4.7k
C91
100nF
0402
U3 MIC6315-30D2UY
Vcc
MR
S1 Tact SW KMR2
L3
V1
VCC
E/D
25MHz
GND
CLOCK
C32
100nF
0402
R27
10k
0603
R28
10k
0603
XP1
Header 5X2
JTAG_TCK
JTAG_TDO
JTAG_TMS
JTAG_TDI
3V3
R29
1k
0603
R21
4.7k
U2
W25Q32JVSSIQ
QSPI_CSN
QSPI_CLK
QSPI_D0
QSPI_D1
QSPI_D2
QSPI_D3
C90
100nF
0402
Title FPGA
Size: A2
Number:*
Revision2.0
Date: 20/02/24
Time: 22:42:35
Sheet3 of 7
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\S3_LED_MAT_FPGA.SCHDOC
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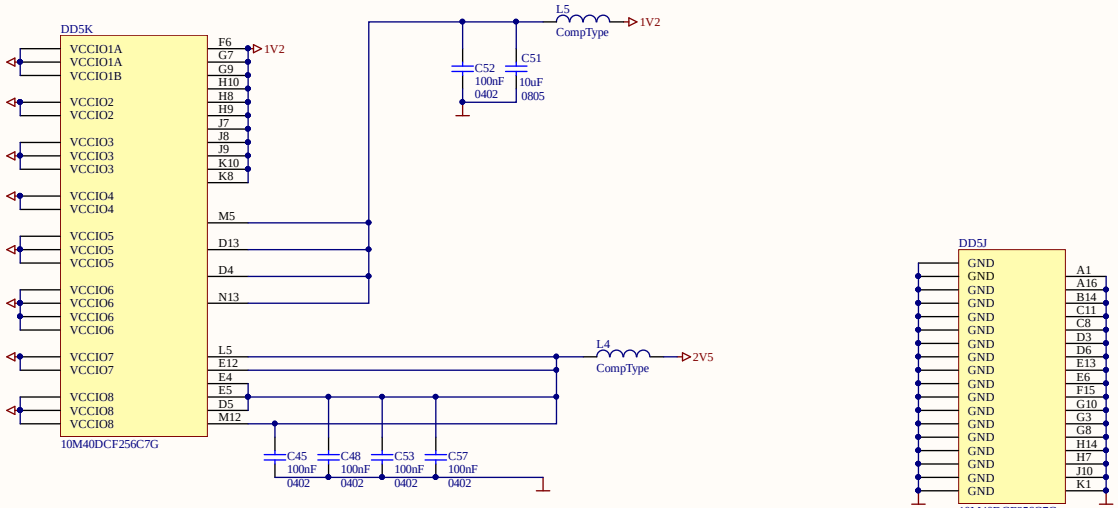

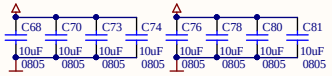

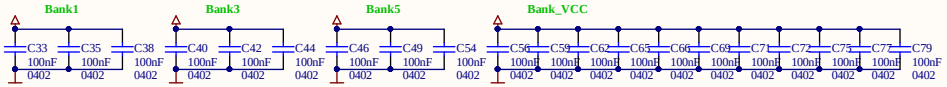

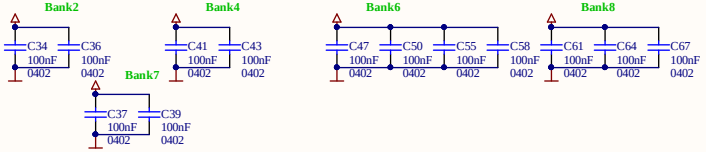

Title	*FPGA Power*		*
Size: A3	Number: *	Revision: 2.0	*
Date: 20/02/24	Time: 22:42:36	Sheet 4 of 7	*
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\S3_LED_MAT_FPGA_POWER.SchDoc			

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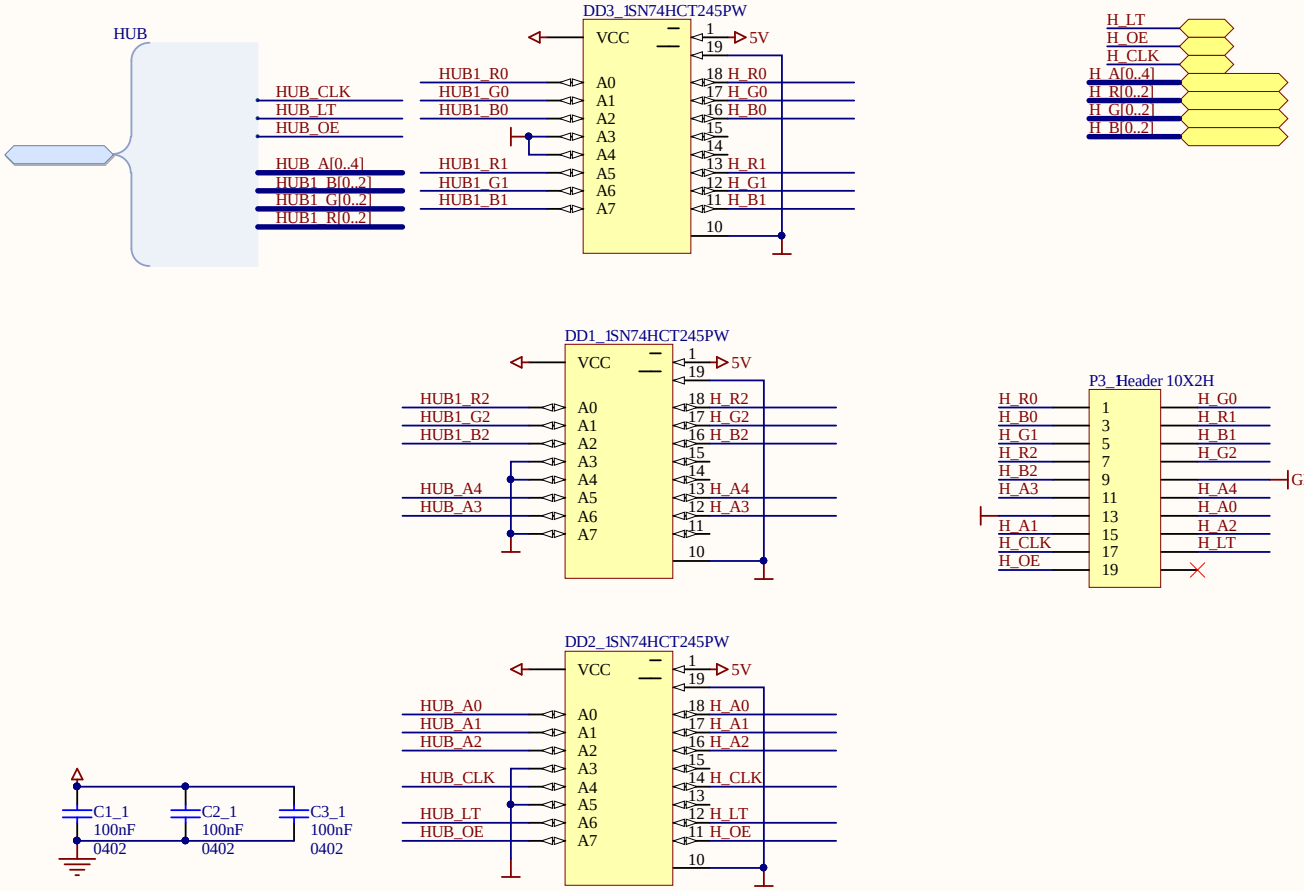
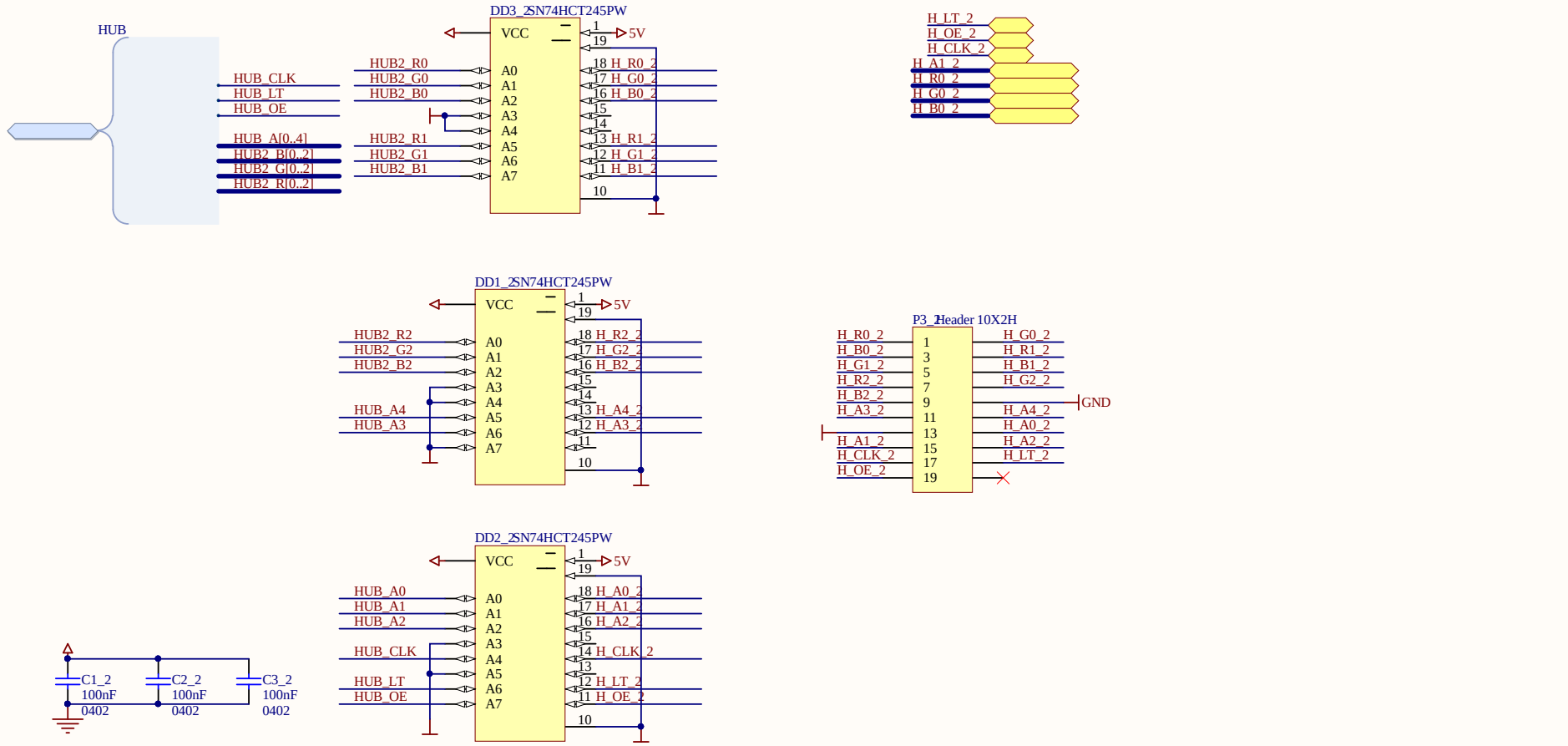
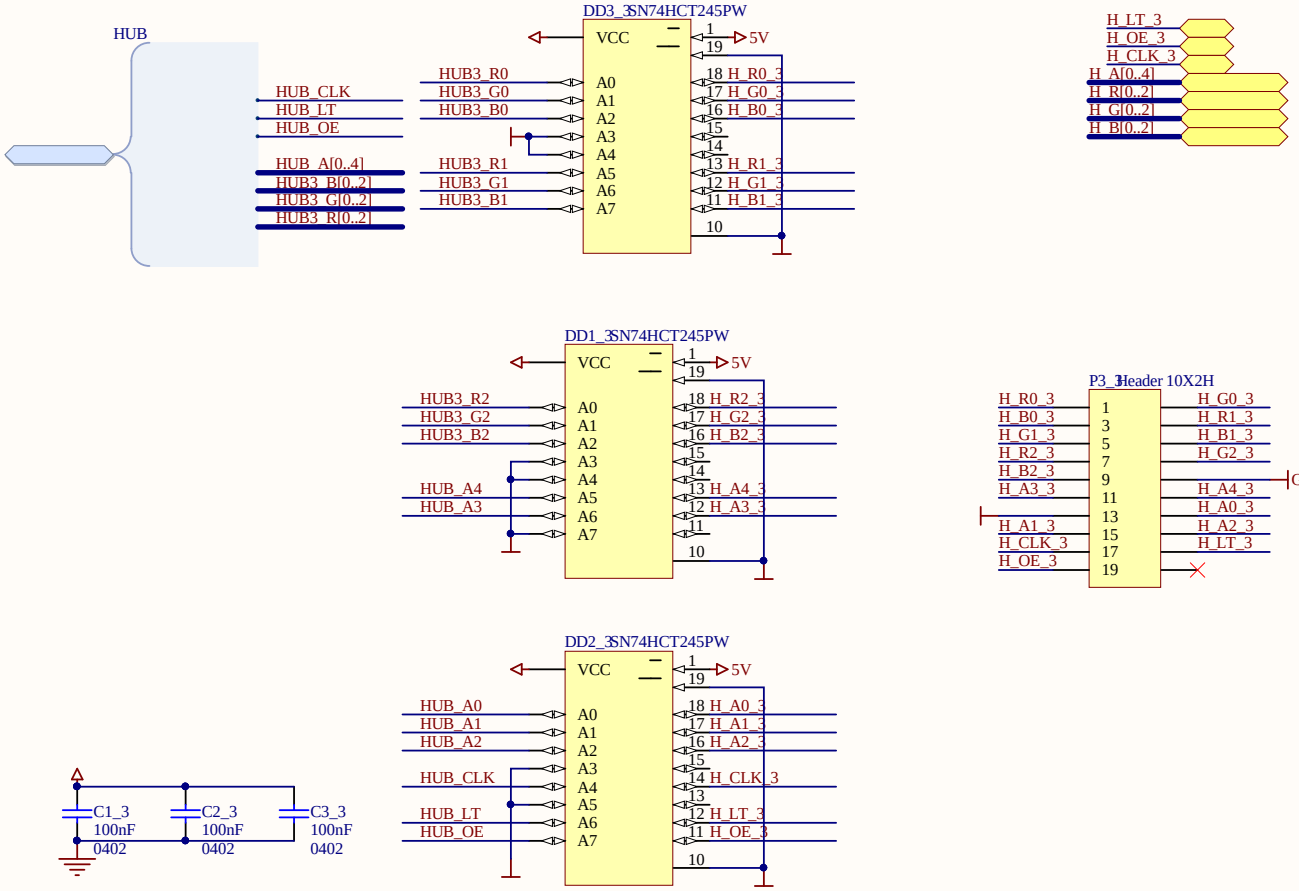


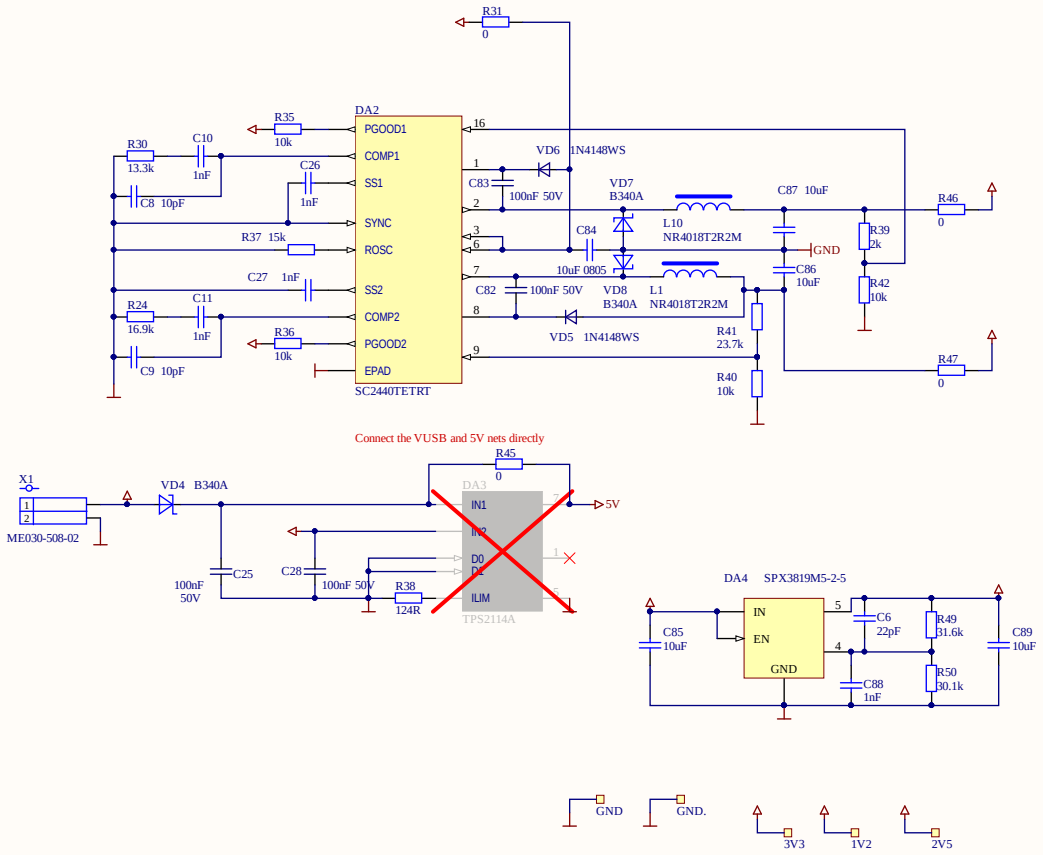
Title	***HUB***		
Size: A4	Number:	Revision: 2.0	
Date: 20/02/24	Time: 22:42:36	Sheet 5 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\LED_MAT_HUB.SchDoc			



Title	***HUB***		
Size: A4	Number:	Revision: 2.0	
Date: 20/02/24	Time: 22:42:36	Sheet 5 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\LED_MAT_HUB.SchDoc			



Title	***HUB***		
Size: A4	Number:	Revision: 2.0	
Date: 20/02/24	Time: 22:42:36	Sheet 5 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\LED_MAT_HUB.SchDoc			



Title	**Power**		
Size: A3	Number: Power	Revision: 2.0	
Date: 20/02/24	Time: 22:42:36	Sheet 6 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\Power.SchDoc			

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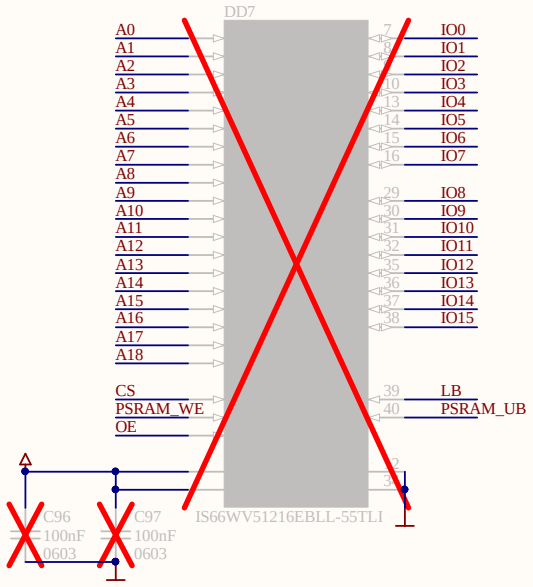
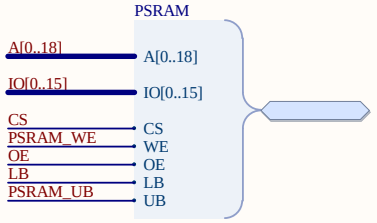
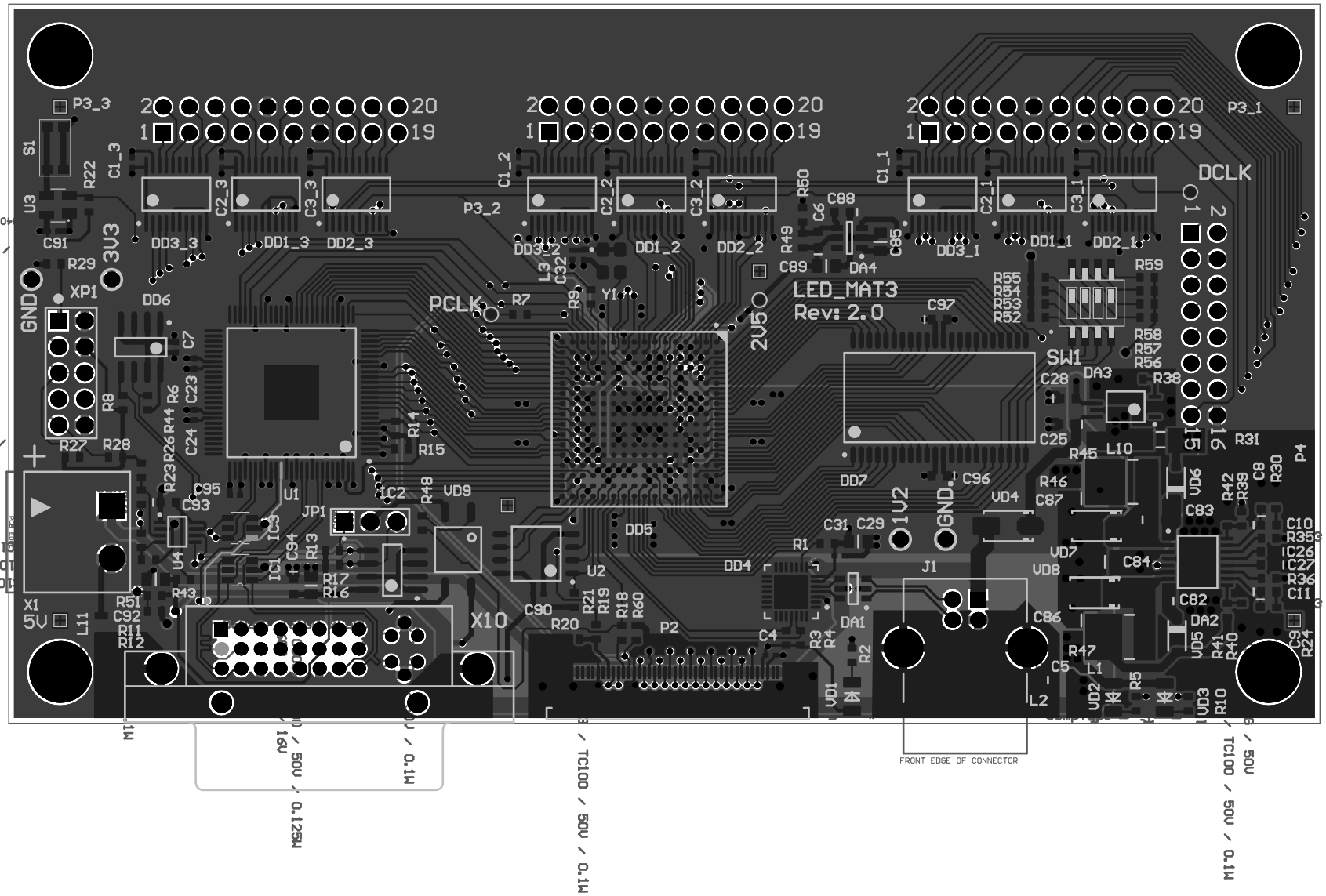




Title	***RAM***		
Size: A4		Number:	Revision:2.0
Date: 20/02/24	Time: 22:42:37	Sheet 7 of 7	
File: D:\Dropbox\Projects\LED_MATRIX\Design\PCB\LED_MAT_3\Release2\PSRAM.SchDoc			


LED_MAT3
Rev: 2.0
DCLK
PCLK
SW1
XP1
X10
P3_1
P3_2
P3_3
FRONT EDGE OF CONNECTOR