// Date: 20171206 // Author: DS // “How to program MBI5153”

Suppose, we have **3** (M) driver ICs connected into the chain, and each IC has **4** (N) channels.

Define the uppermost pixel address in the row (line) : **UPA**  = **LBA + N · M - 1**;

Then the image map in the memory will be looked as following:

1. **RAM\_ADDR = UPA**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RAM\_ADDR** | **LBA**  **(Line Base Addr)** |  |  | **UPA – 2N** |  |  |  | **UPA - N** |  |  |  | **UPA** |
| Line**0** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**1** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**2** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |

1. **RAM\_ADDR = UPA – 1**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RAM\_ADDR** |  |  | **UPA – 1 – 2N** |  |  |  | **UPA – 1 – N** |  |  |  | **UPA - 1** |  |
| Line**0** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**1** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**2** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |

1. **RAM\_ADDR = UPA – 2**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RAM\_ADDR** |  | **UPA – 2 – 2N** |  |  |  | **UPA – 2 – N** |  |  |  | **UPA - 2** |  |  |
| Line**0** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**1** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**2** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |

1. **RAM\_ADDR = UPA – 3**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RAM\_ADDR** | **UPA – 3 – 2N** |  |  |  | **UPA – 3 – N** |  |  |  | **UPA - 3** |  |  |  |
| Line**0** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**1** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**2** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |

**Next Line:**

1. **UPA = UPA + N · M**

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **RAM\_ADDR** | **LBA**  **(Line Base Addr)** |  |  | **UPA – 2N** |  |  |  | **UPA - N** |  |  |  | **UPA** |
| Line**0** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**1** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |
| Line**2** | IC**1** Ch**0** | IC**1** Ch**1** | IC**1** Ch**2** | IC**1** Ch**3** | IC**2** Ch**0** | IC**2** Ch**1** | IC**2** Ch**2** | IC**2** Ch**3** | IC**3** Ch**0** | IC**3** Ch**1** | IC**3** Ch**2** | IC**3** Ch**3** |