Sandeep Dasgupta

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Research Interest

Compiler Optimizations
Static Program Analysis & Verification
Symbolic Execution
Parallel & Power Aware Computation

Academics

PhD Computer Science *August 2013 - untill now*
CS @ University of Illinois Urbana Champaign

- Currently working with LLVM Group led by Prof. Vikram S. Adve

M.Tech Computer Science & Engineering – CPI 9.00/10.00 *August 2009 - June 2011*
Indian Institute Of Technology Kanpur, Kanpur, India.

- Secured **rank** 1 in M. Tech 2009 Batch, IIT Kanpur.

B.E. Computer Science & Engineering – *First Class with Honours*, 85.625/100.00 *August 2002 - June 2006*
Bengal Engineering & Science University, Shibpur, West Bengal, India.

- Awarded **University Gold Medal** for securing 1st Rank in BE, Computer Science & Engineering, 2002 batch.
- Awarded **Best Student Award**, sponsored by Tata Consultancy Services, for outstanding performance in BE, Computer Science & Engineering, 2002 batch.

Graduate Courses & Projects

Graduate Courses

- CS526: Advanced Compiler Construction
- CS533: Parallel Computer Architectures
- CS598lvk: Parallel Programming with Migratable Objects
- CS420/CSE402/ECE492: Introduction to Parallel Programming for Scientists and Engineers

Projects

- **Partial Redundancy Elimination(PRE)** [Github]
  `Abstract:` PRE is a compiler optimization that eliminates expressions that are redundant on some but not necessarily all paths through a program. In this project, we implemented a PRE optimization pass in LLVM and measured results on a variety of applications. It's a powerful technique that subsumes Common Subexpression Elimination (CSE) and Loop Invariant Code Motion (LICM), and hence has a potential to greatly improve performance.
- **Implementing Data flow Analyzer**
  `Abstract:` To Extend the Generic Data Flow Analyzer GDFA (of gcc) to the data flow frameworks where data flow information can be represented using bit vectors but the frameworks are not bit vector frameworks because they are non-separable e.g., faint variable analysis, possible undefined variable analysis, strongly live variable analysis.

- **Mitigating Impact of Heterogeneity Across Power-constrained Nodes on Parallel Applications through Load Balancing** [Github]
  `Abstract:` Different processors across the nodes have different execution times for the same work-loads. This performance imbalance is seen only when the CPU power is capped to low values. This performance imbalance causes increased execution times of the parallel applications. We did a detailed study and proposed a power aware load balancer (using Charm++) which minimized the performance imbalance at the lower power caps by tackling this heterogeneity.
- **Designing superscalar processor** [Github]
  `Abstract:` To design a customized processor (using parallel processing concepts) for the application of document retrieval system. We developed a superscalar processor (with an issue rate of 2) using verilog hdl, and an assembler for that processor using flex and bison.
- **Graph Coloring Using State Space Search** [Github]
  `Abstract:` We plan to leverage the state space search model for implementing graph coloring in parallel in Charm++. Some of the challenges for efficient exploration of space by chares include intelligent pruning of the state space, load balancing, grain-size control and low-overhead communication between chares. We evaluated multiple options for each of these, and come up with design decisions which would work for a large category of real-life graph applications.

M.Tech Thesis — Joint supervision of Dr. Amey karkare & Dr. Sanjeev K Aggarwal

Precise Shape Analysis Using Field Sensitivity [Report]

To disambiguate heap allocated data-structures by estimating the shape (Tree, Dag or Cyclic Graph) of the data structure accessible from each heap directed pointer. This will help in automatic parallelization of sequential code having heap intensive data structures. The work mainly focuses on devising a novel shape analysis technique.

Publications

Papers in Conferences

- Sandeep Dasgupta & Amey Karkare."**Precise shape analysis using field sensitivity**", in *Proceedings of the 27th Annual ACM Symposium on Applied Computing*, SAC 2012, pages 1300-1307, New York, USA. ACM. doi: 10.1145/2231936.2231982, isbn: 978-1-4503-0857-1. [pdf]
- Barnali Basak, Sandeep Dasgupta & Amey Karkare."**Heap Dependence Analysis for Sequential Programs**", *International Conference on Parallel Computing* (ParCo 2011), Ghent, Belgium, August 30 - September 2, 2011. [pdf]
  - Published in: Applications, Tools and Techniques on the Road to Exascale Computing, 22 volume of Advances in Parallel Computing, chapter: Heap Dependence Analysis for Sequential Programs, pages 99–106. IOS Press, May 2012. doi: 10.3233/978-1-61499-041-3-99, isbn: 978-1-61499-040-6.

Posters

- Poster "**Dependence Analysis for Parallelization of Sequential Programs**" got accepted at APLAS'10 (the 8th ASIAN Symposium on Programming Languages & Systems). [pdf]

Journals

- Sandeep Dasgupta, Amey Karkare & P. Vinay K. Reddy. "**Precise shape analysis using field sensitivity**.", in *Innovations in Systems and Software Engineering (ISSE)*, a NASA journal. doi: 10.1007/s11334-013-0198-7. [pdf]

Professional Experience

Intel Technology India Pvt. Ltd., *Component Design Engineer* — *August 2011 - June 2013*

- Worked as Design Automation Engineer for Formal Equivalence Verification of hardware designs.
- Contributed to and supported Broadwell (BDX) and Skylake (SKL) FEV requirements. Played key role in FEV audit checks for BDX.
- Owner of tools and infrastructures for driving FEV central runs for BDX. Worked closely with teams of various design styles in understanding the requirements for customization and also provided the much needed support for successfully deploying those tools.

- Build flows and methodologies to provide solutions on how to formally verify leading next generation CPU designs. Interacted closely with global FEV teams to understand the requirements and contributed to the success of various sprints with timely and quality delivery on assignments.

Interra Systems India Pvt. Ltd., *Senior Member Of Technical Staff* *August 2006 - July 2009*

- Developer of Interra's premiere front-end analyzer products - Cheetah (SystemVerilog) and MVV(Mixed Verilog Vhdl) and provided support for several new constructs of System Verilog IEEE-1800-2005, fixed tool bugs, created applications and contributed in performance Improvement.
- Involved in a critical service project for Atrenta (I) Pvt. Ltd. for the development of System Verilog features in Spyglass DFT.

Teaching Experience

University Of Illinois Urbana Champaign, *August 2013 - December 2013*

- **Teaching Assistant** for CS 427: Software Engineering I: A Graduate level course.
  - Designing the questions for homework and term examinations and grading those.
  - Conducting discussion sessions with the students to answer questions related to lectures/homework.

Indian Institute of Technology, Kanpur, *August 2009 - 2011*

- **Tutor** for ESc 101: Fundamentals of Computing: An undergraduate course.
  - Responsible for weekly lecture class on C - programming language, supervision of programming laboratory and grading assignments and term examinations.
- **Teaching Assistant** for CS 335: Principles of Compiler Design: An undergraduate course.
  - Responsible for mentoring a student group on a course project of developing a simple compiler (using a subset of C-language constructs) demonstrating most of the phases of compiler design starting from Lexical & Syntax analysis upto Intermediate code generation.
  - Grading assignments and term examinations.
- **Teaching Assistant** for CS355: Programming Tools and Techniques: An undergraduate course.
  - Grading assignments related to Software management tools such as make; Programming tools such as Python, Perl; Document preparation systems such as tex; Tools for building programs like Lex and Yacc.

Achievements/Distinctions

- Awarded **University Gold Medal** for securing 1st Rank in BE, Computer Science & Engineering, 2002 batch.
- Awarded **Best Student Award**, sponsored by Tata Consultancy Services, for outstanding performance in BE, Computer Science & Engineering, 2002 batch.
- **Secured Rank** 1, in M. Tech 2009 Batch, IIT Kanpur.
- **Secured All India Rank** 145 (99.64 percentile) in GATE 2009, an exam for admission in Graduate Study.
- **Ranked** 356^{th} (among $\frac{1}{10}$ of Million+ students) in WB-JEE, 2002, an exam for admission in undergraduate study.
- Awarded **Interra Humming Bird Award** in recognition of & appreciation for providing excellent support to Atrenta (I) Pvt. Ltd. in the project "IEEE compliance for Spyglass", awarded by Interra Systems India Pvt. Ltd.