Sandeep Dasgupta

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Interested In

- Compiler Optimizations
- Parallelizing Compilers
- Parallel & Power Aware Computation
- Static/Dynamic Program Analysis & Program Verification
- Dynamic Symbolic Execution

Career Overview

PhD Computer Science *August 2013 - untill now*
CS @ University of Illinois Urbana Champaign

- Working with LLVM Group led by Prof. Vikram S. Adve
- Current Research: To detect static analysis bugs using dynamic symbolic execution. Currently we are focusing on bugs in LLVM's "must alias analysis" (like basicaa).

Component Design Engineer *August 2011 - June 2013*
Intel Technology India Pvt. Ltd.

- Worked as Design Automation Engineer for Formal Equivalence Verification of hardware designs.

M.Tech Computer Science & Engineering – CPI 9.00/10.00 *August 2009 - June 2011*
Indian Institute Of Technology Kanpur, Kanpur, India.

- Secured **rank** 1 in M. Tech 2009 Batch, IIT Kanpur.

Senior Member Of Technical Staff *August 2006 - July 2009*
Interra Systems India Pvt. Ltd.

- Developer of Interra's premiere front-end analyzer products - Cheetah (SystemVerilog) and MVV(Mixed Verilog Vhdl).

B.E. Computer Science & Engineering – *First Class with Honours*, 85.625/100.00 *August 2002 - June 2006*
***Indian Institutes of Engineering Science and Technology, Shibpur*, West Bengal, India.**

- Awarded **University Gold Medal** & **Best Student Award** for securing 1st Rank in BE, Computer Science & Engineering, 2002 batch.

Academic Projects

Projects

- **Partial Redundancy Elimination(PRE)** [Report] [Github]
  `Abstract:` Implemented a PRE optimization pass in LLVM and measured results on a variety of applications and did a detailed study on the performance numbers.
- **Implementing Data flow Analyzer**
  `Abstract:` Extended the Generic Data Flow Analyzer GDFA (of gcc) to the data flow frameworks where data flow information can be represented using bit vectors but the frameworks are not bit vector frameworks because they are non-separable e.g., faint variable analysis, possible undefined variable analysis, strongly live variable analysis.
- **Mitigating Impact of Heterogeneity Across Power-constrained Nodes on Parallel Applications through Load Balancing** [Report] [Github]
  `Abstract:` Different processors across the nodes have different execution times for the same work-loads. This performance imbalance is seen only when the CPU power is capped to low values. This performance imbalance causes increased execution times of the parallel applications. We did a detailed study and proposed a power aware load balancer (using Charm++) which minimized the performance imbalance at the lower power caps by tackling this heterogeneity.
- **Designing superscalar processor** [Github]
  `Abstract:` Developed a superscalar processor (with an issue rate of 2) using verilog hdl, and an assembler for that processor using flex and bison.
- **Graph Coloring Using State Space Search** [Report] [Github]
  `Abstract:` Leveraged the state space search model for implementing graph coloring in parallel in Charm++. Some of the challenges for efficient exploration of space by chares include intelligent pruning of the state space, load balancing, grain-size control and low-overhead communication between chares. Evaluated multiple options for each of these, and come up with design decisions which would work for a large category of real-life graph applications.

Publications

Papers in Conferences

- Sandeep Dasgupta & Amey Karkare."**Precise shape analysis using field sensitivity**", in *Proceedings of the 27th Annual ACM Symposium on Applied Computing*, SAC 2012. [pdf]
- Barnali Basak, Sandeep Dasgupta & Amey Karkare."**Heap Dependence Analysis for Sequential Programs**", *International Conference on Parallel Computing*, ParCo 2011. [pdf]

Posters

- Poster "**Dependence Analysis for Parallelization of Sequential Programs**" got accepted at the 8th ASIAN Symposium on Programming Languages & Systems, APLAS 2010. [pdf]

Journals

- Sandeep Dasgupta, Amey Karkare & P. Vinay K. Reddy. "**Precise shape analysis using field sensitivity**.", in *Innovations in Systems and Software Engineering*, ISSE 2013. [pdf]

Professional Experience

Intel Technology India Pvt. Ltd., *Component Design Engineer* *August 2011 - June 2013*

- Worked as Design Automation Engineer for Formal Equivalence Verification (FEV) of hardware designs for Broadwell (BDX) and Skylake (SKL) projects. Involves building flows and methodologies and interacting closely with global FEV teams to provide FEV solutions.
- Owner of tools and infrastructures for driving FEV central runs for BDX. Invloves working closely with teams of various design styles.

Interra Systems India Pvt. Ltd., *Senior Member Of Technical Staff* *August 2006 - July 2009*

- Developer of Interra's premiere front-end analyzer products - Cheetah (SystemVerilog) and MVV(Mixed Verilog Vhdl) and provided support for several new constructs of System Verilog IEEE-1800-2005.

- Worked with Atrenta (I) Pvt. Ltd. (service project) for the development of System Verilog features in Spyglass DFT.
- Awarded **Interra Humming Bird Award** in recognition of & appreciation for providing excellent support to Atrenta (I) Pvt. Ltd. in the project "IEEE compliance for Spyglass".