



## Sandeep Dasgupta

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### RESEARCH INTEREST

Program Analysis & Verification  
Compiler Optimizations  
Parallel Computing  
Programming Language Design & Implementation  
High performance computing  
Automated software verification & quality assurance.

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### ACADEMICS

#### PhD Computer Science

*CS @ Illinois Urbana Champaign*

- Currently working with [LLVM Group](#) led by Prof. [Vikram S. Adve](#)

#### M.Tech Computer Science & Engineering – CPI 9.00/10.00

*June 2011*

*Indian Institute Of Technology Kanpur, Kanpur, India.*

- Secured **rank 1** in M. Tech 2009 Batch, IIT Kanpur.

#### B.E. Computer Science & Engineering – *First Class with Honours*, 85.625/100.00

*June 2006*

*Bengal Engineering & Science University, Shibpur, West Bengal, India.*

- Awarded **University Gold Medal** for securing 1st Rank in BE, Computer Science & Engineering, 2002 batch.
- Awarded **Best Student Award**, sponsored by [Tata Consultancy Services](#), for outstanding performance in BE, Computer Science & Engineering, 2002 batch.

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### M.TECH THESIS

JOINT SUPERVISION OF [DR. AMEY KARKARE](#) & [DR. SANJEEV K AGGARWAL](#)

#### Precise Shape Analysis Using Field Sensitivity

To disambiguate heap allocated data-structures by estimating the shape (Tree, Dag or Cyclic Graph ) of the data structure accessible from each heap directed pointer. This will help in automatic parallelization of sequential code having heap intensive data structures. The work mainly focuses on devising a novel shape analysis technique.

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### PUBLICATIONS

#### Papers in Conferences

- Sandeep Dasgupta & Amey Karkare. “[Precise shape analysis using field sensitivity](#)”, in *Proceedings of the 27th Annual ACM Symposium on Applied Computing*, SAC 2012, pages 1300-1307, New York, USA. ACM. doi: [10.1145/2231936.2231982](https://doi.org/10.1145/2231936.2231982), isbn: 978-1-4503-0857-1.
- Barnali Basak, Sandeep Dasgupta & Amey Karkare. “[Heap Dependence Analysis for Sequential Programs](#)”, *International Conference on Parallel Computing* (ParCo 2011), Ghent, Belgium, August 30 - September 2, 2011.
  - Published in: Applications, Tools and Techniques on the Road to Exascale Computing, 22 volume of Advances in Parallel Computing, chapter: Heap Dependence Analysis for Sequential Programs, pages 99–106. IOS Press, May 2012. doi: [10.3233/978-1-61499-041-3-99](https://doi.org/10.3233/978-1-61499-041-3-99), isbn: 978-1-61499-040-6.

## Posters

- Poster “[Dependence Analysis for Parallelization of Sequential Programs](#)” got accepted at APLAS’10 (the 8th ASIAN Symposium on Programming Languages & Systems).

## Journals

- Sandeep Dasgupta, Amey Karkare & P. Vinay K. Reddy. “[Precise shape analysis using field sensitivity.](#)”, in *Innovations in Systems and Software Engineering (ISSE)*, a NASA journal. doi: [10.1007/s11334-013-0198-7](#)

## TEACHING EXPERIENCE

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### Indian Institute of Technology, Kanpur,

*August 2009 - 2011*

- **Tutor** for [ESc 101: Fundamentals of Computing](#): An undergraduate course.
  - Responsible for weekly lecture class on C - programming language, supervision of programming laboratory and grading assignments and term examinations.
- **Teaching Assistant** for [CS 335: Principles of Compiler Design](#): An undergraduate course.
  - Responsible for mentoring a student group on a course project of developing a simple compiler (using a subset of C-language constructs) demonstrating most of the phases of compiler design starting from Lexical & Syntax analysis upto Intermediate code generation.
  - Grading assignments and term examinations.
- **Teaching Assistant** for [CS355: Programming Tools and Techniques](#): An undergraduate course.
  - Grading assignments related to Software management tools such as make; Programming tools such as Python, Perl; Document preparation systems such as tex; Tools for building programs like Lex and Yacc.

## PROFESSIONAL EXPERIENCE

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### [Intel Technology India Pvt. Ltd.](#), *Component Design Engineer*

*August 2011 - Present*

- Work on design automation problems related to formal equivalence verification (FEV) of hardware designs.
- Build flows and methodologies to provide solutions to formally verify leading next generation CPU designs.

### [Interra Systems India Pvt. Ltd.](#), *Senior Member Of Technical Staff*

*August 2006 - July 2009*

- Developer of Interra’s premiere front-end analyzer products - Cheetah (SystemVerilog) and MVV(Mixed Verilog Vhdl) and provided support for several new constructs of System Verilog IEEE-1800-2005, fixed tool bugs, created applications and contributed in performance Improvement.
- Involved in a critical service project for [Atrenta \(I\) Pvt. Ltd.](#) for the development of System Verilog features in Spyglass DFT.

## ACHIEVEMENTS/DISTINCTIONS

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- Awarded **University Gold Medal** for securing 1st Rank in BE, Computer Science & Engineering, 2002 batch.
- Awarded **Best Student Award**, sponsored by [Tata Consultancy Services](#), for outstanding performance in BE, Computer Science & Engineering, 2002 batch.
- **Secured Rank 1**, in M. Tech 2009 Batch, IIT Kanpur.
- **Secured All India Rank 145** (99.64 percentile) in GATE 2009, an exam for admission in Graduate Study.
- **Ranked 356<sup>th</sup>** (among 1 Lakh+ students) in WB-JEE, 2002, an exam for admission in undergraduate study.
- Awarded **Interra Humming Bird Award** in recognition of & appreciation for providing excellent support to [Atrenta \(I\) Pvt. Ltd.](#) in the project “IEEE compliance for Spyglass”, awarded by [Interra Systems India Pvt. Ltd.](#)