Summer Internship End Term Report
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Application of Delay in MIMO Systems with One-Bit Quantizers

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Chapter 1

Introduction

1.1 Problem description

One-bit quantization over MIMO channels has long been a topic of intense research activity. As MIMO channels have a high bandwidth, they typically require high resolution quantization for accurate recovery of information which requires a lot of energy and resources. Hence researchers have long been trying to investigate performance bounds in MIMO systems using one-bit quantizers to see if this is a feasible mode of communication. One-bit quantizers significantly cut energy requirements and correspondingly, overhead costs.

Low resolution analog-to-digital combiners (ADCs) such as one-bit quantizers typically do a lot of processing in the digital domain (baseband processing). This can potentially lead to a loss of large amount of information during quantization because of the low resolution. (A back of the envelope calculation can show that potentially infinite bits of information in analog domain reduces to just 1 bit for a SISO channel with 1-bit quantization)

In our project, we seek to do more pre-processing in the analog domain before the quantization process. In essence, we want to investigate the role of delay in MIMO systems and if, by introducing decision delay at the receiver, we are able to obtain a better performance. For this, we need to obtain bounds to the channel capacity analytically and via simulations and compare with existing MIMO channel architectures in literature.

Chapter 2

Procedure and future work

2.1 System model

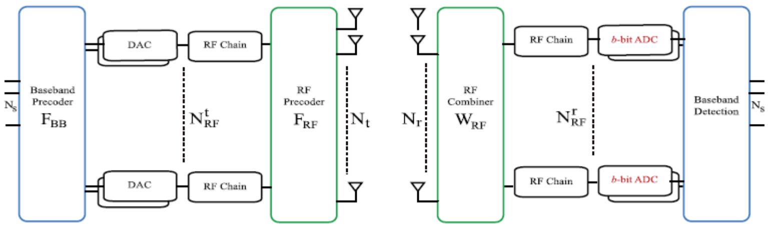

Figure 2.1: A MIMO System with hybrid precoding and few-bit ADCs [1]

In [1], RW Heath et al propose hybrid analog/digital precoding with few bit ADCs at the receiver as shown in Fig. 1, a more elaborate version of their initial channel model in [2]. Clearly, the output of this channel at the receiver prior to analog combining can be written as: $\mathbf{y} = \mathbf{H}\mathbf{F_{RF}}\mathbf{F_{BB}}\mathbf{s} + \mathbf{n}$

After analog and baseband combining, final output at the receiver is:

$\mathbf{v} = \mathbf{W}^*_{\mathbf{BB}}\mathcal{Q}(\mathbf{W}^*_{\mathbf{RF}}\mathbf{H}\mathbf{F_{RF}}\mathbf{F_{BB}}\mathbf{s} + \mathbf{W}^*_{\mathbf{RF}}\mathbf{n})$

For purposes of capacity analysis, we can ignore baseband combining and just consider $\mathbf{r} = \mathcal{Q}(\mathbf{W}^*_{\mathbf{RF}}\mathbf{H}\mathbf{F_{RF}}\mathbf{F_{BB}}\mathbf{s} + \mathbf{W}^*_{\mathbf{RF}}\mathbf{n})$

Capacity of this channel is:

$$C = \max_{p(s),F_{BB},F_{RF},W_{RF},Q()} I(\mathbf{s};\mathbf{r}|\mathbf{H}),$$

2.2 Modification to incorporate delay

If a delay of τ is introduced at the receiver, the vector of symbols sent as input $[\mathbf{s[n]}, \mathbf{s[n-1]}, \ldots, \mathbf{s[n-\tau]}]^T$ all are acted upon by the same channel and the same set of precoders and combiners with the assumption that the channel is deterministic for finite delay.

Hence all the operations and algorithms in [1] can simply be extended by extending the channel diagonally as blocks in the form shown below for as many delays required:

$$\begin{bmatrix} \mathbf{H} & \mathbf{0} & \ldots & \mathbf{0} \\ \mathbf{0} & \mathbf{H} & \ldots & \mathbf{0} \\ \multicolumn{4}{c}{\dotfill} \\ \mathbf{0} & \mathbf{0} & \ldots & \mathbf{H} \end{bmatrix}$$

2.3 Results

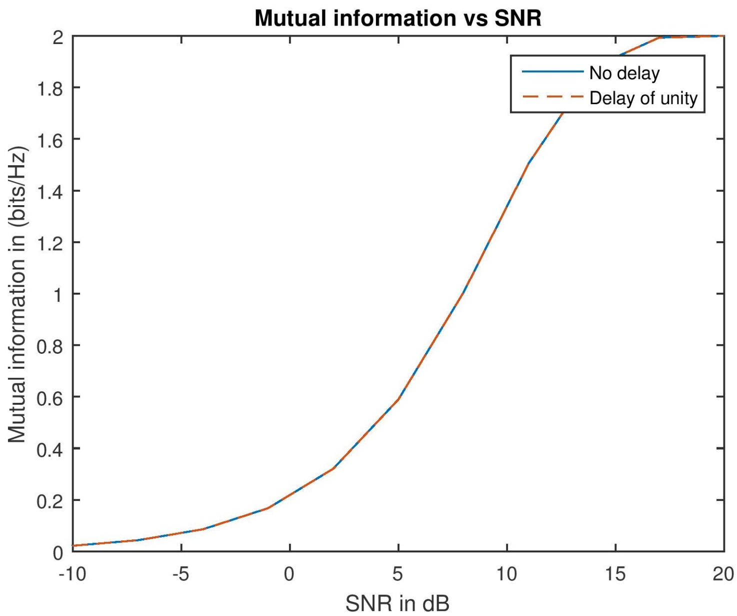

Figure 2.2: Channel inversion method, no improvement observed using delay

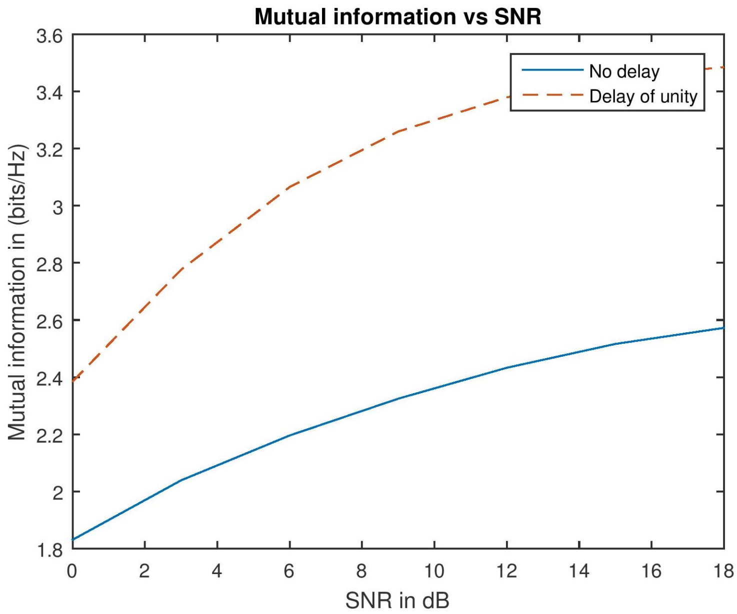

Figure 2.3: Singular Value Decomposition method, noticeable improvement seen

2.4 Future considerations

1. Arrive at more general information theoretic bounds for infinite delay

2. Consider effects of coloured noise and non-deterministic channel

3. Consider using feedback and decision feedback equalization [3]

2.5 References

1. J Mo and RW Heath; Hybrid Architectures with Few-Bit ADC Receivers
2. Mo, Heath et al; Capacity Analysis of One-bit Quantized MIMO with CSIT
3. S. Chen et al; Asymptotic Bayesian DFE using a set of hyperplanes