Lab 3 Report

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0.1 Waveforms

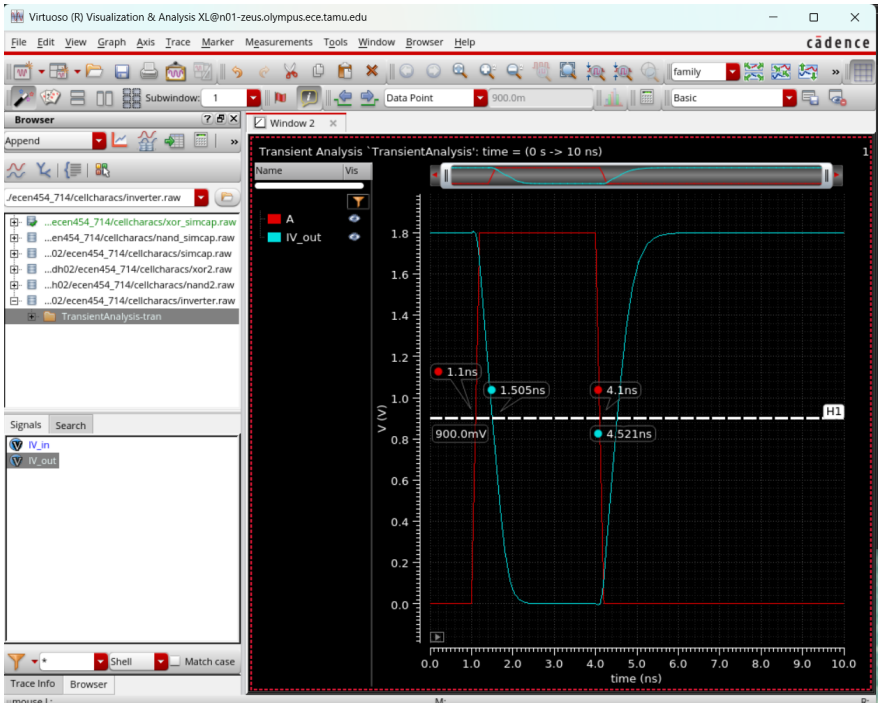

Figure 1: Inverter Wave

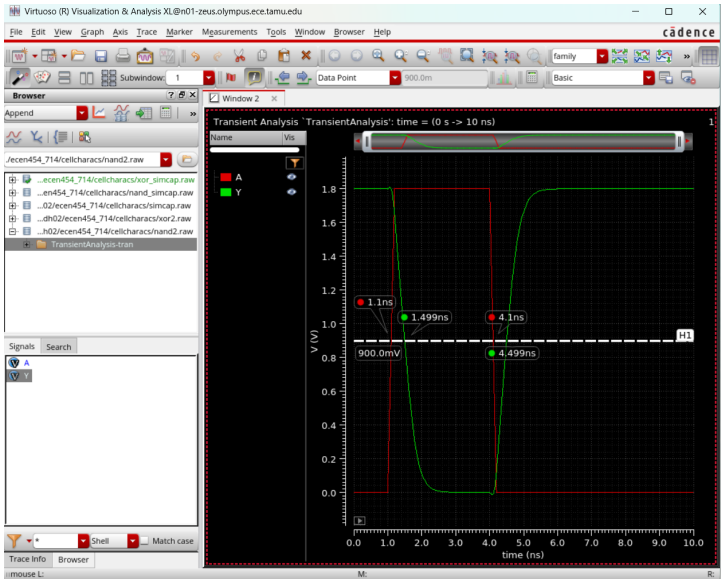

Figure 2: NAND Wave

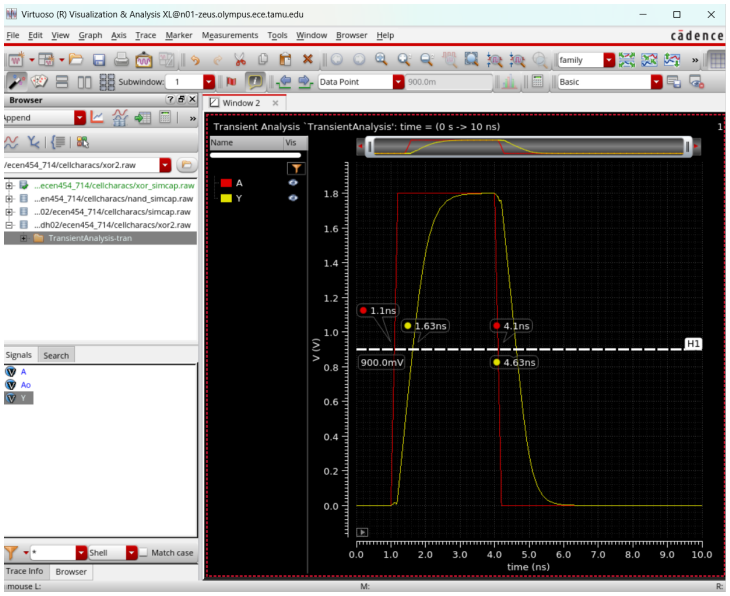

Figure 3: XOR Wave

0.2 Delay Tables

Capacitance	Falling Delay	Rising Delay	Error Percentage
1	0.02664	0.04348	63.2132
7	0.06390	0.07887	23.4272
14	0.09478	0.10760	13.5261
21	0.12036	0.13269	10.2443
28	0.14571	0.15784	8.3248
35	0.17116	0.18368	7.3148
42	0.19646	0.20918	6.4746
49	0.22138	0.23433	5.8497
56	0.24637	0.26130	6.0600
63	0.27147	0.28734	5.8459
70	0.29680	0.31109	4.8147
77	0.32209	0.33872	5.1632
84	0.34887	0.36159	3.6461
91	0.37405	0.39002	4.2695
100	0.40521	0.42091	3.8745

Table 1: Inverter Capacitance vs. Delay and Error Percentage

Capacitance	Falling Delay	Rising Delay	Error Percentage
1	0.0365	0.0520	42.4658
7	0.0692	0.0829	19.7977
14	0.0983	0.1093	11.1902
21	0.1226	0.1326	8.1566
28	0.1469	0.1565	6.5351
35	0.1715	0.1802	5.0729
42	0.1955	0.2038	4.2455
49	0.2200	0.2278	3.5455
56	0.2450	0.2513	2.5714
63	0.2688	0.2738	1.8601
70	0.2925	0.2979	1.8462
77	0.3168	0.3232	2.0202
84	0.3415	0.3449	0.9956
91	0.3660	0.3699	1.0656
100	0.3991	0.3991	0.0000

Table 2: Nand Capacitance vs. Delay and Error Percentage

Capacitance	Falling Delay	Rising Delay	Error Percentage
1	0.106	0.129	21.6981
7	0.133	0.154	15.7895
14	0.163	0.182	11.6564
21	0.210	0.193	8.8083
28	0.238	0.222	7.2072
35	0.266	0.252	5.5556
42	0.294	0.281	4.6263
49	0.322	0.311	3.5370
56	0.351	0.342	2.6316
63	0.379	0.371	2.1563
70	0.408	0.400	2.0000
77	0.436	0.431	1.1601
84	0.465	0.461	0.8677
91	0.490	0.495	1.0204
100	0.530	0.530	0.0000

Table 3: XOR Capacitance vs. Delay and Error Percentage

0.3 AC Simulation

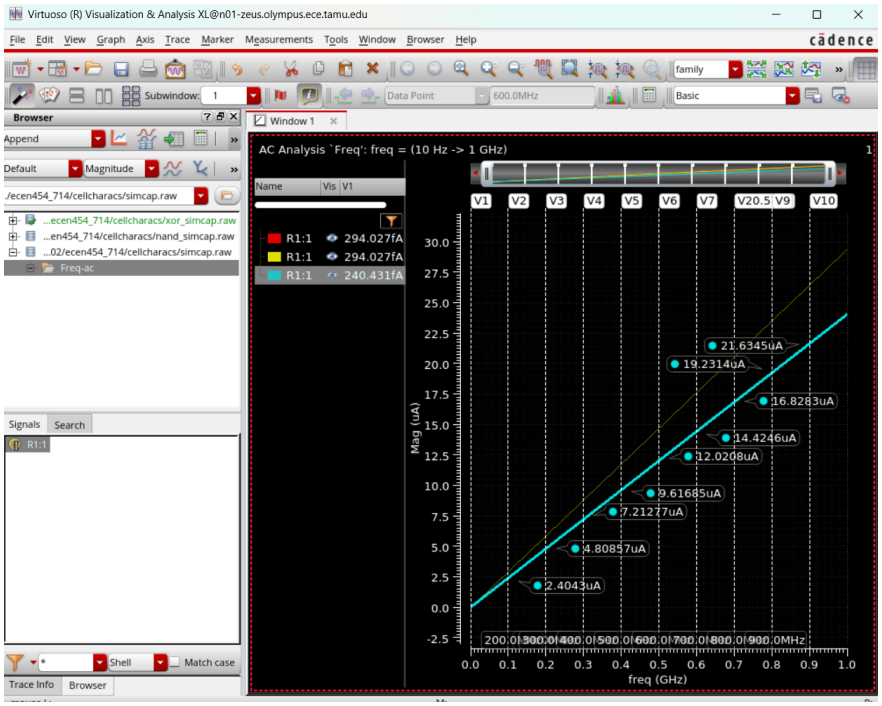

Figure 4: Inverter AC

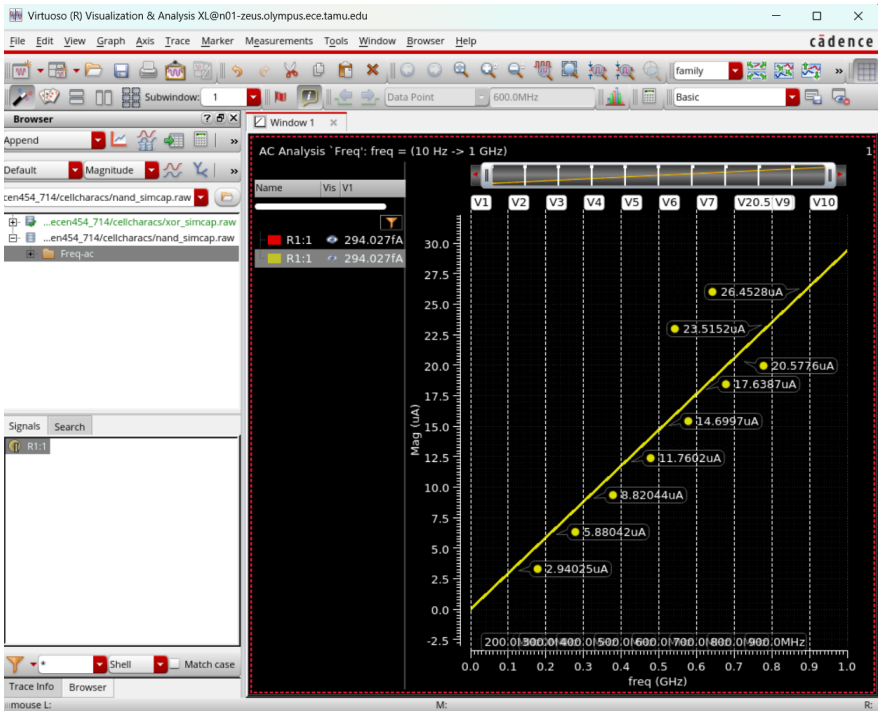

Figure 5: NAND AC

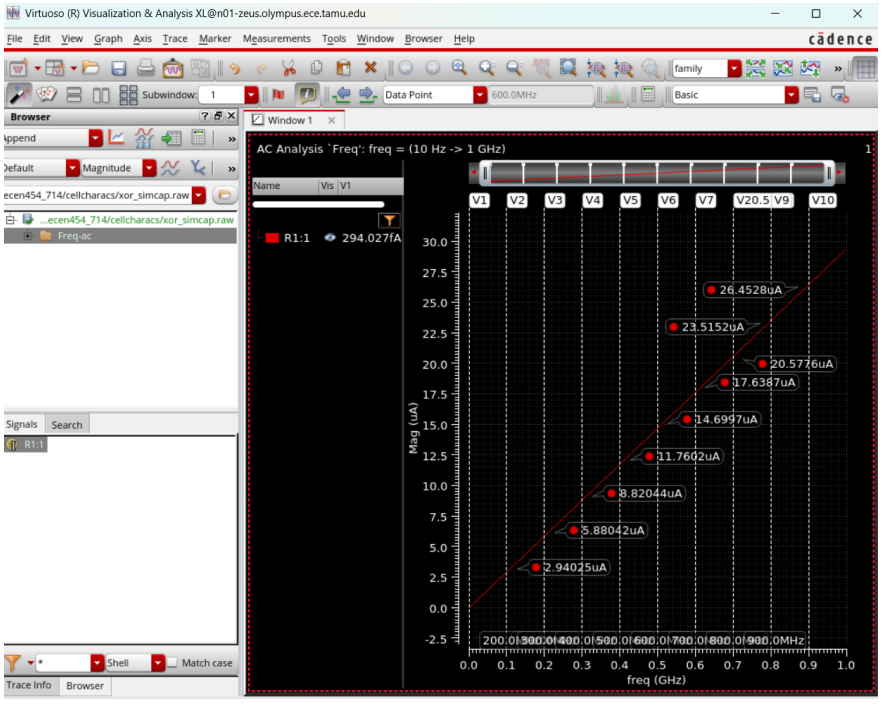

Figure 6: XOR AC

0.4 Sink Tables

Frequency (Hz)	Current (A)	Sink Capacitance (F)
10	2.40E-13	3.83E-15
100000000	2.40E-06	3.83E-15
200000000	4.81E-06	3.83E-15
300000000	7.21E-06	3.83E-15
400000000	9.62E-06	3.83E-15
500000000	1.20E-05	3.83E-15
600000000	1.44E-05	3.83E-15
700000000	1.68E-05	3.83E-15
800000000	1.93E-05	3.84E-15
900000000	2.16E-05	3.83E-15
Final Sink Cap		3.83E-15

Table 4: Inverter Frequency vs. Current and Sink Capacitance

Frequency (Hz)	Current (A)	Sink Capacitance (F)
10	2.94E-13	4.68E-15
100000000	2.96E-06	4.71E-15
200000000	5.88E-06	4.68E-15
300000000	8.82E-06	4.68E-15
400000000	1.18E-05	4.68E-15
500000000	1.47E-05	4.68E-15
600000000	1.76E-05	4.68E-15
700000000	2.06E-05	4.68E-15
800000000	2.35E-05	4.68E-15
900000000	2.65E-05	4.68E-15
Final Sink Cap		4.68E-15

Table 5: Nand Frequency vs. Current and Sink Capacitance

Frequency (Hz)	Current (A)	Sink Capacitance (F)
10	2.94E-15	4.68E-17
100000000	2.94E-06	4.68E-15
200000000	5.88E-06	4.68E-15
300000000	8.82E-06	4.68E-15
400000000	1.18E-05	4.68E-15
500000000	1.47E-05	4.68E-15
600000000	1.76E-05	4.67E-15
700000000	2.06E-05	4.68E-15
800000000	2.35E-05	4.68E-15
900000000	2.65E+01	4.68E-09
Final Sink Cap		4.68E-10

Table 6: XOR Frequency vs. Current and Sink Capacitance

0.5 spi files

```
;Spice netlist for an inverter and a capacitor
simulator lang=spectre

include "~/ecen454_714/cellcharacs/model18.spi"
include "~/ecen454_714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8

vpwl (IV_in 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (IV_in IV_out vdd gnd) IV wp=1.1u lp=0.2u wn=0.4u ln=0.2u

R1 (IV_out 1) resistor r=1
C1 (1 0) capacitor c=100fF

TransientAnalysis tran start=0 stop=10ns step=1ps
save IV_in IV_out
```

Figure 7: Inverter spi

```
;Spice netlist for a NAND and a capacitor
simulator lang=spectre

include "~/ecen454_714/cellcharacs/model18.spi"
include "~/ecen454_714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8


vapwl (A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (A vdd Y vdd gnd) NAND wp=1.2u lp=0.2u wn=0.6716u ln=0.2u

R1 (Y 1) resistor r=1
C1 (1 0) capacitor c=100f

TransientAnalysis tran start=0 stop=10ns step=1ps
save A B Y
```

Figure 8: NAND spi

```
;Spice netlist for a XOR and a capacitor
simulator lang=spectre

include "~/ecen454_714/cellcharacs/model18.spi"
include "~/ecen454_714/cellcharacs/cell18.spi"

vgnd (gnd 0) vsource dc=0
vvdd (vdd 0) vsource dc=1.8


vapwl (A 0) vsource type=pwl wave=[0n 0 1n 0 1.2n 1.8 4n 1.8 4.2n 0]

X1 (A Ao vdd gnd) IV wp=1.1u lp=0.2u wn=0.4u ln=0.2u
XOR (A gnd Ao vdd Y vdd gnd) XOR wp=1.8u lp=0.2u wn=0.5341u ln=0.2u

R1 (Y 1) resistor r=1
C1 (1 0) capacitor c=1f

TransientAnalysis tran start=0 stop=10ns step=1ps
save A Ao B Y
```

Figure 9: XOR spi

```
//Spice netlist for an inverter
simulator lang=spectre
subckt IV (input output VDD VSS)
        parameters wp=0.9u lp=0.2u wn=0.4u ln=0.3u
        M1 output input VDD VDD tsmc18P w=wp l=lp
        M2 output input VSS VSS tsmc18N w=wn l=ln
ends IV
//Spice netlist for NAND2

subckt NAND (A B y VDD VSS)
    parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u

    M1 y A VDD VDD tsmc18P w=wp l=lp
    M2 y B VDD VDD tsmc18P w=wp l=lp

    M3 y A net1 VSS tsmc18N w=wn l=ln
    M4 net1 B VSS VSS tsmc18N w=wn l=ln

ends NAND

//Spice netlist for XOR2

subckt XOR (A B Ao Bo y VDD VSS)
        parameters wp=0.9u lp=0.2u wn=0.4u ln=0.2u
        ; PMOS transistors
        M1 netp1 B VDD VDD tsmc18P w=wp l=lp
        M2 y Ao netp1 VDD tsmc18P w=wp l=lp
        M3 netp2 Bo VDD VDD tsmc18P w=wp l=lp
        M4 y A netp2 VDD tsmc18P w=wp l=lp
        ; NMOS transistors
        M5 netn1 Bo VSS VSS tsmc18N w=wn l=ln
        M6 y Ao netn1 VSS tsmc18N w=wn l=ln
        M7 netn2 B VSS VSS tsmc18N w=wn l=ln
        M8 y A netn2 VSS tsmc18N w=wn l=ln
ends XOR
```

Figure 10: cell18 spi