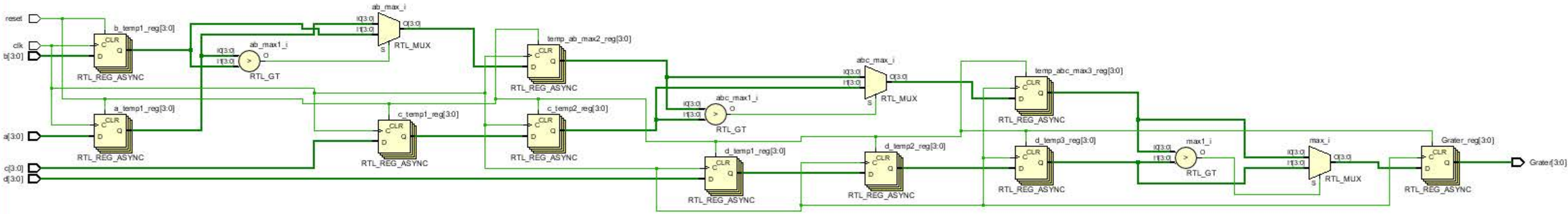
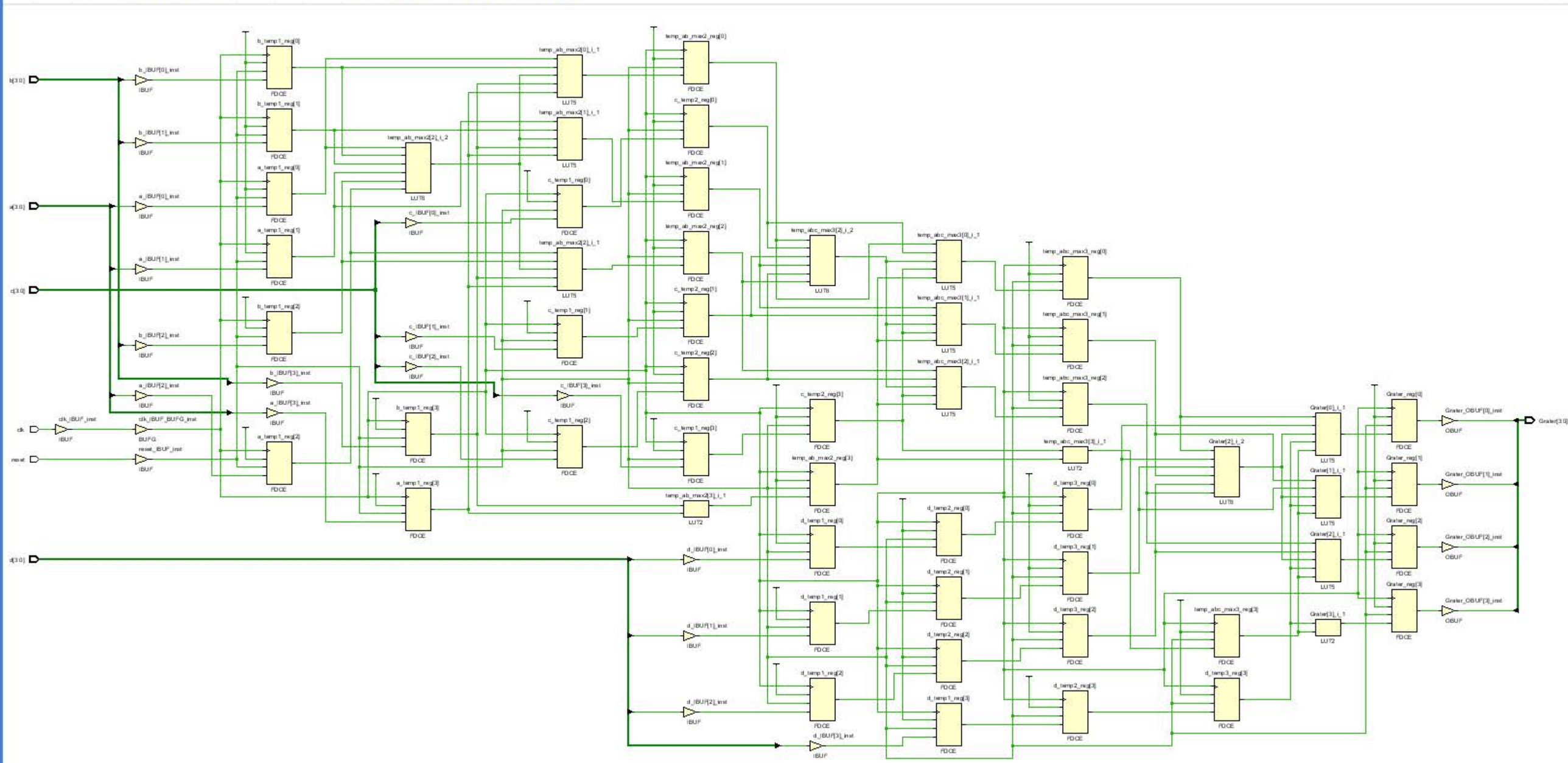
Project Summary | Schematic

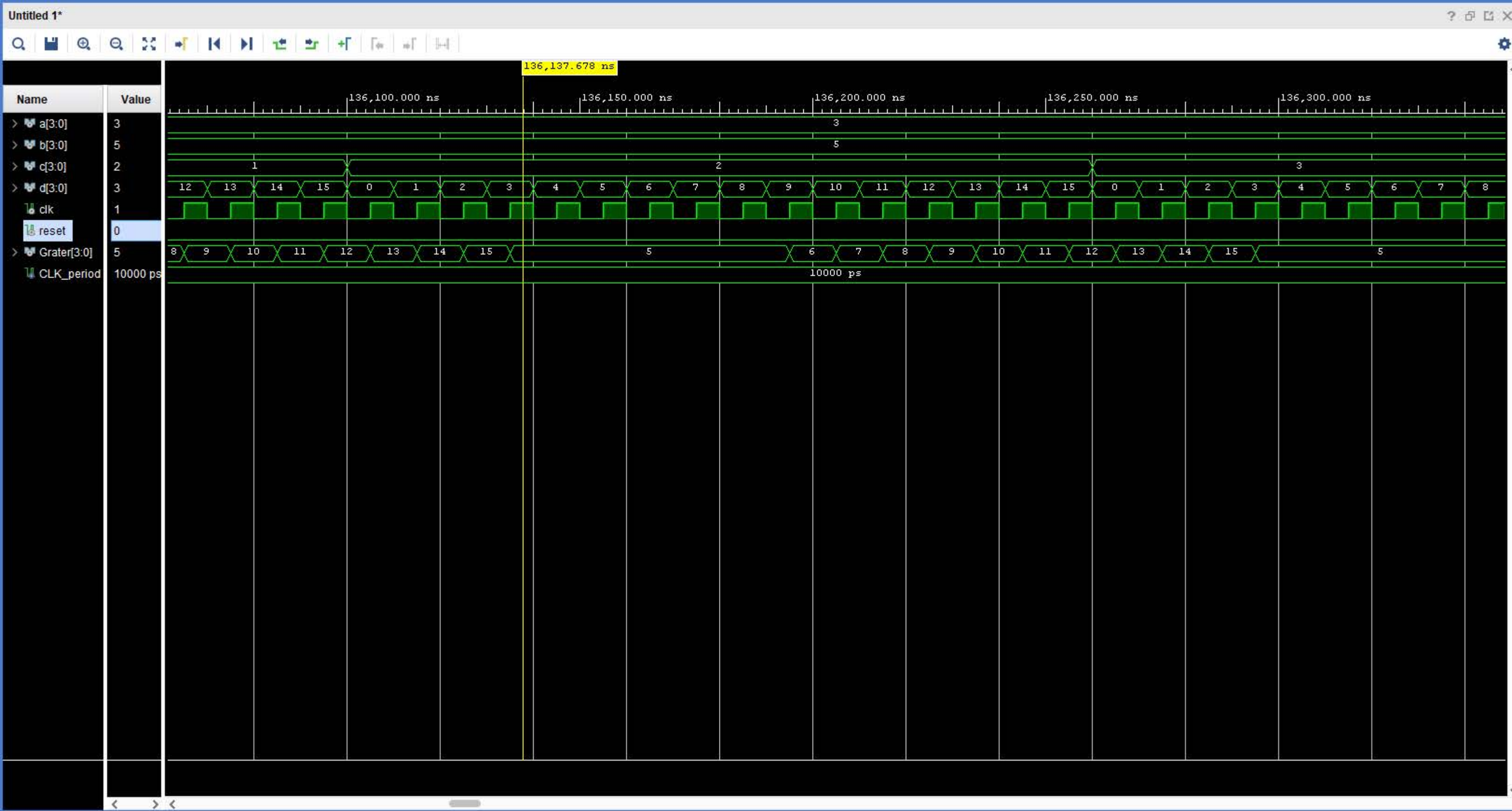
46 Cells | 22 I/O Ports | 73 Nets

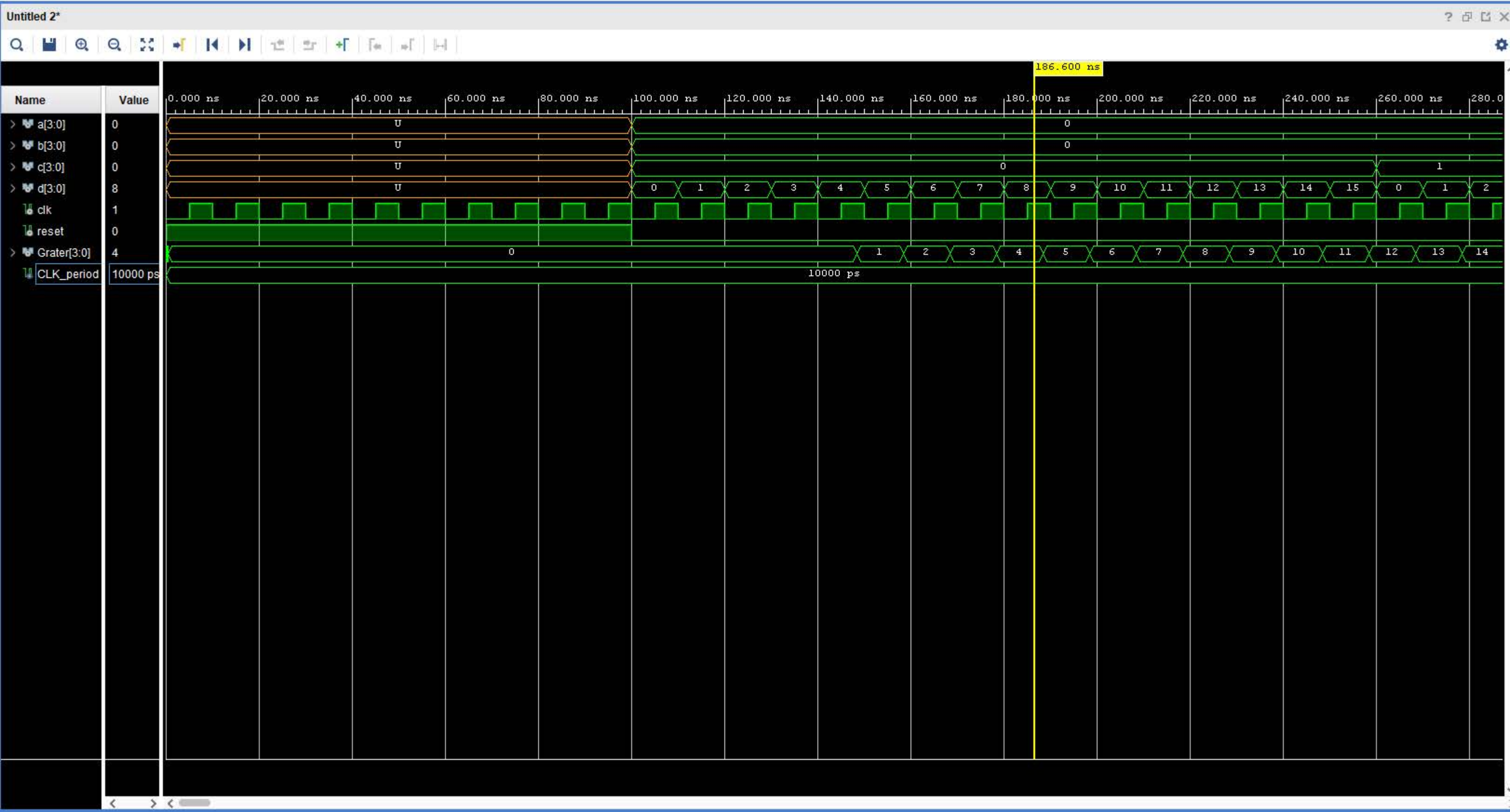


Project Summary | Device | Schematic

78 Cells | 22 I/O Ports | 97 Nets




Untitled 1*
136,137.678 ns
136,100.000 ns
136,150.000 ns
136,200.000 ns
136,250.000 ns
136,300.000 ns
Name
Value
a[3:0]
3
b[3:0]
5
c[3:0]
2
d[3:0]
3
clk
1
reset
0
Grater[3:0]
5
CLK_period
10000 ps
10000 ps


Untitled 2*
Name
Value
a[3:0]
0
b[3:0]
0
c[3:0]
0
d[3:0]
8
clk
1
reset
0
Grater[3:0]
4
CLK_period
10000 ps
186.600 ns
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
240.000 ns
260.000 ns
280.0
10000 ps

Sources | Netlist

GraterA
- Nets (97)
- Leaf Cells (79)

Properties

Select an object to see properties

Project Summary | Device | Schematic | Timing Constraints

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Tcl Console | Messages | Log | Reports | Design Runs | Timing

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths
- Inter-Clock Paths
- Other Path Groups
- User Ignored Paths

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0,000 ns	Worst Hold Slack (WHS):	0,145 ns	Worst Pulse Width Slack (WPWS):	1,185 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	24	Total Number of Endpoints:	24	Total Number of Endpoints:	41

All user specified timing constraints are met.

Sources | Netlist

temp_ab_max2[0]_i_1 (LUT5)
temp_ab_max2[1]_i_1 (LUT5)
temp_ab_max2[2]_i_1 (LUT5)
temp_ab_max2[2]_i_2 (LUT6)
temp_ab_max2[3]_i_1 (LUT2)
temp_ab_max2_reg[0] (FDCE)
temp_ab_max2_reg[1] (FDCE)
temp_ab_max2_reg[2] (FDCE)
temp_ab_max2_reg[3] (FDCE)
temp_abc_max3[0]_i_1 (LUT5)
temp_abc_max3[1]_i_1 (LUT5)
temp_abc_max3[2]_i_1 (LUT5)
temp_abc_max3[2]_i_2 (LUT6)
temp_abc_max3[3]_i_1 (LUT2)
temp_abc_max3_reg[0] (FDCE)

Path Properties

Path 1

Summary

Name	Path 1
Slack	0.000ns
Source	temp_abc_max3_reg[0]/C (rising edge-trigge

General | Properties | **Report** | Cells | Nets | Net Segme

Project Summary | Device | Schematic | **Timing Constraints**

Create Clock

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Tcl Console | Messages | Log | Reports | Design Runs | **Timing**

Intra-Clock Paths - CLK - Setup

Καθυστ. διάδοσης

General Information
Timer Settings
Design Timing Summary
Clock Summary (1)
Check Timing (21)
Intra-Clock Paths
- CLK
  - Setup 0,000 ns (10)
  - Hold 0,145 ns (10)

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Clo
Path 1	0.000	2	3	3	temp_abc_max3_reg[0]/C	Grater_reg[0]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 2	0.000	2	3	3	temp_abc_max3_reg[0]/C	Grater_reg[1]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 3	0.000	2	3	3	temp_abc_max3_reg[0]/C	Grater_reg[2]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 4	0.894	2	3	3	a_temp1_reg[0]/C	temp_ab_max2_reg[0]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 5	0.894	2	3	3	a_temp1_reg[0]/C	temp_ab_max2_reg[1]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 6	0.894	2	3	3	a_temp1_reg[0]/C	temp_ab_max2_reg[2]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 7	0.894	2	3	3	temp_ab_max2_reg[0]/C	temp_abc_max3_reg[0]/D	2.340	0.897	1.443	3.4	CLK	CLK		

Timing Summary - timing_1

Sources | Netlist

GraterA
- Nets (97)
- Leaf Cells (79)
  - a_IBUF[0]_inst (IBUF)
  - a_IBUF[1]_inst (IBUF)
  - a_IBUF[2]_inst (IBUF)
  - a_IBUF[3]_inst (IBUF)
  - a_temp1_reg[0] (FDCE)
  - a_temp1_reg[1] (FDCE)
  - a_temp1_reg[2] (FDCE)
  - a_temp1_reg[3] (FDCE)
  - b_IBUF[0]_inst (IBUF)
  - b_IBUF[1]_inst (IBUF)
  - b_IBUF[2]_inst (IBUF)
  - b_IBUF[3]_inst (IBUF)

Path Properties

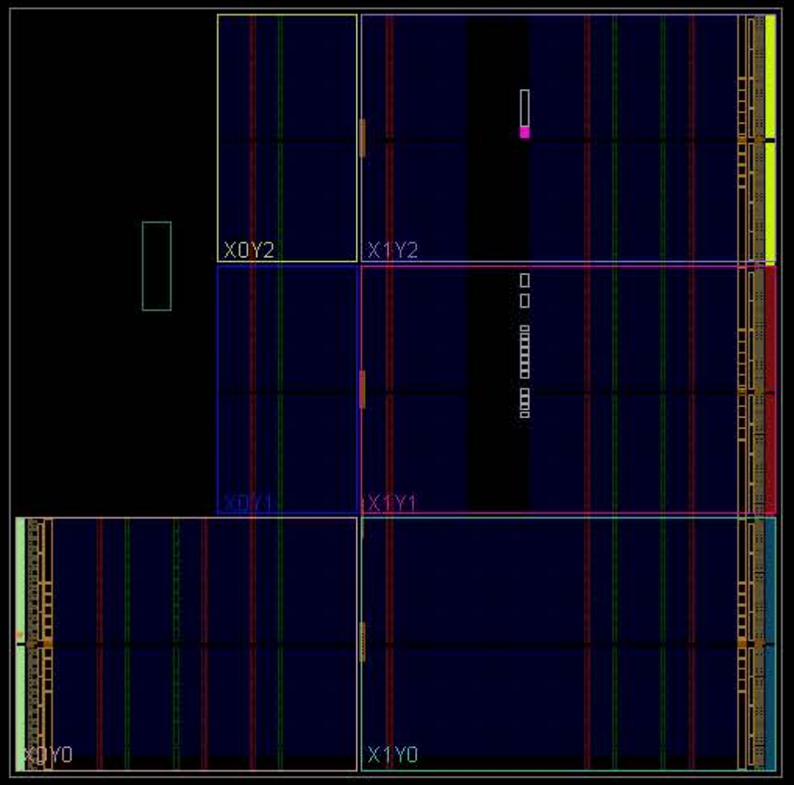
Path 11

Summary

Name	Path 11
Slack (Hold)	0.145ns
Source	a_temp1_reg[3]/C (rising edge-triggered cell FD

General | Properties | **Report** | Cells | Nets | Net Segme

Project Summary | **Device**



Tcl Console | Messages | Log | Reports | Design Runs | **Timing**

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths
  - CLK
    - Setup 0,000 ns (10)
    - Hold 0,145 ns (10)

Intra-Clock Paths - CLK - Hold

καθ.μόλυνσης

Name	Slack	Levels	Routes	High Fanout	From	To	Total	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Cloc
Path 13	0.152	0	1	1	c_temp1_reg[0]/C	c_temp2_reg[0]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 14	0.152	0	1	1	c_temp1_reg[1]/C	c_temp2_reg[1]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 15	0.152	0	1	1	c_temp1_reg[2]/C	c_temp2_reg[2]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 16	0.152	0	1	1	c_temp1_reg[3]/C	c_temp2_reg[3]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 17	0.152	0	1	1	d_temp1_reg[0]/C	d_temp2_reg[0]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 18	0.152	0	1	1	d_temp1_reg[1]/C	d_temp2_reg[1]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 19	0.152	0	1	1	d_temp1_reg[2]/C	d_temp2_reg[2]/D	0.288	0.147	0.141	0.0	CLK	CLK		

Timing Summary - timing_1

Sources | Netlist

- temp_ab_max2[0]_i_1 (LUT5)
- temp_ab_max2[1]_i_1 (LUT5)
- temp_ab_max2[2]_i_1 (LUT5)
- temp_ab_max2[2]_i_2 (LUT6)
- temp_ab_max2[3]_i_1 (LUT2)
- temp_ab_max2_reg[0] (FDCE)
- temp_ab_max2_reg[1] (FDCE)
- temp_ab_max2_reg[2] (FDCE)
- temp_ab_max2_reg[3] (FDCE)
- temp_abc_max3[0]_i_1 (LUT5)
- temp_abc_max3[1]_i_1 (LUT5)
- temp_abc_max3[2]_i_1 (LUT5)
- temp_abc_max3[2]_i_2 (LUT6)
- temp_abc_max3[3]_i_1 (LUT2)
- temp_abc_max3_reg[0] (FDCE)

Path Properties

Path 1

Summary

Name	Path 1
Slack	0.000ns
Source	temp_abc_max3_reg[0]/C (rising edge-trigge

General | Properties | **Report** | Cells | Nets | Net Segme

Project Summary | Device | Schematic | **Timing Constraints**

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

1/3.37=297 MHZ

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Tcl Console | Messages | Log | Reports | Design Runs | **Timing**

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths
  - CLK
    - Setup 0.000 ns (10)
    - Hold 0.145 ns (10)

Intra-Clock Paths - CLK - Hold

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Cloc
Path 11	0.145	1	2	4	a_temp1_reg[3]/C	temp_ab_max2_reg[3]/D	0.389	0.248	0.141	0.0	CLK	CLK		
Path 12	0.145	1	2	4	temp_ab_max2_reg[3]/C	temp_abc_max3_reg[3]/D	0.389	0.248	0.141	0.0	CLK	CLK		
Path 13	0.152	0	1	1	c_temp1_reg[0]/C	c_temp2_reg[0]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 14	0.152	0	1	1	c_temp1_reg[1]/C	c_temp2_reg[1]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 15	0.152	0	1	1	c_temp1_reg[2]/C	c_temp2_reg[2]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 16	0.152	0	1	1	c_temp1_reg[3]/C	c_temp2_reg[3]/D	0.288	0.147	0.141	0.0	CLK	CLK		
Path 17	0.152	0	1	1	d_temp1_reg[0]/C	d_temp2_reg[0]/D	0.288	0.147	0.141	0.0	CLK	CLK		

Timing Summary - timing_1