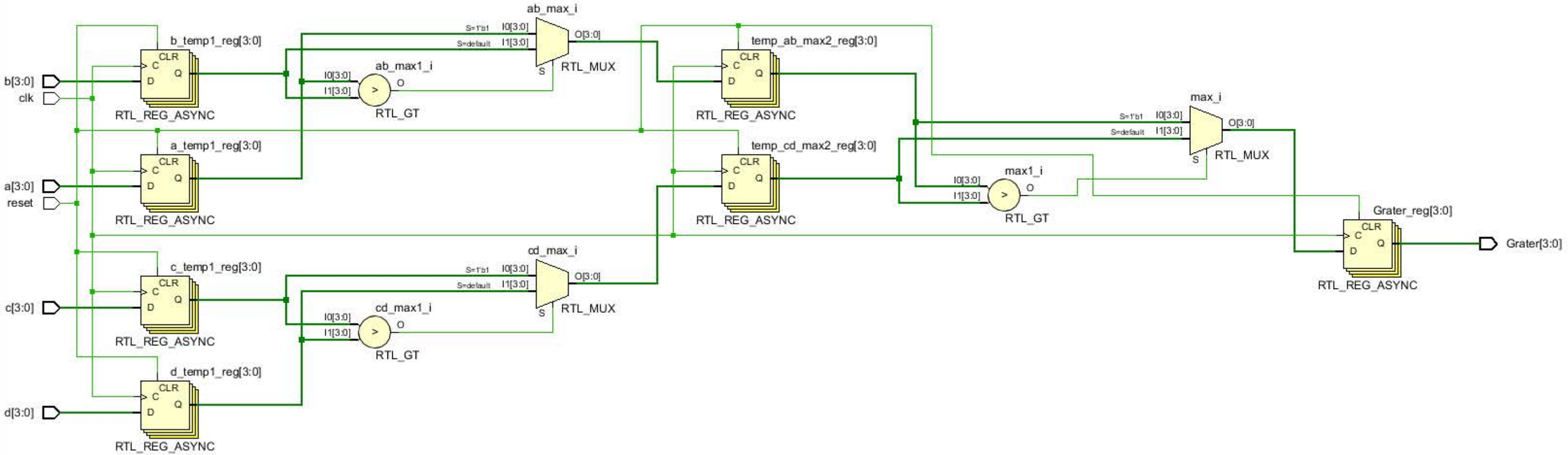
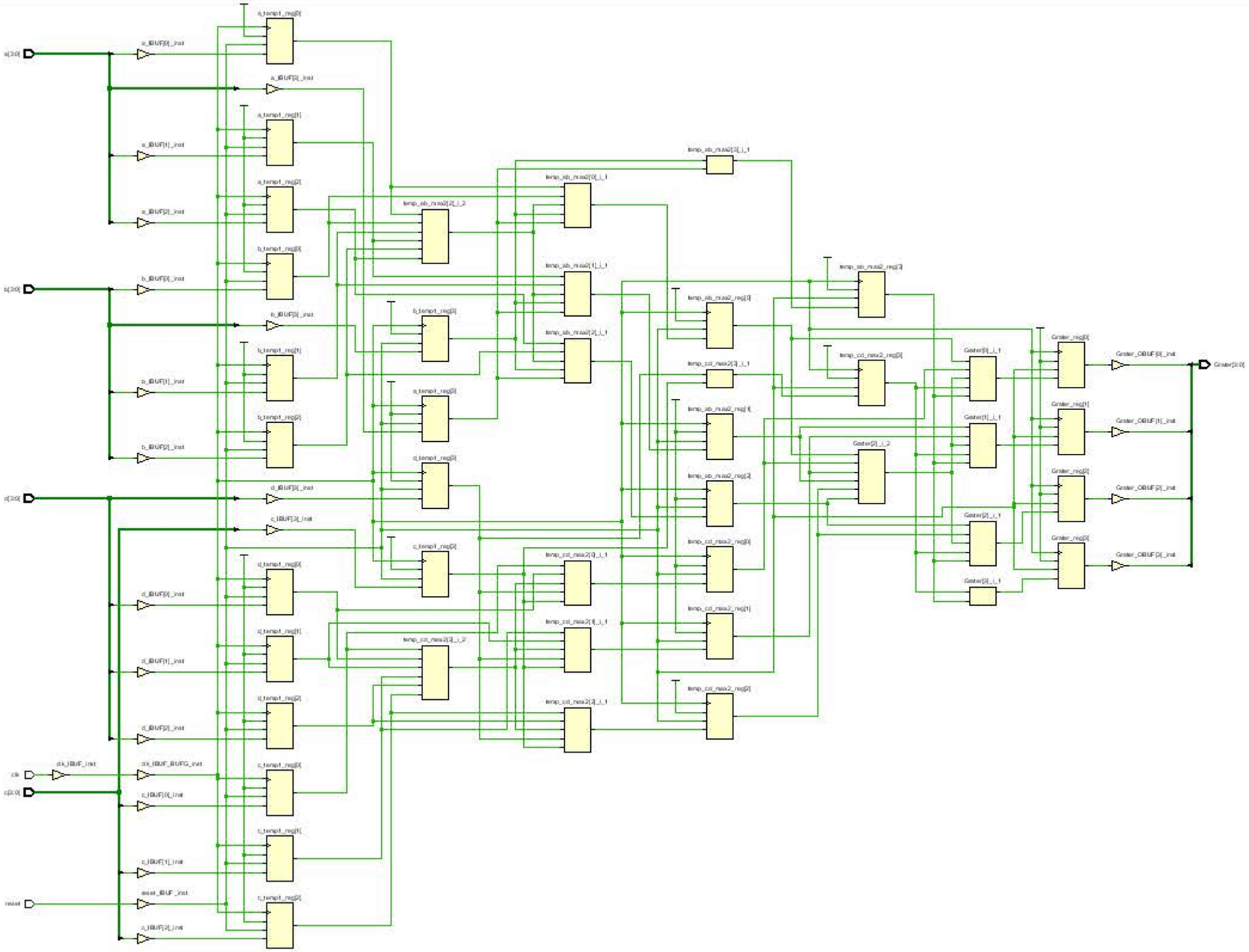
Project Summary | Schematic

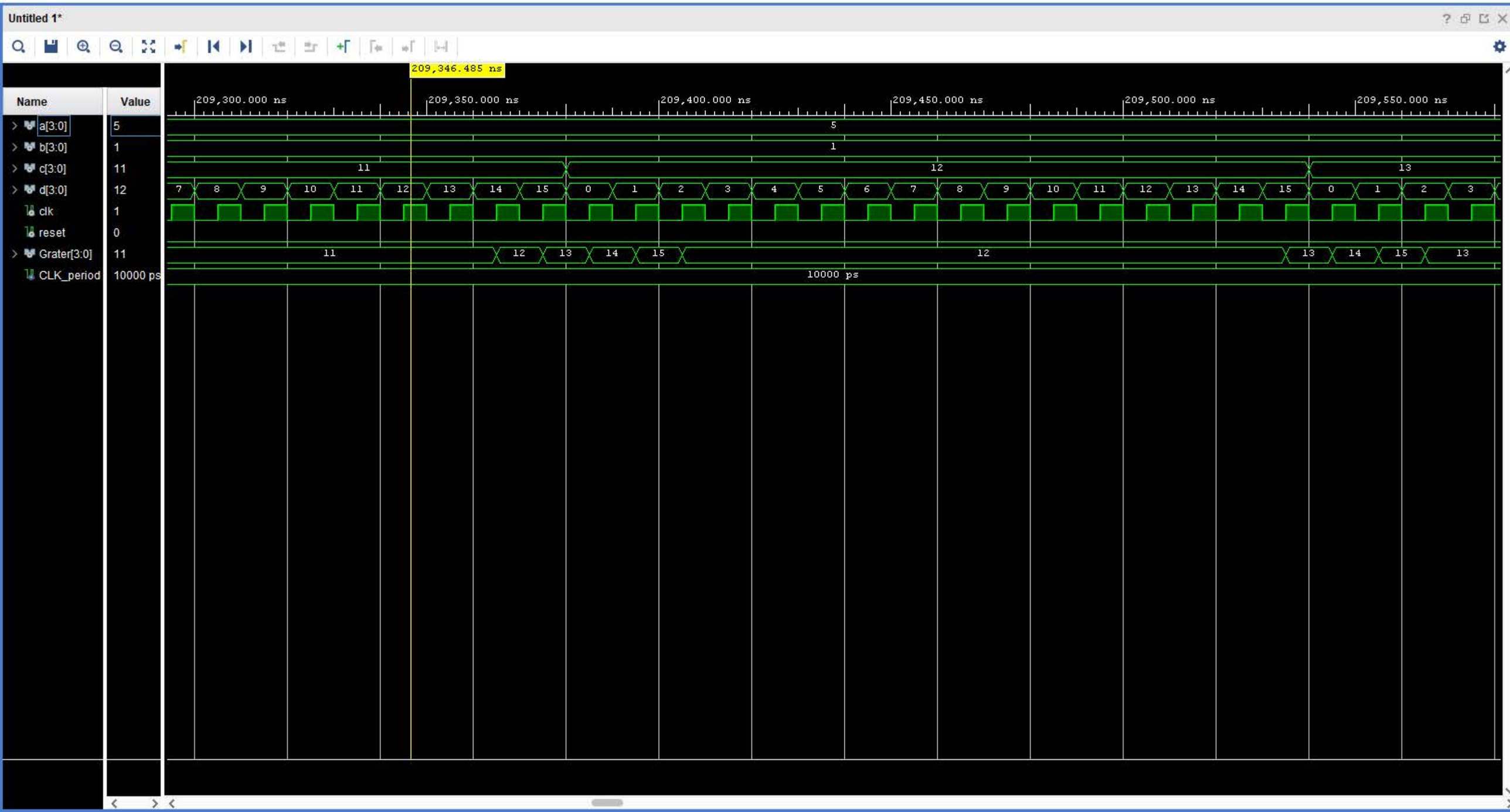
34 Cells | 22 I/O Ports | 61 Nets

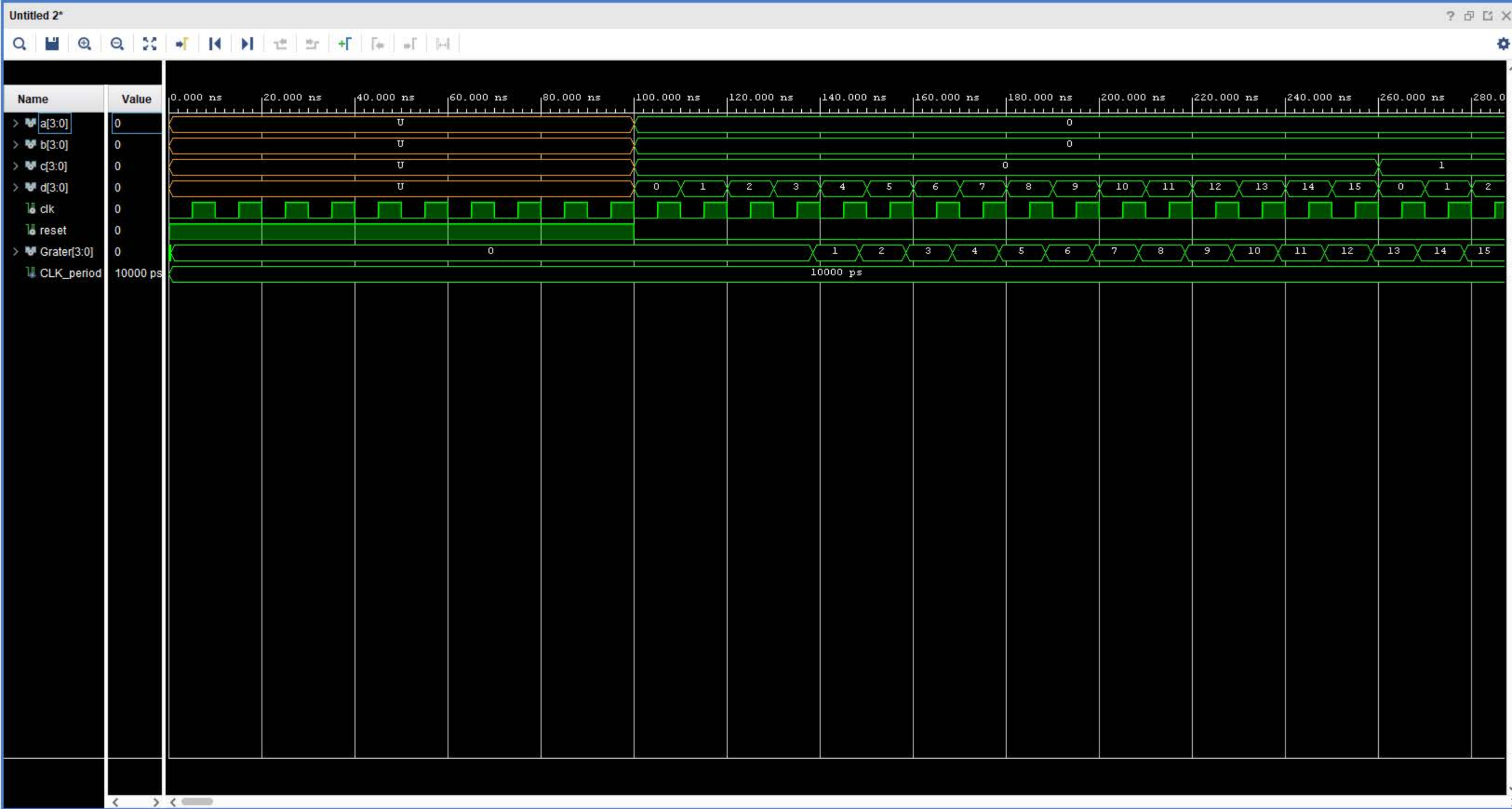


Project Summary | Device | Schematic

66 Cells | 22 I/O Ports | 85 Nets




Untitled 1*
209,346.485 ns
Name
Value
209,300.000 ns
209,350.000 ns
209,400.000 ns
209,450.000 ns
209,500.000 ns
209,550.000 ns
a[3:0]
5
b[3:0]
1
c[3:0]
11
d[3:0]
12
clk
1
reset
0
Grater[3:0]
11
CLK_period
10000 ps
7 8 9 10 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3
11 12 13 14 15 12 13 14 15 13


Untitled 2*
Name
Value
a[3:0]
b[3:0]
c[3:0]
d[3:0]
clk
reset
Grater[3:0]
CLK_period
0
10000 ps
0.000 ns
20.000 ns
40.000 ns
60.000 ns
80.000 ns
100.000 ns
120.000 ns
140.000 ns
160.000 ns
180.000 ns
200.000 ns
220.000 ns
240.000 ns
260.000 ns
280.0
U
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
10000 ps

Project Summary | Device | Schematic | Timing Constraints

- Clocks (1)
  - Create Clock (1)
  - Create Generated Clock (0)
  - Rename Auto-Derived Clock (0)
  - Set Clock Latency (0)
  - Set Clock Uncertainty (0)
  - Set Clock Groups (0)
  - Set Clock Sense (0)
  - Set Input Jitter (0)
  - Set System Jitter (0)
  - Set External Delay (0)
- Inputs (0)
  - Set Input Delay (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Timing

- General Information
- Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0,000 ns	Worst Hold Slack (WHS):	0,145 ns	Worst Pulse Width Slack (WPWS):	1,185 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	12	Total Number of Endpoints:	12	Total Number of Endpoints:	29

Timing Summary - timing_1

Project Summary | Device | Schematic | Timing Constraints

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)
- Set Input Delay (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Timing

- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths
  - CLK
    - Setup 0,000 ns (10)

Intra-Clock Paths - CLK - Setup

Καθ. διάδοσης

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Cl
Path 1	0.000	2	3	3	temp_ab_max2_reg[0]/C	Grater_reg[0]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 2	0.000	2	3	3	temp_ab_max2_reg[0]/C	Grater_reg[1]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 3	0.000	2	3	3	temp_ab_max2_reg[0]/C	Grater_reg[2]/D	2.340	0.897	1.443	3.4	CLK	CLK		
Path 4	0.894	2	3	3	a_temp1_reg[0]/C	temp_ab_max2_reg[0]/D	2.340	0.897	1.443	3.4	CLK	CLK		

Timing Summary - timing_1

Project Summary | Device | Schematic | Timing Constraints

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)
- Set Input Delay (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Timing

Hold 0,145 ns (10)
Pulse Width 1,185 ns (30)
Inter-Clock Paths
Other Path Groups
User Ignored Paths
Unconstrained Paths

Intra-Clock Paths - CLK - Hold

Καθ.μολυνσης

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock	Destination Clock	Exception	Cl
Path 11	0.145	1	2	4	a_temp1_reg[3]/C	temp_ab_max2_reg[3]/D	0.389	0.248	0.141	0.0	CLK	CLK		
Path 12	0.145	1	2	4	c_temp1_reg[3]/C	temp_cd_max2_reg[3]/D	0.389	0.248	0.141	0.0	CLK	CLK		
Path 13	0.209	1	2	4	a_temp1_reg[3]/C	temp_ab_max2_reg[0]/D	0.453	0.245	0.208	0.0	CLK	CLK		
Path 14	0.209	1	2	4	a_temp1_reg[3]/C	temp_ab_max2_reg[1]/D	0.453	0.245	0.208	0.0	CLK	CLK		

Timing Summary - timing_1

Project Summary | Device | Schematic | Timing Constraints

Clocks (1)
- Create Clock (1)
- Create Generated Clock (0)
- Rename Auto-Derived Clock (0)
- Set Clock Latency (0)
- Set Clock Uncertainty (0)
- Set Clock Groups (0)
- Set Clock Sense (0)
- Set Input Jitter (0)
- Set System Jitter (0)
- Set External Delay (0)

Inputs (0)
- Set Input Delay (0)

Create Clock

Position	Clock Name	Period (ns)	Rise At (ns)	Fall At (ns)	Add Clock	Source Objects	Source File	Scoped Cell	Current Instance
1	CLK	3.370	0.000	1.685	☐	[get_ports clk]	compare_xdc.xdc		
Double click to create a Create Clock constraint									

1/3.37 = 297MHz

All Constraints

Position	Command	Scoped Cell
Constraints		
compare_xdc.xdc (C:/Users/rouss/Desktop/compare_xdc.xdc)		
1	create_clock -period 3.370 -name CLK -waveform {0.000 1.685} [get_ports clk]	

Apply | Cancel

Timing

Timer Settings
- Design Timing Summary
- Clock Summary (1)
- Check Timing (21)
- Intra-Clock Paths
  - CLK
    - Setup 0.000 ns (10)

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	0,000 ns	Worst Hold Slack (WHS):	0,145 ns	Worst Pulse Width Slack (WPWS):	1,185 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	12	Total Number of Endpoints:	12	Total Number of Endpoints:	29

Timing Summary - timing_1