

# A Comparative Analysis of 6T, 7T, 8T and 9T SRAM Cells

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**Abstract-** Static Random Access Memory (SRAM) is a type of memory that is meant to enable high-speed and low-power applications. As technology shrinks, so does the power supply, reducing the noise margin of SRAM cells. The smaller noise margin causes even greater leakage power in the SRAM cells. The major goal of this project is to address the power dissipation that happens in traditional Static Random Access Memory (SRAM) cells during read-and-write operations. This issue can be rectified by using dual-threshold voltage for 6T, 7T, 8T, and 9T SRAM Cells. The power dissipation and delay of these cells are estimated and compared. This is implemented in 90nm Generic Process Design Kit (GPDK) using Cadence software (crack version).

**Keywords-** Delay, Dual-threshold-voltage, Noise margin, Power dissipation, SRAM, T(transistor)

## 1. Background

In today's world, devices are being scaled down to achieve high speed and performance, with supply voltage and transistor size being crucial parameters. However, this can lead to increased sub-threshold leakage current, causing static power dissipation. SRAM-based cache memories are ideal for system on-chip applications due to their high speed and low power consumption. The cache occupies over 50% of a microprocessor's chip area, making leakage power a major source of power dissipation. This paper compares the performance of six transistor (6T), seven transistor (7T), S transistor (ST), and nine transistor (9T) SRAM cells, designed using dual-threshold voltage techniques. The delays and power consumption of these cells were calculated using Cadence tool in GPDK 90 nm technology.

**6T SRam:** During a read operation in a conventional 6T SRAM cell, the data storage nodes (Node Q and Node QB) are directly accessed via the bitline access transistors (NM1 & NM0 in fig-1). The storage nodes are disrupted during reading due to voltage division between cross-coupled inverters and bit-line access transistors. The data is most vulnerable to external

noise during a read operation due to the intrinsic disturbance produced by a standard 6T SRAM cell.

The basic requirement for a write operation in the 6T SRAM cell is that the strength ratio of the pass-gate transistor to that of the pull-up transistor be sufficiently large. The term for this is cell gamma ratio. The bit-lines (BL and BLB) are driven to complementary voltage levels before selecting the wordline (WL). The bit-line (BL) receives the input. When the access transistors (NM1 & NM0) are accessed via word-line (WL), the data from the input is written in the cell.

The basic condition for a read operation in a 6T SRAM cell is that the strength of the pull-down transistor (drive current) to that of the pass-gate transistor is sufficiently large. It's known as cell beta ratio. The bit-lines (BL and BLB) are typically precharged to a high level (Vdd), and the word-line (WL) is then pulsed to a low level to read the data previously written to the cell.

**7T SRam:** A 7T SRAM cell structure employs single-ended read and write mechanisms. For reading data from the cell, the read bitline (RBL) and the transistor stack formed by NM7 and NM6 are used in fig-9.

To begin the write operation, the write signal 'W' is set to Vdd, while the read signal 'R' remains at Vss. The write bit-line (WBL) receives the input. The write-line (W) is used to access the access transistors (NM8), and the data from the input is written in the cell. The pass transistor NM8 must be more powerful than the pull-up transistor PM1.

The 'RBL' is precharged to Vdd prior to a read operation. The cell's written data can be read by precharging the read bitline (RBL) and read-line (R) to Vdd. To read the data previously written to the cell, charge the read-line (R) to Vdd and pulse the write-line (W) to a low level. If a '1' is stored at Node Q, the transistor stack formed by NM7 and NM6 discharges 'RBL'. Alternatively, if a '0' is stored at Node Q, the value 'RBL' is kept at Vdd. During a read operation, the storage nodes (NodeQ and NodeQB) are completely isolated from the bit lines.

**8T SRam:** The memory cell area is reduced by using single-ended data access for read operations with an alternative 8T SRAM circuit structure. The dual-Vt 8T SRAM cell provides the best overall performance. The 8T memory cell's left subcircuit is a standard 6T SRAM cell. The write operation is identical to that of a standard 6T SRAM cell. For reading the stored data from the cell, an alternative communication channel composed of a read bit line (RBL) and a transistor stack of 2 nmos (NM4 & NM5 in fig-17) is used.

When performing a write operation, the input is sent to write bitline-1 (WBL-1) and its complement is sent to write bitline-2 (WBL-2). The write-line (W) access transistor (NM2) is accessed, the data from the input is written in the cell, and the write process is completed.

By performing a read operation, the read line (R) is precharged to Vdd, and the read transistor turns on. Precharging the read bit-line (RBL) and read-line (R) to Vdd allows the written data to be read from the cell. To read the data previously written to the cell, the write-line (W) should be pulsed to a low level.

**9T SRam:** A dual-Vt 9T SRAM cell with improved data stability is presented. The upper subcircuit of the memory cell is essentially a 6T SRAM cell with minimum-sized devices. A write signal (W) controls the two write access transistors. This upper memory subcircuit stores the data. The lower subcircuit of the new cell is made up of bit-line access transistors and read access transistors. The operations of bit-line access transistors are controlled by the data stored in the cell, whereas the read access transistor is controlled by a separate read signal (R).

During a write operation, the write signal 'W' is high while the read signal 'R' is kept low. The read access transistor has been disabled. The two write access transistors have been activated. The bitline (BL) receives the input. When the access transistors are accessed via write-line(W), the data from the input is written in the cell.

During a read operation, the read signal 'R' is high while the write signal 'W' is low. The read access transistor is turned on. By connecting the 'BL' and 'BLB' to Vdd, the written data can be read from the cell.

To read the data previously written to the cell, charge the read-line (R) to Vdd and pulse the write-line (W) to a low level. When compared to a standard 6T

SRAM cell, the read stability of the 9T SRAM cell is improved.

## 2. Future Aspects

SRAM cells, which serve as rapid and low-power memory storage units, are essential components of modern electronic gadgets. As technology advances, the following are some potential future elements and trends for 6T, 7T, 8T, and 9T SRAM cells:

**Lower Power Consumption:** Future SRAM cells will almost certainly focus on lowering power consumption even further. This is especially significant in mobile devices and IoT devices, where energy economy is critical for increasing battery life. SRAM cells may be able to operate successfully at lower supply voltages thanks to advanced designs and circuit optimizations.

**Greater Density:** As transistor sizes shrink and fabrication techniques improve, SRAM cell density on a device will increase. This may result in larger on-chip caches or additional memory storage in the same region. However, as transistor sizes decrease, they become more vulnerable to leakage currents and other quantum mechanical effects, necessitating novel solutions to ensure cell stability and data integrity.

**Better Reliability:** As SRAM cell sizes and transistor counts fall, there is growing worry regarding reliability and susceptibility to various types of noise, including as manufacturing variation, radiation-induced soft mistakes, and electromigration. To improve overall reliability, future designs may use error correction techniques or innovative cell architectures.

**Multiport and Multi-Function SRAM:** There may be a shift towards SRAM cells with multiple read and write ports, allowing for quicker and more parallel memory access. This is beneficial in applications that require concurrent access from numerous components or processes, such as GPUs or neural network accelerators.

**Variability and Process Tolerance:** As transistor sizes shrink, process variance becomes a serious issue. Future SRAM designs could incorporate mechanisms to adjust to process differences, ensuring constant performance and data retention across a wide range of manufacturing environments.

**FinFET and Beyond:** Today's SRAM designs rely heavily on planar transistor technology. Future SRAM cells may use more advanced transistor designs, such as FinFET or nanowire transistors, which provide

better leakage current management and allow for even lower cell sizes.

**Non-Volatile SRAM:** Research on merging the speed and volatility of SRAM with non-volatile memory features is ongoing. This could lead to the development of non-volatile SRAM cells that keep data even when power is turned off, blurring the distinction between SRAM and traditional non-volatile memories like Flash.

### 3. Conclusion

The delay, leakage, static and dynamic power dissipation of various SRAM cells such as six-transistor (6T), seven-transistor (7T), eight-transistor (8T), and nine-transistor (9T) SRAM cells are compared utilizing CADENCE GPDK 90nm dual-threshold-voltage CMOS technology. The leakage power is lowered in the 7T SRAM cell, the static and dynamic power is reduced in

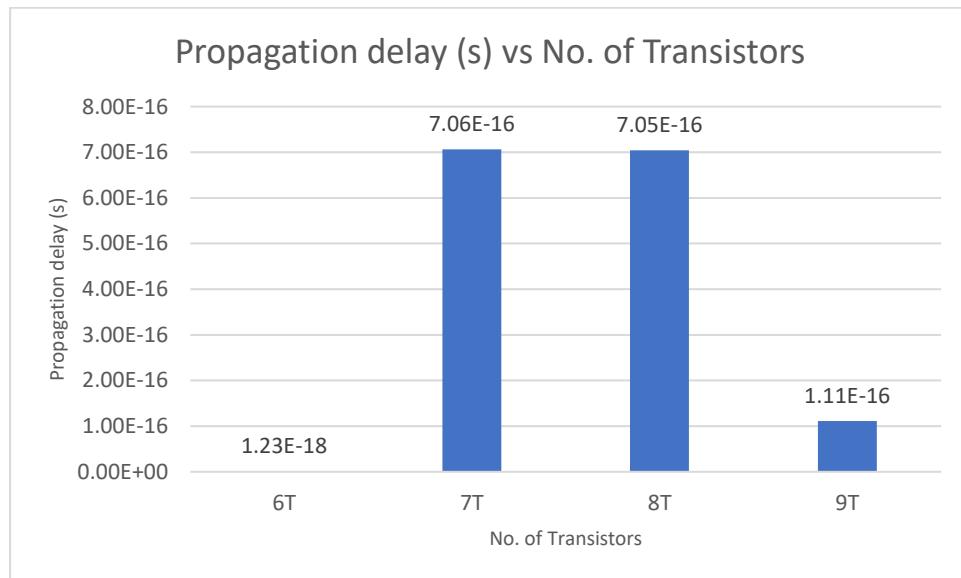
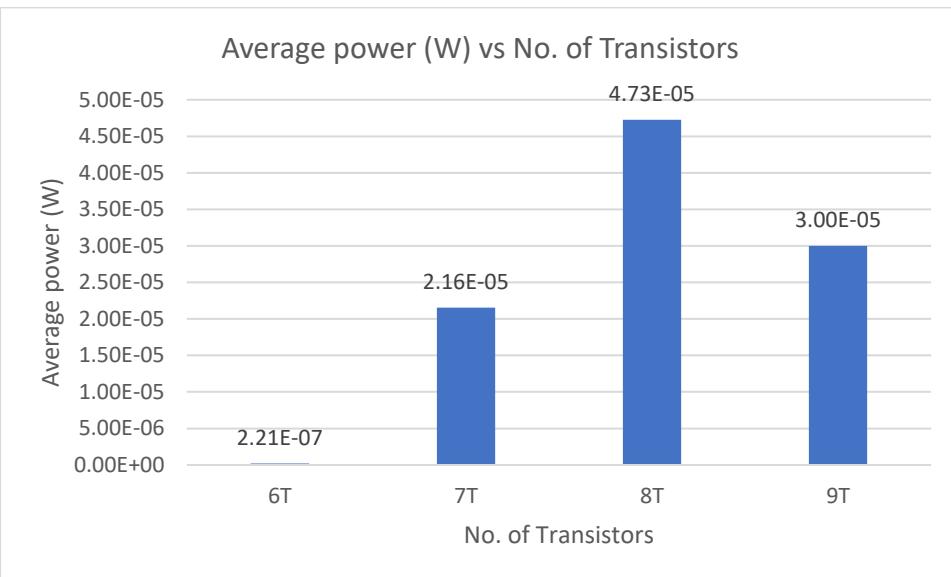
the 6T SRAM cell, and the latency is reduced in the 8T SRAM cell. There is no uniform solution to avoid tradeoffs between power, latency, and area. Designers must select appropriate procedures that meet the needs of the application and product. Thus, power dissipation and delay are decreased according to cell shape in CADENCE GPDK 90nm technology employing dual-threshold voltage approach.

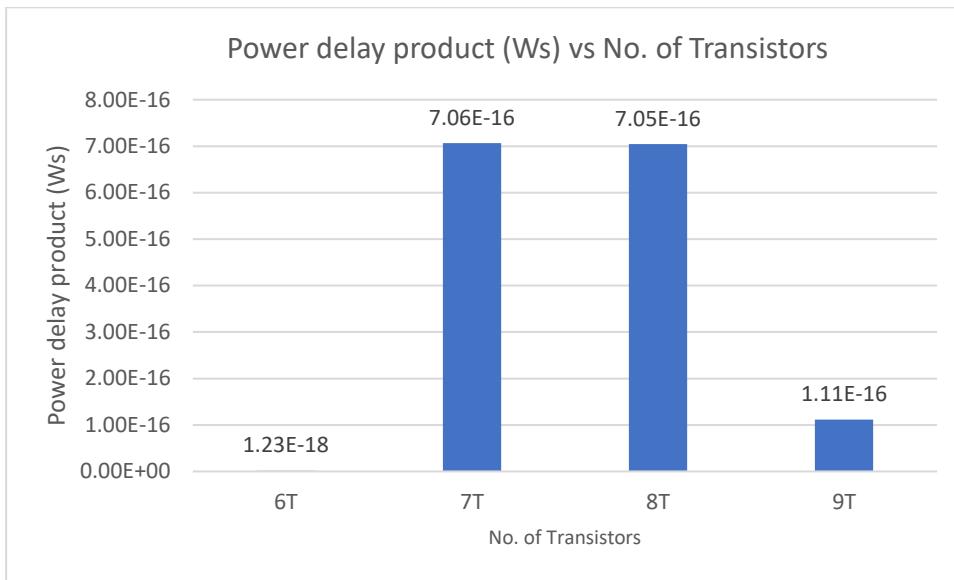
### 4. Reference

1. *A Comparative Analysis of 6T, 7T, 8T and 9T SRAM Cells in 90nm Technology, 2015* (C. Premalatha, K. Sarika, P. Mahesh Kannan Department of ECE, Department of ECE Karpaga Vinayaga College of Engineering and Technology, affiliated to Anna University, Pondicherry Engineering College, Affiliated to Pondicherry University Tamil Nadu, India)

## 5. Result (Data Representation)

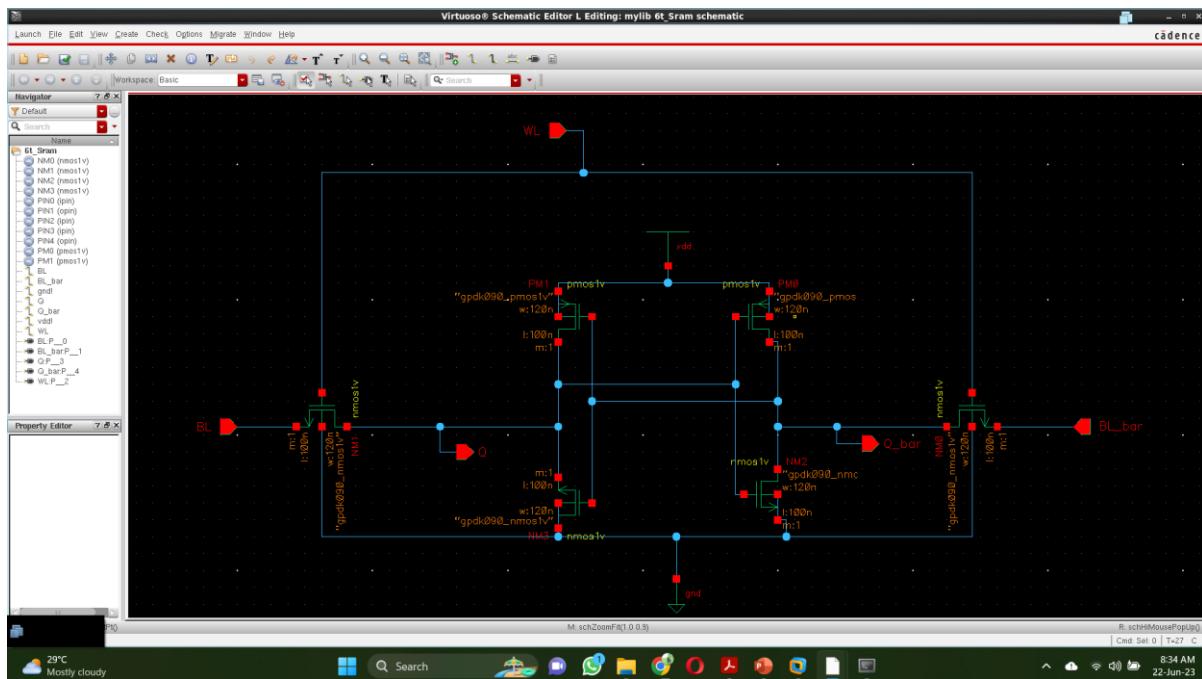
Topology	No. of transistors	Average power (W)	Propagation delay (s)	Power delay product (Ws)	Cell area ( $\mu\text{m}^2$ )	No. of DRC errors	No. of LVS mismatch
6T	6	220.8E-9	5.55E-12	1.225E-18	23.2	0	0
7T	7	21.56E-6	32.76E-12	7.063E-16	37	0	0
8T	8	47.25E-6	14.91E-12	7.045E-16	35.433875	2	1
9T	9	30E-6	4.368E-12	1.114E-16	130.1323	0	0





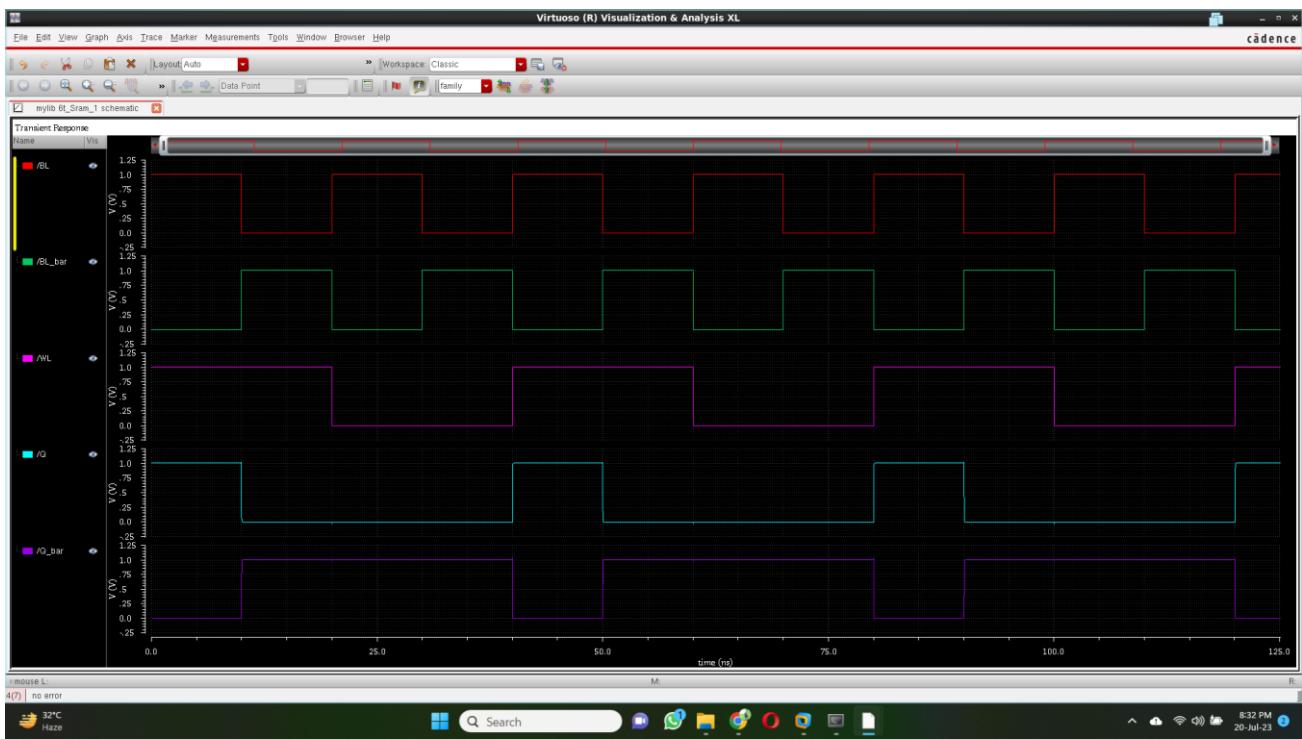
## 6. Result (Pictorial Representation)

### 6T SRam:

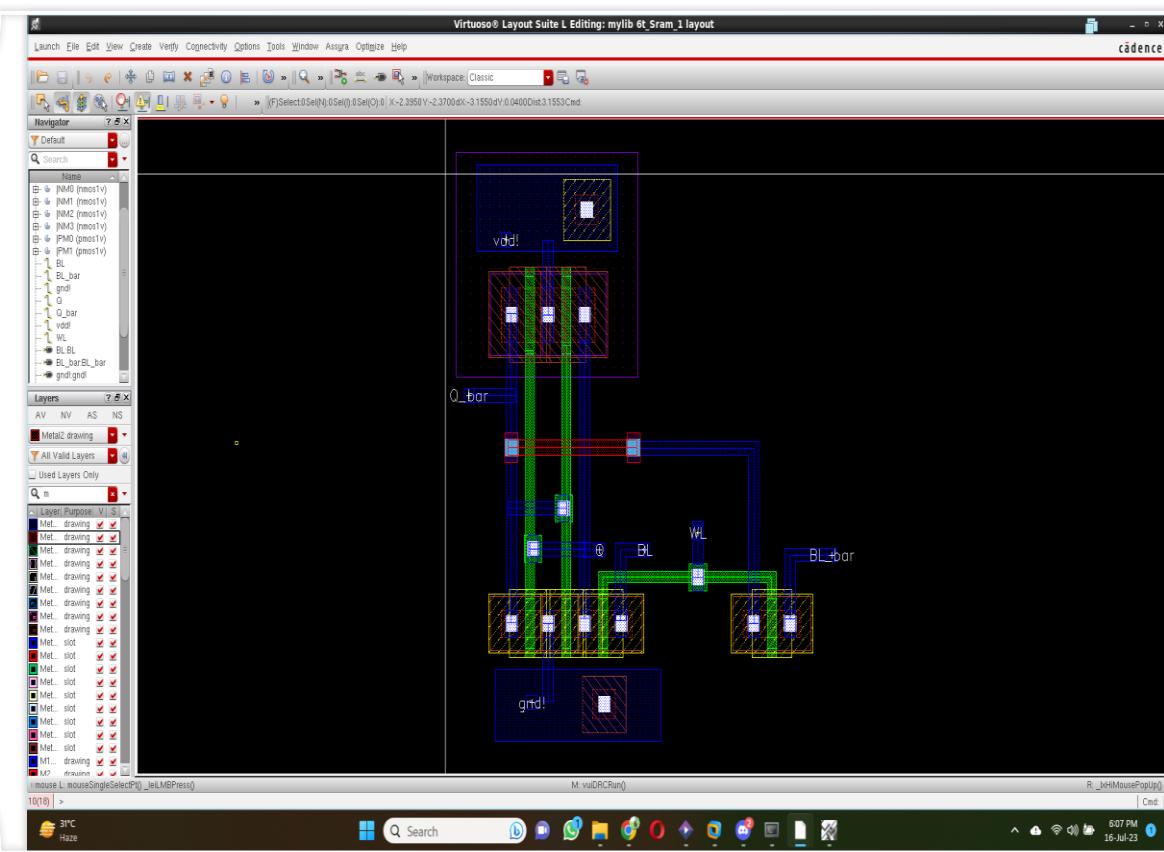


**Fig.1 6T SRAM cell schematic**

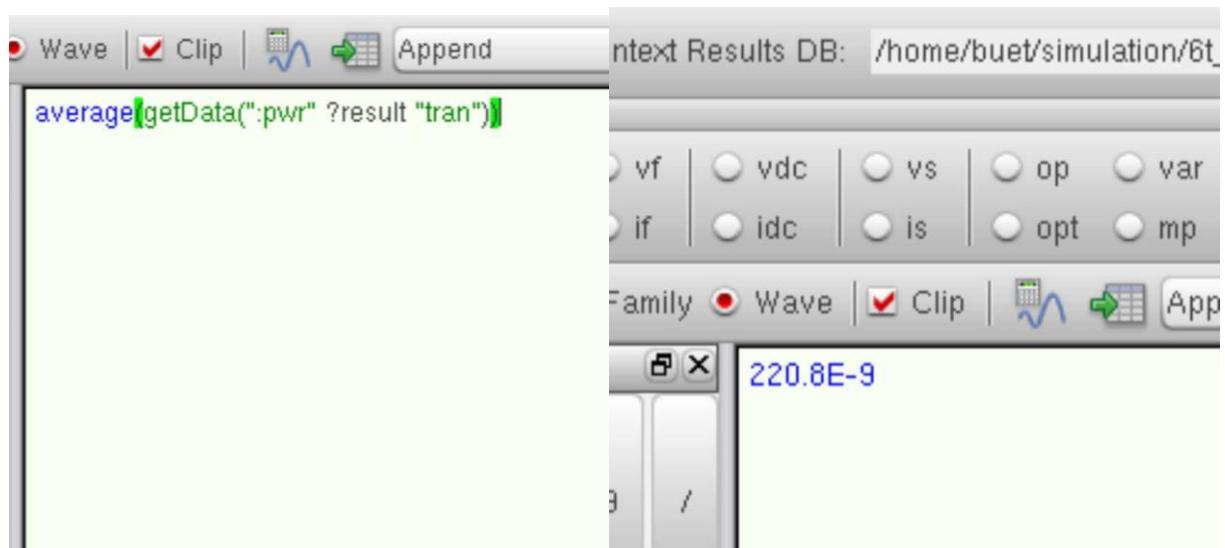
**Output:** Fig. 2 shows that 6T SRAM cell output using dual threshold voltage in Cadence 90nm technology in which the data '1' is written first when the word-line (WL) is pulsed to Vdd and then '0' is written to the cell. The data '1' written to the cell previously can be read by precharging both the bit-lines (BL and BLB) to Vdd and the word-line (WL) is kept low



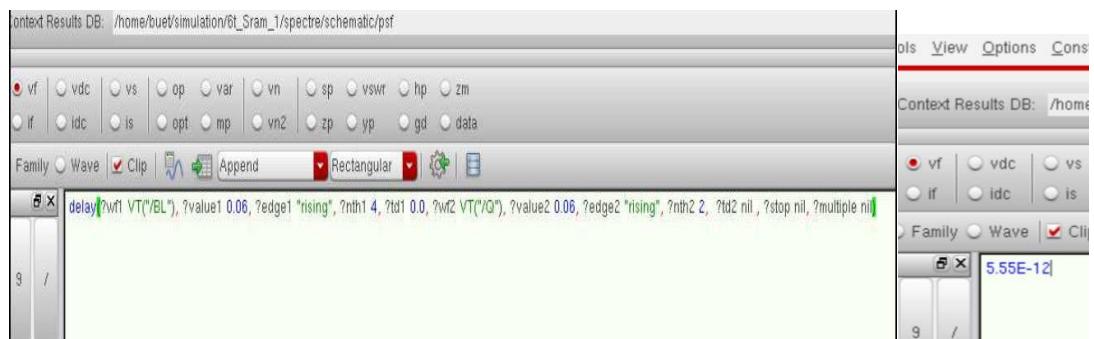
**Fig.2 Output waveform of 6T SRAM**



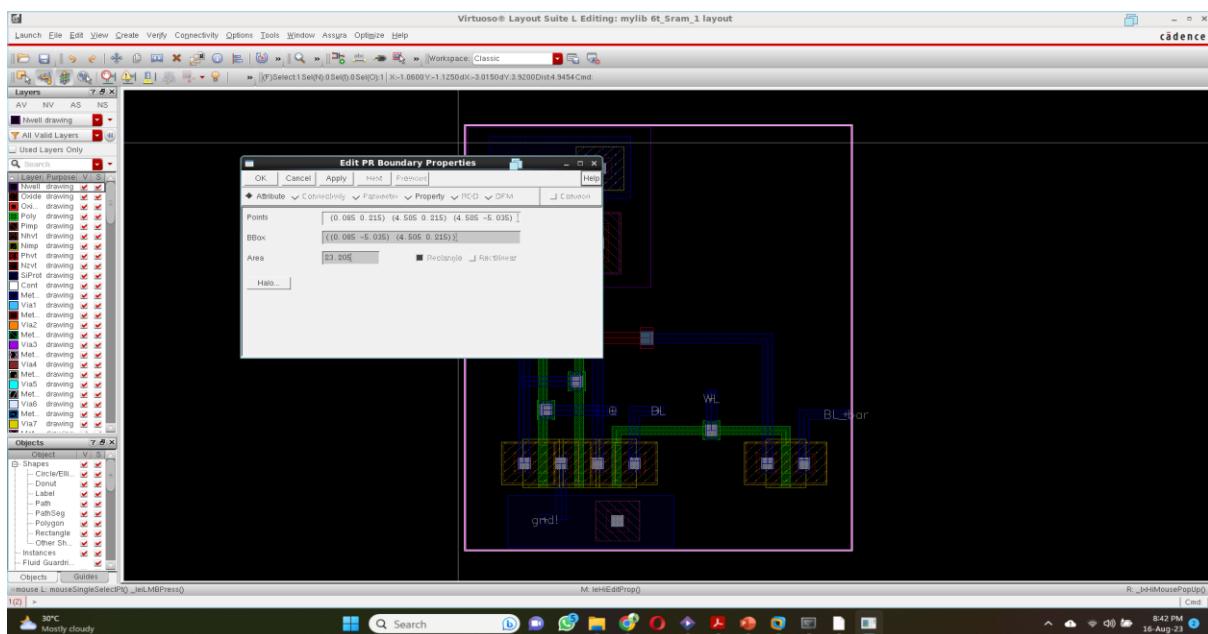
**Fig.3 Layout of 6T SRAM**



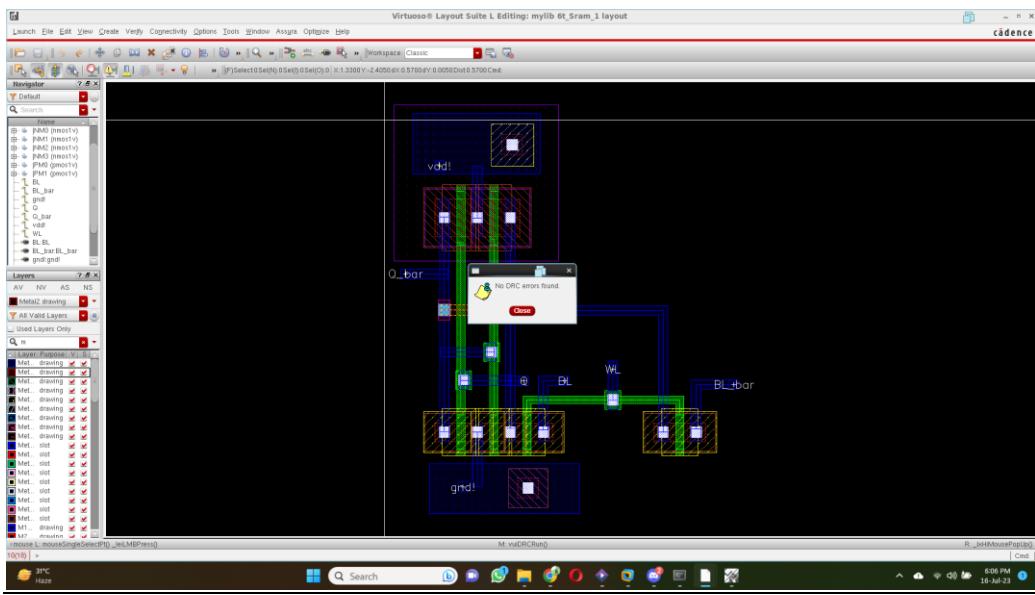
**Fig.4 Average power of 6T SRAM**



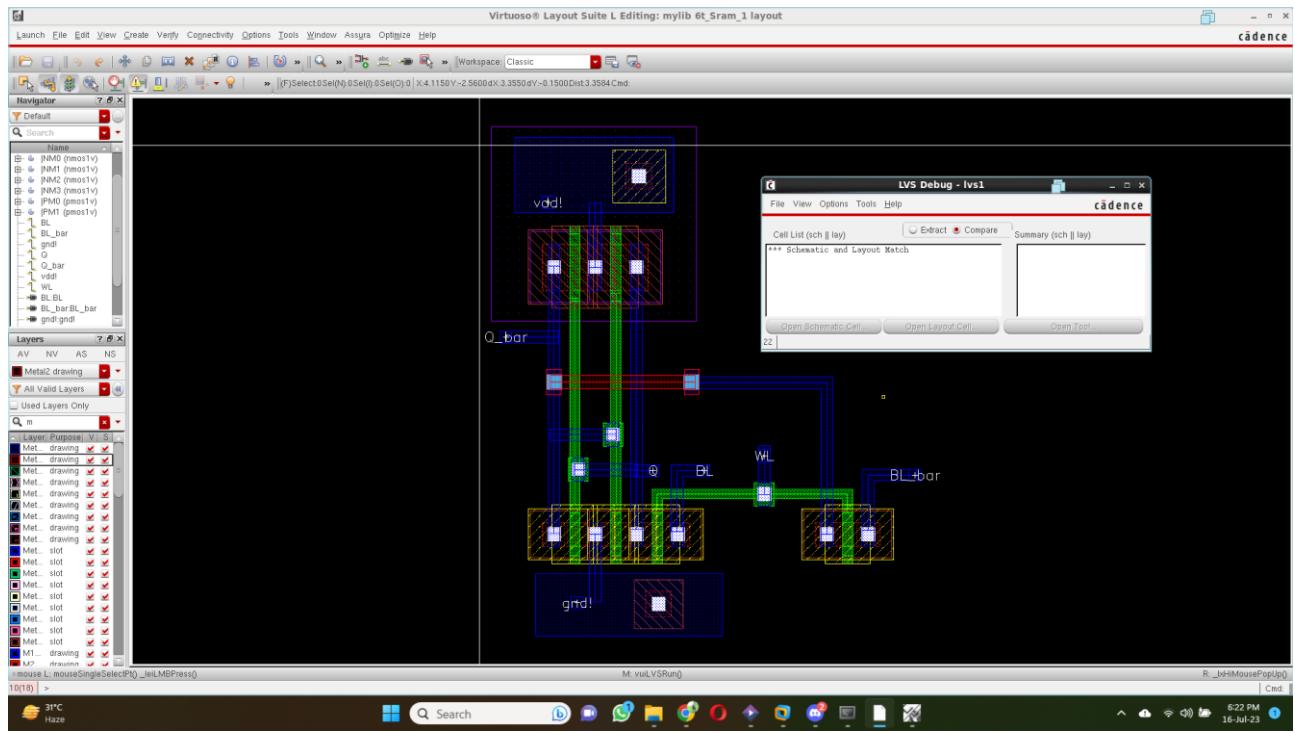
**Fig5. Delay of 6T SRAM**



**Fig6. Layout Area of 6T SRAM**

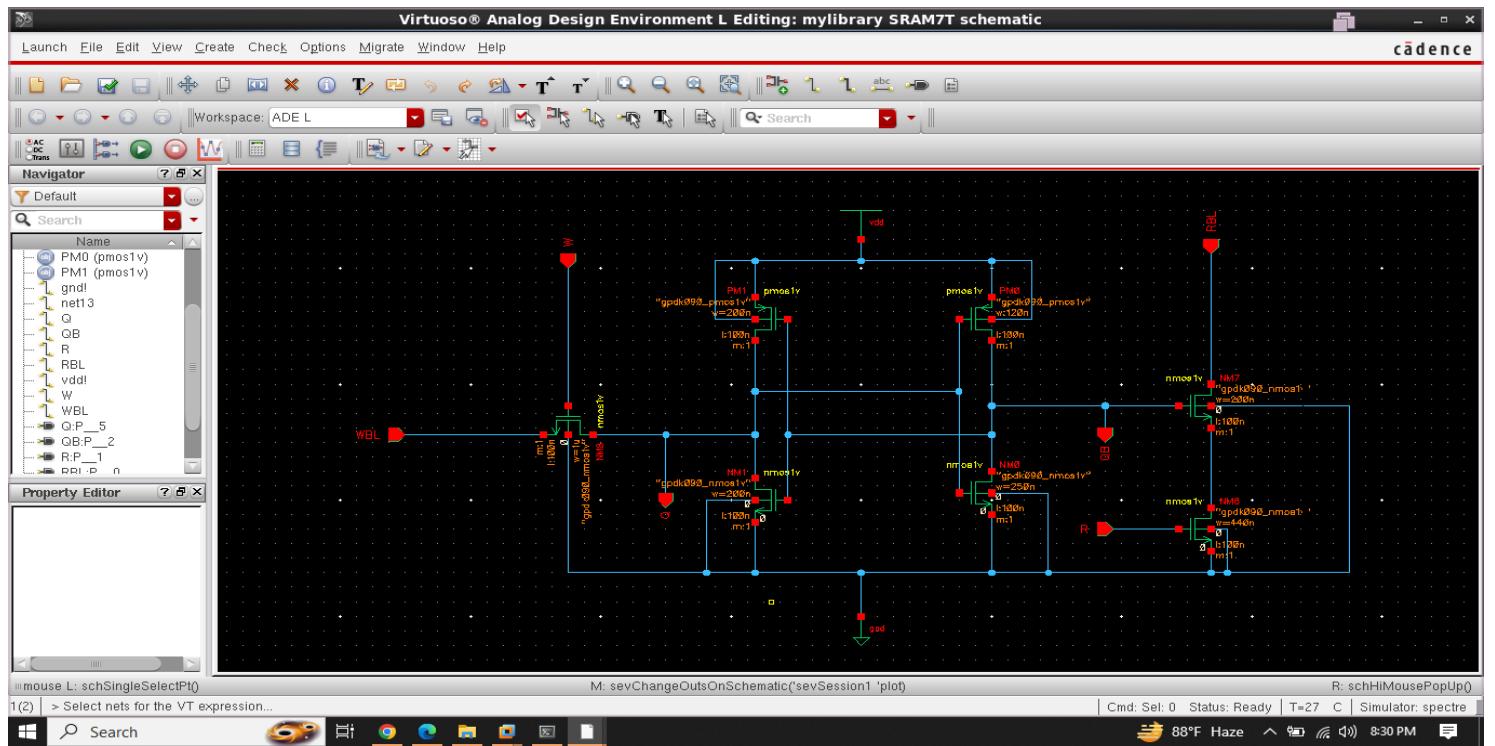


**Fig7. DRC check of 6T SRAM**



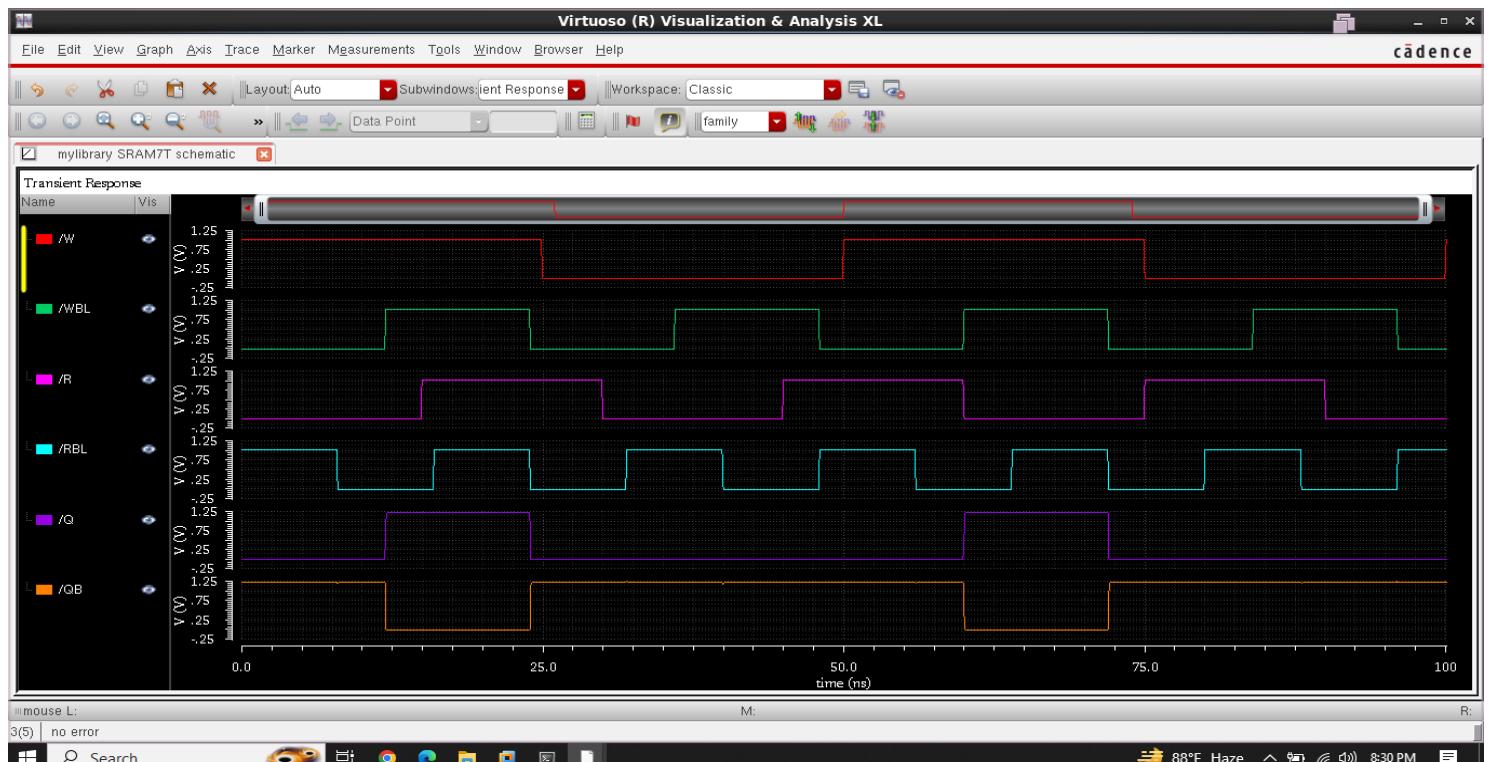
**Fig8. LVS check of 6T SRAM**

## 7T SRam:

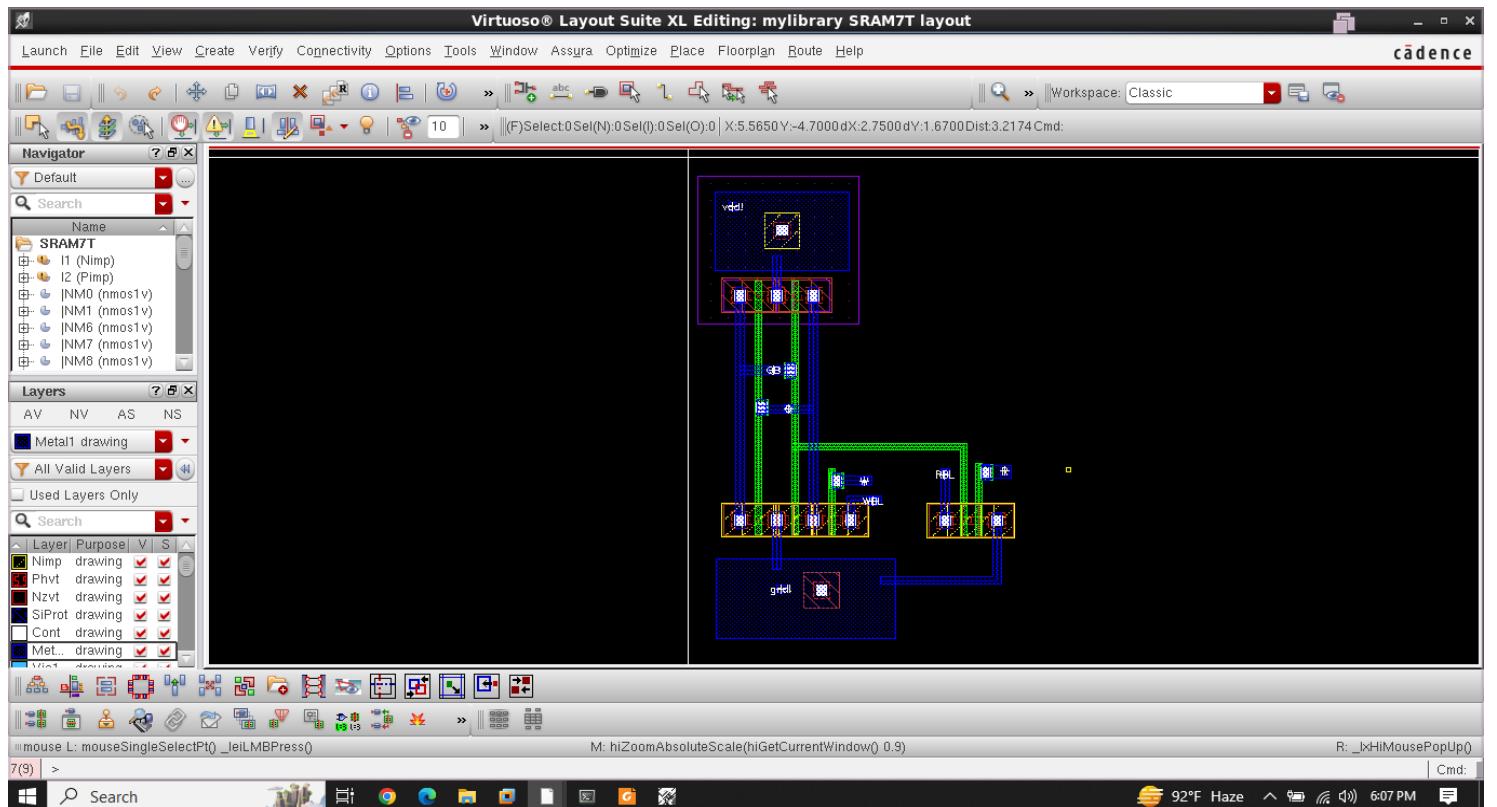


**Fig.9 7T SRAM cell schematic**

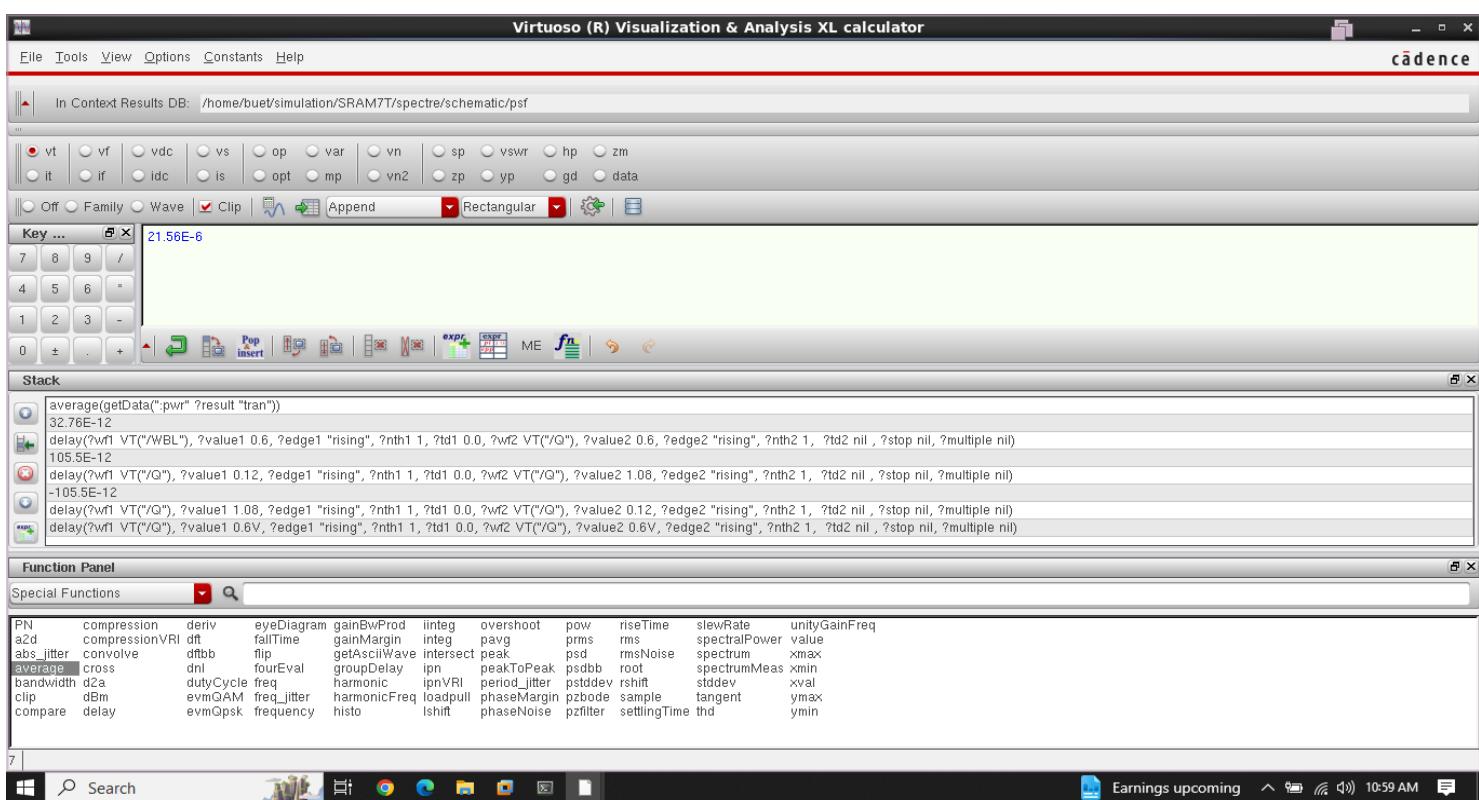
**Output:** Fig. 10 shows the output of the 7T SRAM cell in which the data '1' is written first when the write-line (WL) is pulsed to Vdd and then '0' is written to the cell. The data '1' written to the cell previously can be read by precharging the 'R' and 'RBL' to V dd when the read-line (R) is kept high and write-line (W) to low



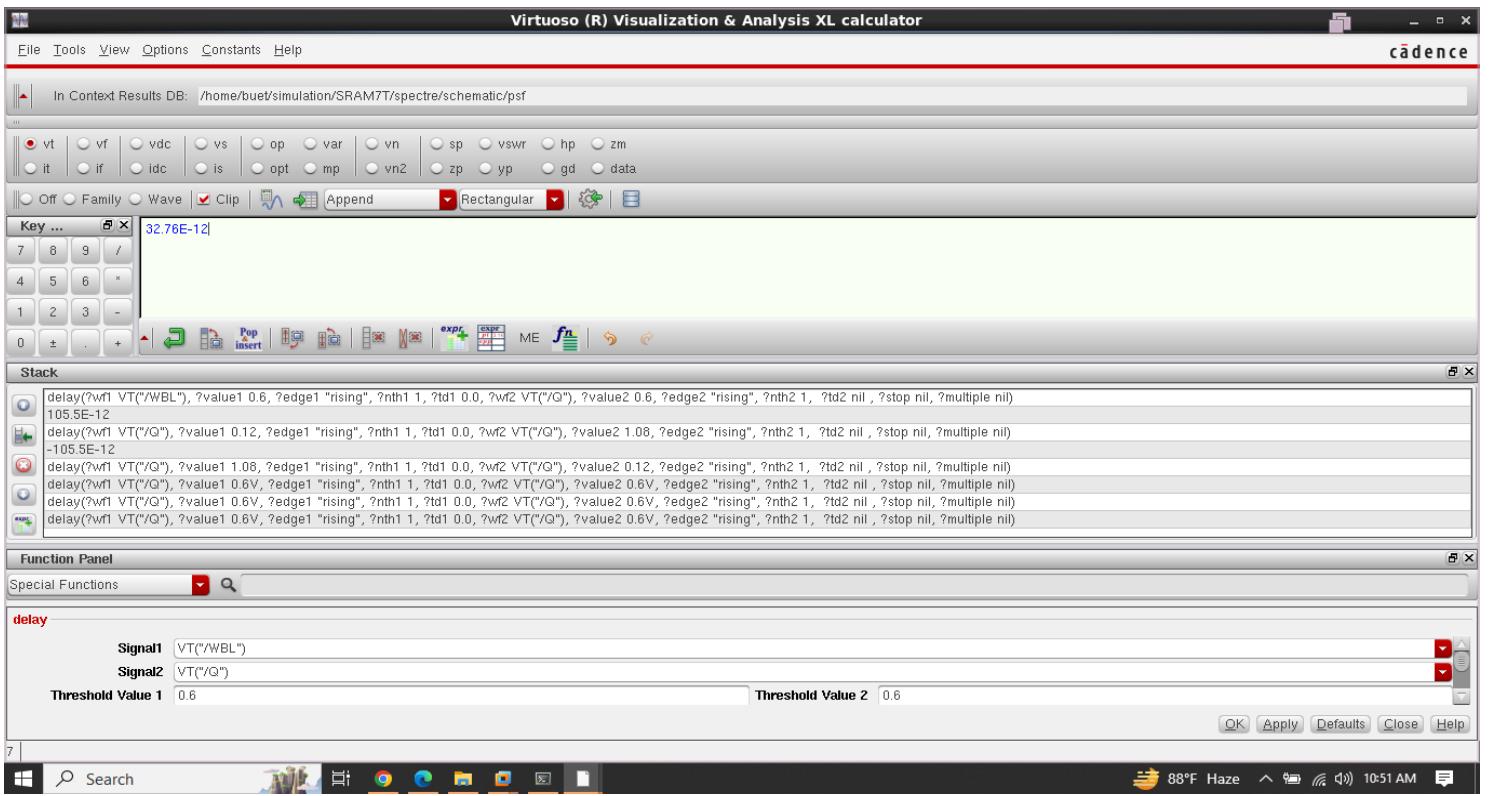
**Fig.10 Output Waveform of 7T SRAM**



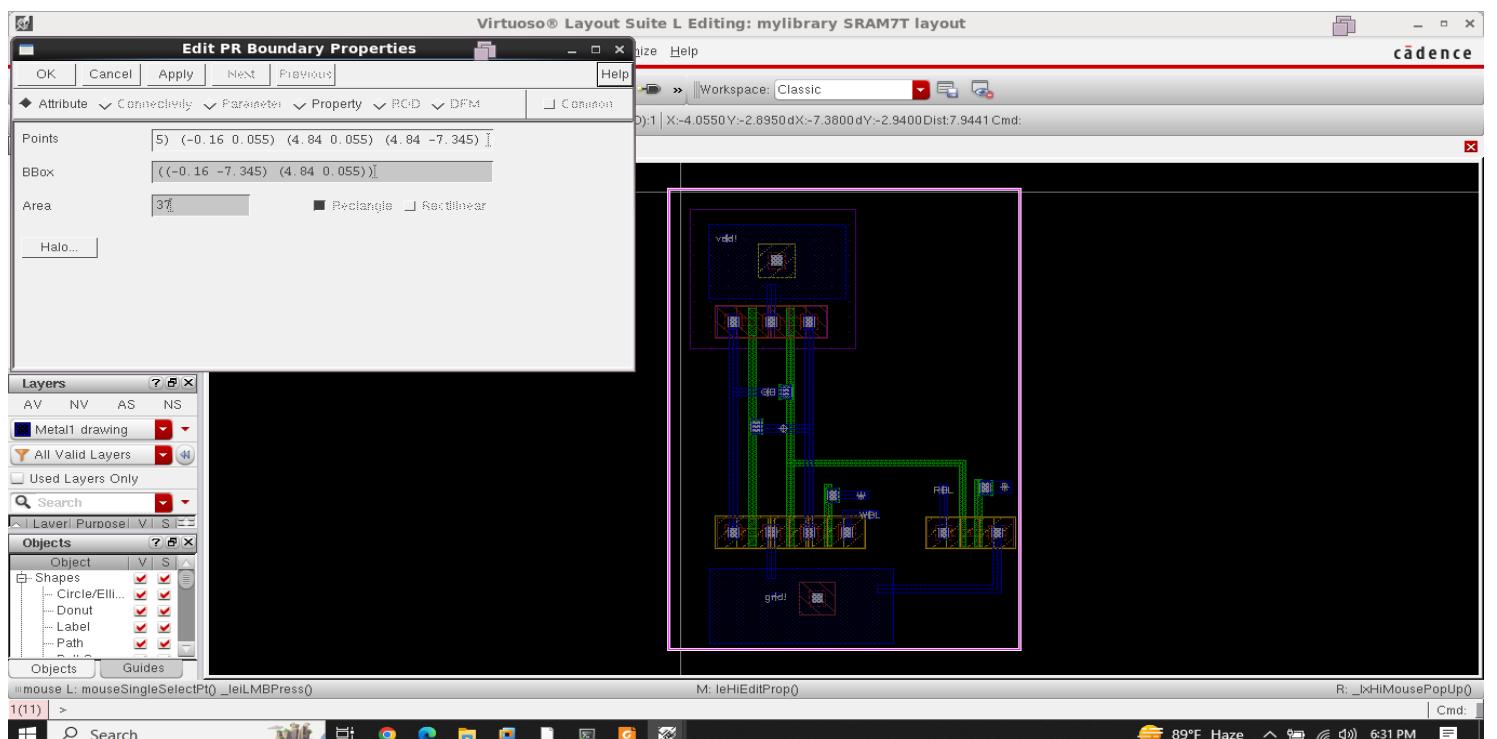
**Fig.11 Layout of 7T SRAM**



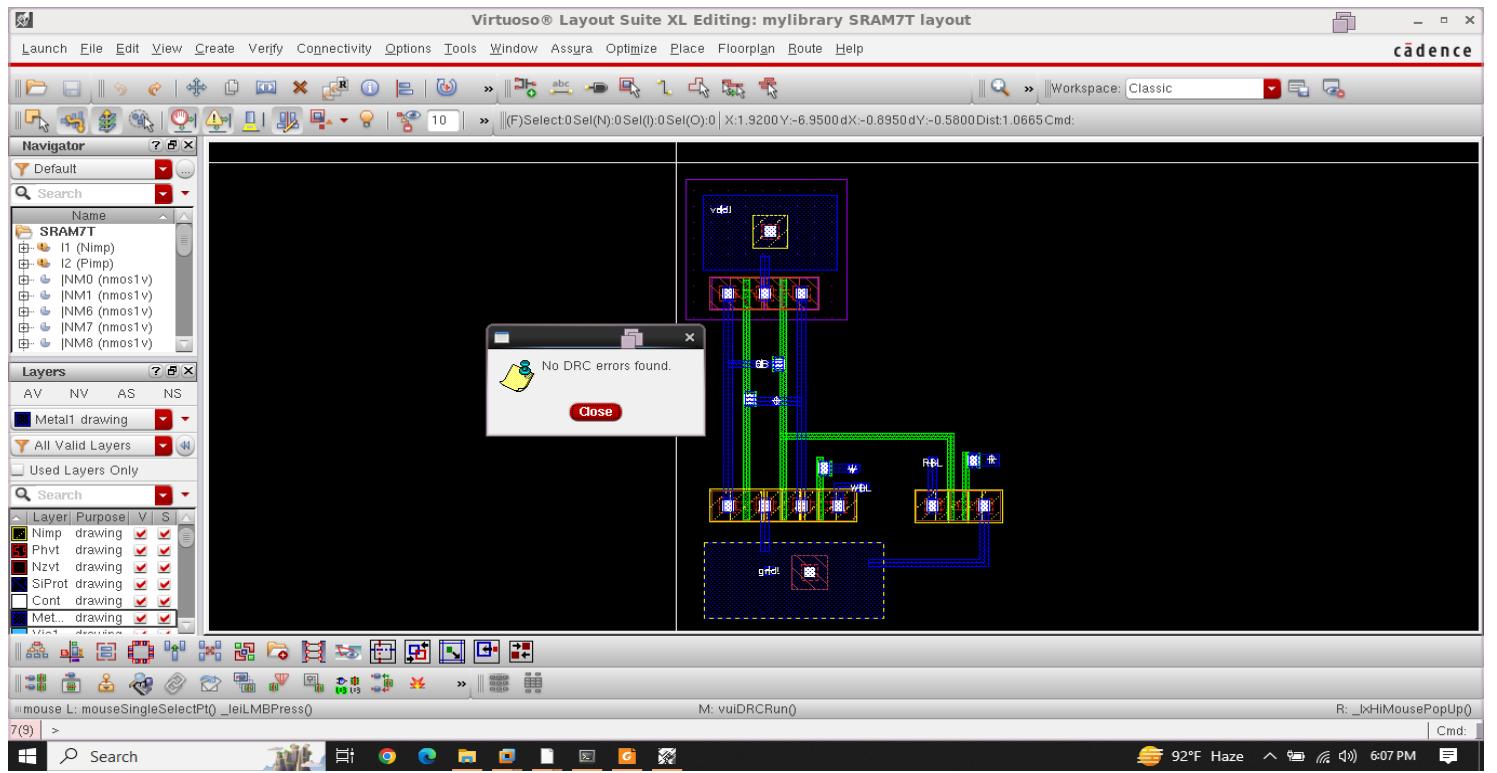
**Fig.12 Average power of 7T SRAM**



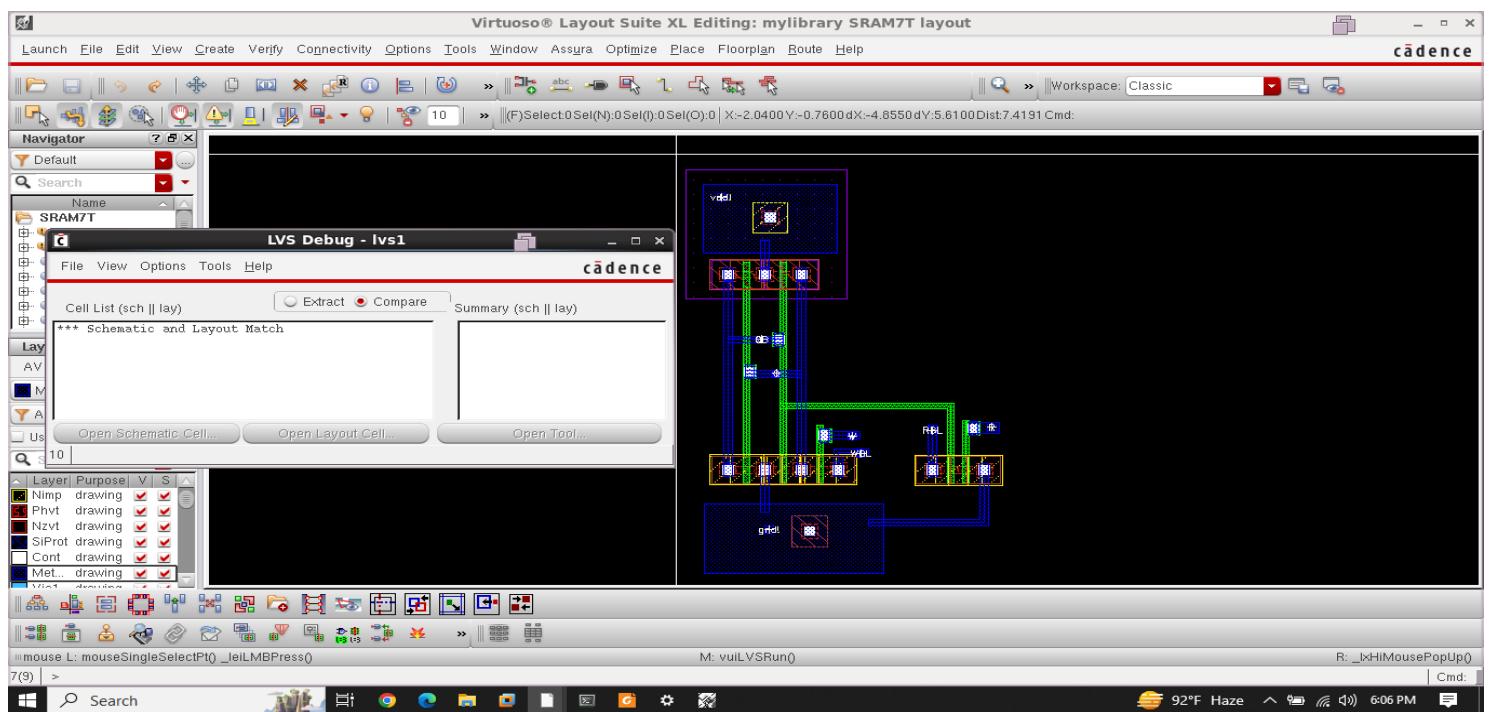
**Fig13. Delay of 7T SRAM**



**Fig14. Layout Area of 7T SRAM**

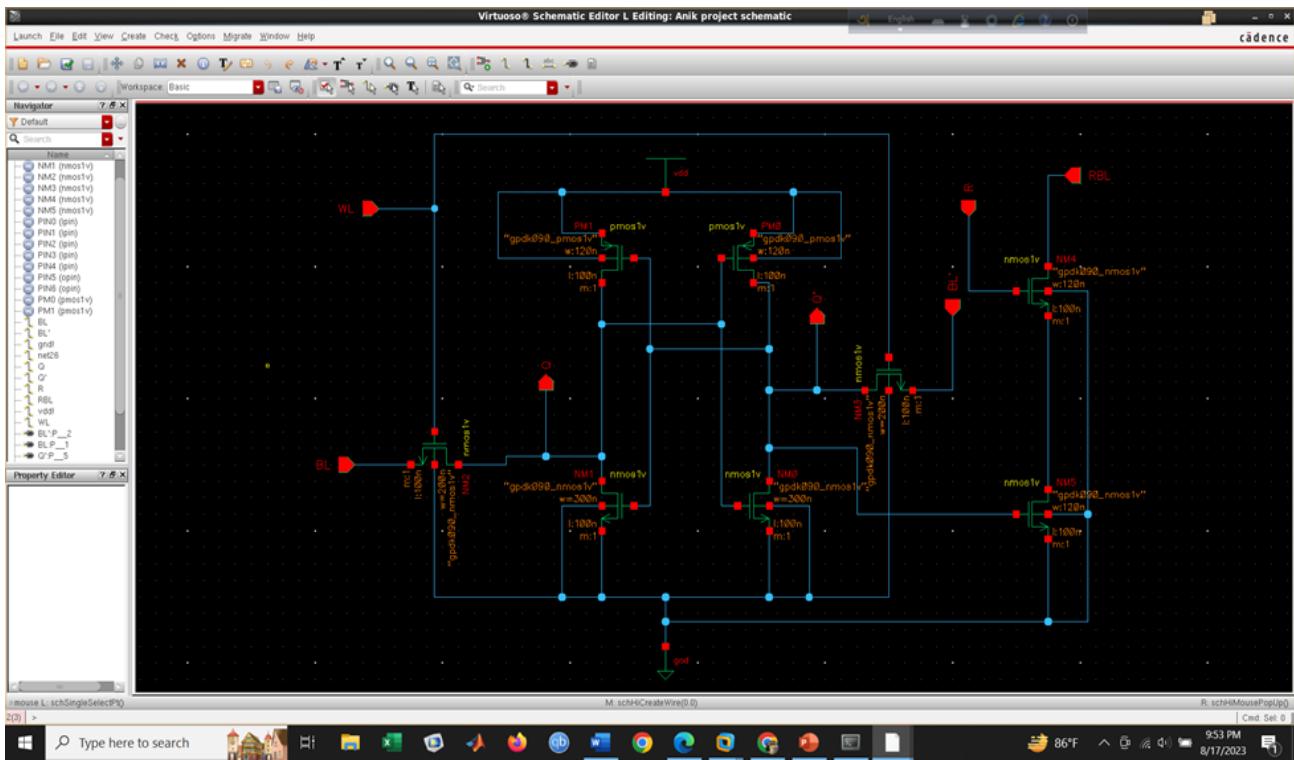


**Fig15. DRC check of 7T SRAM**



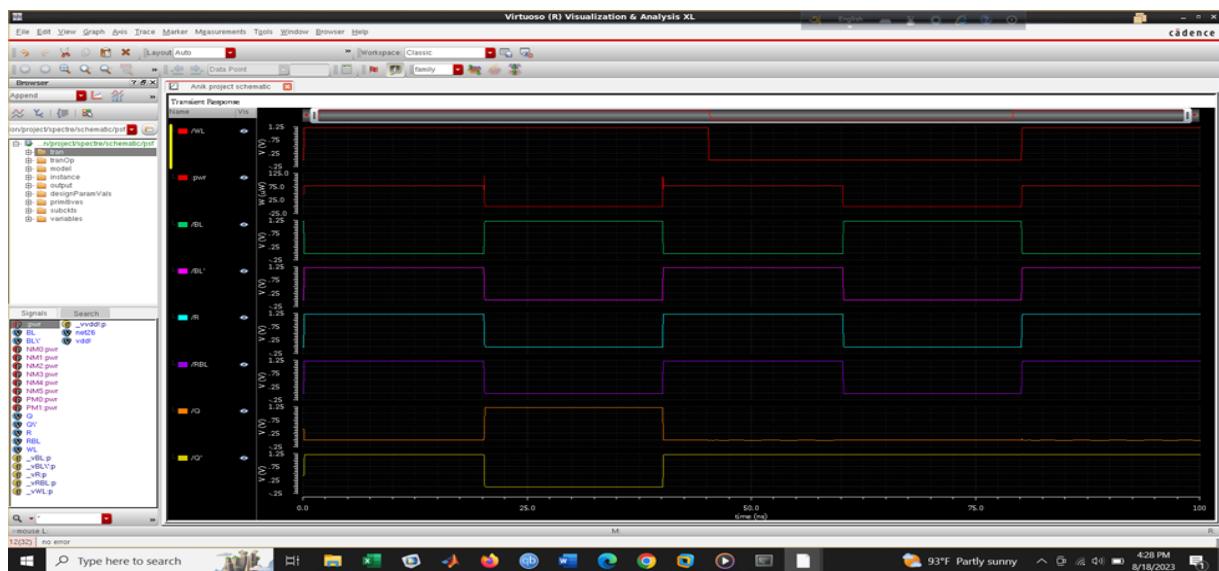
**Fig16. LVS check of 7T SRAM**

## 8T SRam:

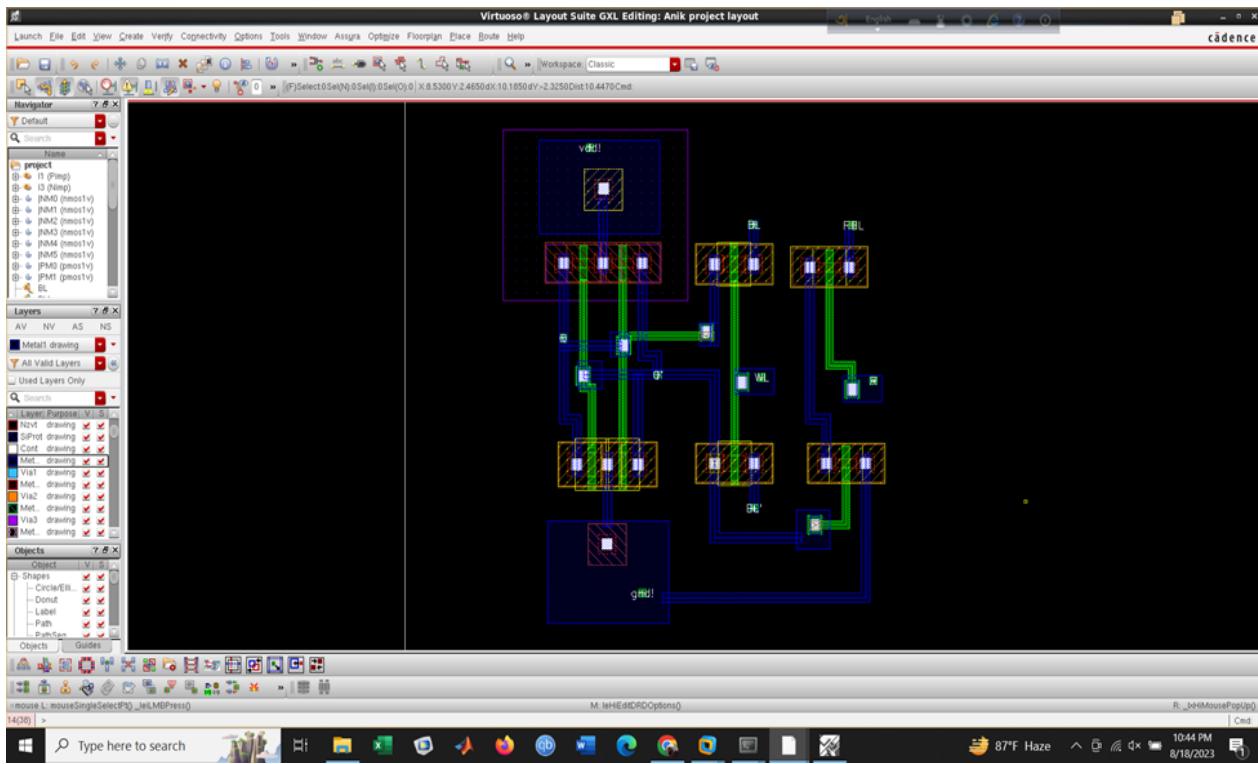


**Fig.17 8T SRAM cell schematic**

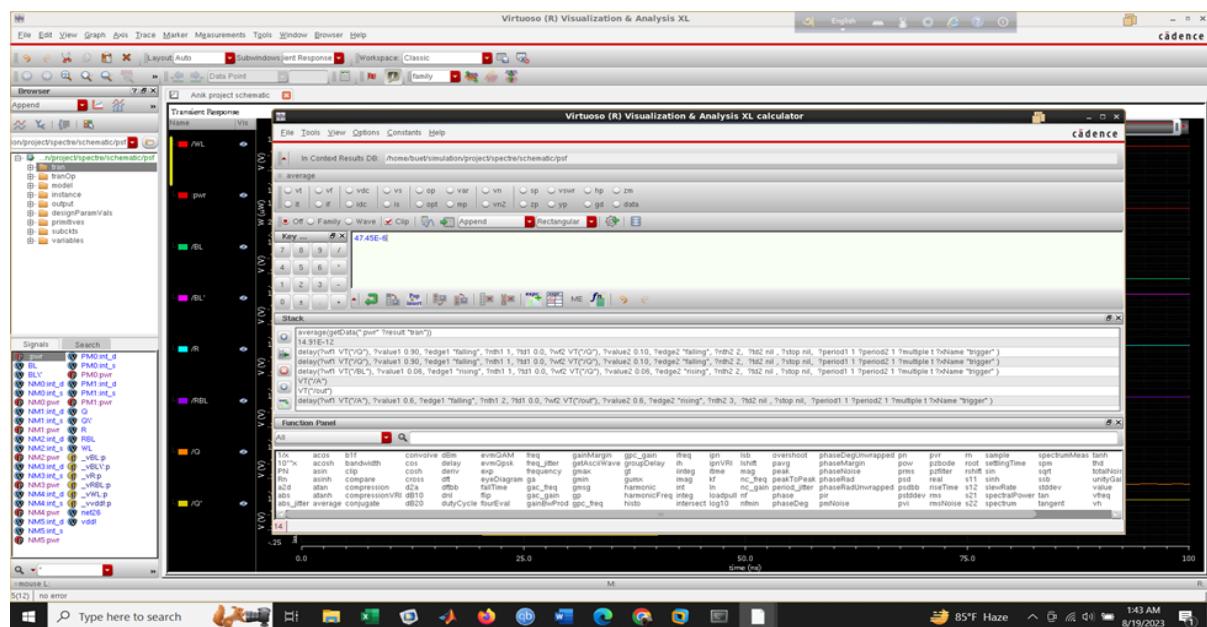
**Output:** The Fig. 18 shows the output of the 8T SRAM cell in which the data '1' is written first when the write-line (WL) is pulsed to Vdd and then '0' is written to the cell when the write-line (W) is pulsed to Vdd. The data '1' written to the cell previously can be read by precharging both the 'R' and 'RBL' to Vdd when the read-line (R) is kept high and write-line (WL) to low.



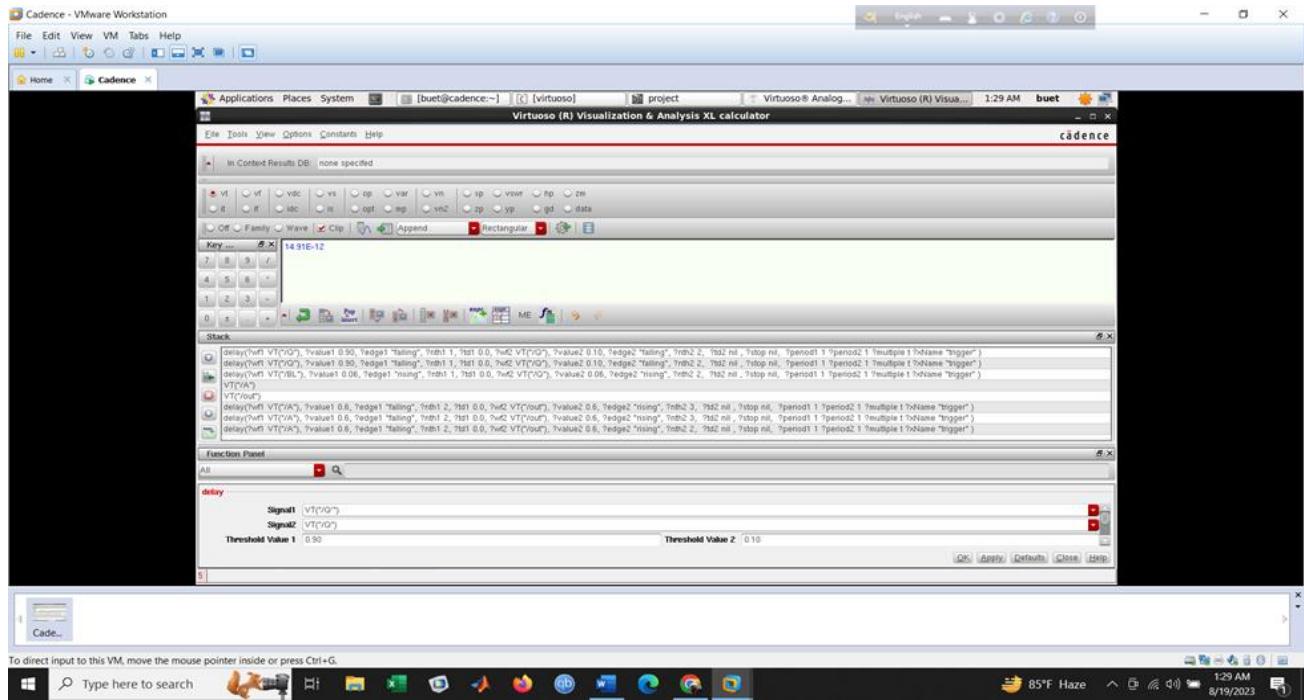
**Fig 18 Output waveform of 8T SRAM**



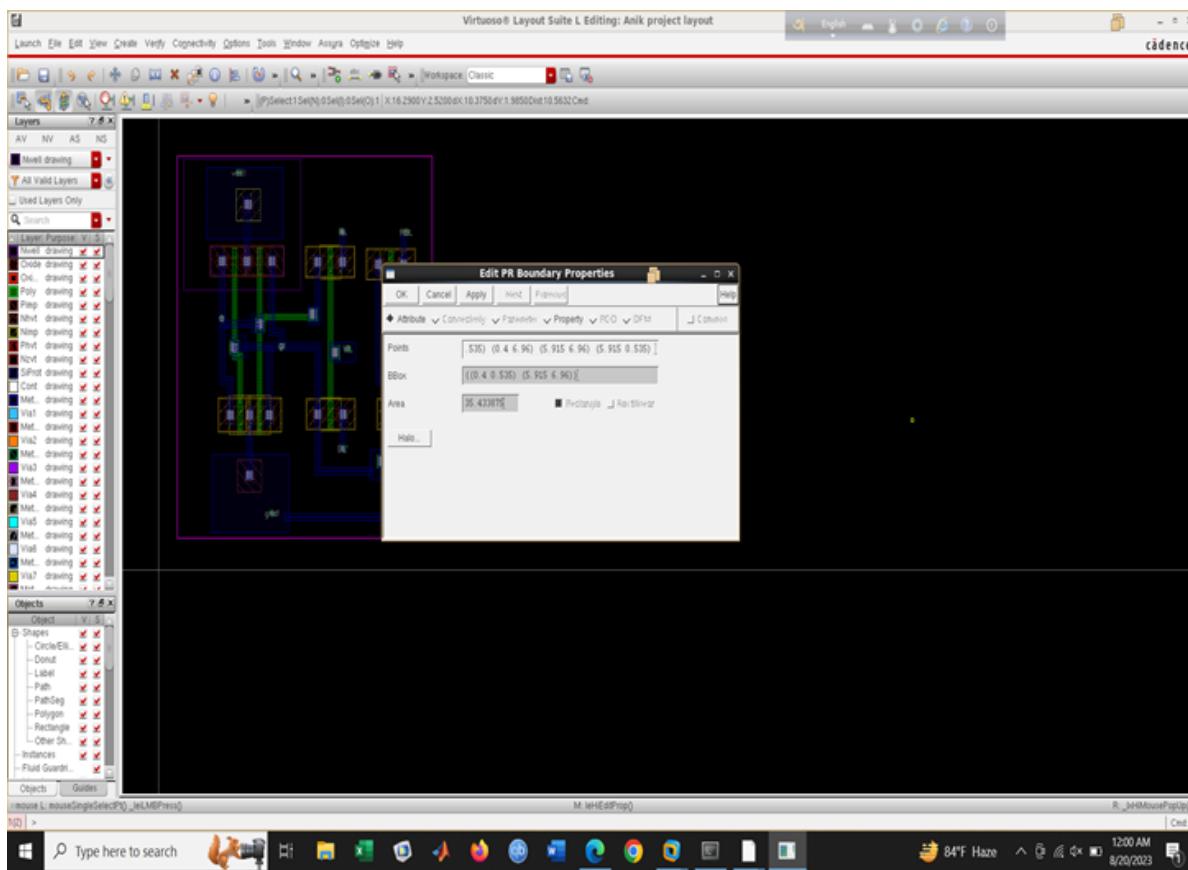
**Fig.19 Layout of 8T SRAM**



**Fig.20 Average power of 8T SRam**



**Fig21. Delay of 8T SRAM**



**Fig22. Layout Area of 8T SRAM**

## 9T SRAM:

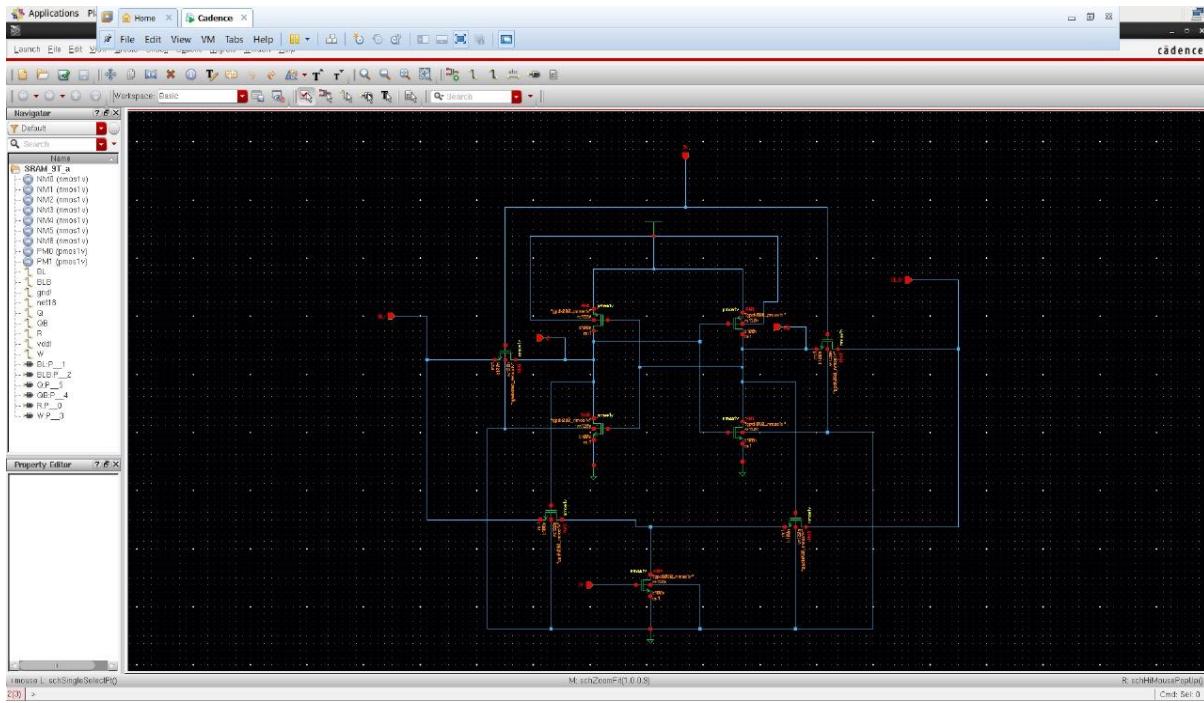
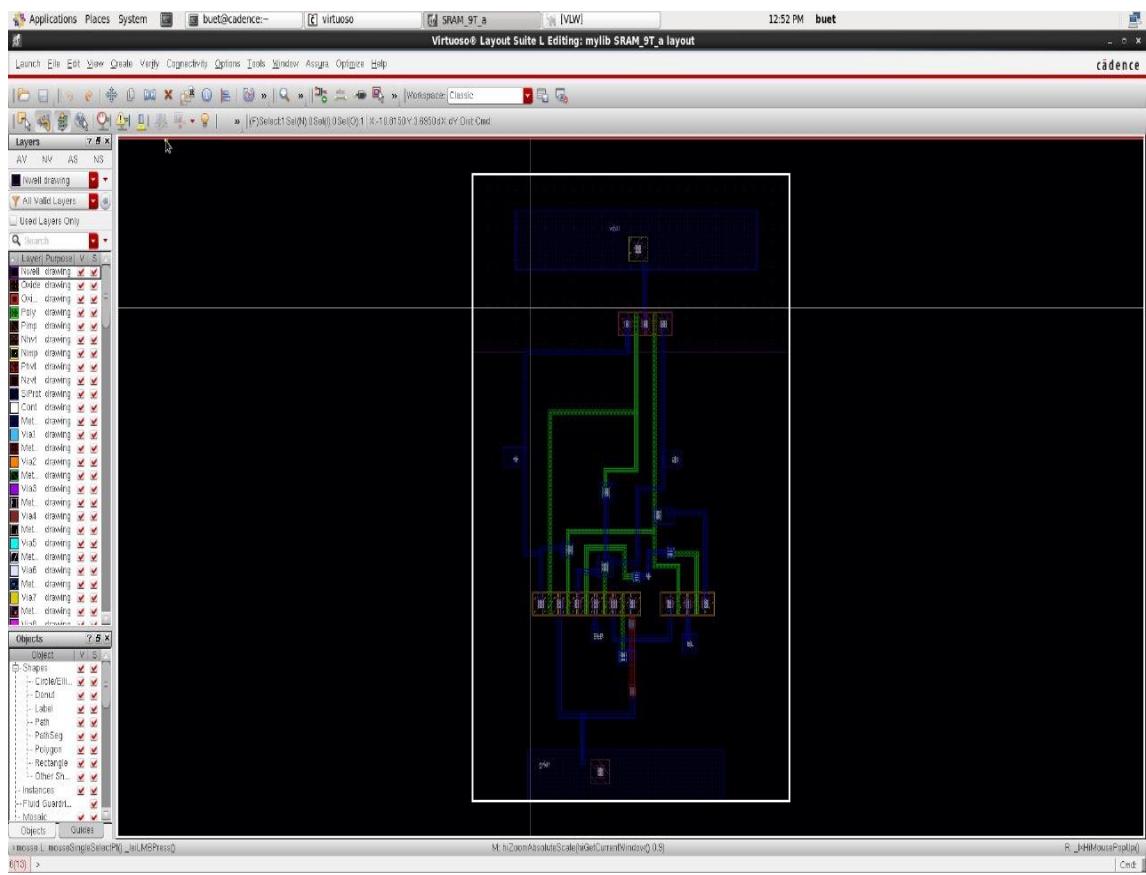


Fig.23 9T SRAM cell schematic

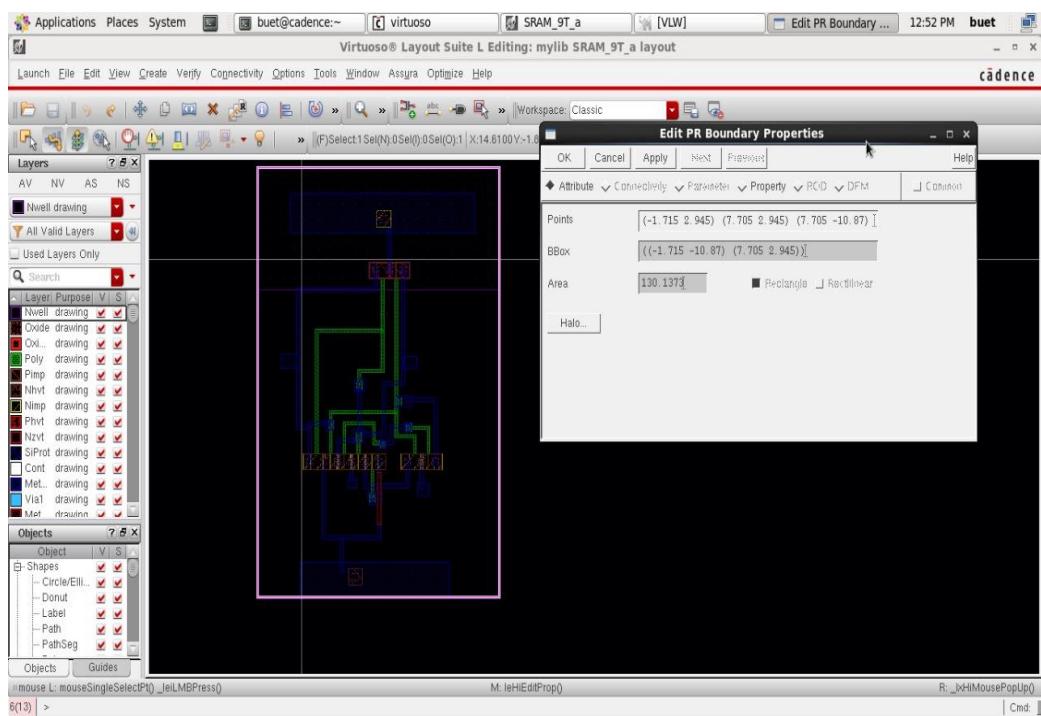
**Output:** Fig.24 shows the output of the 9T SRAM cell in which the data '1' is written first when the word-line (WL) is pulsed to Vdd and then '0' is written to the cell. The data '1' written to the cell previously can be read by precharging both the bit- lines (BL and BLB) to Vdd when the read-line (R) is kept high and write-line (W) to low.



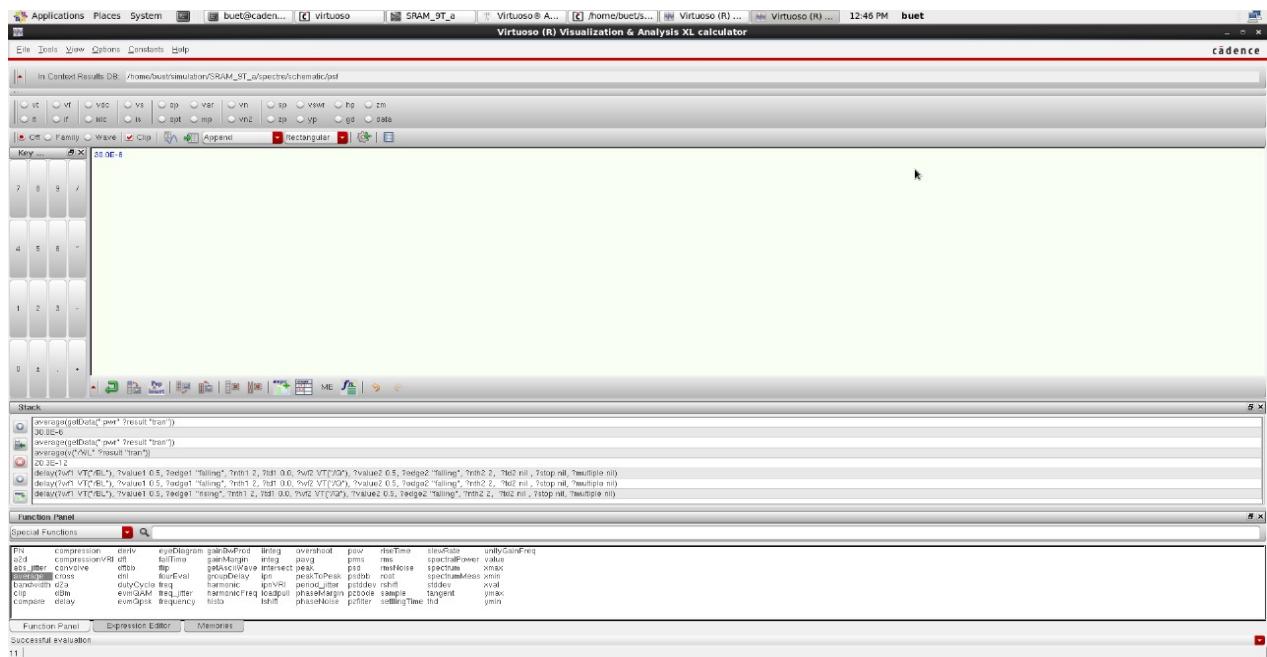
**Fig.24 Output waveform of 9T SRAM**



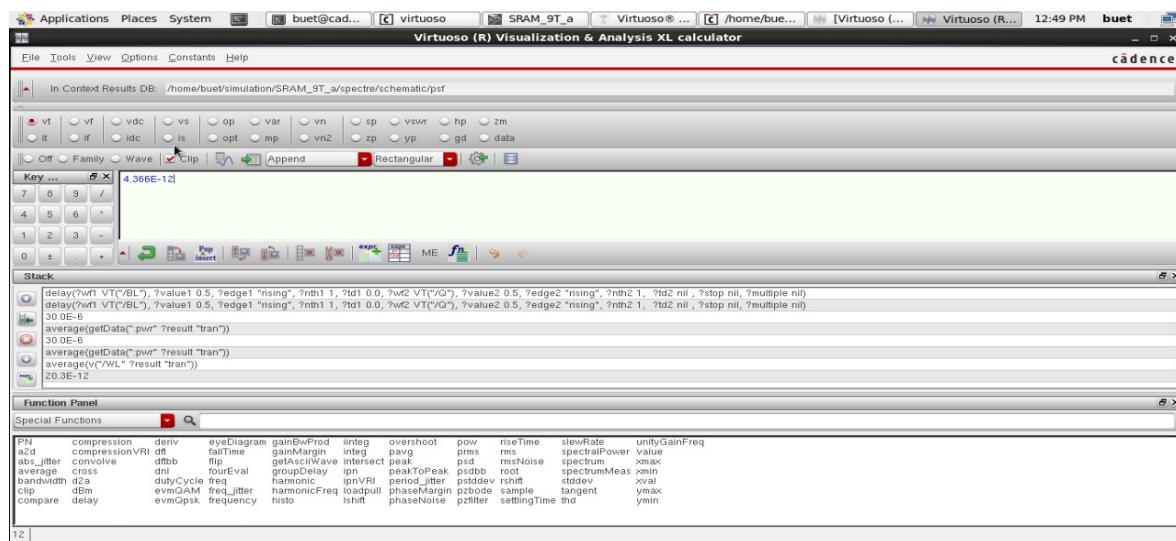
**Fig.25 Layout of 9T SRAM**



**Fig26. Layout Area of 9T SRAM**



**Fig.27 Average power of 9T SRAM**



**Fig28. Delay of 9T SRAM**