Design and Implementation of Oven Operation from FSM to system on chip using block-level netlist with io pad cells and corner cells

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***Abstract*— This investigation paves the way to an oven-functional design using a VLSI design. This paper is prepared using the background information on Verilog HDL and placement and routing. We have designed and implemented a highly efficient System-on-Chip (SoC) using Block-Level Netlist, Pad Cells, Corner Cells, and gpdk45 to achieve optimal performance, power efficiency, and robustness under various operating conditions. Views and studies were analyzed from different research to design an oven operation. The software and modern tools used in the whole process are Modelsim, Genus Synthesis Solution, and Innovus Implementation System.**

METHODOLOGY

The step-by-step procedure is carefully explained in a numbered sequence below,

1. *Design of the RTL*

HDL: Verilog, Tool: EDA Playground.

2. *Testbench*

HVL: System Verilog, Tool: EDA Playground

3. *Synthesis using Genus*

Synthesis using Genus is performed according to the SDC constraints shown in Table I.

TABLE I. SDC CONSTRAINTS

Parameters	Values
Initial Clock frequency (MHz)	205
Maximum transition (ns)	0.9
Driving cell	BUFX8
Input delay (ns)	1.86
Output delay (ns)	2.38
Max Fanout	8

4. *Gates and power information*

After synthesis, the total number of gates is 1323. The total internal power is 6.17, the total switching power is 0.07, the total leakage power is 0.38 and the total power is 6.629.

5. *Layout of the IC*

From the post-synthesized netlist and SDC files, we have designed the IC layout with proper design constraints, pad cells, and comer cells using Innovus.

6. *Removement of violation before CTS*

Generated STA reports before CTS and cleared all violations.

7. *Removement of violation after routing*

Generate STA reports alter routing and clear all violations.

8. *Physical verifications*

Performed DRC, Geometry Connectivity, ARC and cleared the violations.

All the experimental variables are identified and named below,

```
create_clock -name clk -period 4.87 [get_ports clk]
set_clock_uncertainty -setup 0.5
set_clock_uncertainty -hold 0.5 [get_clocks clk]
set_max_transition 0.9 [get_ports clk]
set_clock_transition -min -fall 0.5 [get_clocks clk]
set_clock_transition -min -rise 0.5 [get_clocks clk]
set_clock_transition -max -fall 0.5 [get_clocks clk] S
set_clock_transition -max -rise 0.5 [get_clocks clk]
DRIVING_CELL BUFX8
Set_max_fanout number 8
set_load 0.5 [all_outputs]
set_input_delay -max 1.86 [all_inputs]
set_output_delay -max 0.5 [all_outputs]
remove_assign -buffer_or_inverter BUFX16 -
design [current_design]
```

A brief description of the approaches to meet Independent variable constraints are discussed below,

Firstly, GaInP and Laser are described broadly. Then in methodology, we set the parameters and described how those are related in this paper. The equations are developed and described for analysis and simulation. Finally, we have discussed the benefits, shortcomings, results, and conclusion are provided.

RESULT ANALYSIS

The final density, total placed cells, remaining violations, and other important parameters are presented as shown in Table II.

TABLE II. OBTAINED PARAMETERS.

Parameters	Values
Final density	????
Total placed cells	172
Remaining violations	0
Warnings	0
Total Cap	2.82889e-12 F
Total instances	181

Total fillers and decap	0
Area	1323

CONCLUSION

In Innovus the VDD and the VSS don't get connected, as blockage occurs, which is a drawback. So, the wire is not correctly in its required position which causes the dangling problem.

The code was modified in PAD cells, then we performed synthesis, then we performed floor planning, power planning, pin assignment, shown placed cells, remaining violations, and other important parameters were extracted. The overall processes were well and the connections and other parameters were as we expected.

PICTORIAL REPRESENTATION

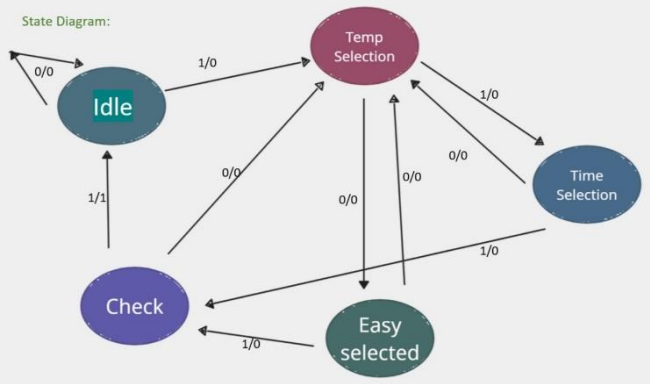


Fig. 1. Operation Diagram

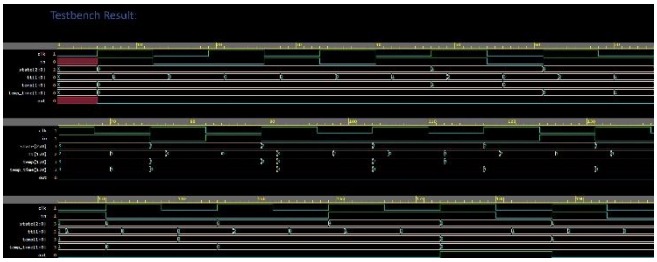
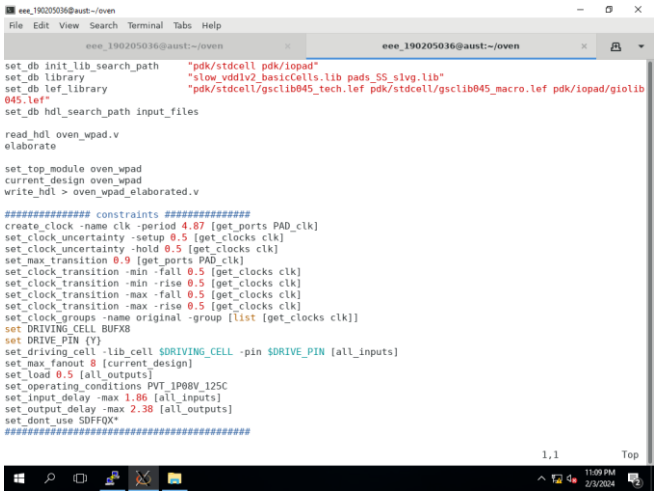
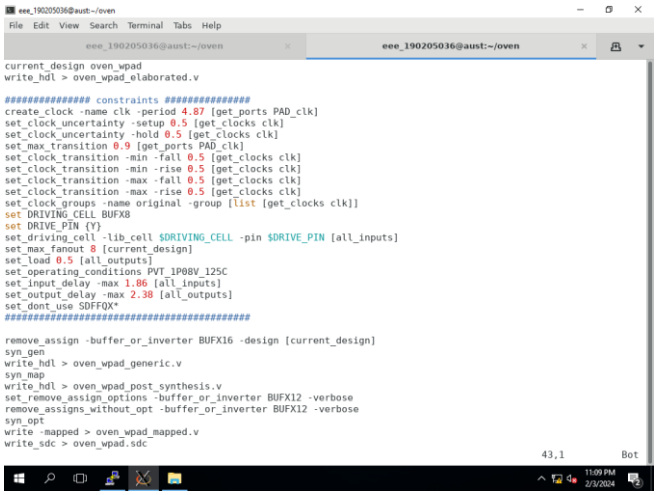


Fig. 2. Testbench



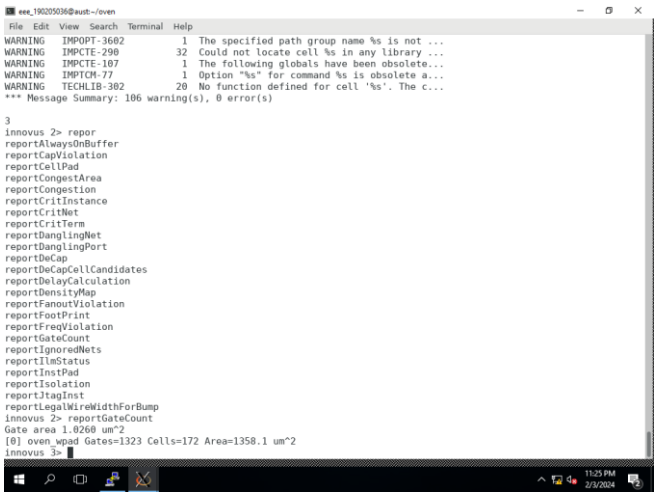
```
set_db init_lib_search_path      "pdk/stdcell pdk/iopad"
set_db library                   "slow_vdd1v2_basicCells.lib pads_SS_s1vg.lib"
set_db lef_library               "pdk/stdcell/gsclib045_tech.lef pdk/stdcell/gsclib045_macro.lef pdk/iopad/giolib
045.lef"
set_db hdl_search_path input_files

read_hdl oven_wpad.v
elaborate

set_top_module oven_wpad
current_design oven_wpad
write_hdl > oven_wpad_elaborated.v

############## constraints ##############
create_clock -name clk -period 4.87 [get_ports PAD_clk]
set_clock_uncertainty -setup 0.5 [get_clocks clk]
set_clock_uncertainty -hold 0.5 [get_clocks clk]
set_max_transition 0.9 [get_ports PAD_clk]
set_clock_transition -min -fall 0.5 [get_clocks clk]
set_clock_transition -min -rise 0.5 [get_clocks clk]
set_clock_transition -max -fall 0.5 [get_clocks clk]
set_clock_transition -max -rise 0.5 [get_clocks clk]
set_clock_groups -name original -group [list [get_clocks clk]]
set DRIVING_CELL BUFX8
set DRIVE_PIN {Y}
set_driving_cell -lib_cell $DRIVING_CELL -pin $DRIVE_PIN [all_inputs]
set_max_fanout 8 [current_design]
set_load 0.5 [all_outputs]
set_operating_conditions PVT_1P08V_125C
set_input_delay -max 1.86 [all_inputs]
set_output_delay -max 2.38 [all_outputs]
set_dont_use SDFFQX*
##########################################
```

Fig. 3. Synthesis tcl



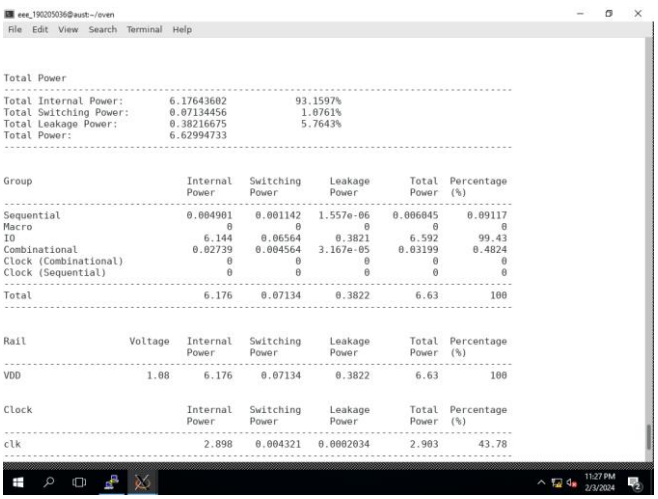
```
current_design oven_wpad
write_hdl > oven_wpad_elaborated.v

############## constraints ##############
create_clock -name clk -period 4.87 [get_ports PAD_clk]
set_clock_uncertainty -setup 0.5 [get_clocks clk]
set_clock_uncertainty -hold 0.5 [get_clocks clk]
set_max_transition 0.9 [get_ports PAD_clk]
set_clock_transition -min -fall 0.5 [get_clocks clk]
set_clock_transition -min -rise 0.5 [get_clocks clk]
set_clock_transition -max -fall 0.5 [get_clocks clk]
set_clock_transition -max -rise 0.5 [get_clocks clk]
set_clock_groups -name original -group [list [get_clocks clk]]
set DRIVING_CELL BUFX8
set DRIVE_PIN {Y}
set_driving_cell -lib_cell $DRIVING_CELL -pin $DRIVE_PIN [all_inputs]
set_max_fanout 8 [current_design]
set_load 0.5 [all_outputs]
set_operating_conditions PVT_1P08V_125C
set_input_delay -max 1.86 [all_inputs]
set_output_delay -max 2.38 [all_outputs]
set_dont_use SDFFQX*
##########################################

remove_assign -buffer_or_inverter BUFX16 -design [current_design]
syn_gen
write_hdl > oven_wpad_generic.v
syn_map
write_hdl > oven_wpad_post_synthesis.v
set_remove_assign_options -buffer_or_inverter BUFX12 -verbose
remove_assigns_without_opt -buffer_or_inverter BUFX12 -verbose
syn_opt
write -mapped > oven_wpad_mapped.v
write_sdc > oven_wpad.sdc
```

Fig. 4. Synthesis tcl



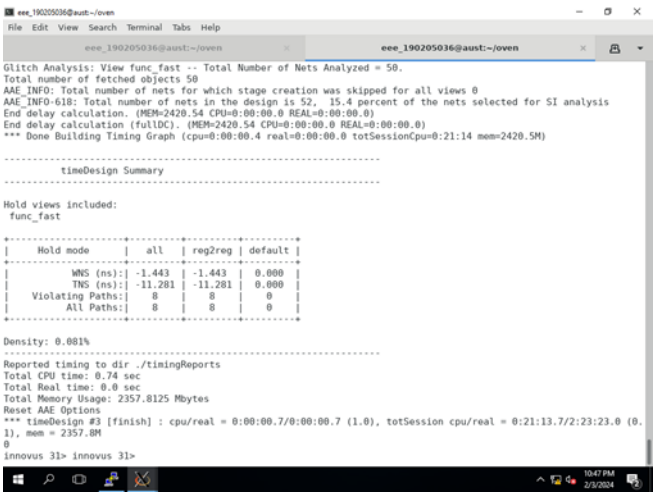
```
WARNING   IMPOPT-3602          1  The specified path group name %s is not ...
WARNING   IMPCTE-290          32  Could not locate cell %s in any library ...
WARNING   IMPCTE-107           1  The following globals have been obsolete...
WARNING   IMPTCM-77            1  Option "%s" for command %s is obsolete a...
WARNING   TECHLIB-302         20  No function defined for cell '%s'. The c...
*** Message Summary: 106 warning(s), 0 error(s)

3
innovus 2> repor
reportAlwaysOnBuffer
reportCapViolation
reportCellPad
reportCongestArea
reportCongestion
reportCritInstance
reportCritNet
reportCritTerm
reportDanglingNet
reportDanglingPort
reportDeCap
reportDeCapCellCandidates
reportDelayCalculation
reportDensityMap
reportFanoutViolation
reportFootPrint
reportFreqViolation
reportGateCount
reportIgnoredNets
reportIlmStatus
reportInstPad
reportIsolation
reportJtagInst
reportLegalWireWidthForBump
innovus 2> reportGateCount
Gate area 1.0260 um^2
[0] oven_wpad Gates=1323 Cells=172 Area=1358.1 um^2
innovus 3>
```

Fig. 5. Gate Count



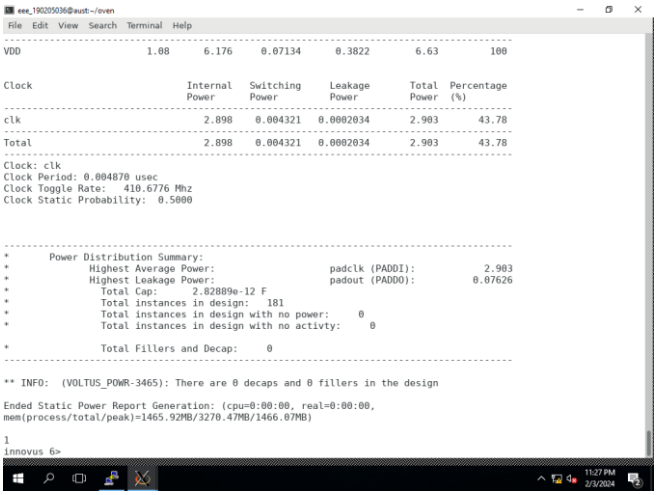
```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:        6.17643602            93.1597%
Total Switching Power:       0.07134456             1.0761%
Total Leakage Power:         0.38216675             5.7643%
Total Power:                 6.62994733
--------------------------------------------------------------------------------

Group                          Internal  Switching    Leakage      Total  Percentage
                               Power     Power        Power        Power  (%)
--------------------------------------------------------------------------------
Sequential                     0.004901  0.001142  1.557e-06    0.006045     0.09117
Macro                                 0         0          0           0           0
IO                                6.144   0.06564     0.3821       6.592       99.43
Combinational                  0.02739  0.004564  3.167e-05     0.03199      0.4824
Clock (Combinational)                 0         0          0           0           0
Clock (Sequential)                    0         0          0           0           0
--------------------------------------------------------------------------------
Total                             6.176   0.07134     0.3822        6.63         100
--------------------------------------------------------------------------------

Rail                  Voltage  Internal  Switching    Leakage      Total  Percentage
                               Power     Power        Power        Power  (%)
--------------------------------------------------------------------------------
VDD                      1.08     6.176   0.07134     0.3822        6.63         100

Clock                          Internal  Switching    Leakage      Total  Percentage
                               Power     Power        Power        Power  (%)
--------------------------------------------------------------------------------
clk                               2.898  0.004321  0.0002034      2.903       43.78
```

Fig. 6. Power calculation



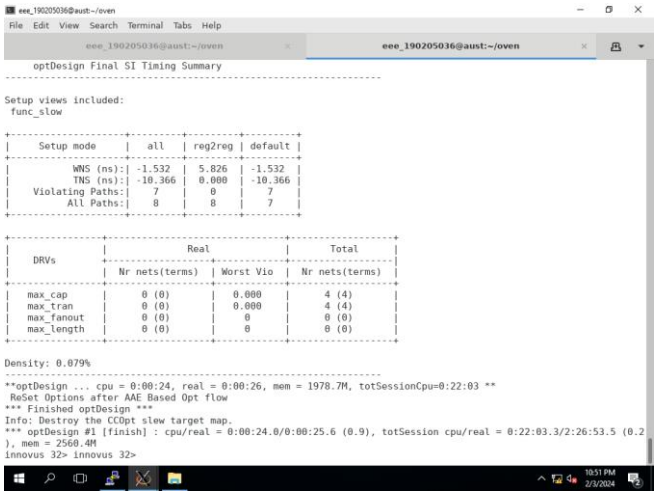
```
Glitch Analysis: View func_fast -- Total Number of Nets Analyzed = 50.
Total number of fetched objects 50
AAE_INFO: Total number of nets for which stage creation was skipped for all views 0
AAE_INFO-618: Total number of nets in the design is 52,  15.4 percent of the nets selected for SI analysis
End delay calculation. (MEM=2420.54 CPU=0:00:00.0 REAL=0:00:00.0)
End delay calculation (fullDC). (MEM=2420.54 CPU=0:00:00.0 REAL=0:00:00.0)
*** Done Building Timing Graph (cpu=0:00:00.4 real=0:00:00.0 totSessionCpu=0:21:14 mem=2420.5M)

------------------------------------------------------------------
        timeDesign Summary
------------------------------------------------------------------

Hold views included:
 func_fast

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -1.443  | -1.443  |  0.000  |
|           TNS (ns):| -11.281 | -11.281 |  0.000  |
|    Violating Paths:|    8    |    8    |    0    |
|        All Paths:  |    8    |    8    |    0    |
+--------------------+---------+---------+---------+

Density: 0.081%
------------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 0.74 sec
Total Real time: 0.0 sec
Total Memory Usage: 2357.8125 Mbytes
Reset AAE Options
*** timeDesign #3 [finish] : cpu/real = 0:00:00.7/0:00:00.7 (1.0), totSession cpu/real = 0:21:13.7/2:23:23.0 (0.
1), mem = 2357.8M
0
innovus 31> innovus 31>
```

Fig. 9. Route hold



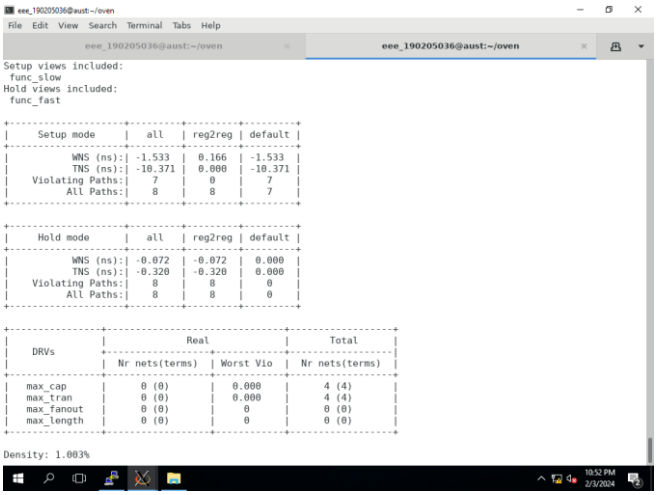
```
VDD                      1.08     6.176   0.07134     0.3822        6.63         100

Clock                          Internal  Switching    Leakage      Total  Percentage
                               Power     Power        Power        Power  (%)
--------------------------------------------------------------------------------
clk                               2.898  0.004321  0.0002034      2.903       43.78
--------------------------------------------------------------------------------
Total                             2.898  0.004321  0.0002034      2.903       43.78
--------------------------------------------------------------------------------
Clock: clk
Clock Period: 0.004870 usec
Clock Toggle Rate:   410.6776 Mhz
Clock Static Probability:  0.5000


--------------------------------------------------------------------------------
*       Power Distribution Summary:
*             Highest Average Power:                padclk (PADDI):           2.903
*             Highest Leakage Power:                padout (PADDO):         0.07626
*               Total Cap:      2.02889e-12 F
*               Total instances in design:   181
*               Total instances in design with no power:     0
*               Total instances in design with no activty:     0

*               Total Fillers and Decap:     0
--------------------------------------------------------------------------------

** INFO:  (VOLTUS_POWR-3465): There are 0 decaps and 0 fillers in the design

Ended Static Power Report Generation: (cpu=0:00:00, real=0:00:00,
mem(process/total/peak)=1465.92MB/3270.47MB/1466.07MB)

1
innovus 6>
```

Fig. 7. Power calculation



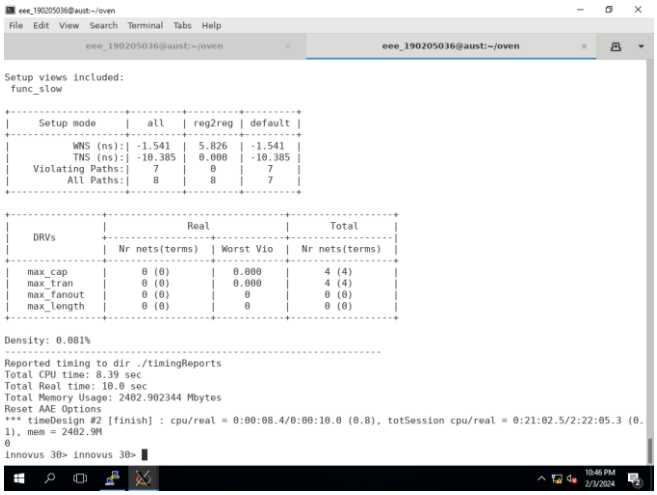
```
     optDesign Final SI Timing Summary
------------------------------------------------------------------

Setup views included:
 func_slow

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -1.532  |  5.826  | -1.532  |
|           TNS (ns):| -10.366 |  0.000  | -10.366 |
|    Violating Paths:|    8    |    0    |    7    |
|        All Paths:  |    8    |    8    |    7    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)    |    0.000   |      4 (4)       |
|   max_tran     |      0 (0)    |    0.000   |      4 (4)       |
|   max_fanout   |      0 (0)    |      0     |      0 (0)       |
|   max_length   |      0 (0)    |      0     |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 0.079%
------------------------------------------------------------------
**optDesign ... cpu = 0:00:24, real = 0:00:26, mem = 1978.7M, totSessionCpu=0:22:03 **
 ReSet Options after AAE Based Opt flow
*** Finished optDesign ***
Info: Destroy the CCOpt slew target map.
*** optDesign #1 [finish] : cpu/real = 0:00:24.0/0:00:25.6 (0.9), totSession cpu/real = 0:22:03.3/2:26:53.5 (0.2
), mem = 2560.4M
innovus 32> innovus 32>
```

Fig. 10. Route setup hold



```
Setup views included:
 func_slow
Hold views included:
 func_fast

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -1.533  |  0.166  | -1.533  |
|           TNS (ns):| -10.371 |  0.000  | -10.371 |
|    Violating Paths:|    7    |    0    |    7    |
|        All Paths:  |    8    |    8    |    7    |
+--------------------+---------+---------+---------+

+--------------------+---------+---------+---------+
|     Hold mode      |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -0.072  | -0.072  |  0.000  |
|           TNS (ns):| -0.320  | -0.320  |  0.000  |
|    Violating Paths:|    8    |    8    |    0    |
|        All Paths:  |    8    |    8    |    0    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)    |    0.000   |      4 (4)       |
|   max_tran     |      0 (0)    |    0.000   |      4 (4)       |
|   max_fanout   |      0 (0)    |      0     |      0 (0)       |
|   max_length   |      0 (0)    |      0     |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 1.003%
```

Fig. 8. Route hold opt



```
Setup views included:
 func_slow

+--------------------+---------+---------+---------+
|     Setup mode     |   all   | reg2reg | default |
+--------------------+---------+---------+---------+
|           WNS (ns):| -1.541  |  5.826  | -1.541  |
|           TNS (ns):| -10.385 |  0.000  | -10.385 |
|    Violating Paths:|    7    |    0    |    7    |
|        All Paths:  |    8    |    8    |    7    |
+--------------------+---------+---------+---------+

+----------------+-------------------------------+------------------+
|                |             Real              |       Total      |
|    DRVs        +---------------+---------------+------------------|
|                |  Nr nets(terms)  | Worst Vio  |  Nr nets(terms)  |
+----------------+---------------+---------------+------------------+
|   max_cap      |      0 (0)    |    0.000   |      4 (4)       |
|   max_tran     |      0 (0)    |    0.000   |      4 (4)       |
|   max_fanout   |      0 (0)    |      0     |      0 (0)       |
|   max_length   |      0 (0)    |      0     |      0 (0)       |
+----------------+---------------+---------------+------------------+

Density: 0.081%
------------------------------------------------------------------
Reported timing to dir ./timingReports
Total CPU time: 8.39 sec
Total Real time: 10.0 sec
Total Memory Usage: 2402.902344 Mbytes
Reset AAE Options
*** timeDesign #2 [finish] : cpu/real = 0:00:08.4/0:00:10.0 (0.8), totSession cpu/real = 0:21:02.5/2:22:05.3 (0.
1), mem = 2402.9M
0
innovus 30> innovus 30>
```

Fig. 11. Route setup

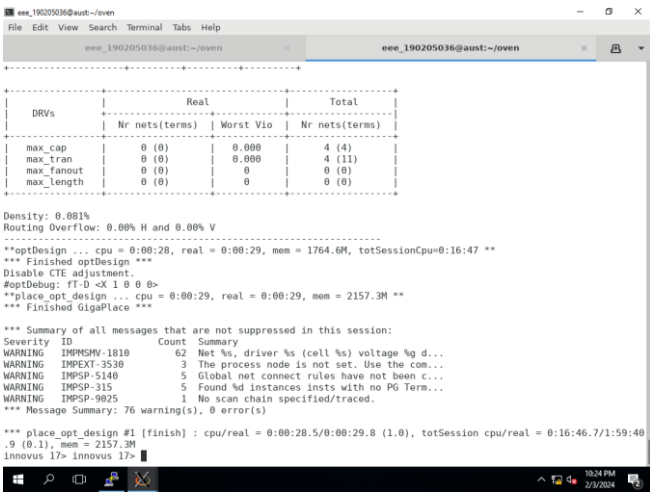


Fig. 12. STA CTS optimized

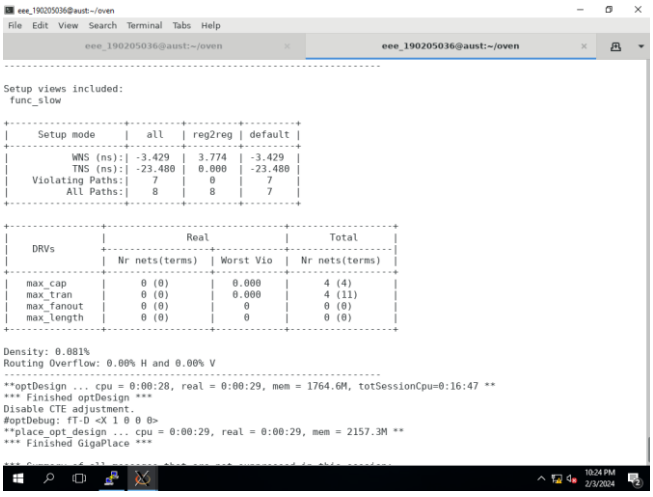


Fig. 13. STA CTS optimized

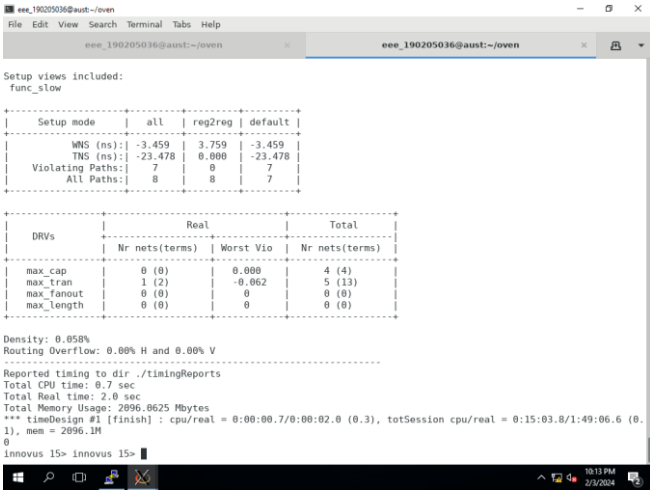


Fig. 14. STA pre CTS

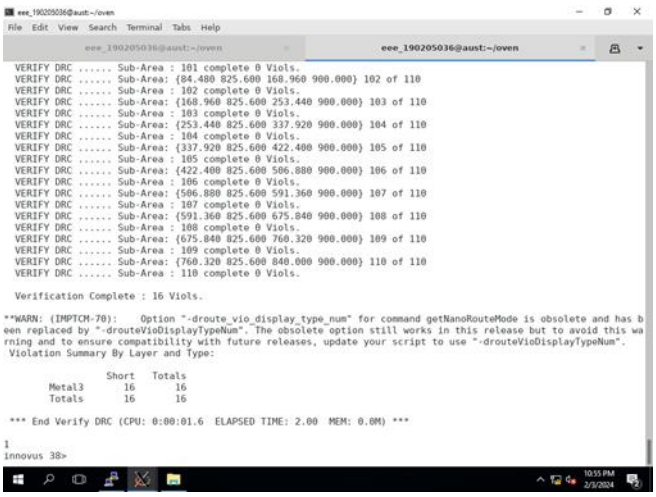


Fig. 15. DRC

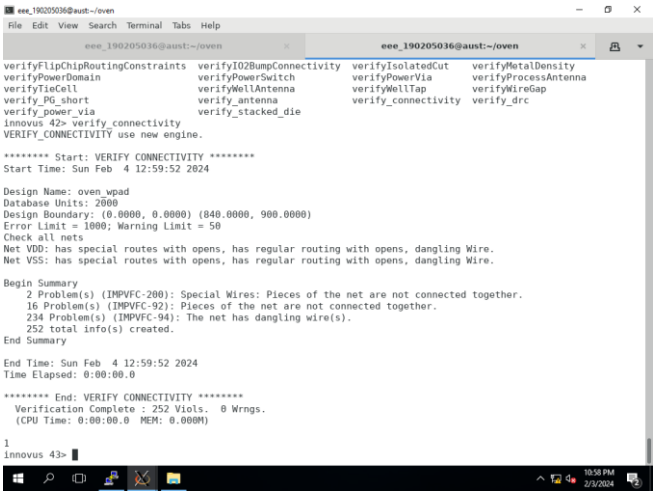


Fig. 16. Verify connectivity

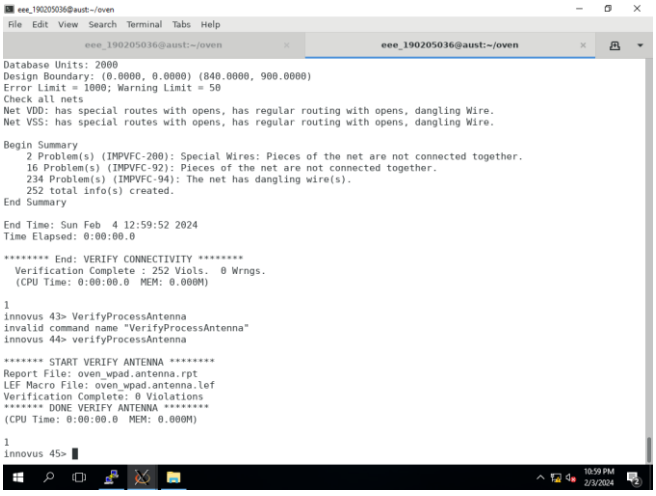


Fig. 17. Verify process antenna

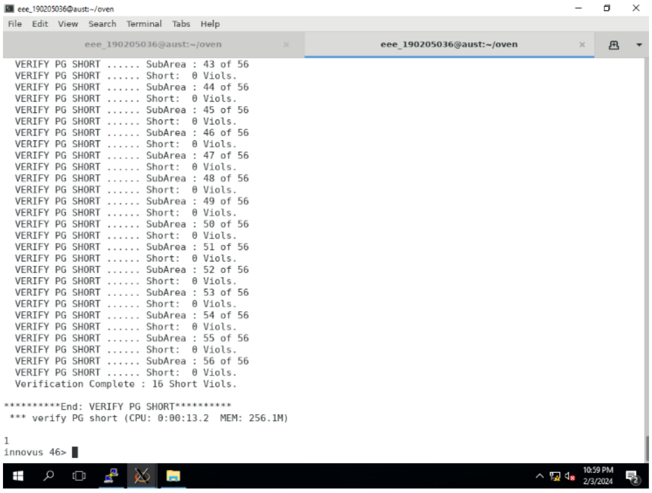


Fig. 18. Verify pg short

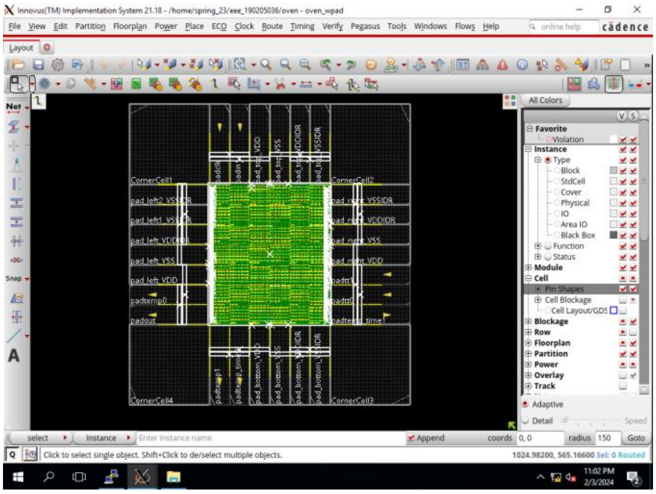


Fig. 21. Final Designed IC

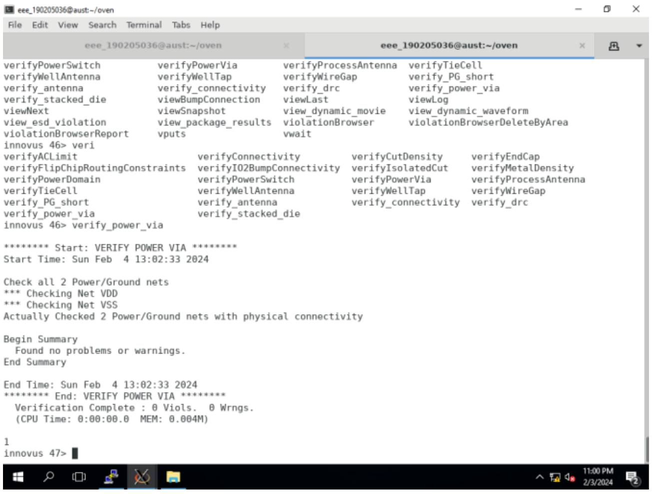


Fig. 19. Verify power via

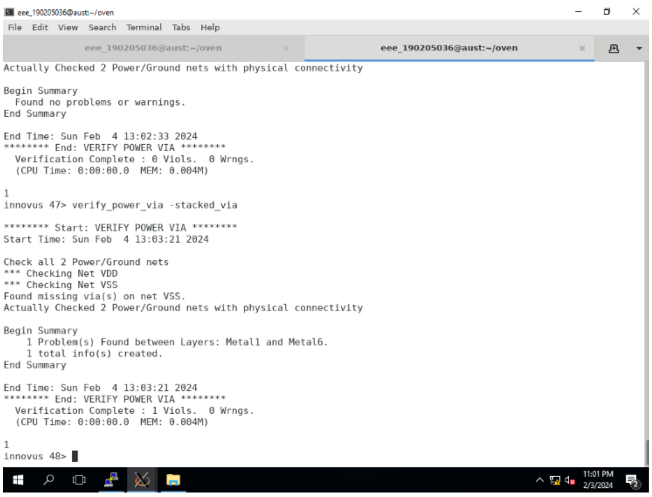


Fig. 20. Verify power stacked