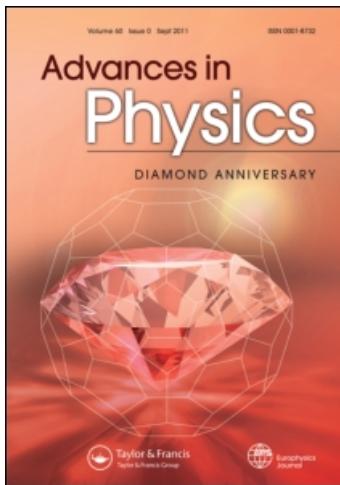


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Memory effects in complex materials and nanoscale systems

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REVIEW ARTICLE

Memory effects in complex materials and nanoscale systems

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Memory effects are ubiquitous in nature and are particularly relevant at the nanoscale where the dynamical properties of electrons and ions strongly depend on the history of the system, at least within certain time scales. We review here the memory properties of various materials and systems which appear most strikingly in their non-trivial, time-dependent resistive, capacitative and inductive characteristics. We describe these characteristics within the framework of memristors, memcapacitors and meminductors, namely memory-circuit elements with properties that depend on the history and state of the system. We examine basic issues related to such systems and critically report on both theoretical and experimental progress in understanding their functionalities. We also discuss possible applications of memory effects in various areas of science and technology ranging from digital to analog electronics, biologically inspired circuits and learning. We finally discuss future research opportunities in the field.

PACS: 84.32.-y Passive circuit components; 72.20.-i Conductivity phenomena in semiconductors and insulators; 72.25.-b Spin polarized transport; 84.30.-r Electronic circuits; 84.35.+i Neural networks

Keywords: memory; dynamical systems; nanostructures; resistance; capacitance; inductance

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1. Introduction

The concept of memory may assume various connotations in different contexts. For instance, when referring to humans, we generally mean the act of recalling past experiences. In the context of computer architectures, we mean the ability to store digital information for use in computation. In fact, if we look closer to these two examples – or any other case in which the word “memory” is used – we realize that they all share a common thread that allows us to define it as follows: “memory is the ability to store the state of a system at a given time, and access such information at a later time”. The physical process of storing such information may be realized in a variety of ways. In the brain, for instance, the information seems to be stored in the synapses (or connections) that are established among different neurons via the chemicals that are released when the synapses are excited by ionic (action) potentials [1]. In computer memories of present use, a bit of information can be either stored as a charge in a capacitor (or transistor gate) [2] or as spin polarization of certain magnetic materials [3]. Ultimately, all these examples show that a memory state is related to some *dynamical* properties of the constituents of condensed matter, namely electrons and ions. Indeed, a closer look would show that history-dependent features are related to how electrons and/or ions rearrange their state in a given material under the effect of external perturbations. It is then not surprising that understanding how memory arises in physical systems requires us to analyze the properties of materials at the nanoscale. In turn, as we will emphasize in this review, memory will emerge quite naturally in systems of nanoscale dimensions: the change of state of electrons and ions is not instantaneous, and it generally depends on the past dynamics [4]. This means that the resistive, capacitive and/or inductive properties of these systems show interesting time-dependent (memory) features when subject to time-dependent perturbations. In other words, the systems we will be discussing in this review demonstrate properties of *memristors* [5], *memcapacitors* or *meminductors* [6], namely circuit elements with resistance, capacitance and inductance, respectively, which depends on the past states through which the system has evolved.

Our scope for this review is then two-fold. On the one hand, we will briefly examine the most likely microscopic physical mechanisms that lead to storing of information in several complex materials and nanoscale systems. Our choice of not delving too much into all possible explanations for each material and/or system is because, in many instances, these mechanisms are still not completely clear or not agreed upon. Therefore, each case would require an extensive review by itself. For instance, in some correlated oxides it is not completely clear whether the dependence on the past dynamics emerges only from the formation of structural transitions or an electronic correlated state forms as well, and whether these two can, under certain conditions, be separated [7–9]. In the same manner, the spin response of certain systems shows a peculiar history dependence upon time-dependent bias [10]. However, the relationship between spin and charge memory effects has not been fully explored. Moreover, mechanisms of resistance switching in some materials [11] are not yet fully understood and are sometimes explained based on totally different physical phenomena [11,12]. We will briefly investigate these and other open questions and critically analyze the results in the existing literature. We will also point out possible future research directions to explore them in more depth. Clearly, space limitations do not allow us to cover the huge existing literature on materials/systems that exhibit memory features. We will then select specific cases that are particularly instructive and are representative of larger classes of memory systems.

Irrespective – and this is the main scope of this review – of almost all memory examples considered, we are in a position to state the general framework in which this memory fits. We

will indeed show that essentially all systems that exhibit memory fall into one or more of the above categories of memory-circuit elements. This last aspect is not just an academic exercise. Rather, the classification of physical processes in the context of memory-circuit elements sheds more light on the physical mechanisms at play and suggests new ways these systems could be combined to obtain new functionalities. For instance, the fact that the potassium and sodium channel conductances in the classic nerve membrane model of neurons [13] can, in fact, be both identified as memristive [5], has recently inspired these authors to formulate a simple electronic memristive circuit that accomplishes the tasks of learning and associative memory of neurons and their networks [14]. Likewise, the memcapacitive properties enabled by the metal–insulator transition (MIT) of certain oxides, such as VO_2 , have suggested ways to tune the frequency response of metamaterials [15].

The review is then organized as follows: in Section 2, we introduce the notion of memory-circuit elements, describe their general properties and give one simple example for each memory-circuit element. This mathematical framework will be the basis upon which all memory properties of the materials and systems, we introduce later in the review, will be discussed. We will then discuss actual systems that show memristive (Section 3), memcapacitive (Section 4), and meminductive (Section 5) behavior based on different physical properties that lead to memory: structure, charge and spin. In Section 6, we will consider memory systems with structure and/or dynamics which require a more involved analysis with a combination of the three memory device classes and/or other basic circuit elements, and in Section 7 we discuss applications ranging from information storage to biologically inspired circuits. Finally, we conclude in Section 8 and present our outlook for the field.

2. Definition and properties of memory-circuit elements

We know from the classical circuit theory that there are three fundamental circuit elements associated with four basic circuit variables, namely the charge, voltage, current and flux (or the time integral of the voltage). For linear elements, these relations take the forms

$$V = RI, \quad (1)$$

for a resistor of resistance R , given the current I and the voltage response V ;

$$q = CV_C, \quad (2)$$

for a capacitor of capacitance C that holds a charge q and sustains a voltage V_C and

$$\phi = LI, \quad (3)$$

when the flux ϕ is generated by an inductor of inductance L when a current I flows across it. In Equations (1)–(3), the constants R , C and L describe the linear response of the resistor, capacitor and inductor, respectively.

2.1. General definition

From both formal and practical points of view, relations (1)–(3) can be generalized to time-dependent and non-linear responses. In addition, all responses may depend not only on the circuit variables (such as current, charge, voltage or flux), but also on other state variables. The latter ones follow their own equations of motion and they provide memory to the system (we will give explicit examples of these variables as we proceed with this review).

Discrete memory elements. If $u(t)$ and $y(t)$ are any two complementary constitutive circuit variables (current, charge, voltage or flux) denoting the input and the output of the system, respectively,

and x is an n -dimensional vector of internal state variables, we may then postulate the existence of the following n th-order u -controlled memory element as that defined by [6]:

$$y(t) = g(x, u, t)u(t), \quad (4)$$

$$\dot{x} = f(x, u, t). \quad (5)$$

Here, g is a generalized response and f is a continuous n -dimensional vector function. Generally, the relation between current and voltage defines a *memristive system* [16], while the relation between charge and voltage specifies a *memcapacitive system* [6], and the flux–current relation gives rise to a *meminductive system* [6]. Two other pairs (charge–current and voltage–flux) are linked through equations of electrodynamics and therefore do not define any elements. Devices defined by the relation of charge and flux (which is the time integral of the voltage) are not considered as a separate group since such devices can be redefined on the current–voltage basis [16]. *Memristors* (short for memory resistors) [5], *memcapacitors* (for memory capacitors) [6] and *meminductors* (memory inductors) [6] are special *ideal* instances of memristive, memcapacitive and meminductive systems the definitions of which are given in what follows.

Continuum memory elements. Furthermore, there are systems in which the internal state is described by a continuous function or functions instead of discrete variables. An example of such a situation is spintronic memristive systems [17] with spin polarization density (defining the internal state of the device) which is a function of coordinates. Therefore, in order to cover such cases, the definition of memory elements given by Equations (4) and (5) has to be generalized appropriately. This can be done in the following way:

$$y(t) = g(X(s, t), u, t)u(t), \quad (6)$$

$$\dot{X}(s, t) = f(X(s, t), u, t), \quad (7)$$

where, generally, $X(s, t)$ is a vector function (such as a spin-polarization density), s symbolically represents a set of continuum variables (such as coordinates) and $g(\dots)$ and $f(\dots)$ are now functionals. We will call these physical systems described by Equations (6) and (7) as *continuous* u -controlled memory elements.

Stochastic memory elements. Finally, the state variables – whether defining a continuum or a discrete set of states – may follow a *stochastic differential equation* rather than a deterministic one. In this case, assuming the input $u(t)$ to be deterministic, we may formally define u -controlled *stochastic* memory elements as

$$\{y(t)\}_{\xi} = \{g(x, u, t)\}_{\xi} u(t), \quad (8)$$

$$\dot{x} = f(x, u, t) + H(x, u, t)\xi(t), \quad (9)$$

for discrete elements, and similarly for continuum elements. Here, $H(x, u, t)$ is some $n \times n$ matrix function of the state variables allowing for coupling of the noise components, and $\xi(t)$ is an n -dimensional vector of noise terms defined by

$$\langle \xi_i(t) \rangle = 0, \quad \langle \xi_i(t)\xi_j(t') \rangle = k_{ij}(t, t'), \quad i, j = 1, \dots, n, \quad (10)$$

where $\langle \dots \rangle$ indicates ensemble average and $k_{ij}(t, t')$ is the autocorrelation matrix. The symbol $\{\dots\}_{\xi}$ has then the meaning of a realization of the stochastic process $\xi(t)$. For white noise on each independent state variable, we can choose $k_{ij}(t, t') = \Gamma_i \delta_{ij} \delta(t - t')$ with Γ_i some constants. For colored noise, one would have different autocorrelation functions. For instance, for uncoupled

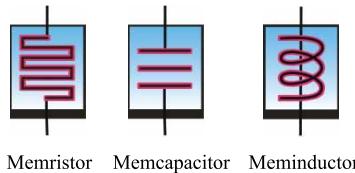


Figure 1. Symbols of the three different devices defined in the text: memristor, memcapacitor and meminductor. The same symbols are used to represent the more general classes of memristive, memcapacitive and meminductive systems. These devices are generally asymmetric as indicated by the black thick line. The following convention could then be used whenever possible or appropriate: when a positive voltage is applied to the second (upper) terminal with respect to the terminal denoted by the black thick line, the memory device goes into a state of high resistance, capacitance or inductance, respectively. Correspondingly, the device goes into a state of low resistance, capacitance or inductance when a negative voltage (with respect to the lower terminal) is applied.

colored noises on each state variable, we could choose the noise to follow the stochastic differential equations ($i = 1, \dots, n$)

$$\dot{\xi}_i(t) = -\frac{1}{\tau_i} \xi_i(t) + l_i(t), \quad (11)$$

with $l_i(t)$ being the white noise defined by $\langle l_i(t) \rangle = 0$ and $\langle l_i(t) \rangle = \Gamma_i \delta(t - t')$, and $1/\tau_i$ the frequencies (colors) of the noise. To the best of our knowledge, stochastic memory elements have not been thoroughly studied in literature even though we anticipate many interesting and important effects due to noise in these systems.

Figure 1 shows the circuit symbols of memristor, memcapacitor and meminductor. The same symbols are used for memristive, memcapacitive and meminductive systems. In the following sections, we will discuss in detail these three memory elements and their properties. Since the majority of examples we provide in this review are in regard with *discrete* memory elements, we will drop the word “discrete” in those cases and explicitly specify when the elements are continuum or stochastic.

2.2. Hysteresis loops

Here, we point out that a distinctive signature of memory devices is a hysteresis loop. Such loops are very frequently reported in experimental papers when the response function $g(t)$ or the function $y(t)$ (or both) are plotted versus $u(t)$. The shape of a loop is determined by both the device properties and the input $u(t)$ applied. In particular, it depends on both the amplitude and the frequency of the input. Therefore, the input $u(t)$ should be fully specified when measurement results are reported, which is regrettably not always the case in the existing literature.

Let us now consider the situation in which hysteresis loops are well defined in the sense that $y(t)$ and $g(t)$ are periodic with a period T of the applied ac voltage. This may not always be the case, e.g. whether Equation (5) involves a stochastic component or when the switching gradually occurs only in one direction. There are some common properties of these hysteresis loops. First of all, we note that as it follows from Equation (4) for well-defined generalized response functions g (by “well-defined” we mean $g \neq 0$ and $g \neq \pm\infty$), the function $y(t)$ hysteresis loop passes through the origin (y is zero whenever u is zero and vice versa). This is called a “pinched” hysteresis loop. A pinched loop may be “not self-crossing” or “self-crossing” (see Figure 2).

The symmetry of Equations (4) and (5) does not always define the type of crossing. However, as it follows from examples considered in this review, “not self-crossing” loops are very often

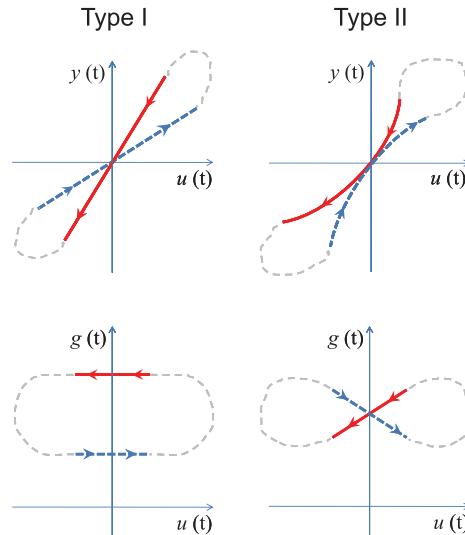


Figure 2. The pinched hysteresis loop of memory elements when subject to a periodic stimulus can be “self-crossing” (type I crossing behavior) or not (type II crossing behavior). The latter property often (but not always) arises when the state dynamic function f and the response function g are even functions of the input variable u .

observed when $g(x, u)$ and $f(x, u)$ are even functions of u . We emphasize that this is not a necessary condition for “not self-crossing”. For instance, in the case of unipolar resistance switching (Section 3.2.2), $g(x, u)$ and $f(x, u)$ are even functions of u , but $I-V$ hysteresis loops show “self-crossing”. In the opposite case, when $f(x, u)$ is an odd function of u , “self-crossing” behavior of $y-u$ curves is more common.

The feature of “not self-crossing” loops is observed, e.g. in the case of thermistors and elastic memcapacitive systems (see, e.g. Sections 3.1 and 4.1.2). We define this hysteresis of *type II crossing behavior* because it normally results in a double loop in the response g as a function of the input (see Figure 2, right panel). The other type of hysteresis – shown in the left panel of Figure 2 – involves typically a single loop in the response g as a function of the input. Therefore, we call such a hysteresis *type I crossing behavior*.

We also note that there are situations when the response function g becomes zero or infinite when $y = 0$ or $u = 0$ as in the example of superlattice memcapacitive systems considered in Section 4.2.1. In this situation, $y-u$ curves do not pass through the origin. Moreover, in some systems, additional crossings are possible at $u \neq 0$ as in the case of ionic channels. We will discuss this example explicitly in Section 3.6.

2.3. Some remarks on time scales

The ability to categorize experimental systems as memristive, memcapacitive and meminductive in terms of general equations (4) and (5) (or their continuum and/or stochastic counterparts) provides the opportunity to understand some of their general properties following directly from the above-mentioned equations. For clarity, let us consider discrete memory elements. The steady state values of x can be found as a solution of the algebraic equation

$$f(x, u_0, t) = 0, \quad (12)$$

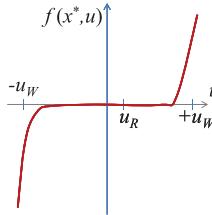


Figure 3. Schematics of the function $f(x^*, u)$ suitable for non-volatile information storage. Here, x^* is an intermediate value of x , u_W and u_R stand for values of u used to write and read the information, respectively. For non-volatile memory applications, it is desirable to have zero or very small $f(x, u_R)$ and finite $f(x^*, \pm u_W)$.

which follows from Equation (5) assuming a constant value of the external control parameter $u = u_0$ and the existence of a steady state. In particular, for non-volatile information storage, Equation (12) should provide at least two possible solutions at $u_0 = 0$.

Moreover, the magnitude of $f(x, u, t)$ in Equation (5) can be used to estimate the rates of change of the internal state variables or, in other words, the relevant time scales. This information is especially important for non-volatile memory applications when fast writing and reading time scales, as well as long-term data retention capability are required. Figure 3 shows a sketch of a one-dimensional $f(x, u)$ desirable for non-volatile information storage (for the sake of simplicity, we assume that f does not depend explicitly on time t) evaluated at a certain value of $x = x^*$ selected between the minimum x_{\min} and maximum x_{\max} values of x (assuming that such values do exist).

Generally, the function f can be asymmetric with respect to u , and therefore, it can be reasonable to define ON and OFF write times $t_{W,\pm}$ separately. In particular, the writing time $t_{W,\pm}$ is of the order

$$t_{W,\pm} \sim \frac{x_{\max} - x_{\min}}{f(x^*, \pm u_W)} \quad (13)$$

while the change of x during the reading is of the order

$$\delta x \sim f(x^*, u_R) t_R, \quad (14)$$

where t_R is the read time. In addition, Equation (14) can be used to determine the amount of read cycles before the device state is altered by consecutive read operation. Roughly, the allowed number of read operations is of the order

$$N_R \sim \frac{x_{\max} - x_{\min}}{\delta x}. \quad (15)$$

We also note that sequential readings of information are not the only source leading to changes in the internal state of the device. In some cases, the state degradation can occur naturally, e.g. because of diffusion or certain stochastic processes. Both these effects, in fact, can be taken into account explicitly using the formalism of stochastic memory-circuit elements given in Section 2.1.

After these general considerations, we are now ready to define the three different classes of memory elements.

2.4. Memristors and memristive systems

2.4.1. Definitions

The relation between the charge and the flux has been recognized long ago as a missing connection between the four different circuit variables [5]. For the sake of this completeness let us then

postulate a relation of the type

$$\phi(t) = M(F(t))q(t), \quad (16)$$

between the charge that flows in the system and the flux ϕ , which does not need to have a magnetic interpretation. The proportionality function $M(F(t))$ is some response functional, with $F(t)$ being a time-dependent function to be specified later. Recalling that the flux is related to the voltage via

$$\phi(t) = \int_{-\infty}^t dt' V(t'), \quad (17)$$

we can re-write Equation (16) as

$$\int_{-\infty}^t dt' V(t') = M(F(t))q(t). \quad (18)$$

By differentiating the above relation with respect to time and recalling that the current $I(t) = dq/dt$, we obtain

$$V(t) = \frac{dM}{dt'} \Big|_{t'=t} q(t) + M(F(t))I(t). \quad (19)$$

Let us now define the quantity

$$R_M(t) \equiv I^{-1}(t) \frac{dM}{dt'} \Big|_{t'=t} q(t) + M(F(t)), \quad (20)$$

which has the dimensions of a resistance, so that Equation (19) can be compactly written as

$$V(t) = R_M(t)I(t). \quad (21)$$

If the response M depends only on the charge ($F(t) = q(t)$), namely $M = M(q(t))$, then the simple chain rule

$$\frac{dM}{dt} = \frac{\delta M}{\delta q} \times \frac{dq}{dt}, \quad (22)$$

with $\delta M/\delta q$ being the functional derivative of M with respect to the charge function $q(t)$, implies that Equation (20) simplifies as

$$R_M(q(t)) = \frac{\delta M}{\delta q} q(t) + M(q(t)), \quad (23)$$

and Equation (21) as

$$V(t) = R_M(q(t))I(t) = R_M \left[\int_{-\infty}^t dt' I(t') \right] I(t), \quad (24)$$

where the last step is a simple substitution of $q(t)$ with the time integral of the current. The lower limit of integration can also be chosen zero, provided $\int_{-\infty}^0 I(t') dt' = 0$. Equation (24) defines the relation between the current and voltage but unlike its ohmic counterpart, Equation (1), it is *non-linear* and the function R_M depends not just on the state of the system at a given time t , but also *on the entire history of states through which the system has evolved*. This is in fact explicit in the functional derivative of the response M with respect to the charge dynamics $q(t)$.

Relation (24) is the definition of an *ideal current-controlled* memristor [16]. It has become standard in circuit theory to represent it as in Figure 1. It is clear that if the response function M does not depend on time, then we find from Equation (20) that also R_M is independent of time, and Equation (24) reduces to the ohmic form (1).

A memristor with M depending only on the flux, i.e. $M = M(\phi(t))$, is instead called an *ideal voltage-controlled* memristor. It is described by

$$V(t) = R_M \left[\int_{-\infty}^t dt' V(t') \right] I(t), \quad (25)$$

with the possibility of the lower limit of integration to be zero, provided $\int_{-\infty}^0 V(t') dt' = 0$.

However, as we will discuss in the following sections, it may occur – and this is probably the norm rather than the exception in real systems – that the response function M depends not just on the charge that flows across the system, but also on one or more state variables that determine the state of the system at any given time. This could be, e.g. the position of oxygen vacancies in TiO_2 thin films [11], which determines the resistance of the film, or the temperature of a thermistor [16], or the degree of spin polarization in certain structures [10,17]. Let us then group in the symbol x the set of n possible state variables (related to a particular device) of which we know their time evolution via

$$\frac{dx}{dt} = f(x, I, t), \quad (26)$$

where f is a continuous n -dimensional vector function. The relation between voltage and current can then be written as

$$V(t) = R_M(x, I, t)I(t), \quad (27)$$

and needs to be solved together with Equation (26) for the state variables dynamics. These systems (with f and/or R_M depending on I) have been called current-controlled *memristive systems* [16]. The voltage-controlled ones are those that satisfy the relations

$$I(t) = G(x, V, t)V(t) \quad (28)$$

$$\dot{x} = f(x, V, t), \quad (29)$$

where G is called the *memductance* (for memory conductance).

It might be well to point out that the classification of memristive systems (as well as memcapacitive and meminductive systems, which we discuss in the next sections) into current-controlled and voltage-controlled types is, in most cases, rather a matter of mathematical (or experimental) convenience. In particular, if we consider Equation (27) describing a current-controlled memristive system and algebraically solve it with respect to the current I (assuming a unique solution at any given time), then we actually obtain Equation (28) of the voltage-controlled memristive system. Secondly, Equation (29) can be obtained if we substitute I obtained from Equation (27) into Equation (26). Thus, having equations of a current-controlled memristive system, we can re-write them in the form of a voltage-controlled one and vice versa, provided that a unique solution of Equation (27) with respect to the current, or a unique solution of Equation (28) with respect to the voltage, can be found.

As noted before, in real systems, it is very unlikely that the memristor's state depends only on the charge that flows through the system or on the integral over the applied voltage. In other words, ideal memristors are probably rare – a notable exception is a small dissipative component in Josephson junctions (see Section 6.2). That is possibly the reason why many authors use these words interchangeably so that the word “memristor” indicates any resistive system with memory that satisfies the coupled Equations (27) and (26) or (28) and (29). In fact, even Strukov *et al.* [18], who have rejuvenated this field, label their TiO_2 device as memristor while, in reality, it is a memristive system. Actually, an attempt to describe the response of such memristive systems using the ideal memristor's Equation (24) or Equation (25) can result in inadequate results, e.g.

in switching at low applied biases or currents. The experimental evidence of ideal memristor behavior should contain, for instance, a ϕ - q plot showing a single (non-linear) curve when the device is driven by a periodic input. In this review, in order to avoid additional confusion, we will use the terms “memristor” and “memristive system” consistently with the definitions given above. The same will be applied also to “memcapacitors” and “memcapacitive systems” as well as to “meminductors” and “meminductive systems”.

2.4.2. Properties of memristors and memristive systems

There are several properties that are relevant to identifying materials and systems as memristors or memristive. As anticipated in Section 2.2, arguably the most important one is the appearance of a “pinched hysteresis loop” in the current–voltage characteristics of these systems when subject to a periodic input [16]. This is obvious from Equations (27) and (26), because when $V = 0$ then $I = 0$ (and vice versa), as illustrated in Figure 4. In addition, if the state equation (26) has a unique solution at any given time $t \geq t_0$, if the voltage (or current) is periodic, then during each period the I - V curve is a simple loop passing through the origin, namely there may be at most two values of the current I for a given voltage V , if we consider a voltage-controlled device, or two values of the voltage V for a given current I , for a current-controlled system.

Moreover, when subject to a periodic stimulus, a memristive system typically behaves as a linear resistor in the limit of infinite frequency, and as a non-linear resistor in the limit of zero frequency (provided that $\dot{x} = f(x, I) = 0$ in Equation (26) has a steady-state solution) – see Figure 4. These last two properties can be understood quite easily. Irrespective of the physical mechanisms that define the state of the system, at very low frequencies, the system has enough time to adjust its value of resistance to the instant value of the voltage (or current), so that the device behaves as a non-linear resistor. On the other hand, at very high frequencies, there is not enough time for any kind of resistance change during a period of oscillations of the control parameter, so that the device operates as a usual (typically linear) resistor [16].

If $R_M(x, I, t) \geq 0$, namely the resistance is positive at any given time, then the quantity (which is the energy stored in the system)

$$U_M = \int_{t_0}^t V(\tau)I(\tau) d\tau = \int_{t_0}^t I^2(\tau)R_M(x, I, t) d\tau \geq 0 \quad (30)$$

is always positive or zero. In other words, memristors and memristive systems are *passive* devices. Typically, the electrical energy transforms into heat, which is then dissipated due to a heat exchange with the environment. Another important feature, that follows from the fact that the current is zero when the voltage is zero (and vice versa), is the so-called “no energy discharge property” namely

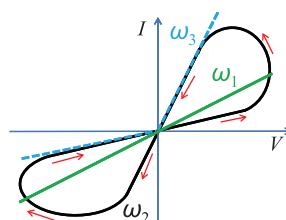


Figure 4. Schematics of a pinched hysteresis loop of a memristive system subject to a periodic stimulus. The size of the hysteresis depends on the applied voltage frequency: at low frequencies, memristive systems typically behave as non-linear resistors, at intermediate frequencies they exhibit pinched hysteresis loops, and at high frequencies they typically operate as linear resistors. On the plot, $\omega_1 \gg \omega_2 \gg \omega_3$.

a memristive system cannot store energy, like a capacitor or an inductor. These are the main properties that we will use to identify memristive systems when discussing practical examples.

2.4.3. Simple example: thermistors

Let us consider one of the first identified memristive systems: the thermistor. The latter one is a temperature-sensitive resistor. Although all resistances generally vary with temperature, thermistors are built of semiconducting materials that are especially sensitive to temperature, such as different oxides of metals including manganese, iron, nickel, cobalt, copper and zinc. Memristive properties of thermistors are based on self-heating and were noticed by Chua and Kang in 1976 [16]. To show that these are indeed memristive systems, let us consider a negative temperature coefficient (NTC) thermistor that is described by the current–voltage relation [19]:

$$V = R_0 e^{\beta((1/T)-(1/T_0))} I \quad (31)$$

where the constant R_0 denotes the resistance at a certain temperature T_0 , T the absolute temperature of thermistor (all temperatures are in Kelvin) and β a material-specific constant. It follows from Equation (31) that the resistance of NTC thermistors decreases with temperature. The temperature of the thermistor T depends on the power dissipated in the thermistor and is described by the heat transfer equation

$$C_h \frac{dT}{dt} = V(t)I(t) + \delta(T_{\text{env}} - T) \quad (32)$$

where C_h is the heat capacitance, δ is the dissipation constant of the thermistor [16], and T_{env} is the background (environment) temperature. In the memristive description of thermistor, its temperature T plays the role of the internal state variable. In order to obtain a memristive model of thermistor, we substitute V from Equation (31) into Equation (32). Table 1 summarizes the memristive model of thermistor.

As an example of the previously mentioned equivalence of current-controlled and voltage-controlled memristive system's formulations, we would like to demonstrate that the thermistor can alternatively be described as a voltage-controlled memristive system. For this purpose, we can express the current I from Equation (31) and substitute it into Equation (32). Table 2 provides a description of thermistor as a voltage-controlled memristive system. Such a transformation between current-controlled and voltage-controlled description and vice versa can easily be performed for many systems. Therefore, in the following, we will avoid giving a dual description, since very often the transformation between different descriptions is trivial.

Figure 5 illustrates a solution of the equations given in Table 2. It is worth noting that, because of the symmetry of the equation for the internal state variable with respect to the change of the voltage sign, the I – V lines in Figure 5(b) do not self-intersect when passing through (0,0) and are, therefore, of type II crossing behavior (cf. Figure 2). This is an interesting distinctive feature

Table 1. Memristive model of thermistor.

Physical system	Thermistor
Internal state variable(s)	Temperature, $x = T$
Mathematical description	$V = R_0 e^{\beta((1/x)-(1/T_0))} I$ $\frac{dx}{dt} = C_h^{-1} R_0 e^{\beta((1/x)-(1/T_0))} I^2 + C_h^{-1} \delta(T_{\text{env}} - x)$
System type	First-order current-controlled memristive system

Table 2. Alternative memristive model of thermistor in terms of equations of voltage-controlled memristive system.

Physical system	Thermistor
Internal state variable(s)	Temperature, $x = T$
Mathematical description	
	$I = [R_0 e^{\beta((1/x) - (1/T_0))}]^{-1} V$
	$\frac{dx}{dt} = C_h^{-1} [R_0 e^{\beta((1/x) - (1/T_0))}]^{-1} V^2 + C_h^{-1} \delta(T_{\text{env}} - x)$
System type	First-order voltage-controlled memristive system

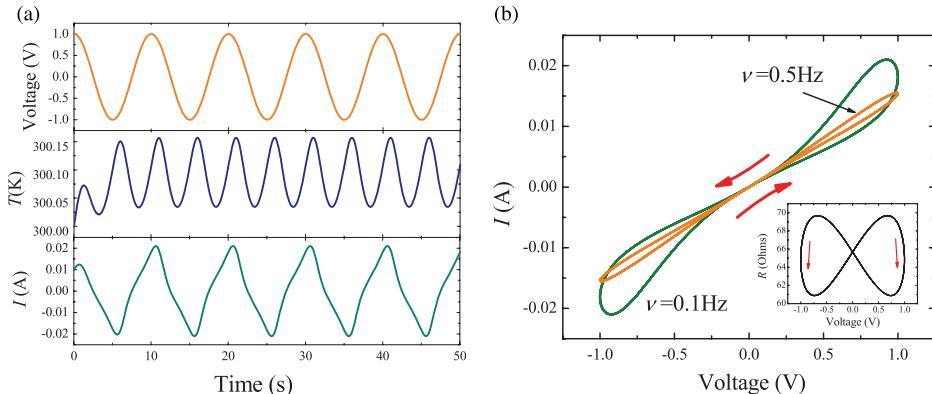


Figure 5. Simulations of an ac-biased thermistor. It should be emphasized that the I - V lines in (b) do not self-cross at $(0,0)$ (see also Figure 2). The plots were obtained using the parameter values $T_0 = T_{\text{env}} = 300 \text{ K}$, $R_0 = 100 \Omega$, $C_h = 0.1 \text{ J/K}$, $\delta = 0.1 \text{ J/(s}\cdot\text{K)}$, $\beta = 5 \times 10^5 \text{ K}$. The applied voltage is $V(t) = V_0 \cos(2\pi\nu t)$ with $V_0 = 1 \text{ V}$ and $\nu = 0.1 \text{ Hz}$ in (a). The inset in (b) shows the resistance versus voltage obtained at $\nu = 0.5 \text{ Hz}$.

of pinched hysteresis loops of the thermistor compared with others, which we will discuss later. We also note that the I - V curves for the thermistor demonstrate frequency-dependent hysteresis typical of memristive systems.

2.5. Memcapacitors and memcapacitive systems

2.5.1. Definitions

Let us now extend the above concept of resistor with memory to the other two fundamental circuit elements, namely capacitors and inductors, and define corresponding memory-circuit elements [6]. It is worth pointing out that for these memory elements, a microscopic derivation based on response functions has not been developed yet. We thus follow the axiomatic definitions of [6]. We will then show in the following sections that several systems do indeed fall within these classifications.

From Equations (4) and (5), we define a *voltage-controlled memcapacitive system* by the following:

$$q(t) = C(x, V_C, t)V_C(t), \quad (33)$$

$$\dot{x} = f(x, V_C, t), \quad (34)$$

where $q(t)$ is the charge on the capacitor at time t , $V_C(t)$ the corresponding voltage and C the *memcapacitance* (for memory capacitance) which depends on the state and history of the system,

as it is evident in its dependence on the state variables x . Relations

$$V_C(t) = C^{-1}(x, q, t)q(t), \quad (35)$$

$$\dot{x} = f(x, q, t), \quad (36)$$

define a *charge-controlled memcapacitive system*, where C^{-1} is an inverse memcapacitance.

A subclass of the above systems corresponds to the case in which the capacitance depends only on the full history of the voltage, namely

$$C(t) = C \left[\int_{t_0}^t V_C(\tau) d\tau \right]. \quad (37)$$

This equation defines an ideal *voltage-controlled memcapacitor*. In this case, Equations (33) and (34) reduce to

$$q(t) = C \left[\int_{t_0}^t V_C(\tau) d\tau \right] V_C(t). \quad (38)$$

Similarly, for a *charge-controlled memcapacitor*

$$V_C(t) = C^{-1} \left[\int_{t_0}^t q(\tau) d\tau \right] q(t), \quad (39)$$

where, in the above two equations, the lower integration limit (initial moment of time) may be selected as $-\infty$, or 0 if $\int_{-\infty}^0 V_C(\tau) d\tau = 0$ (in Equation (38)) and $\int_{-\infty}^0 q(\tau) d\tau = 0$ (in Equation (39)).

We note that in this review (similarly to [6]), the name “memcapacitor” will be reserved for the special class defined by Equation (38) or Equation (39) which represents *ideal* memory capacitors and the term “memcapacitive systems” will be used for the broader class of elements defined by Equations (33) and (34). Similar to the case of memristive systems, we expect memcapacitive systems to be the norm rather than the exception. For the sake of clarity, we will not use the terms “memcapacitor” and “memcapacitive systems” interchangeably.

2.5.2. Properties of memcapacitors and memcapacitive systems

It follows from Equation (33) or Equation (35) that, apart from specific cases that we will discuss later (see, e.g. Section 4.2.1), the charge is zero whenever the voltage is zero. Note, however, that in this case, $q = 0$ does not imply $I = 0$ (and vice versa), and thus this device can store energy. Therefore, the latter can be both added to and removed from a memcapacitive system. However, unlike memristive systems, it is easy to see that in the present case the relation

$$U_C = \int_{t_0}^t V(\tau) I(\tau) d\tau \geq 0 \quad (40)$$

does not always hold. This implies that Equations (33) and (34) or Equations (35) and (36) for the memcapacitive systems postulated above may, in principle, describe both active and passive devices. To see this point more clearly, consider Figure 6 where a schematic memcapacitive system hysteresis loop passing through the origin is shown when the system is subject to a periodic stimulus

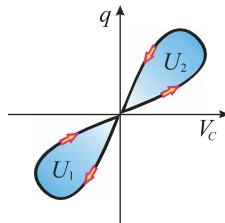


Figure 6. Schematics of a pinched hysteresis loop of a memcapacitive system subject to a periodic stimulus. The energy added to or removed from the system is the area between the curve and the q -axis (namely $\int V_C(q) dq$). The areas of shaded regions U_1 (U_2) give the amount of added (removed) energy in each half-period. The signs of U_1 and U_2 are determined by the direction on the loop. For the direction shown here, U_2 is positive and U_1 is negative.

of period T . The shaded areas give the energies

$$U_1 = \int_0^{T/2} V_C(q) dq \quad (41)$$

and

$$U_2 = \int_{T/2}^T V_C(q) dq, \quad (42)$$

added to or removed from the system, respectively, when the integral runs over half of the period. The memcapacitive system can then be

$$U_1 + U_2 = 0 \quad (\text{non-dissipative}), \quad (43)$$

$$U_1 + U_2 > 0 \quad (\text{dissipative}) \quad (44)$$

or

$$U_1 + U_2 < 0 \quad (\text{active}). \quad (45)$$

The fact that a memcapacitive system may be dissipative can be seen by looking at a practical realization of memory capacitance. This can be accomplished in two different ways, or their combination. The simplest realization is via a geometrical change of the system (e.g. a variation in its structural shape as in nano-electromechanical systems [20]). Alternatively, one may rely on the quantum-mechanical properties of the free carriers and bound charges of the materials comprising the capacitor that could give rise, for instance, to a history-dependent permittivity $\varepsilon(t)$. In either case, inelastic (dissipative) effects may be involved in changing the capacitance of the system upon application of the external control parameter, whether charge or voltage. These dissipative processes release energy in the form of heating of the materials composing the capacitor. We will discuss some of these cases in Section 4.

On the other hand, an active device may be realized when, in order to vary the capacitance, one needs energy from sources that control the state variable dynamics, Equation (34), other than the energy from the control parameter. This energy could be, e.g. in the form of elastic energy or provided by a power source that controls, say, the permittivity of the system via a polarization field. This energy can then be released in the circuit thus amplifying the current.

Memcapacitive systems share with memristive systems the property that they typically behave as linear elements in the limit of infinite frequency, and as non-linear elements in the limit of zero frequency, assuming that Equations (34) and (36) admit a steady-state solution. The origin

of this behavior rests again on the ability of the system to adjust to a slow change in bias (for low frequencies) and its inability to respond to extremely high frequency oscillations.

In addition, if the state Equation (34) has only a unique solution at any given time $t \geq t_0$, then if $V_C(t)$ is periodic, the $q-V_C$ curve is a simple loop during a period (as shown in Figure 6), namely there may be at most two values of the charge q for a given voltage V_C , for a voltage-controlled device, or two values of the voltage V_C for a given charge q , for a charge-controlled system. This loop is also anti-symmetric with respect to the origin if, for the case of Equations (33) and (34), $C(x, V_C, t) = C(x, -V_C, t)$ and $f(x, V_C, t) = f(x, -V_C, t)$.

Finally, we anticipate an important point we will come back to in Sections 2.8 and 4.2.1. Equations (33) and (34) for memcapacitive systems say nothing about whether these devices may or may not be constructed as a combination of the basic circuit elements (resistors, capacitors and inductors) and elements that can, in fact, be derived from these.

Furthermore, some of these memcapacitive systems show interesting features which are evident from definitions (33) and (34). In fact, there may be cases in which, at certain instants of time, both the charge and the capacitance are zero, and thus the voltage across the capacitor may be finite. Similarly, there may be times when the capacitance *diverges*, while the voltage vanishes [21,22]. This gives rise to a finite charge on the plate of the capacitor. Finally, nothing in definitions (33) and (34) prohibits the voltage to change sign, while the charge does not. This situation represents the case of *dynamical over-screening* and produces a *negative* capacitance [21,22], and this may occur without the need of, e.g. ferroelectric materials.

2.5.3. Simple example: elastic memcapacitive system

Let us consider a model of a simple electro-mechanical device with memory, which we call *elastic memcapacitive system*. Some authors also call such a system an elastic capacitor [23]. An elastic memcapacitive system is a parallel-plate capacitor with an elastically suspended upper plate and a fixed lower plate as shown in Figure 7. When a charge is added to the plates, the separation between plates changes as oppositely charged plates attract each other. The dynamics of the system depends on initial conditions and time-dependent fields, thus providing a memory mechanism. Previously, the model of elastic memcapacitive system was used in studies of lipid bilayers and to explain electrical breakdown of biological membranes [23,24]. From the memory-elements standpoint, the elastic memcapacitive system is an important example of passive memcapacitive device.

The internal state variable y of the elastic memcapacitive system is the displacement of the upper plate from its equilibrium uncharged position, d_0 , under the action of a Coulomb interaction of oppositely charged plates. Mathematically, the charge dynamics on the elastic memcapacitive system is described by a parallel-plate capacitor model with variable separation between the plates

$$q = \frac{C_0}{1 + y/d_0} V_C, \quad (46)$$

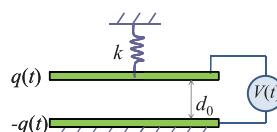


Figure 7. Elastic memcapacitive system connected to a voltage source $V(t)$.

where C_0 is the equilibrium capacitance at $q = 0$, and the dynamics of y is given by the classical harmonic oscillator equation including damping and driving terms:

$$\frac{d^2y}{dt^2} + \gamma \frac{dy}{dt} + \omega_0^2 y + \frac{q^2}{2\varepsilon_0 m S} = 0. \quad (47)$$

Here, γ is a damping coefficient representing dissipation of the elastic excitations, $\omega_0 = \sqrt{k/m}$, k is the spring constant, m is the mass of the upper plate, S is the area of the plate. It follows from Equations (46)–(47) that the elastic memcapacitive system is a second-order charge-controlled memcapacitive system. It is dissipative when $\gamma > 0$ and non-dissipative when $\gamma = 0$. The model of elastic memcapacitive system is summarized in Table 3.

Figure 8 shows simulations of the elastic memcapacitive system. When a single voltage pulse is applied to the elastic memcapacitive system (Figure 8(a)), the upper plate begins oscillating. These oscillations last for an extended period of time, keeping the memory about the pulse. In the equation of motion for the state variable (Equation (47)), the driving force is proportional to q^2 . As a consequence, the hysteresis q – V curves of the elastic memcapacitive system (Figure 8(b)) do

Table 3. Model of elastic memcapacitive system.

Physical system	Elastic memcapacitive system
Internal state variable(s)	Displacement and velocity of upper plate, $x_1 = y, x_2 = \frac{dy}{dt}$
Mathematical description	$V_C = \left[\frac{C_0}{1 + x_1/d_0} \right]^{-1} q$ $\frac{dx_1}{dt} = x_2$ $\frac{dx_2}{dt} = -\left(\gamma x_2 + \omega_0^2 x_1 + \frac{q^2}{2\varepsilon_0 m S} \right)$
System type	Second-order charge-controlled memcapacitive system

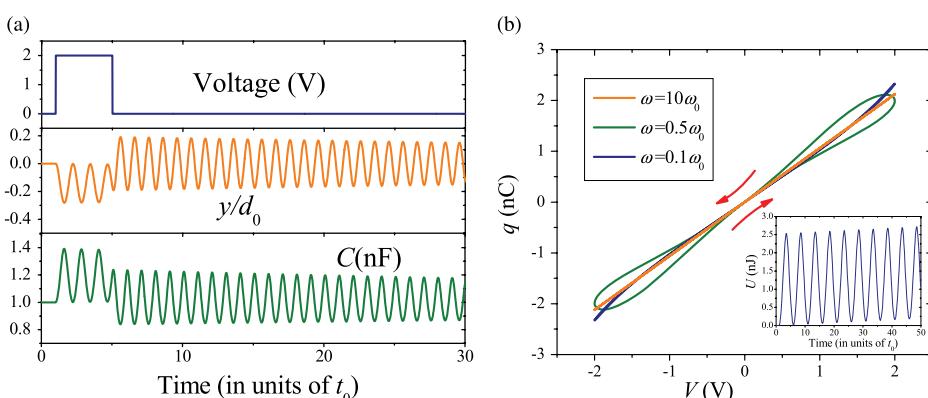


Figure 8. Simulations of the elastic memcapacitive system excited by a single voltage pulse (a) and an ac voltage (b) obtained with the initial conditions $y = 0$ and $dy/dt = 0$ at $t = 0$. We used $C_0 = 1 \text{ nF}$, $\gamma t_0 = 0.02$, $t_0 = 2\pi/\omega_0$, $2\pi^2/(md_0^2\omega_0^2 C_0) = 10^{18}$ and the ac voltage amplitude in (b) is 2 V. It is interesting to note the absence of self-crossing in (b) at $(0,0)$ (cf. Figure 2). The inset in (b) shows the capacitor energy, Equation (40), calculated at $\omega = 0.1\omega_0$ proving that this element is dissipative.

not self-intersect at $(0,0)$, namely they are of type II, similar to the I - V curves of the thermistor (Section 2.4.3, see also Figure 2).

2.6. Meminductors and meminductive systems

2.6.1. Definitions

Let us now introduce the third class of memory devices, namely that of memory inductors [6]. In order to do this, let us first define the flux

$$\phi(t) = \int_{-\infty}^t V_L(t') dt', \quad (48)$$

where $V_L(t)$ is the induced voltage on the inductor (equal to minus the electromotive force). In analogy with memristive and memcapacitive systems we then define from Equations (4) and (5) a *current-controlled meminductive system* one that follows the relations:

$$\phi(t) = L(x, I, t)I(t), \quad (49)$$

$$\dot{x} = f(x, I, t), \quad (50)$$

where L is the *meminductance*. Similarly, we define a *flux-controlled meminductive system* as follows:

$$I(t) = L^{-1}(x, \phi, t)\phi(t) \quad (51)$$

$$\dot{x} = f(x, \phi, t) \quad (52)$$

with L^{-1} being the inverse of the meminductance.

In this work, we will not use interchangeably the terms “meminductive system” and “meminductor”, reserving the latter for *ideal meminductors* [6]. Those are a subclass of the above systems, when Equations (49) and (50) reduce to

$$\phi(t) = L \left[\int_{t_0}^t I(\tau) d\tau \right] I(t) \quad (53)$$

for a current-controlled system, or when Equations (51) and (52) can be written as

$$I(t) = L^{-1} \left[\int_{t_0}^t \phi(\tau) d\tau \right] \phi(t), \quad (54)$$

for a flux-controlled meminductor. In the above two equations, the lower integration limit may be selected as $-\infty$, or 0 if $\int_{-\infty}^0 I(\tau) d\tau = 0$ and $\int_{-\infty}^0 \phi(\tau) d\tau = 0$, respectively.

2.6.2. Properties of meminductors and meminductive systems

Meminductors and meminductive systems share essentially the same properties of memcapacitive systems, such as an hysteretic loop that may or may not be pinched – and situations in which the meminductance may diverge and become negative, see, e.g. Equations (49) and (51) – non-linearity at very low frequencies and linearity at high frequencies, energy storage and the possibility to behave as non-dissipative, dissipative or active elements.

The energy stored in the system can be evaluated as follows. For the sake of definiteness, let us consider only the current-controlled meminductive systems. Taking first the time derivative of both sides of Equation (49) yields

$$V_L = \frac{d\phi}{dt} = L \frac{dI}{dt} + I \frac{dL}{dt}, \quad (55)$$

which shows that the second term on the right-hand side of the above equation is an additional contribution to the induced voltage due to a time-dependent inductance L . The energy stored in the current-controlled meminductive system can then be calculated as

$$U_L(t) = \int_{t_0}^t V_L(\tau) I(\tau) d\tau = \int_{t_0}^t \left[L \frac{dI}{dt} + I \frac{dL}{dt} \right] I(\tau) d\tau. \quad (56)$$

When the inductance, L , is constant, we readily obtain the well-known expression for the energy $U_L = LI^2/2$. This is interpreted as the energy of the magnetic field generated by the current. However, in the meminductive case, the extra term due to the time derivative of L may be related to other processes that control the meminductance and which are formally represented by the state variables x . These processes could be related, for instance, to the elastic energy required to modify the shape of the inductor in time, or an external energy source that controls the permittivity of the inductor as a function of time.

In general, we can formulate the passivity criterion of meminductive systems by stating that if at $t = t_0$ they are in their minimal energy state then $U_L(t) \geq 0$ at any subsequent moment of time, with the inequality sign indicating the presence of energy storage and dissipative processes.

2.6.3. Simple example: elastic meminductive system

We here introduce the model of *elastic meminductive system*, namely an inductor which is formed by two parallel wires of length l separated by a distance $d_0 + y$ as we depict in Figure 9(a). One of the wires is kept fixed, while the other is allowed to move under the effect of a spring, and we assume for simplicity that both wires have the same radius r . The two wires are connected together as illustrated in Figure 9(a) in such a way that they carry currents of equal magnitude but opposite in direction. This system can, in principle, be realized using micro-electromechanical systems (MEMS) as we will discuss in Section 5.1. As current flows through the wires, the repulsive magnetic force pushes the top wire up compressing the spring. In this way, the distance between the wires increases resulting in a different value of inductance as follows:

$$L(y) = \frac{\mu_0 l}{\pi} \ln \frac{d_0 + y}{r}, \quad (57)$$

where μ_0 is the vacuum permeability, d_0 the equilibrium distance between the wires when $I = 0$ and y the displacement of the top wire from its equilibrium position at $I = 0$.

The classical equation of motion of the top wire, taking into account damping and the interaction force of the current, can be written as

$$\frac{d^2y}{dt^2} + \gamma \frac{dy}{dt} + \omega_0^2 y - \frac{\mu_0 l I^2}{2\pi m(d_0 + y)} = 0. \quad (58)$$

Here, γ is a damping coefficient representing dissipation of the elastic excitations, $\omega_0 = \sqrt{k/m}$, k is the spring constant and m is the mass of the upper wire. It follows from Equation (58) that the elastic meminductive system is a second-order current-controlled meminductive system. Its properties are presented in Table 4.

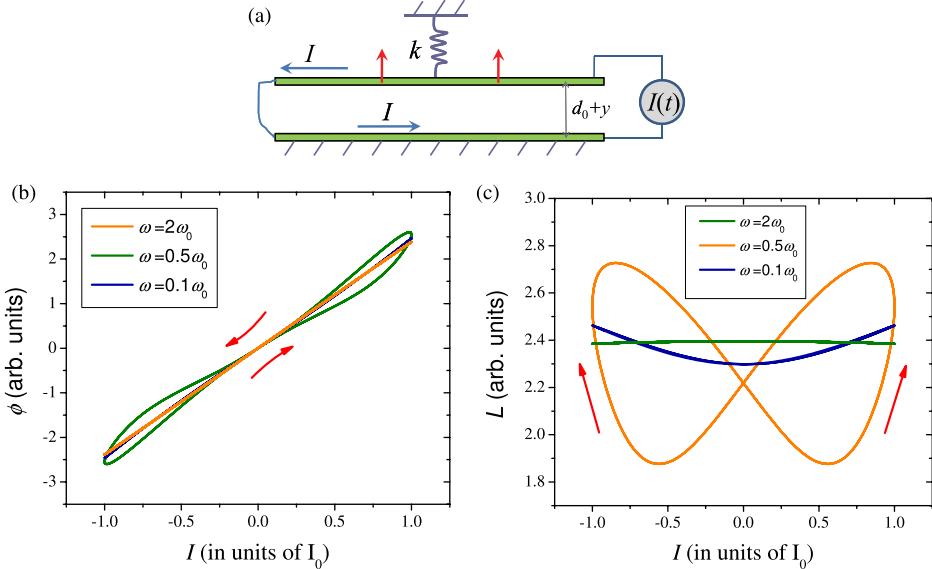


Figure 9. (a) Schematic of an elastic meminductive system based on repulsion (vertical red arrows represent a repulsive force) of current-carrying wires of opposite current. The inductance of the system increases with increasing wires separation $d_0 + y$ from the equilibrium distance d_0 . (b) and (c): $\phi - I$ and $L - I$ curves of elastic meminductive system, respectively obtained with the initial conditions $y = 0$ and $dy/dt = 0$ at $t = 0$. The shape of the curves indicate type II hysteretic behavior. These plots were obtained using parameter values $\gamma/\omega_0 = 0.2$, $r/d_0 = 0.1$, $\mu_0 l I_0^2 / (2\pi m \omega_0^2 d_0^2) = 0.2$. Here, I_0 is the ac-current amplitude.

Table 4. Model of elastic meminductive system.

Physical system	Elastic meminductive system
Internal state variable(s)	Displacement and velocity of upper wire, $x_1 = y$, $x_2 = \frac{dy}{dt}$
Mathematical description	$\phi = \frac{\mu_0 l}{\pi} \ln \left(\frac{d_0 + x_1}{r} \right) I$ $\frac{dx_1}{dt} = x_2$ $\frac{dx_2}{dt} = - \left(\gamma x_2 + \omega_0^2 x_1 - \frac{\mu_0 l I^2}{2\pi m (d_0 + x_1)} \right)$
System type	Second-order current-controlled meminductive system

It is dissipative when $\gamma > 0$, and non-dissipative when $\gamma = 0$. The overall form of the equation describing dynamics of elastic meminductive system (Equation (58)) is similar to that of elastic memcapacitive system (47), with the difference that the interaction in the case of the meminductive system is repulsive and depends on the separation of the wire (in the case of elastic memcapacitive system, the interaction force is attractive and does not depend on the separation between the plates).

Selected results of elastic meminductive system's simulations are presented in Figure 9(b) and (c). These plots demonstrate typical frequency dependencies of memory elements. It is interesting

to note the absence of self-crossing in the ϕ - I curves, and a self-crossing of L - I curves. Therefore, following our suggested classification scheme, such a system shows a type II hysteresis.

2.7. Combination of memory features

At this stage, it is worth pointing out that in real systems, the above three memory features may appear simultaneously [6,15,21]. This is not surprising, especially at the nanoscale. To give just an example we recall that when a current flows in a resistor, at the microscopic level local resistivity dipoles form due to scattering of carriers at interfaces [25]. Namely, charges accumulate on one side of the resistor with a consequent depletion on the other side, with possible accumulation and depletion over the whole spatial extent of the resistor [4]. It was shown numerically that these dipoles develop *dynamically* over length scales of the order of the screening length [26]. This means that the formation of these local resistivity dipoles takes some time and is generally accompanied by some energy storage related to the capacitance of the system. It is also known that memristive and memcapacitive effects can be simultaneously observed in the resistance switching memory cells [27]. The experimental data reproduced in Figure 10 from [27] clearly show that the changes in memristance and memcapacitance are correlated and, are therefore, in this example, most probably related to the same state variables.

We thus expect that in nanoscale systems memristive behavior is always accompanied, to some extent, by a (possibly very small) capacitative behavior. In this case, the I - V hysteresis loop may not exactly cross the origin at frequencies comparable to the inverse characteristic time of charge equilibration processes. We will give explicit examples of this effect in Section 3.5.1 when discussing the transverse voltage memory response of the spin Hall effect in inhomogeneous semiconductor systems [10] (note that the curves in Figure 33 do not cross $(0, 0)$ exactly), and in Section 4.3.2, where the memristance and memcapacitance induced by the MIT of VO_2 is made clear in the optical response of metamaterials [15].

The analysis of these systems may be done by combining a number of three memory-circuit elements in parallel and/or in series, possibly together with standard resistors, capacitors and

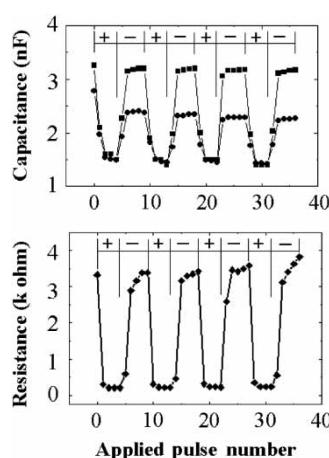


Figure 10. Nonvolatile capacitance and resistance changes versus number of applied pulses for a Au/PCMO/YBCO/LAO sandwich structure at room temperature. Here, PCMO is $\text{Pr}_{0.7}\text{Ca}_{0.3}\text{MnO}_3$, YBCO is $\text{YBa}_2\text{Cu}_3\text{O}_{7-x}$ and LAO is LaAlO_3 . The capacitance values shown by solid circles and square dots were measured at 200 and 20 kHz, respectively. Reprinted with permission from S. Liu *et al.*, Journal of Applied Physics 100, p. 056101, 2006 [27]. Copyright (2009) American Institute of Physics.

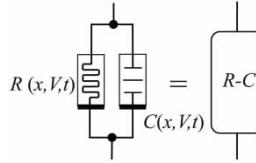


Figure 11. The combination of two or more memory-circuit elements in parallel or in series may result in the compact description of a single circuit element with non-algebraic dependence on the control parameters. In this particular case, a voltage-controlled memristive system and a voltage-controlled memcapacitive system in parallel can be compactly described as a voltage-controlled effective memristive system with non-algebraic dependence on bias.

inductors. It is worth mentioning that combination of these elements may result in compact descriptions of memory systems with non-algebraic dependence on the control parameters. As an example of this, let us consider a voltage-controlled memristive system (described by Equations (28) and (29)) and a voltage-controlled memcapacitive system (Equations (33) and (34)) coupled in parallel (see Figure 11).

For simplicity, we may assume that the same state variables determine the memory of both the resistor and the capacitor. This, however, may not always hold true. This latter case, however, can easily be accounted for by expanding the range of state variables x to include both sets. Using Kirchhoff's law, the total current of the parallel circuit is

$$I(t) = I_M + \frac{dq}{dt}, \quad (59)$$

where I_M indicates the current that flows across the memristive system. Introducing the definitions of the two memory elements (and noticing that in a parallel circuit the voltage drop across the resistor $V(t)$ is the same as that across the capacitor), we then obtain

$$I(t) = G(x, V, t)V(t) + \frac{d}{dt}[C(x, V, t)V(t)]. \quad (60)$$

By defining the effective memductance

$$G_{\text{eff}}(x, V, t) = G(x, V, t) + \frac{1}{V(t)} \frac{d}{dt}[C(x, V, t)V(t)], \quad (61)$$

we find that the whole circuit behaves like a voltage-controlled memristive system with current

$$I(t) = G_{\text{eff}}(x, V, t)V(t), \quad (62)$$

and non-algebraic dependence on the bias V .

Along similar lines, Mouttet [28] has suggested a memadmittance (memory admittance) model in order to describe simultaneous memristive and memcapacitive properties of a system. This idea was applied to thin-film memory materials. Based on this approach, equations relating the cross-sectional area of conductive bridges in resistive switching films to shifts in capacitance were derived [28]. Moreover, Riaza [29] has proposed a *hybrid memristor* that is described by a relation involving all four circuit variables q , φ , I and V . Such an element may account for physical devices in which memory effects of different nature coexist. Several examples of hybrid memristors as well as corresponding extension of circuit theory is given in his work [29].

2.8. Are memristors, memcapacitors and meminductors fundamental circuit elements?

Finally, it is worth mentioning that the behavior of an *ideal* memristor, namely that which is described by relation (24) (or Equation (25)) cannot be simulated by any combination of “standard” – namely two-terminal, time-independent, albeit possibly non-linear – resistors, capacitors and inductors. In other words, there is no possible finite combination of standard circuit elements that can reproduce the dynamical properties of ideal memristors. This can be shown by recalling that a memristor does not store energy so that capacitors and inductors cannot possibly be used to simulate it, while a finite number of non-linear resistors cannot reproduce, e.g. the current history as required by definition (24). It is for this reason that an ideal memristor is sometimes called the “fourth” circuit element [5].

However, also an ideal memcapacitor and an ideal meminductor (see, e.g. Equations (39) and (53)) cannot be simulated by combinations of standard resistors, capacitors and inductors, because, in this case as well, the lack of time dependence does not allow us to retain information on the full charge (memcapacitor) or current (meminductor) dynamics. For instance, one could argue that since standard capacitors store information on the *current* history (the integral of the current is the charge on the capacitor) they could be used to simulate the behavior of meminductors. However, if this were the case, the resulting circuit would have capacitative components and therefore would not be an ideal meminductor. The same reasoning can be made for using inductors to simulate memcapacitors.

Therefore, it is in this sense that *ideal* memristors, memcapacitors and meminductors can be considered as “fundamental” circuit elements, and it would thus be tempting to call the last two the “fifth” and “sixth” circuit elements. These authors, however, do not share this view, and prefer to subscribe to the notion that there are only three fundamental circuit elements: resistors, capacitors and inductors, with or without memory.

We also note that the above considerations cannot be extended to memristive, memcapacitive and meminductive elements because in that case, the internal state variables could have a physical origin which could be simulated by standard (possibly non-linear) circuit elements. For instance, as we will discuss in Section 4.2.1, some memcapacitive systems may be represented by a combination of basic circuit elements (capacitors and non-linear resistors; for examples of these, see, e.g. [21,22]). Or one could envision a combination of non-linear resistors with negative differential resistance [30] to retain the history of the voltage or current and thus simulate memristive systems. Irrespective of the above, these types of memory elements are still of great importance since they provide a complex functionality within a single electronic structure [21].

After these general considerations we are now ready to discuss several systems that exhibit memory features and the physical mechanisms that generate these phenomena.

3. Memristive systems

Many systems exhibit memristive behavior with underlying physical mechanisms that vary considerably (see Figure 12 for a list of common mechanisms). Examples that were identified early in [16] include thermistors [19] and ionic systems, in particular, membranes in neuron cells [13]. For the reasons we have anticipated in Section 1, recent interest has been focussed on the dynamics of nanostructures. Some of them were intensely studied in the context of the development of resistive-switching memory during the last 10–15 years. To the best of our knowledge, this area of research was initiated by Hickmott in 1962 by observing hysteretic behavior in oxide insulators [31]. Later, resistance switching was demonstrated in thin films of silicon monoxide (SiO) between metal electrodes by Simmons and Verderber [32] and in TiO_2 by Argall [33]. (These and other earlier works in the field were reviewed by Dearnaley *et al.* [34].) However, it was only in 2008

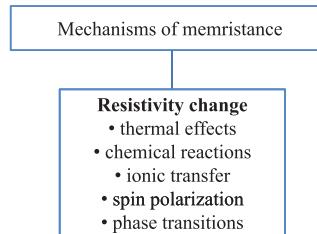


Figure 12. Classification scheme of memristance mechanisms.

that resistive switching devices were recognized as memristive systems [18]. Additional examples of memristive systems include spintronic devices [17,35], phase-transition materials [15,36] and polaronic systems [37]. Below we discuss memristive properties of a variety of physical systems in detail.

3.1. Thermistors

Thermistors were considered in Section 2.4.3, and we refer the reader to that section for details on a mathematical model to describe them.

3.2. Resistance switching memory cells

At the present time, it is well known that resistive switching effects can be observed in such diverse classes of materials as binary oxides (TiO_2 , SiO_2 , CuO , NiO , CoO , Fe_2O_3 , MoO , VO_2) [11,15,36,38–42], nanogap systems on SiO_2 [43], metal nanogap junctions [44], perovskite-type oxides ($Pr_{1-x}Ca_xMnO_3$, $SrTiO_3:Cr$) [45–49], sulfides (Cu_2S , Ag_2S) [50–52], semiconductors (Si, GaAs, ZnSe–Ge) [53–55] and organics [56–58]. The basic mechanisms of switching are not yet well understood in all cases; however, quite generally, the related memory devices can be separated into the following most important categories: nanoionic, nanothermal (a sub-class of nanothermal memory devices, phase-change memory cells, are considered in Section 3.3), macromolecular memory and molecular effects memory devices [59]. Due to this wide range of physical systems and memory mechanisms, we will provide specific examples with particular focus on the state variables responsible for memory and their theoretical description, if available. The reader interested in some more comprehensive reviews on just resistive switching is urged to look into the recently published ones [52,60–63].

Very often, the experimental setup showing resistive switching involves an array (called a crossbar array) of capacitor-like cells. Each capacitor-like cell contains a layer of an insulating material sandwiched between two metal layers (which may be made of the same or different materials) as depicted in Figure 13. In what follows, we will discuss the behavior of separate cells. Although each cell in the crossbar architecture can be addressed independently by an appropriate selection of a word (say, horizontal) and bit (vertical) lines, the current between two such lines can flow across many paths causing a potential problem for the crossbar memory implementation. As a possible solution of this problem, additional individual access devices (such as transistors or diodes) may be required.

Typically, an as-fabricated cell is in a highly resistive state and, in order to obtain resistance switching operation, an electroforming step is needed. This is an important step of device fabrication defining its future operation [64]. In this step, a high-voltage amplitude pulse is applied to the cell producing a nondestructive (soft) breakdown, with the creation of single “filaments” inside the main material matrix. This process of breakdown is usually controlled by selecting a

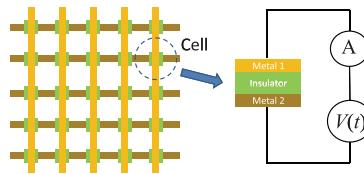


Figure 13. A single metal–insulator–metal memory cell (shown on the right) is often fabricated as part of a crossbar array as shown on the left. Crossbar arrays consist of two perpendicular sets of wires separated by an insulating material. Each cell can be generally addressed independently, although the current, in a purely resistive structure, can flow through different cells. e.g. in two-dimensional crossbar arrays, a voltage is applied to one of the lines and one to the perpendicular wires in the array. Here, “A” indicates an ammeter.

compliance current value (namely a limiting current of the external input) that induces, at least in some cases, the type of switching effect [65,66]. For example, Jeong *et al.* [65] have observed that the electroforming of a Pt/TiO₂/Ti structure with a lower compliance current (<0.1 mA) results in a bipolar hysteresis, while a higher compliance current (1–10 mA) leads to unipolar resistance switching (the meaning of these two types of hysteresis will become clear in a moment). A detailed experimental study of the electroforming process in TiO₂ was reported recently [67]. The dielectric breakdown in SiO₂ was investigated in [68]. A deficiency of oxygen atoms along the breakdown path was observed, caused by large currents through the percolation path. As a result, it is believed that the local energy gap could have collapsed after the removal of oxygen atoms with consequent rearrangement of local atomic structure [68].

Let us now consider the different types of resistance switching reported in the literature. Figure 14 illustrates the three most general behaviors: bipolar, unipolar and irreversible. Such a classification of I – V curves can be used in addition to the categorization in terms of the crossing type at the origin suggested in Section 2.2. Below we will consider these three cases in more detail.

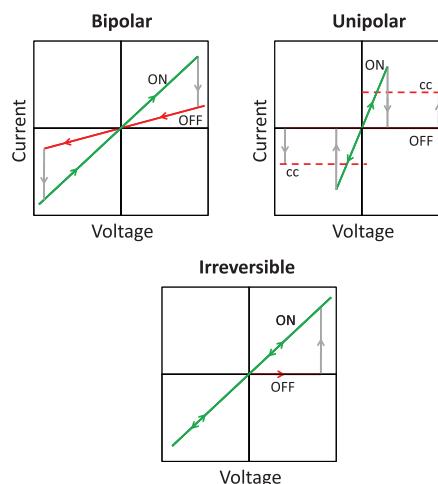


Figure 14. Three commonly observed types of I – V curves in a voltage sweeping experiment showing bipolar switching, unipolar switching and irreversible switching. The term “cc” means “compliance current” (see text for details).

3.2.1. Bipolar resistance switching

In the case of *bipolar switching*, both voltage polarities are required to switch a device from a low-resistance state (ON) to a high-resistance state (OFF) and back. A typical shape of I - V curve in the case of bipolar switching as shown in Figure 14 provides just a general topology of these curves. Experimentally measured loops depend on both the system type and measuring conditions, and can thus be quite different from this ideal topology. In the bipolar case, the hysteresis process often is of a threshold type: while a high applied voltage is needed to change the device state, at low applied voltages the resistance of the device remains unchanged. This is very often associated with ionic transport and electrochemical reactions, even though the exact experimental cause is not always clear and may originate from a combination of effects [52]. Moreover, we note that in most cases the switching has a gradual character: the change of, say, resistance of a device proceeds continuously (not as an abrupt jump between two limiting values). Such a property is promising for multi-state memory in which a single memory cell can store several bits of information.

We now consider several examples of bipolar switching observed in devices fabricated from different materials. Our first example is a titanium dioxide (TiO_2) thin film sandwiched between metal electrodes (see Figure 15). This resistive feature has been known since 1968 [33]. Recently, however, the switching behavior of this binary oxide has been explained within the context of a memristive model [11,18]. In the case of $\text{Pt}/\text{TiO}_2/\text{Pt}$, it was suggested that the switching involves changes in the electronic barrier at the Pt/TiO_2 interface induced by drift of oxygen vacancies under an applied electric field. When vacancies drift towards the interface, they create conducting channels that short-circuit the electronic barrier. When vacancies drift away from the interface, they eliminate these channels, restoring the original electronic barrier [11]. This explanation, however, has recently been challenged [12]. In this alternative explanation, the conductivity change of TiO_2 is associated with an electrochemical reduction of Ti^{IV} oxide to the much more conductive Ti^{III} oxide, analogous to a solid-state redox reaction [12]. A similar reaction-based mechanism taking place at the interface between Pt and TiO_2 was considered by Jeong *et al.* [69]. They [69] state that the electrochemical reactions modulating the Schottky barrier height at the interface play the dominant role in the device behavior.

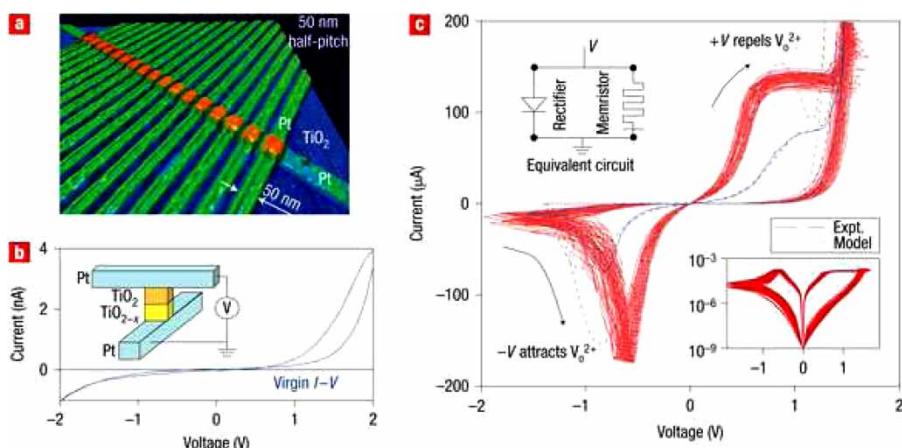


Figure 15. (a) An AFM image of 17 nano-crosspoint devices containing a 50-nm thick TiO_2 thin film sandwiched between Pt electrodes. (b) The initial (before electroforming step) I - V curve of the device and experimental scheme. (c) Experimental and modeled I - V curves. Reprinted with permission from Macmillan Publishers Ltd: Nature Nanotechnology 3, pp. 429–433, 2008, Copyright © (2008) [11].

Irrespective of the basic physical mechanism at play, this material demonstrates promising characteristics for future ultra-high density memory applications such as fast read/write times (~ 10 ns), high ON/OFF ratios ($\sim 10^3$), suitable range of programming voltages, and possibility to fabricate small-sized cells. The latter, in particular, is viewed as an advantage in fabricating high-density neuromorphic circuits, namely circuits that simulate neurological functions, because of the possibility to reach structure densities comparable to (or even larger than) the density of neurons and synapses (connections among neurons) in the human brain. We will come back to this type of applications in Section 7.2.1.

An interesting TiO_2 -based device is a flexible memristive system as presented in [70]. This device was fabricated on an HP laser-jet transparency using an inexpensive room temperature solution processing. The device demonstrates ON/OFF ratios larger than 10^4 , about 10^6 s memory storage potential and the ability to operate after being physically flexed 4000 times [70]. Multiple consecutive mechanical deformations of the device lead to an increase in resistance in both ON and OFF states, while keeping ON/OFF ratios almost unchanged (see Figure 16). Such devices have the potential for use in flexible lightweight portable electronics [70].

In nanoionics-based memories [52], a memory cell is composed of a couple of metal electrodes separated by a thin film of insulating material playing the role of solid-state electrolyte, such as an oxide NiO [40], SiO_2 [71,72], $SrTiO_3$ [73] or higher chalcogenides – Ag_2S [50], Ge_xSe_{1-x} [74,75]. One of the electrodes is made of a relatively inert metal (such as Pt) and the other electrode is electrochemically active (e.g. Ag or Cu). A negative bias applied to the inert electrode forces a flow of metal ions in the electrolyte (originating from the now-positive active electrode) toward the inert metal electrode. After a short period of time, these ions compose a filament that connects two metal electrodes. This filament dramatically reduces the resistance of the cell. Applied bias of the opposite polarity drifts the active electrode ions in the opposite direction destroying the filament. The basic scheme of operation of such a cell is shown in Figure 17. Such a memory technology is often called programmable metallization cell (PMC) [74] or electrochemical metallization cell (ECM) or CBRAM (conductive-bridging random access memory) [76]. Figure 17 shows a pinched $I-V$ hysteresis curve observed in $Cu-SiO_2$ -based electrochemical metallization memory cells. This figure also shows dynamics of filament formation.

Recently, nanoionic resistive switching in silicon-based materials was experimentally demonstrated [53–55]. In these experiments, amorphous-Si is used as the switching medium, one of

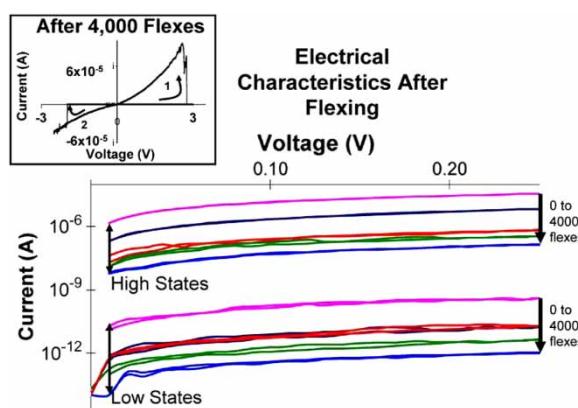


Figure 16. $I-V$ curves of flexible memristive system after 0, 100, 2000, 3000 and 4000 flexes. Inset: switching curve after 4000 flexes. Reprinted with permission from N. Gergel-Hackett *et al.*, IEEE Transactions on Electron Device Letters 30, pp. 706–708, 2009 [70]. Copyright © (2009) by the IEEE.

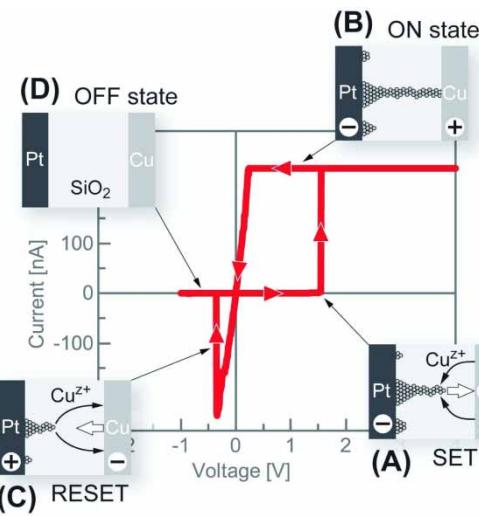


Figure 17. Current–voltage characteristic of a Cu/SiO₂/Pt electrochemical metallization cell using a triangular voltage sweep. The positive bias current is limited by 250 nA compliance current value. The insets show dynamics of metallic filament formation. Reprinted with permission from C. Schindler *et al.*, Applied Physics Letters 94, p. 072109, 2009 [72]. Copyright (2009), American Institute of Physics.

the electrodes is metallic (typically Ag) and the other electrode is p-type Si. In this case, the hysteresis is explained by the formation of conductive filaments consisting of Ag particles inside the amorphous-Si. A filament growth is a step-by-step process by which a new Ag particle hops into a new trapping site. Such devices are CMOS (complementary metal oxide semiconductor) compatible and offer promising characteristics such as fast writing (<10 ns), reasonable endurance (>10⁵ cycles) and good retention time (~7 years). Moreover, a high-density crossbar array based on such materials was fabricated [55]. In Figure 18 we show an image of this array as well as the *I*–*V* characteristics of a single cell. Such a structure exhibits a symmetric bipolar switching together with a high ON/OFF conductance ratio.

The mechanism of hysteresis in perovskite oxide films Pr_{0.7}Ca_{0.3}MnO₃ (PCMO) was recently investigated [49,77]. These materials show a bipolar switching as we demonstrate in Figure 19. Nian *et al.* [49] suggest an oxygen vacancies diffusion model to explain the hysteresis phenomenon. Within this model, a switching pulse results in a pileup of oxygen ions near metal electrodes thus changing the resistance. Moreover, it is proposed that this mechanism can explain the resistance switching in binary transition metal oxides and other complex oxides as well. Rozenberg *et al.* [77] suggest a discrete vacancies diffusion model. Their study underlines the important role of highly resistive dielectric–electrode interfaces and shows a qualitative agreement with experimental data.

Bipolar resistance switching is also observed in structures containing organic materials (see [56,57,78]), although its origin is not yet fully understood. In particular, Stewart *et al.* [56] have demonstrated that hysteresis characteristics of different molecular materials sandwiched between Pt and Ti electrodes are very similar, suggesting a molecular-independent hysteresis mechanism. Moreover, they have shown that in a structure with similar (Pt) electrodes, the switching becomes irreversible. Stewart *et al.* [56] suggest that a possible reason could be related to formation of electromigration-induced filaments, or incomplete electrochemical reaction of one electrode and the molecular monolayer [56].

Cai *et al.* [78] have reported a reversible hysteresis in nanoscale thiol-substituted oligoaniline molecular junctions. In their experiments, the switching occurs at ±1.5 V threshold voltage, with

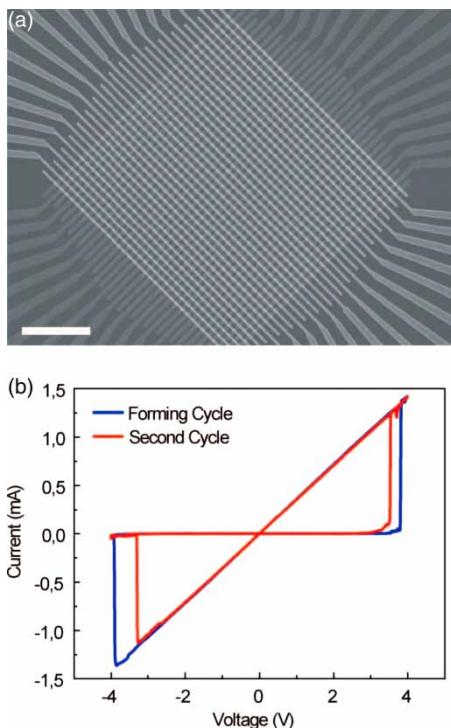


Figure 18. (a) SEM image of Si-based memristive crossbar. (b) Switching I – V characteristics of an individual cell. Reprinted with permission from S.H. Jo *et al.*, Nano Letters 9, pp. 870–874, 2009 [55]. Copyright (2009) American Chemical Society.

a high-to-low conductance ratio of up to 50, and high-state storage times much longer than 22 h. In Figure 20, we show selected results of their measurements. Cai *et al.* have concluded that reversible bistable switching in their experimental system is an inherent molecular phenomenon, most likely arising from a concerted shift in charge delocalization and molecular conformation when the applied voltage across the molecular junction exceeds a critical threshold value [78].

3.2.2. Unipolar resistance switching

The *unipolar switching* (see Figure 14) is considered by some authors to be based on a thermal effect [52]. The switching is defined by two voltages: the set (driving OFF → ON transition) and the reset (driving ON → OFF transition) voltages (see Figure 14). The set voltage is always higher than the reset one. Physically, in samples with this type of hysteresis, a weak conducting filament with a controlled resistance is formed in the electroforming process. During the reset operation, this filament is partially destroyed because of the large amount of heat released, similarly to a traditional household fuse [52]. In the set operation, the filament is reconstructed again. The nanoscale filament formation was recently observed experimentally in materials such as TiO₂ [79] and NiO [80].

In Figure 21, we show examples of unipolar switching behavior observed in metal/binary-transition-metal oxides/metal structures based on Fe₂O₃ and NiO [38]. In order to clarify the hysteresis mechanism, Inoue *et al.* [38] have studied several different structures, in particular, varying a top Pt electrode area. They found that in the ON state the current does not depend on the area of the top electrode, while in the OFF state the current is proportional to the top electrode area. Based on these findings, they have suggested a “faucet” model of resistance switching in

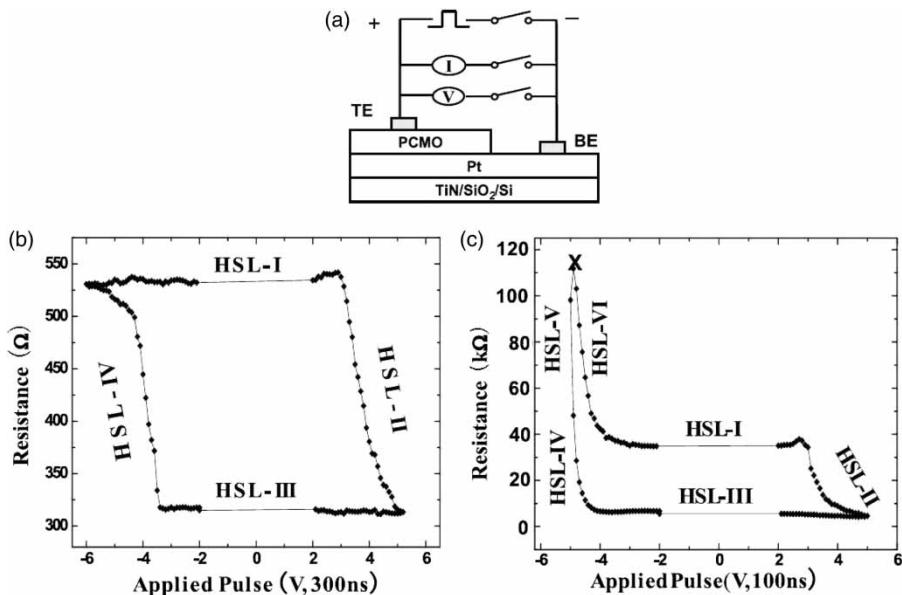


Figure 19. (a) Schematic of the experimental setup to observe resistive switching with perovskite oxide films PCMO. The top electrode (TE) is made of Ag, while the bottom electrode (BE) is made of Pt films on TiN/SiO₂/Si substrate. (b,c) Hysteresis switching loops (HSL) were measured by applying a sequence of pulses with a constant voltage step. In (b), the PCMO film is grown in an oxygen environment, while in (c) the environment is oxygen-free. Reprinted figure with permission from Y.B. Nian *et al.*, Physical Review Letters 98, p. 146403, 2007 [49]. Copyright © (2007) by the American Physical Society.

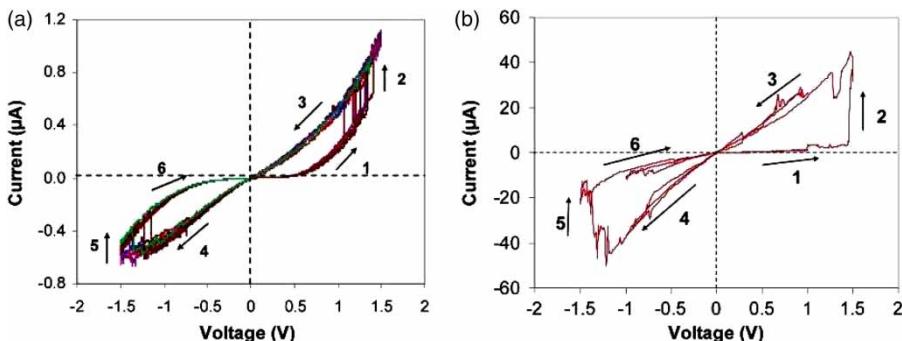


Figure 20. (a) Reversible switching behavior in a Au-SAM-Pd molecular junction, and (b) Pd-SAM-Pd molecular junction. Here, SAM stands for self-assembled monolayer of oligoaniline dimers. Reprinted with permission from L. Cai *et al.*, Nano Letters 5, pp. 2365–2372, 2005 [78]. Copyright (2005) American Chemical Society.

which an “electric faucet” opens/closes in one or both interfaces between metal electrodes and oxide when the device switches into the ON/OFF state [38]. However, a complete understanding of this effect is still lacking.

Our next example is the unipolar switching in a polymer material poly(3,4-ethylene-dioxythiophene):polystyrenesulfonate, commonly referred to PEDOT:PSS. The hysteresis mechanisms in PEDOT:PSS are still generally unknown, and those suggested in the literature are highly speculative [81]. This material, in fact, can exhibit all types of switching behavior shown in Figure 14, depending on the type of material electrodes used. Moller *et al.* [82] have observed

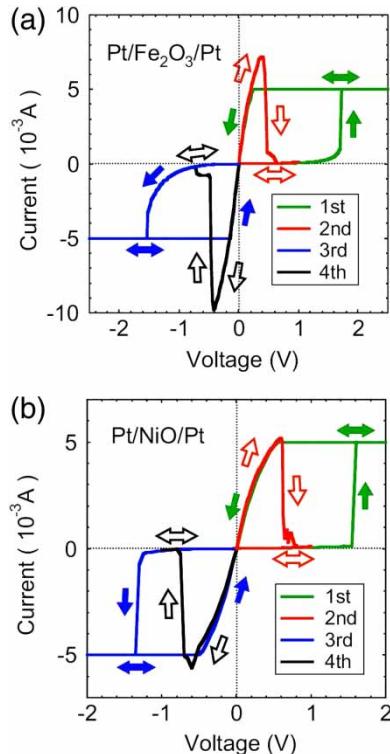


Figure 21. I - V characteristics of (a) Pt/Fe₂O₃/Pt and (b) Pt/NiO/Pt devices showing unipolar switching. The oxide thickness is 100 nm (Fe₂O₃) and 60 nm (NiO). Reprinted figure with permission from I.H. Inoue *et al.*, Physical Review B 77, p.035105, 2009 [38]. Copyright © (2009) by the American Physical Society.

an irreversible switching in a Au/PEDOT:PSS/Si p-i-n diode structure. In experiments with ITO/PEDOT:PSS/Al devices [83], bipolar switching characteristics were observed. Finally, in recent papers [81,84] studying Au/PEDOT:PSS/Au and Al/PEDOT:PSS/Al structures, respectively, the unipolar switching was reported.

We show I - V switching characteristics of a Au/PEDOT:PSS/Au device [81] in Figure 22. In this plot, the sweep sequence is indicated by the alphabets. The probable mechanism in this case is the forming and rupture of conductive paths, presumably related to the oxidation and reduction of the PEDOT:PSS film [81]. A resistive ratio of 10^3 and no significant degradation over 10^4 s under continuous readout testing were found.

3.2.3. Irreversible resistance switching

The third type of switching, the *irreversible switching*, is of little interest from the point of view of memristive systems since, in this case, the initially fabricated device can only be switched toward a different state irreversibly (only in one direction). However, it is evident that these devices are memristive since the resistance at any given moment of time is defined by the history of the system (e.g. voltages applied to the device in the past). Of course, some typical features of memristive systems such as repeatable hysteresis loops cannot be observed with such devices.

Systems with irreversible resistance switching represent a simple, non-volatile, WORM (write-once-read-many-times) memory. Very often, this type of memory is observed in organic devices

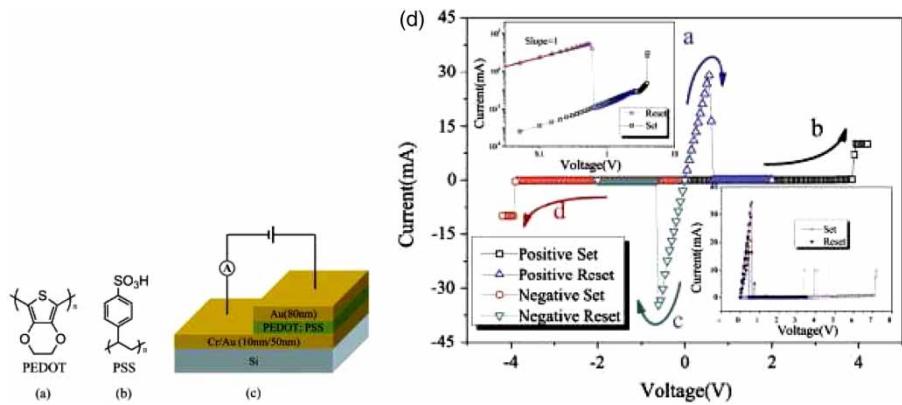


Figure 22. Structure of (a) PEDOT and (b) PSS complexes. (c) Schematic of experimental setup. (d) Unipolar switching characteristics of Au/PEDOT:PSS/Au memory devices. Reprinted from Organic Electronics 10, X. Liu *et al.*, pp. 1191–1194, Copyright (2009) with permission from Elsevier [81].

[56,82,85,86]. Figure 14 shows a schematic of irreversible switching loop when the device initially fabricated in the OFF state is switched into the ON state. This type of behavior is indeed observed experimentally [86]. Figure 23 shows an example of I – V characteristics of a flexible polymer device based on the conjugated copolymer 9,9-dihexylfluorene and benzoate with chelated europium thenoyl trifluoroacetone ligand complex (P6FBEu). This device shows an irreversible

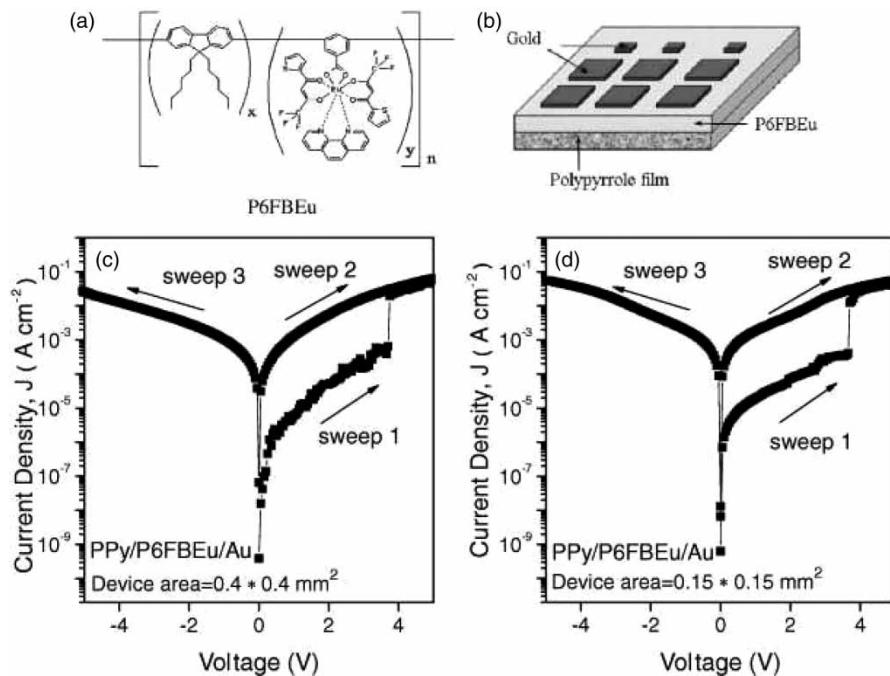


Figure 23. Flexible WORM memory device demonstrating irreversible OFF → ON switching. (a) Molecular structure of P6FBEu polymer. (b) Schematics of memory cells consisting of a thin film ($\sim 50\text{nm}$) of P6FBEu located between a flexible PPy substrate and gold top electrodes. (c,d) I – V characteristics of cells with different size of gold electrodes. Reprinted from Organic Electronics 8, L. Li *et al.*, p. 401, Copyright (2007) with permission from Elsevier [86].

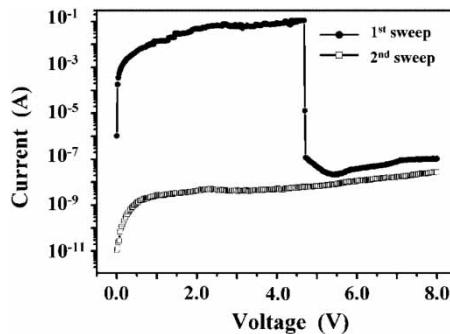


Figure 24. Irreversible resistance switching in ITO/HCuPc/Ti device. S. Choi *et al.*, Advanced Materials, 2008, 20, pp. 1766–1771 [85]. Copyright © Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.

OFF → ON switching at a bias of ~ 4 V, ON/OFF current ratio of 200 and stability of the ON and OFF states up to 10^6 reading cycles at 1 V read voltage [86]. Baikalov *et al.* [86] have suggested a charge-migration mechanism to explain the hysteresis.

Moreover, the different direction of switching, when a device fabricated in ON state is switched into an OFF state, is also possible [56,82,85]. For example, in Figure 24, we report I – V curves of indium–tin–oxide/hyperbranched copper phthalocyanine polymer/Ti (ITO/HCuPc/Ti) device [85]. Such a device shows an irreversible ON → OFF switching behavior at approximately 4.75 V with a titanium top electrode, and at 2.5 V with a gold electrode instead of Ti [85]. Moreover, the authors of this work report a stability of ON and OFF states during 10^{12} , 1 V amplitude read pulses, and a stability of both states after 1 year of storing. The switching into the OFF state is explained by rupture of filaments which takes place when a high voltage is applied [85]. However, the origin of the filaments in a virgin device is not elucidated and more work in this direction is thus highly desirable.

3.2.4. Models of resistance switching devices

Several models of resistance switching have been proposed recently [18,49,87–96] including molecular dynamics simulations approach [97]. Some of them were implemented in SPICE (Simulation Program with Integrated Circuit Emphasis) [98–103]. Here, we consider several models of memristive devices [18,92,94] that elucidate the resistance switching from the point of view of memristive theory [16].

A simple model of titanium dioxide memristive system was suggested by Strukov *et al.* [18]. In this work, a semiconductor film of thickness D sandwiched between two metal electrodes is modeled using two variable resistors connected in series (see Figure 25(a)). These resistors represent two spatial regions with a high and low concentration of dopants. The application of the external bias $V(t)$ causes charged dopants to drift, thus moving the boundary between the regions. This process is described by the equations

$$V(t) = \left(R_{\text{ON}} \frac{w(t)}{D} + R_{\text{OFF}} \left[1 - \frac{w(t)}{D} \right] \right) I(t), \quad (63)$$

$$\frac{dw(t)}{dt} = \mu \frac{R_{\text{ON}}}{D} I(t). \quad (64)$$

Here, μ denotes the ion mobility. Equation (64) gives

$$w(t) = \mu \frac{R_{\text{ON}}}{D} q(t) \quad (65)$$

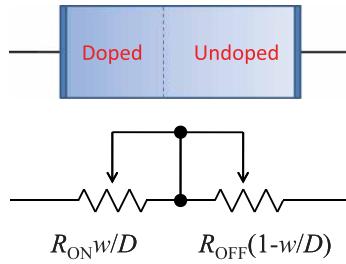


Figure 25. Two variable resistors model of a resistance switching device: R_{ON} and R_{OFF} are variable resistors describing doped and undoped regions, respectively.

which, when substituted into Equation (63), in the limit of $R_{ON} \ll R_{OFF}$, gives the memory resistance

$$R_M(q) = R_{OFF} \left(1 - \frac{\mu R_{ON}}{D^2} q(t) \right). \quad (66)$$

The latter equation describes an ideal current-controlled memristor (see Section 2.4). We note, however, that the derivation of Equation (66) is based on several assumptions such as current-controlled drift, constant mobility and does not account for the boundary conditions. Many of these assumptions may, in fact, not hold in the actual experimental conditions. Moreover, experimentally observed curves actually correspond to a memristive system (in the sense of Equations (27) and (26)) rather than to an ideal memristor. The model of Strukov *et al.* [18] was later improved by Joglekar and Wolf [94], who introduced a function that ensures no drift at the boundaries. Their model is summarized in Table 5.

Several later papers by Hewlett-Packard [91,104,105] report on further developments of resistance switching theory for TiO_2 devices. A model of threshold-type switching is suggested in [104]. Within this model, the ion drift in a periodic potential is facilitated when the potential is significantly tilted by the applied electric field. Pickett *et al.* [105] have considered a model that involves an exponential dependence of the switching time on the device current. A coupled drift-diffusion equations approach to ionic and electronic transport was instead considered in [91].

We have recently introduced [92] a different model of memristive system that takes into account a threshold-type switching and boundary conditions (imposed on the memristance of the system). The former is frequently observed in the bipolar resistance switching devices considered in Section 3.2.1. This model is based on the assumption that the rate of the resistance change is

Table 5. Nonlinear drift model of a memristive device [94]. Here, $F(y)$ is the window function such that $F(0) = F(1) = 0$. This condition ensures no drift at the boundaries. Joglekar and Wolf [94] suggest a family of window functions $F_p(y) = 1 - (2y - 1)^{2p}$, where p is a positive integer number.

Physical system	Solid state memristive device
Internal state variable(s)	Doped region size, $x = w$
Mathematical description	$V = \left(R_{ON} \frac{x}{D} + R_{OFF} \left[1 - \frac{x}{D} \right] \right) I$ $\frac{dx}{dt} = \mu \frac{R_{ON}}{D} I(t) F\left(\frac{x}{D}\right)$
System type	First-order current-controlled memristive system

Table 6. Threshold model of a memristive device [92]. Here, $x = R_M$ is the resistance of the memristive system and $\theta(\cdot)$ is the step function indicating that the memristance acquires the limiting values R_{\min} and R_{\max} . The parameters α and β are constants defining the memristance rate of change below and above the threshold voltage V_T ; V is the voltage across the system.

Physical system	Solid state memristive device
Internal state variable(s)	Resistance, $x = R_M$
Mathematical description	$I = x^{-1}V$ $\frac{dx}{dt} = (\beta V + 0.5(\alpha - \beta)[V + V_T - V - V_T])$ $\times \theta(x - R_{\min})\theta(R_{\max} - x)$
System type	First-order voltage-controlled memristive system

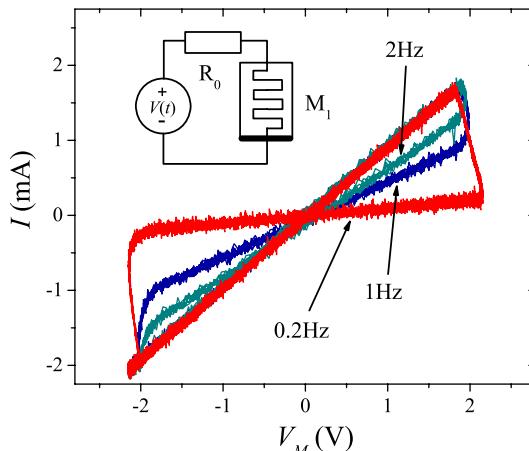


Figure 26. Frequency-dependent I - V curves obtained using the model presented in the Table 6 preprogrammed into a memristor emulator (see Section 7.2.5). These particular curves were obtained for $\alpha = 0$. Such a choice allows memristance change only when the applied voltage magnitude is above the threshold voltage $V_T = 1.75$ V in the present case. Reprinted with permission from Y.V. Pershin and M. Di Ventra, IEEE Transactions on Circuits and Systems I 57, p. 1857, 2010 [106]. Copyright © (2010) by the IEEE.

small below a threshold voltage V_T and fast above V_T , and was inspired by the experimental work of [18]. The mathematical formulation of this model is provided in Table 6.

The model from Table 6 was used to describe learning of simple biological organisms (see Section 7.2.3) as well as in several other publications [14,106,107]. In Figure 26, we demonstrate I - V curves of a memristive system described by equations shown in Table 6 and obtained using a memristor emulator (see Section 7.2.5). Note the similarity of these curves with those, e.g. in Figure 18.

3.3. Phase-change memory cells

Phase-change memory cells employ phase-change materials that can exist in at least two different phases: amorphous and crystalline. These two different phases are characterized by distinctive physical properties such as resistivity, optical reflectivity, etc. The idea of phase-change

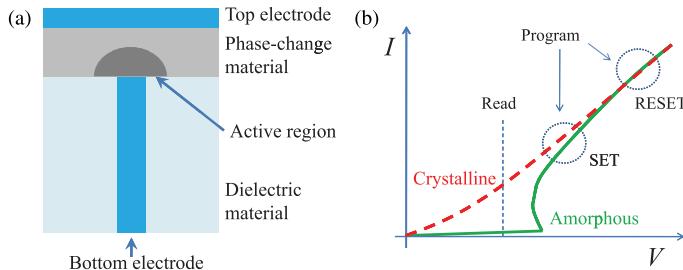


Figure 27. (a) Schematic cross section of a phase-change memory cell. (b) Shape of typical I - V curves for crystalline and amorphous phases of phase-change materials.

memory (also known as PCM, PRAM, PCRAM, Ovonic Unified Memory, Chalcogenide RAM and C-RAM) relies on abilities to electrically induce switching between amorphous and crystalline states by the Joule heating due to the current flow and to probe the state of the cell by measuring its resistance. Since both states are stable, no energy is required to store data. Chalcogenides constitute most of the phase-change materials. They include Ge–Te [108], GeSeTe₂ [109], Ge₂Sb₂Te₅ [110], AgSbSe₂ [111], Sb–Se [112], Ag–In–Sb–Te [113]. Here, we would like to focus only on memristive aspects of a phase-change memory cell that is a unit element of phase-change memory. Additional information about properties of phase-change materials and phase-change memory technology can be found in recent review papers [114–116].

Figure 27(a) shows schematically the so-called contact-minimized (“mushroom”) phase-change memory cell [115]. It consists of a phase-change material sandwiched between large-area (top) and small-area (bottom) electrodes. The active (switchable) region of the phase-change material is located right above the bottom electrode where the current density is high. The cell design and operation regime normally do not allow the active region to contact the top electrode. Typical experimentally measured I - V curves [117] of phase-change materials are shown schematically in Figure 27(b). The switching from crystalline (low-resistive) to amorphous (high-resistive) state (RESET operation) is performed by melting and quenching the material quickly enough. In this case, the material solidifies in the amorphous state. The switching from amorphous to crystalline state (SET operation) occurs when the material is heated above its crystallization temperature (which is below its melting temperature) for sufficiently long time. SET and RESET operations are achieved by *unipolar* pulses of appropriate amplitude and duration. Moreover, we note that the switching from amorphous (highly resistive) to crystalline state would not be possible without a threshold-type increase of conductivity above a certain strength of the applied electric field (see Figure 27(b)). Such an effect is not yet well understood and is currently related to the interplay between impact ionization and carrier recombination [115,117].

Theoretical and numerical modeling [117–121] of phase-change memory cells was previously reported focusing on either the total device operation or just some particular processes within a device (such as crystallization dynamics). In Table 7, we summarize a memristive model of phase-change material cell based on the idea suggested by Sonoda *et al.* [121]. This model employs three rate equations to describe the following factors: temperature of active region, crystallization dynamics, and the threshold behavior of conductivity of amorphous state. From the electrical point of view, the cell can be represented as three resistors R_{bottom} , R_{gst} and R_{top} connected in series [121]. Here, R_{gst} describes variable resistance of active region, while R_{bottom} and R_{top} the resistances below and above the active region, respectively (see Figure 27(a)). In Table 7, we provide the memristive model with respect to the voltage drop on R_{gst} as in [121]. As the total cell consists of only resistive elements, it is memristive [16]. We also note that phase-change memory cells have potential for multi-state applications [122–125].

Table 7. Memristive model of phase-change memory cells. Here, T_b is the temperature of active layer and C_a is the amorphous ratio that changes between 0 and 1. The complete (cumbersome) expression for $G(x_2, x_3, V_{\text{gst}})$ and $f_2(x_1, x_2)$ can be read from [121]. P_t is the dissipated electric power [121], T_0 is the temperature of environment, R_t is the total thermal resistance, C_t is the thermal capacitance, V_t is the threshold voltage (we control G by voltage instead of current as in [121]) and τ_f is the switching time.

Physical system	Phase-change memory cell
Internal state variable(s)	Temperature, $x_1 = T_b$ Amorphous ratio, $x_2 = C_a$ Switching variable, $x_3 = F$
Mathematical description	$I = G(x_2, x_3, V_{\text{gst}})V_{\text{gst}}$ $\frac{dx_1}{dt} = C_t^{-1} \left(P_t(x_2, x_3, V_{\text{gst}}) - \frac{x_1 - T_0}{R_t} \right)$ $\frac{dx_2}{dt} = f_2(x_1, x_2)$ $\frac{dx_3}{dt} = -\frac{x_3 - \theta(V_{\text{gst}} - V_t)}{\tau_f}$
System type	Third-order voltage-controlled memristive system

3.4. Metal–insulator phase transition memristive systems

In strongly interacting electron materials, a complex interplay between charge, lattice and spin degrees of freedom can result in the resistance switching effect [47,126]. Driscoll *et al.* have recently used a vanadium dioxide-based device to demonstrate memristive [36] and memcapacitive behavior [15] of systems comprising this oxide. In both types of experiments, the behavior is driven by the MIT of this material [127–134]. Here, we focus on the memristive behavior. The memcapacitive behavior of VO_2 is discussed in Section 4.3.2.

Using the experimental setup schematically shown in Figure 28 where a film of VO_2 , deposited on a sapphire substrate, is connected to two electrodes, the memristive behavior was demonstrated as follows. The operation temperature was selected near the onset of the phase transition (340 K)

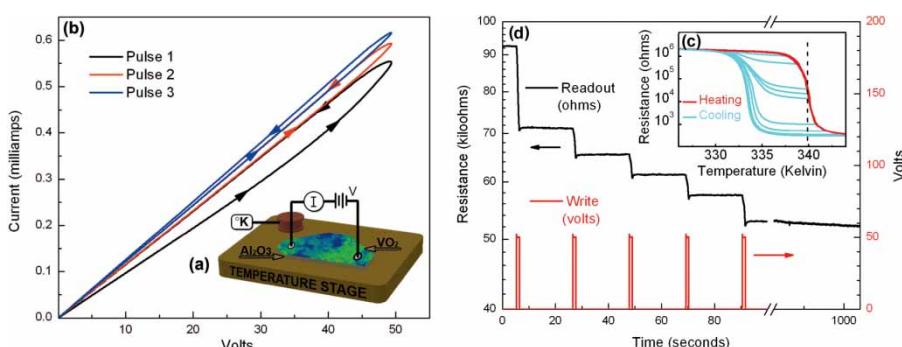


Figure 28. (a) Phase-transition-driven memristive device. (b) Hysteretic I – V curves under application of three ramped voltage pulses. The ramp used for each pulse is 50 V in 5 s. (c) The insulator–metal transition in VO_2 device. (d) Analog information storage in memristive VO_2 film: resistance changes in steps with each 50 V pulse. Reprinted with permission from T. Driscoll *et al.*, Applied Physics Letters 95, p. 043503, 2009 [36]. Copyright (2009), American Institute of Physics.

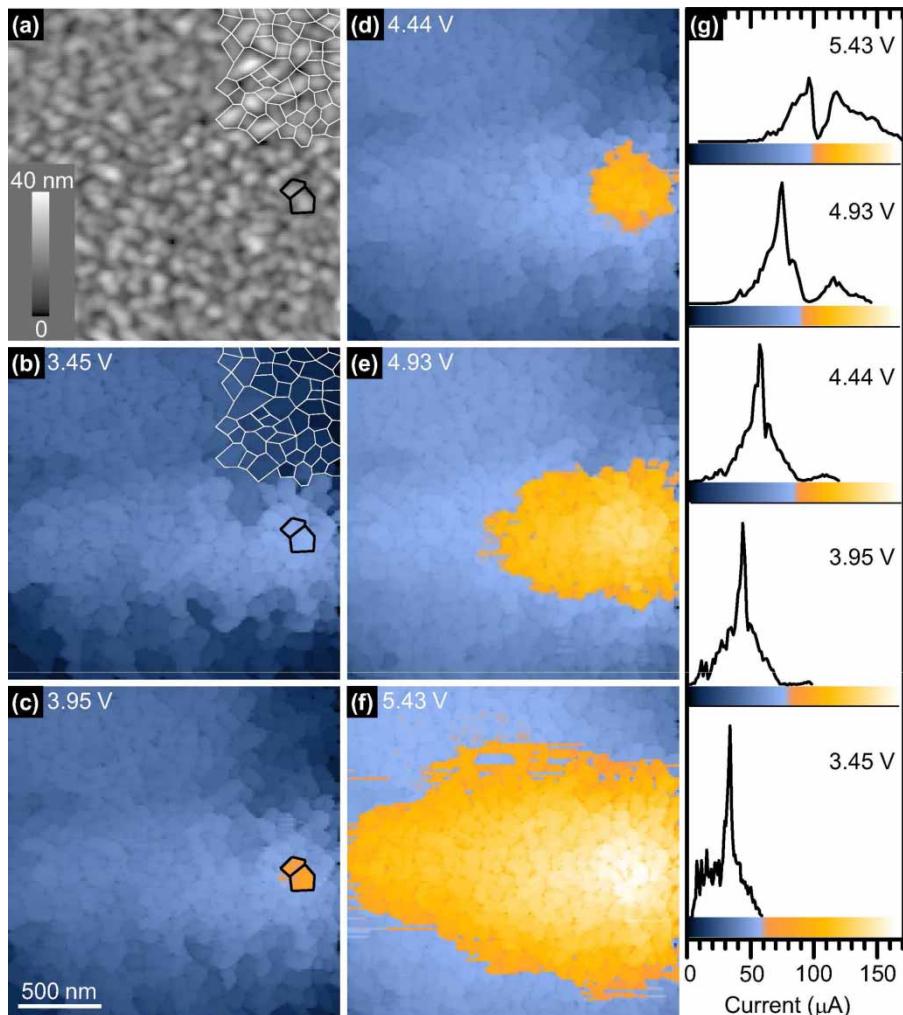


Figure 29. (a) Conducting AFM topography of a VO_2 surface. (b–f) Current maps at different biases showing a metallic paddle (yellow color) increasing in size with bias. (g) Current distributions at different biases showing the transition between insulating and metallic states. Reprinted with permission from J. Kim *et al.*, Applied Physics Letter 96, p. 213106, 2010 [136]. Copyright (2010), American Institute of Physics.

where properties of VO_2 are very sensitive to temperature changes. High-amplitude voltage pulses (50 V) were used to increase VO_2 temperature for short periods of time, thus promoting the MIT. Triggered by each pulse, nanoscale metallic regions develop within the insulating host, increasing in number and size to form a percolative transition [135] (see Figure 29 for an AFM image of these metallic regions).

Figures 28(b) and (d) shows experimental results when ramping and step pulses are applied. The experimentally observed memristive properties of vanadium dioxide are related to power dissipated in VO_2 [36]. Therefore, in such a device $f(x, I, t) \propto I^2$ and it can be classified as an even-function current-controlled memristive system. Consequently, the resistance rate of change does not depend on the applied signal polarity and can be switched only in one direction. Nonetheless, memory storage duration of more than several hours and the possibility to store up to 2^{10} resistance values

in a single device have been reported [36], thus making this system a good model exhibiting multi-bit information storage.

We now introduce a mathematically transparent model of vanadium dioxide memristive system (the models summary is given in Table 8). It can be developed assuming that the hysteresis in R - T curves is well defined [137–139]. This is a reasonable approximation taking into account that the resistance drift at a fixed temperature in the transition region is not very strong [134]. The local temperature T of the vanadium dioxide material can then be described by a heat transfer equation (similar to the heat equation of the thermistor (32))

$$C_h \frac{dT}{dt} = R_M I^2 + \delta(T_{\text{stage}} - T), \quad (67)$$

while the equation for the resistance dynamics can be written as

$$\frac{dR_M}{dt} = \theta[R_M - R_1(T)] \frac{R_1(T) - R_M}{\tau} + \theta[R_2(T) - R_M] \frac{R_2(T) - R_M}{\tau}, \quad (68)$$

where C_h is the heat capacitance, δ the dissipation constant, T_{stage} the temperature of the thermal stage, $\theta[\dots]$ the step function, $R_1(T)$ and $R_2(T)$ ramp up and down $R(T)$ curves, respectively, and τ the resistance relaxation time that can be considered to be much shorter than characteristic thermal times. The first term on the right-hand side of Equation (68) describes a decrease in resistance when temperature increases, and the second term is responsible for the opposite process. As the resistance relaxation time τ is short, Equation (68) represents very fast transition $R_M \rightarrow R_1(T)$ if $R_M > R_1(T)$ and $R \rightarrow R_2(T)$ if $R_M < R_2(T)$. It is clear that, according to Equation (68), R does not change if its value falls inside of the hysteresis loop.

Thus, our description of MIT in VO_2 involves two state variables: the temperature and resistance. The time dependence of state variables is given by Equations (67) and (68). Since the current enters the right-hand-side of Equation (67), our model describes a second-order current-controlled memristive system.

The experimentally measured profile of the hysteresis [15,36] suggests that the functions $R_1(T)$ and $R_2(T)$ can be selected of the same shape displaced by 2Δ , where 2Δ is the hysteresis width. For example, in our numerical simulations of memristive properties of vanadium dioxide shown in Figure 30, we have employed the following profile for $R_1(T)$ and $R_2(T)$:

$$R_1(T) = F(T - \Delta) \quad (69)$$

$$R_2(T) = F(T + \Delta) \quad (70)$$

$$F(x) = \left(\frac{1}{\pi} \arctan \left[\frac{T_0 - x}{\eta} \right] + 0.5 \right) [R_{\max} - R_{\min}] + R_{\min}, \quad (71)$$

where R_{\max} and R_{\min} are asymptotic values of resistance below and above the transition temperature, respectively, T_0 is the average transition temperature and η is the parameter defining the sharpness of the resistance step at the MIT. An example of a hysteresis loop based on Equations (69)–(71) is demonstrated in Figure 30(a). We emphasize that the choice of $R_1(T)$ and $R_2(T)$ given by Equations (69)–(71) is not unique and possibly better fits to experimental curves can be found.

The application of voltage pulses to vanadium dioxide memristive system results in a local heating as demonstrated in Figure 30(b). Since the resistance of the system decreases with each pulse, the amount of heat released due to subsequent pulses increases. This can be clearly seen in the magnitude of the increasing pulses in the $T(t)$ curve. This mechanism permits the progress of the insulator-to-metal transition using pulses of fixed amplitude and width. The resulting $R_M(T)$ steps shown in Figure 30(b) are similar to those observed experimentally [36] (compare with Figure 28).

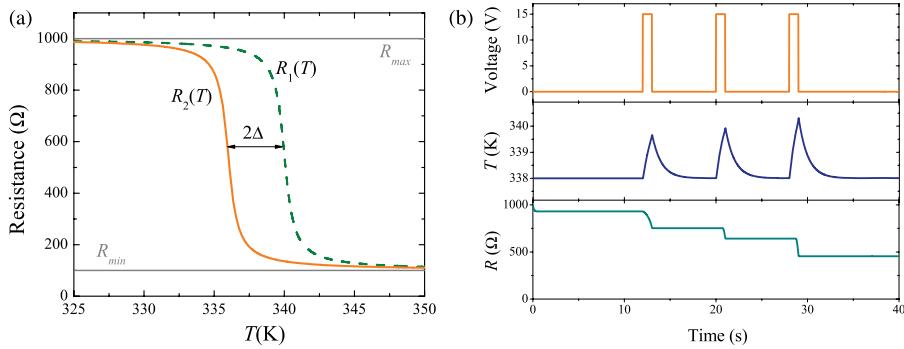


Figure 30. (a) $R - T$ hysteresis loop obtained using Equations (69)–(71). (b) Simulations of vanadium dioxide memristive system response to three 15 V pulses. These plots were obtained using parameter values $R_{\max} = 1000 \Omega$, $R_{\min} = 100 \Omega$, $T_0 = 338 \text{ K}$, $\eta = 0.5 \text{ K}$, $\Delta = 4 \text{ K}$, $R(t = 0) = 1000 \Omega$, $T(t = 0) = 338 \text{ K}$, $\tau = 0.1 \text{ s}$, $C_h = 0.1 \text{ J/K}$, $\delta = 0.1 \text{ J/(s K)}$. No attempt has been made here to perfectly match the experimental curves.

Table 8. Memristive model of vanadium dioxide device. The notation are given in the text, and the functions $R_1(y)$ and $R_2(y)$ are defined by Equations (69) and (70).

Physical system	Vanadium dioxide memristive device
Internal state variable(s)	Temperature and resistance, $x_1 = T$, $x_2 = R_M$
Mathematical description	$V = x_2 I$ $\frac{dx_1}{dt} = C_h^{-1} [x_2 I^2 + \delta(T_{\text{stage}} - x_1)]$ $\frac{dx_2}{dt} = \theta[x_2 - R_1(x_1)] \frac{R_1(x_1) - x_2}{\tau}$ $+ \theta[R_2(x_1) - x_2] \frac{R_2(x_1) - x_2}{\tau}$
System type	Second-order current-controlled memristive system

The reversible resistance switching was recently observed in a manganite $\text{La}_{0.225}\text{Pr}_{0.4}\text{Ca}_{0.375}\text{MnO}_3$ at low temperatures [140]. In this material, the resistance switching effect is explained by a Joule heat-induced transition between charge-ordered insulator and ferromagnetic metal phases [140]. Yan *et al.* show that such a transition is bidirectional and can be uniquely controlled by current pulse pairs [140]. Below 30 K, the system enters a frozen state in which the phase separation is blocked. Under this condition, low- and high-resistance states become nonvolatile. Figure 31 demonstrates that the resistance switching in $\text{La}_{0.225}\text{Pr}_{0.4}\text{Ca}_{0.375}\text{MnO}_3$ has a pronounced frequency dependence. This feature is typical of memristive systems and can be potentially used in multi-state memory. However, we emphasize that the hysteresis in this particular material is not suitable for room-temperature applications.

3.5. Spintronic systems

Memory is not necessarily confined to structural or charge properties, but may also arise from the spin degree of freedom. This is particularly an important result in view of the possible development of devices that operate with low dissipation and show high reliability under ac-bias conditions. In the following, we then discuss memory effects in the two major areas of spintronic research: semiconductor [141] and metal [3,142] spintronics.

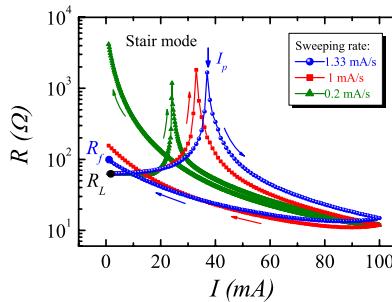


Figure 31. Resistance–current characteristics of a $\text{La}_{0.225}\text{Pr}_{0.4}\text{Ca}_{0.375}\text{MnO}_3$ device measured under the current sweeping in the stair mode with different rates as indicated. All curves start with the same initial resistance. The strongest resistance change is observed at the slowest sweeping rate. Reprinted with permission from Z.B. Yan *et al.*, Applied Physics Letters 95, p. 143502, 2009 [140]. Copyright (2009), American Institute of Physics.

3.5.1. Semiconductor spintronic systems

It was shown by Pershin and Di Ventra [17] that memory effects are an intrinsic feature of many semiconductor spintronic systems. These effects have a spin-related origin and, consequently, cannot be observed in spin unpolarized systems. The general idea behind these memory phenomena is as follows. If we consider a structure (such as, for example, a semiconductor/ferromagnet junction) driven by a time-dependent external control parameter (such as applied voltage or current) then, when the external control parameter changes, it takes some time for the electron-spin polarization to adjust to a new control parameter value – typically, the equilibration is governed by electron-spin diffusion and relaxation processes [17]. Within the time scale of this “spin-polarization adjustment”, the system keeps its memory on the past dynamics. In addition, when the level of electron-spin polarization influences the resistance of the system, it exhibits memristive behavior.

As an example, let us consider current flowing through a semiconductor-half-metal (namely, a perfect ferromagnet [144]) junction (see Figure 32(a)) in such a way that the electron flow is directed from the semiconductor into the ferromagnet (this process is called spin extraction). It is known that spin extraction is accompanied by the phenomenon of spin blockade [145] characterized by a saturated I – V curve [143]. Physically, the outflow of majority-spin electrons from the semiconductor leaves a cloud of minority-spin electrons near the junction. This minority-spin cloud can limit the majority-spin current creating a pronounced spin-blockade at a critical current density [145]

$$j_c = eN_0 \sqrt{\frac{D}{2\tau_{sf}}}, \quad (72)$$

where N_0 is the electron density in the semiconductor, D the diffusion coefficient and τ_{sf} the spin-relaxation time.

The time evolution of the electron-spin polarization in a non-degenerate semiconductor can be described by the two-component drift–diffusion model [146]

$$e \frac{\partial n_{\uparrow(\downarrow)}}{\partial t} = \frac{\partial j_{\uparrow(\downarrow)}}{\partial y} + \frac{e}{2\tau_{sf}}(n_{\downarrow(\uparrow)} - n_{\uparrow(\downarrow)}), \quad (73)$$

$$j_{\uparrow(\downarrow)} = \sigma_{\uparrow(\downarrow)} E + eD\nabla n_{\uparrow(\downarrow)}, \quad (74)$$

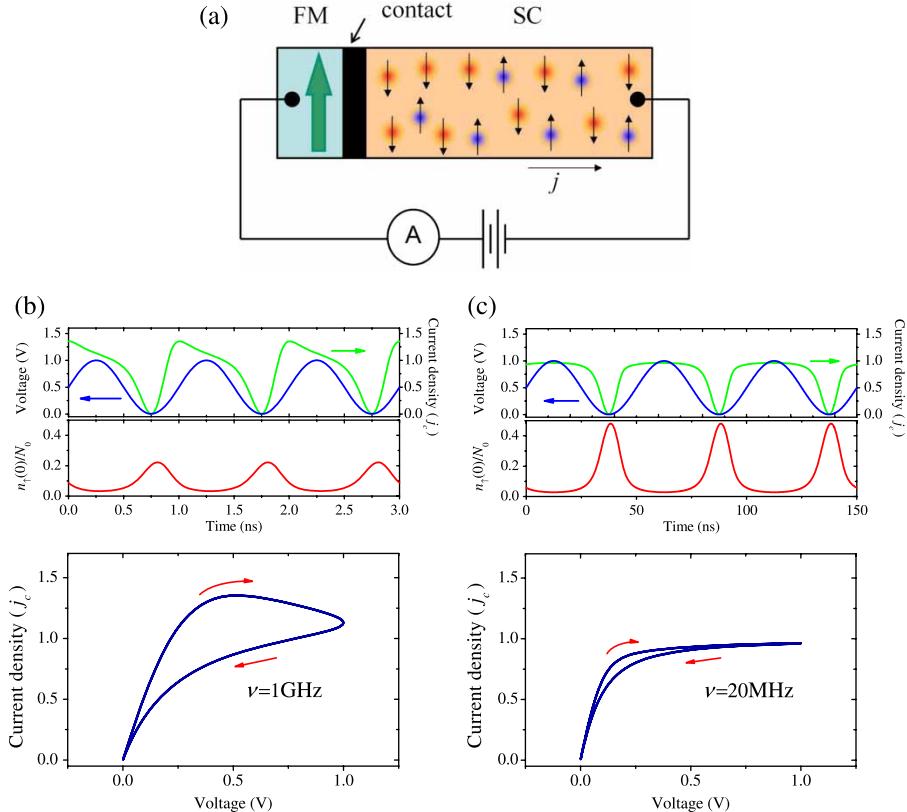


Figure 32. Memristive effects in semiconductor/ferromagnet junctions: (a) schematic representation of the circuit containing an interface between a semiconductor material and a half-metal; (b,c) simulations of ac response of the system. The applied voltages (blue lines) are $V = V_1 + V_2 \sin(2\pi\nu t)$ with $V_1 = V_2 = 0.5\text{ V}$, $\nu = 10^9\text{ Hz}$ in (b) and $\nu = 2 \times 10^7\text{ Hz}$ in (c). In both cases, the current densities (in units of the critical current density, Equation (72)) and spin-up electron densities near the contact (in units of the electron density in the semiconductor) show saturation typical of spin blockade [143]. It is clearly seen that the I - V hysteresis is significantly reduced in the low-frequency case. For more details, see [17].

which are accompanied by an equation for the total voltage drop [145]

$$V = \left[\rho_s L + \rho_c^0 \frac{N_0}{2n_{\uparrow}(0)} \right] j \quad (75)$$

where $-e$ is the electron charge, $n_{\uparrow(\downarrow)}$ the density of spin-up (spin-down) electrons, $j_{y,\uparrow(\downarrow)}$ the corresponding current density, $\sigma_{\uparrow(\downarrow)} = en_{\uparrow(\downarrow)}\mu$ the conductivity, μ the mobility, L the length of the semiconductor region, E the electric field, ρ_s the semiconductor resistivity and ρ_c^0 the contact resistivity at $V \rightarrow 0$.

Clearly, Equations (73) and (75) define a continuum current-controlled memristive system (note that by inverting Equation (75), it can also be redefined as a voltage-controlled memristive system). In such a system, the majority-spin density at the boundary $n_{\uparrow}(0)$ defines (through Equation (75)) the resistance of the device. The details of the memristive model of semiconductor/half-metal junctions (in the assumption of constant electron density) is summarized in Table 9. The differential equation for the continuous state variable $X = n_{\uparrow}(y, t)$ (y is the direction perpendicular to

Table 9. Memristive model of transport through a semiconductor/half-metal junction. It is assumed that the total electron density in the semiconductor is constant, i.e. $n_{\uparrow} + n_{\downarrow} = N_0$. Correspondingly, the electric field in the semiconductor region is homogeneous. The boundary conditions for X follow from the equations $j_{\uparrow}(0) = j$ and $j_{\uparrow}(\infty) = j/2$.

Physical system	Semiconductor/half-metal junction
Internal state variable(s)	Density of spin-up electrons, $X(y, t) = n_{\uparrow}(y, t)$
Mathematical description	$V = \left[\rho_s L + \rho_c^0 \frac{N_0}{2X(0, t)} \right] j$ $\frac{\partial X}{\partial t} = \frac{j}{eN_0} \frac{\partial X}{\partial y} + D \frac{\partial^2 X}{\partial y^2} + \frac{N_0 - 2X}{2\tau_{sf}}$
System type	Continuum current-controlled memristive system

the interface) should be solved with the boundary conditions specified in the caption of Table 9. In Figure 32(b) and (c) we show a numerical solution of the above equations with appropriate boundary conditions [17]. The hysteresis loops demonstrate typical frequency behavior for memristive systems.

In addition to the above results, in certain semiconductor spintronic systems, spin memory effects can be observed directly in the transverse voltage. For example, this occurs in spin Hall effect systems [147,148] with an inhomogeneous electron density in the direction perpendicular to the direction of main current flow [10]. Figure 33 shows transverse voltage hysteresis loops that demonstrate typical memristive behavior: non-linear dependence at low frequencies, pronounced hysteresis at higher frequencies and hysteresis collapse at very high frequencies [10]. The physical origin of this effect is similar to what we have discussed above: the time it takes for the electron-spin polarization to relax to its instantaneous equilibrium configuration is finite, thus leading to a history-dependent observable.

3.5.2. Metal spintronic systems

A different class of spin-based memristive systems takes advantage of all-metal spintronic devices [3,142]. The operation of such devices can employ spin-torque-induced magnetization switching or magnetic-domain-wall motion [35]. Figure 34 depicts both schemes.

Spin-torque transfer systems. One realization (Figure 34(a)) is based on spin-torque transfer [149–152]. In spin-torque transfer systems, the resistance is determined by the relative magnetization between opposite sides of a magnetic tunnel junction. Current flowing through the junction induces spin torque, in turn changing the relative magnetization.

Quite generally, considering injection of spin-polarized electrons from a reference layer (with a fixed direction of magnetization) into a free layer (the magnetization direction of which can change), the magnetization dynamics of the free layer can be described by the Landau–Lifshitz–Gilbert equation [150,153,154]. Parameterizing the magnetization direction of the free layer by two angles θ and ϕ (according to [155], θ is the angle between the magnetization direction and an uniaxial anisotropy axis assumed to be in the interface plane, and φ is the angle in the plane perpendicular to the uniaxial anisotropy axis), the Landau–Lifshitz–Gilbert equation can be written as [155]

$$\frac{d}{dt} \begin{pmatrix} \theta \\ \varphi \end{pmatrix} = \begin{bmatrix} f_1(\theta, \varphi) \\ f_2(\theta, \varphi) \end{bmatrix}, \quad (76)$$

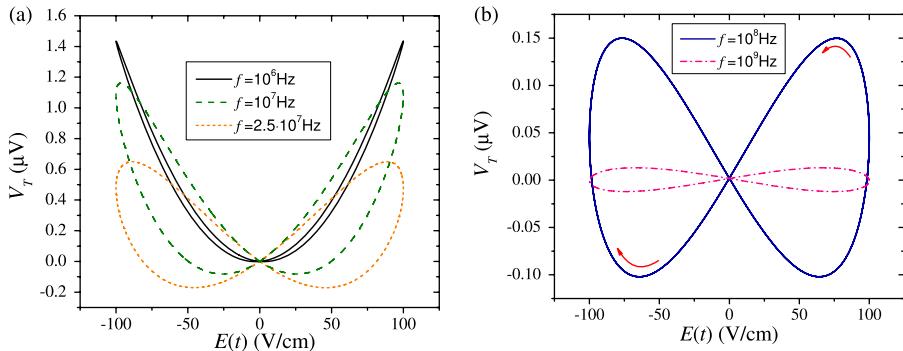


Figure 33. Spin memristive effects in a semiconducting system with inhomogeneous electron density in the direction perpendicular to main current flow [10]. Here, we show the transverse voltage as a function of applied electric field at different applied field frequencies as indicated. Reprinted figure with permission from Y.V. Pershin and M. Di Ventra, Physical Review B 79, p. 153307, 2009 [10]. Copyright © (2009) by the American Physical Society.

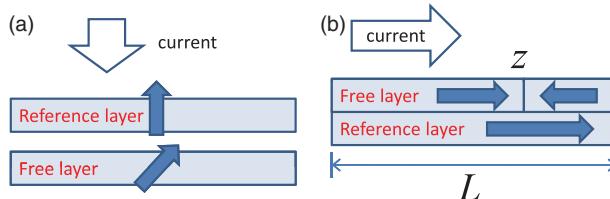


Figure 34. All-metal spintronic memristive systems: (a) magnetic tunnel junction with spin-torque-induced magnetization switching, and (b) spin valve of width L with spin-torque-induced domain-wall motion [35]. The arrows indicate the direction of spin polarization and z is the position of the domain wall.

where the functions $f_1(\theta, \phi)$ and $f_2(\theta, \phi)$ on the right-hand side take into account different factors influencing magnetization dynamics such as uniaxial anisotropy, easy-plane anisotropy, magnetic field, spin-torque and dissipation [155]. The resistance of the magnetic tunnel junction is determined by the angle between magnetization directions of the free and reference layers that can be expressed using θ and ϕ . Consequently, from the point of view of memory systems, the magnetic tunnel junctions can be categorized as second-order current-controlled memristive systems.

To illustrate the origin of memory behind these concepts, let us consider a simple system of a free layer with uniaxial anisotropy only. In this case, the Landau–Lifshitz–Gilbert equation involves only θ and the order of the memristive system is reduced. For this specific situation, Equation (76) is written as [35,155]

$$\frac{d\theta}{dt} = \alpha\gamma H_k(-\sin\theta\cos\theta + p\sin\theta), \quad (77)$$

where θ is the angle between the free-layer magnetization direction and the pinned-layer (reference layer) magnetization direction, γ the gyromagnetic ratio, α is the damping parameter and H_k the perpendicular anisotropy of the free layer, and $p = \eta\hbar I/2\alpha e M_s H_k V$ describes the effect of the polarized-current (I) spin-torque. Here, η is the polarization efficiency, V the film-element volume and M_s the magnetization saturation.

Table 10. Memristive model of a spin-torque transfer device [35].

Physical system	Spin-torque transfer device
Internal state variable(s)	Magnetization direction angle, $x = \theta$
Mathematical description	$V = \frac{1}{G_0(1 + (\text{TMR}/(\text{TMR} + 2)) \cos x)} I$ $\frac{dx}{dt} = \alpha\gamma H_k \left(-\sin x \cos x + \frac{\eta\hbar I}{2\alpha e M_s H_k V} \sin x \right)$
System type	First-order current-controlled memristive system

Resistance of the corresponding magnetic tunnel junction (MTJ) is given by

$$R_M(\theta) = \frac{1}{G_0(1 + (\text{TMR}/(\text{TMR} + 2)) \cos \theta)}, \quad (78)$$

where G_0 is the MTJ conductance when $\theta = \pm\pi/2$, and the tunneling magnetoresistance, TMR, is the ratio of the difference between high and low conductance to low conductance (high conductance occurs when both layers of magnetizations are parallel to each other and low conductance when the magnetizations are antiparallel). The model of spin-torque transfer device discussed above is condensed in Table 10. Its memristive origin is evident. In fact, an interesting feature of this system is the periodicity of the angle when it is changed by 2π . The state variable θ , actually, cannot record such a change. This feature should be taken into account in studies of such structures.

Spin-torque-induced domain-wall motion. In the second realization of metallic spintronics (Figure 34(b), Table 11), a long spin-valve structure is realized with domain-wall motion in the free layer induced by the current [35]. In this geometry, the current flows in both free and reference layers. The resistance of such a structure depends on the domain-wall position z (along the direction of current flow) as

$$R_M(z) = \frac{R_l z}{L} + \frac{R_h(L - z)}{L}. \quad (79)$$

Here, L is the free-layer length, R_l is the low resistance when magnetizations of free and reference layers are parallel and R_h is the high resistance when magnetizations of both layers are antiparallel. In a linear approximation, the domain-wall velocity is proportional to the current strength

$$\frac{dz}{dt} = \Gamma I, \quad (80)$$

where Γ is a proportionality coefficient. Equation (80) should be solved with the boundary conditions $0 \leq z \leq L$. It follows from Equations (79 and 80) that the device is described by general equations

$$V = R_M(z)I, \quad \frac{dz}{dt} = f(I). \quad (81)$$

Therefore, this spin-valve structure with domain-wall motion is also a first-order current-controlled memristive system. When the position of the domain wall z is confined inside the free layer ($0 < z(t) < L$), we can integrate Equation (80) obtaining $z(t) = \Gamma q(t)$. In this regime, the device behaves as an ideal memristor with memristance

$$R_M = R_h - \frac{(R_h - R_l)\Gamma \int_{-\infty}^t I(t') dt'}{L}. \quad (82)$$

In reality, the domain-wall motion is a complex process. Consequently, Equation (82) provides only a first approximation [35] to the device response.

Wang *et al.* have suggested the use of the temperature dependence of the domain-wall mobility – which is observed within a certain range of parameters – to sense an external temperature [156]. Generally, the domain-wall velocity as a function of the driving current has a threshold-type dependence [157]. Around the critical current value, the thermal fluctuations play an important role in the domain wall de-pinning from crystallographic defects, thus providing a basis for thermal sensitivity [156]. The resulting *spintronic memristor temperature sensor* has the same device structure as shown in Figure 34(b). It is suggested to apply a voltage pulse of a constant magnitude to the device for temperature sensing. The resistance difference before and after the voltage pulse is measured and calibrated to sense the temperature. Theoretically, the domain-wall motion in the critical current region is described by stochastic differential equations [158]. Therefore, this system is an example of a *stochastic memory-circuit element* introduced in Section 2.1.

A different approach to memristive switching of magnetic junctions was followed by Krzyszczko *et al.* [159]. These authors have fabricated an MgO-modified magnetic tunnel junction with a resistive switching material inside. As shown in Figure 35, resistive switching results in a splitting of magnetoresistance curves. The authors observed a tunnel magnetoresistance of about 100% ratio and bipolar resistive switching of about 6%. Five resistance states were demonstrated. This approach is thus a promising alternative to create multi-bit states for storage and logic.

3.6. Ionic channels

Another important memristive system pertains to biological neural networks, and in particular, to the functioning of membranes in axon cells. In fact, in 1952 Hodgkin and Huxley suggested a model of action potentials [13] in neurons that employs history-dependent channel conductances that are essentially memristive. This model is one of the most significant conceptual achievements

Table 11. Memristive model of spin-torque-induced domain-wall motion.

Physical system	Domain wall
Internal state variable(s)	Position, $x = z$
Mathematical description	$V = \left[R_h - \frac{(R_h - R_l)\Gamma \int_{-\infty}^t I(t') dt'}{L} \right] I$
System type	Current-controlled memristor

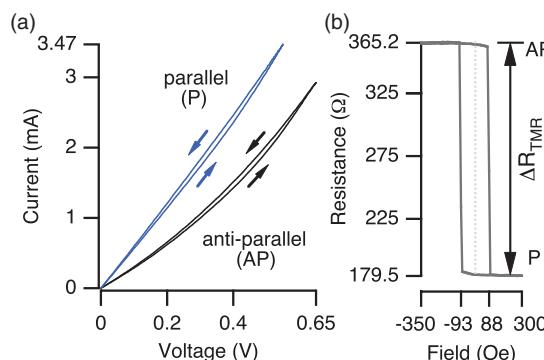


Figure 35. Simultaneous manifestation of resistive and magnetoresistive switching. (a) Due to resistive switching, splitted I - V curves are observed for both magnetic configurations (parallel and anti-parallel) of TMJ device. (b) Magnetic hysteresis loop showing magnetoresistive switching of the device. Reprinted with permission from P. Krzyszczko *et al.*, Applied Physics Letters 95, p. 112508, 2009 [159]. Copyright (2009), American Institute of Physics.

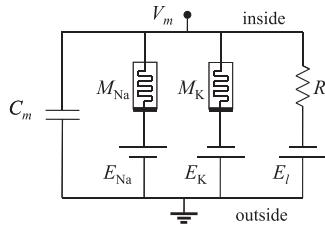


Figure 36. Equivalent electrical circuit for a short segment of squid axon membrane (A.L. Hodgkin and A.F. Huxley, *The Journal of Physiology*, 1952, 117, pp. 500–544 [13]. Copyright © John Wiley & Sons Ltd. modified with permission.). Here, C_m is the membrane capacitance, V_m the membrane potential, M_{Na} and M_K the memristive systems describing conductivity of Na and K channels, respectively, R_l the leakage resistance, E_{Na} , E_K and E_l the reverse ion channel potentials, and by “inside” and “outside” we mean the interior of the axon and its exterior with the membrane delimiting the two sides.

in neuroscience [160]. In its original formulation, the nerve membrane (specifically, the membrane of the squid giant axon) was described by three types of ion channels: leakage channels (primarily carrying chloride ions), Na channels and K channels. Leakage channels are mainly responsible for the resting membrane potential and have a relatively low constant conductance. The conductance of the other two channels changes as a function of time and voltage, and here lies the memristive behavior we are interested in. Hodgkin and Huxley have demonstrated that step depolarizations of the squid axon trigger a rapid inward current across the membrane carried by Na^+ ions, followed by an outward current due to K^+ ions.

In order to quantitatively understand the experimental data, they have then suggested an equivalent circuit model of the membrane as shown in Figure 36. In this plot, we use symbols of memristors in order to denote variable conductance channels. Mathematically, the membrane current is written as [13]

$$I = C_m \frac{dV_m}{dt} + M_{\text{Na}}^{-1}(V_m - E_{\text{Na}}) + M_K^{-1}(V_m - E_K) + R_l^{-1}(V_m - E_l), \quad (83)$$

where the memory conductances $M_{\text{Na}}^{-1} = \bar{g}_{\text{Na}} m^3 h$ and $M_K^{-1} = \bar{g}_K n^4$, with \bar{g}_{Na} and \bar{g}_K , being constants, R_l describes the leakage resistance and all other circuit quantities can be read from the circuit diagram. The time dependencies of voltage-dependent gating variables n , m and h are given by:

$$\frac{dn}{dt} = \alpha_n(1 - n) - \beta_n n, \quad (84)$$

$$\frac{dm}{dt} = \alpha_m(1 - m) - \beta_m m, \quad (85)$$

$$\frac{dh}{dt} = \alpha_h(1 - h) - \beta_h h, \quad (86)$$

where $\alpha_{n(m,h)}$ and $\beta_{n(m,h)}$ are voltage-dependent constants [13] defined as

$$\alpha_n = 0.01 \frac{(V_m + 10)}{e^{(V_m + 10)/10} - 1}, \quad (87)$$

$$\beta_n = 0.125 e^{V_m/80}, \quad (88)$$

$$\alpha_m = 0.1 \frac{(V_m + 25)}{e^{(V_m + 25)/10} - 1}, \quad (89)$$

$$\beta_m = 4 e^{V_m/18}, \quad (90)$$

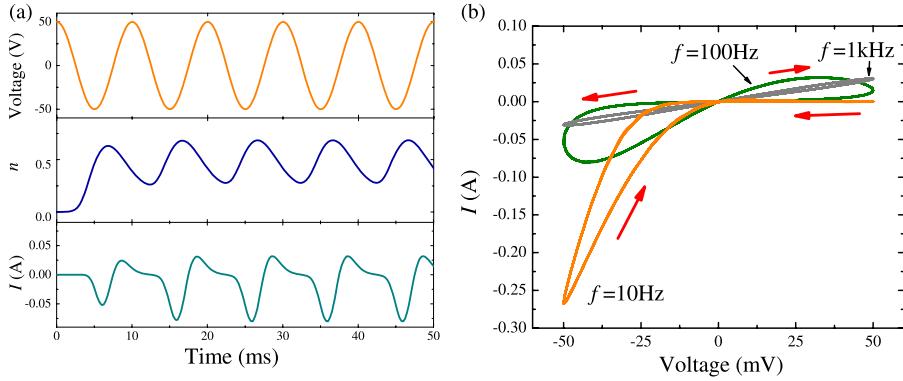


Figure 37. Simulations of the potassium channel memristive system (M_K) response. We have used $\bar{g}_K = 10 \text{ mS}$. The applied voltage is $V(t) = V_0 \cos(2\pi f t)$ with $V_0 = 50 \text{ mV}$ and $f = 0.1 \text{ kHz}$ in (a).

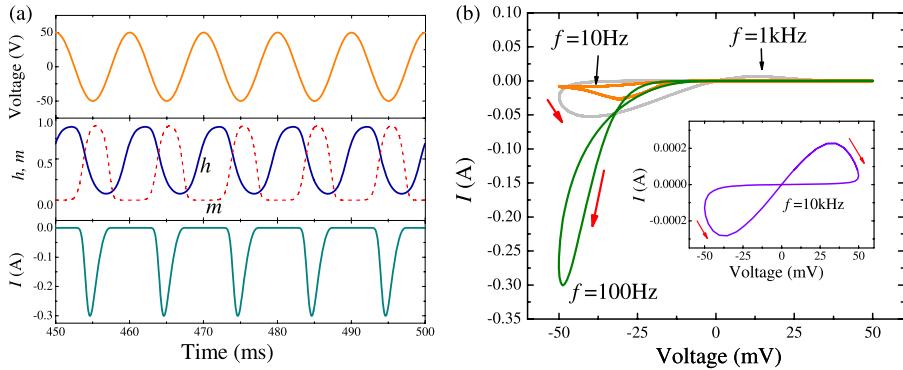


Figure 38. Simulations of the sodium channel memristive system (M_{Na}) response. We have used $\bar{g}_{Na} = 33 \text{ mS}$. The applied voltage is $V(t) = V_0 \cos(2\pi f t)$ with $V_0 = 50 \text{ mV}$ and $f = 0.1 \text{ kHz}$ in (a).

$$\alpha_h = 0.07 e^{V_m/20}, \quad (91)$$

$$\beta_h = \frac{1}{e^{(V_m+30)/10} + 1}. \quad (92)$$

In the above equations, the voltage is in millivolts and time is in milliseconds. The quantities *n*, *m* and *h* take values between 0 and 1, thus representing variation of conductances in time of the channels.

It follows from the expressions of M_{Na} and M_K (given below Equations (83)) and (84)–(86) that the potassium channels can be classified as first-order voltage-controlled memristive systems and the sodium channels as second-order voltage-controlled memristive systems [16]. In Figures 37 and 38 we plot simulations of potassium and sodium channel memristive systems biased by an ac voltage. These plots demonstrate frequency-dependent *I*–*V* curves typical of memristive systems. There is, however, an interesting feature that can be seen in Figure 38(b) for the *f* = 100 Hz curve: at negative voltages, the curve has a self-crossing. To the best of our knowledge we are not aware of experimental results for these systems that employ ac biases, and thus this self-crossing feature remains to be verified.

Modern models of neuronal dynamics are based on similar equations, but often involve many more ion channel types, with the ion channels possibly located on different parts of a spatially

extended neuron [161]. Therefore, a single neuron description may involve a large number of memristive systems.

4. Memcapacitive systems

Having discussed experimental realizations of memristive systems, in this section we consider systems showing memcapacitive behavior. Under the term capacitor, we understand a general electronic device capable of storing charge and energy. Such a device normally includes a couple of external metal plates having negligible resistance and a dielectric medium between the plates. In capacitors, memory effects can originate from changes in the geometry and/or permittivity (Figure 39).

Under *geometrical mechanisms* of memcapacitance, we understand situations when geometrical morphology of the plates changes in time (e.g. their relative distance and/or shape). In permittivity-related mechanisms, dielectric properties of the material between the plates provide the memory. We can identify three most probable permittivity-related mechanisms (Figure 39): *delayed-response mechanism*, when dielectric permittivity dynamics involves a time delay, *permittivity-switching mechanism*, when the dielectric constant changes its value under the external input (but the response is fast), and *spontaneously polarized medium mechanism*, in which a spontaneously polarized material (ferroelectric) is used in the capacitor structure.

We discuss below physical systems demonstrating these different mechanisms of memcapacitance. Known mathematical models of some of these systems are also presented. We also note that a methodology for SPICE modeling of memcapacitive systems has been developed recently [162].

4.1. Geometrical memcapacitive systems

4.1.1. Micro- and nano-electro-mechanical systems

MEMS and nano-electro-mechanical system (NEMS) capacitors [20,163–168] are variable capacitors based on an interplay of mechanical and electrical properties of micro- and nano-size systems. Such elements are key components in many radio-frequency (RF) applications such as tunable filters, impedance matching circuits and voltage-controlled oscillators [163,164]. In addition, these structures, on the nanoscale, are considered for memory applications [166] and sensitive measurements [169]. Normally, capacitors built from these systems utilize a diaphragm-based, a microbridge-based or a cantilever-based structure fabricated via micromachining [163,164].

Figure 40 shows an experimental image of a memcapacitive system constructed from MEMS technology and measured capacitance as a function of voltage. The capacitance curve shows a

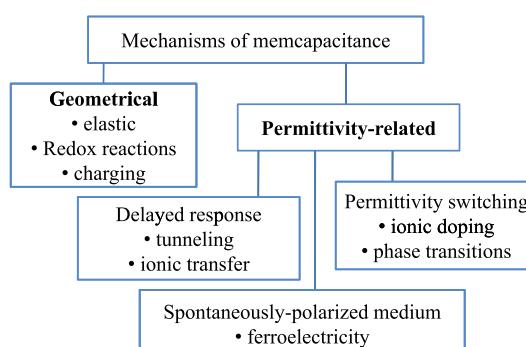


Figure 39. Classification scheme of memcapacitance mechanisms.

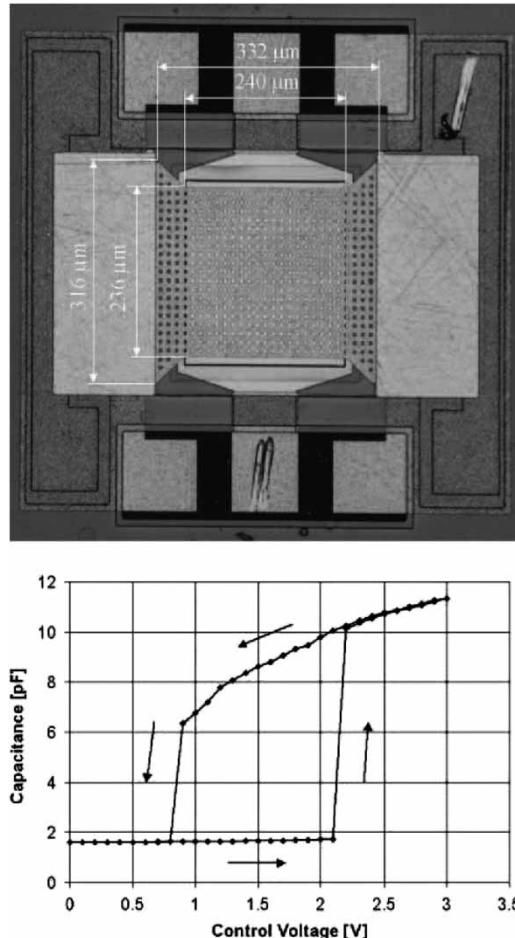


Figure 40. Image of a two-state memcapacitive system constructed from MEMS technology, and its capacitance as a function of applied voltage. Reprinted figure with permission from H. Nieminen *et al.*, Journal of Micromechanics and Microengineering 12, pp. 177–186, 2002 [168]. Copyright © (2002) by the Institute of Physics.

well-defined hysteresis which is a manifestation of memory effects in the structure. Memory effects are related to displacement of a top capacitor plate that can be considered to be suspended by a spring [168]. Below, we consider a model of *elastic memcapacitive system* that (with appropriate boundary conditions) can be used to describe the capacitor features of the MEM system shown in Figure 40. For more details on MEMS and NEMS, we refer to [163,164,170].

4.1.2. Elastic memcapacitive systems

A model of a simple elastic memcapacitive system is discussed in Section 2.5.3. Here, we would like to mention about a different elasticity-based memcapacitive system [171] shown schematically in Figure 41. In this realization, the capacitor is formed by a strained membrane (upper plate) and a flat fixed lower plate. In this model two equilibrium states (up-bent and down-bent membranes) coexist that can be used for a non-volatile storage of a bit of information. The possibility of switching between the two states as well as chaotic behavior of such a system in a certain range

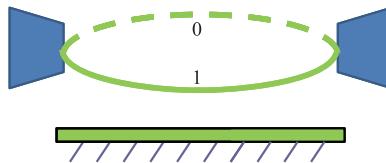


Figure 41. Strained membrane memcapacitive system. The top plate of a regular parallel-plate capacitor is replaced by a flexible strained membrane. Because of two equilibrium positions of the membrane (with potential energy modeled by a double-well potential), stable high and low capacitance configurations are possible in such a system. Both configurations are perfectly stable providing a non-volatile information storage capability. However, since the system is bistable, an analog value cannot be stored in such a device.

Table 12. Model of strained membrane memcapacitive system. Here, $C_0 = \epsilon_0 S/d$, S is the area of the plate, d_0 is the separation between the bottom plate and middle position of the membrane, ω_0 the natural angular frequency of the system, γ a damping coefficient representing dissipation of the elastic excitations, m the mass of the upper plate and z_0 defines the two equilibrium positions of the membrane [171].

Physical system	Strained membrane memcapacitive system
Internal state variable(s)	Displacement and velocity of upper plate, $x_1 = z, \quad x_2 = \frac{dz}{dt}$
Mathematical description	$V_C = \left[\frac{C_0}{1 + x_1/d_0} \right]^{-1} q$ $\frac{dx_1}{dt} = x_2$ $\frac{dx_2}{dt} = -\omega_0^2 x_1 \left[\left(\frac{x_1}{z_0} \right)^2 - 1 \right] - \gamma x_2 - \frac{q^2}{2\epsilon_0 m S}$
System type	Second-order charge-controlled memcapacitive system

of parameters has also been demonstrated [171]. For reference, we provide the model of strained membrane memcapacitive system in Table 12.

4.1.3. Other geometrical memcapacitive systems

There are other possible realizations of geometrical memcapacitive systems. In many memristive systems, for example, the morphology of conducting regions changes in time [52]. Therefore, in addition to a resistance change, the capacitance of such systems changes as well. In particular, co-existence of memristive and memcapacitive behavior has also been observed in perovskite thin films [27] (see Figure 10).

4.2. Delayed-response memcapacitive systems

4.2.1. Superlattice memcapacitive systems

A solid-state memcapacitive system based on the slow polarization rate of a medium between plates of a regular parallel-plate capacitor has recently been proposed [21]. The key idea is to use non-linear electron transport (tunneling) for fast writing and long storage capabilities. Figure 42(a) shows a particular example of memcapacitive system in which N metal layers are embedded into an insulating material between external capacitor plates. The structure is designed in such a way

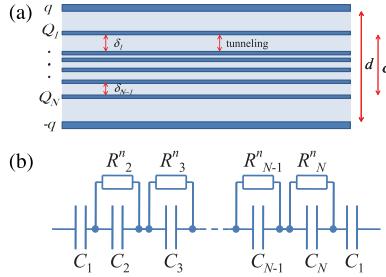


Figure 42. (a) Schematics of a superlattice memcapacitive system. A superlattice medium consisting of N metal layers embedded into an insulator is inserted between the plates of a parallel-plate capacitor. $\pm q$ and Q_k are charges on external plates and on internal metal layers, respectively. (b) Equivalent circuit model of N -layer memcapacitive system. Reprinted figure with permission from J. Martinez-Rincon *et al.*, Physical Review B 81, p.195430, 2010 [21]. Copyright © (2010) by the American Physical Society.

that the electron transport between external plates and internal layers is not possible. Therefore, the internal charges Q_k can only be redistributed between the internal layers creating a medium polarization. Correspondingly, there is a constraint imposed on the total internal charge:

$$\sum_{i=1}^N Q_i = 0. \quad (93)$$

The capacitance of the total structure is given by [21]

$$C = \frac{q}{V_C} = \frac{2C_0}{2 + \sum_{i=1}^N [\Delta - 2\Delta_{i-1}]Q_i/q}. \quad (94)$$

where Δ and Δ_i are geometry-related parameters. The dynamics of the charge at a metal layer k is determined by the currents flowing to and from that layer:

$$\frac{dQ_k}{dt} = I_{k-1,k} - I_{k,k+1}, \quad (95)$$

where $I_{k,k+1}$ is the tunneling electron current flowing from layer k to layer $k+1$ (for more details, see [21]). It follows from Equations (93)–(95) that such a superlattice memcapacitive system is an $N-1$ order charge-controlled memcapacitive system. Table 13 presents summary of the superlattice memcapacitive system.

Simulations of a two-layer memcapacitive system with symmetrically positioned internal layers is depicted in Figure 43. Interesting features of this memcapacitive system include non-pinched

Table 13. Superlattice memcapacitive system. Here, N is the number of the embedded internal metal layers.

Physical system	Superlattice memcapacitive system
Internal state variable(s)	Charges on internal metal plates, $x_i = Q_i$ ($i = 1, \dots, N-1$)
Mathematical description	$V_C = \frac{1 + \sum_{i=1}^{N-1} [\Delta_{N-1} - \Delta_{i-1}]x_i/q}{C_0} q$ $\frac{dx_k}{dt} = I_{k-1,k} - I_{k,k+1}$
System type	$(N-1)$ -order charge-controlled memcapacitive system

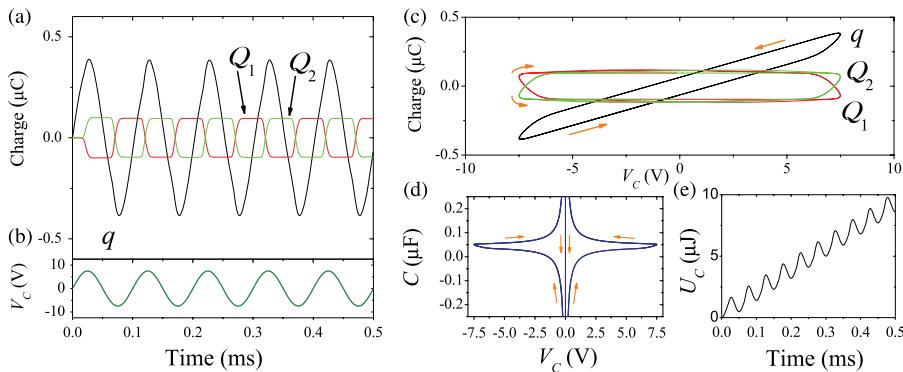


Figure 43. (a) The charge on internal metallic layers and superlattice memcapacitive system plates as a function of time t . (b) Voltage on memcapacitive system, V_C , as a function of time t . Charge–voltage (c) and capacitance–voltage (d) plots. (e) Added/removed energy as a function of time t . These plots were obtained using the parameter values $V_0 = 7.5 \text{ V}$, $f = 10 \text{ kHz}$, $d = 100 \text{ nm}$, $\delta = 66.6 \text{ nm}$, $S = 10^{-4} \text{ m}^2$, $\epsilon_r = 5$, $U = 0.33 \text{ eV}$, $R = 1 \Omega$. Reprinted figure with permission from J. Martinez-Rincon *et al.*, Physical Review B 81, p.195430, 2010 [21]. Copyright © (2010) by the American Physical Society.

$q - V_C$ hysteresis loop (Figure 43(c)), and both negative and diverging capacitance (Figure 43(d)). Moreover, since electron tunneling between the layers is accompanied by energy loss, the memcapacitive system is dissipative (Figure 43(e)). Using a set of non-linear resistors and usual capacitors, an equivalent model of the given memcapacitive system can be formulated (see Figure 42(b)). This is an example of the situation – anticipated in Section 2.8 – in which a memcapacitive system can be constructed from classical circuit elements. We reiterate here that this is not a trivial point because one can use a unified set of equations, (4) and (5), describing a single memory system to represent a complex functionality as that reported here.

4.2.2. Ionic memcapacitive systems

Memcapacitive behavior can be observed also in certain ionic systems because of their relatively slow dielectric response. A typical nanopore sequencing setup [172,173] is an example of such a system. Let us then consider two chambers with ionic solution separated by a membrane with a nanopore [22]. When a varying voltage is applied to electrodes located in different chambers, ions redistribute with a time lag affecting the total system capacitances. In particular, it has been shown [22] that the ac response of such a system demonstrates non-pinched $q - V_C$ hysteresis loops and both negative and divergent capacitances. Moreover, the equivalent scheme of this setup can also be modeled using a set of classical circuit elements [22]. Since nanopores are ubiquitous on membranes of biological cells (e.g. the nerve cells), we expect these phenomena to be observable (at appropriate frequencies) even in those cases. We are not aware, though, of either theoretical or experimental work along these lines.

4.3. Permittivity-switching memcapacitive systems

4.3.1. Polymer-based memcapacitive systems

An analog memory capacitor has been reported in [174]. In this work, the programmable capacitance was achieved in a field-configurable doped polymer, in which the modification of ionic concentrations induces a nonvolatile change in the polymer dielectric properties. Several device structures were investigated and two of them are shown in Figure 44. In both structures, the

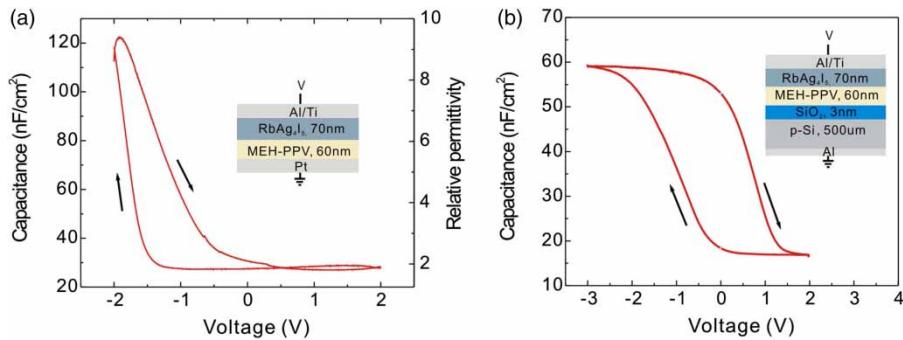


Figure 44. Programmable device capacitances as a function of the applied voltage for the device structures shown in the insets. A better device performance is achieved when a 3-nm thick SiO_2 insulating layer blocking the leakage current is inserted as in (b). Reprinted with permission from Q. Lai *et al.*, Applied Physics Letters 95, p. 213503, 2009 [174]. Copyright (2009), American Institute of Physics.

RbAg_4I_5 ionic conductor functions as an ionic source. It contains Ag cations having a higher mobility and iodine anions the mobility of which is lower and, in a polymer, is of a threshold type. The latter is because the iodine anions, having a much larger radius, can form a large ionic complex I_3^- , and/or chemically bond with the MEH-PPV polymer used in the memory capacitor.

Negative voltage pulses above a threshold were used to inject iodine anions into the polymer, while positive voltage pulses (above the threshold) were used to extract iodine anions from the polymer. Some of the Ag cations follow the iodine anions because of electrostatic interactions. When in the polymer, the anions and the cations form ionic dipoles increasing the polymer permittivity and device capacitance [174]. Since a voltage above a threshold is needed to overcome the ionic bonding with the polymer, the devices provide reasonably nonvolatile memory characteristics [174]. In particular, it has been reported that after the analog capacitance was configured to a certain value, it changed by less than 10% under continuous reading for 5 days.

4.3.2. Phase-transition memcapacitive systems

During the process of an MIT both resistance (as we discussed in Section 3.4) and dielectric properties [175,176] are affected. The latter property was used to fabricate a memory metamaterial in which a persistent electrical tuning of a resonant frequency was demonstrated [15]. In this particular case, vanadium dioxide has been used as the memory material undergoing the MIT, which we have discussed in Section 3.4 in the context of memory resistance. In the experimental setup, a split-ring resonator array was patterned on a 90-nm thin film of vanadium dioxide connected by two electrodes to a voltage source. The device was mounted on a temperature-controlled stage and a temperature of 338.6 K was selected. At this temperature, the slope of the resistance as the function of temperature is the steepest because of the proximity to the MIT. Therefore, even small-amplitude voltage pulses have a notable effect on material characteristics [15]. Such electrical pulses directly applied to vanadium dioxide were used to modify its dielectric properties. The latter ones were registered by measuring the modification of the resonant frequency of the split-ring resonator array.

Figure 45(a) demonstrates the experimentally measured increase in the metamaterial capacitance with each applied voltage pulse. As the input power per pulse increases with pulse number (see Figure 45(b)), the MIT in vanadium dioxide progresses causing the permittivity increase. Overall, the resonant frequency can be red-shifted by as much as 20% from its spectral maximum at $\omega_0 = 1.65 \text{ THz}$ [15]. It is also worth noting that the effective circuit model of split-ring

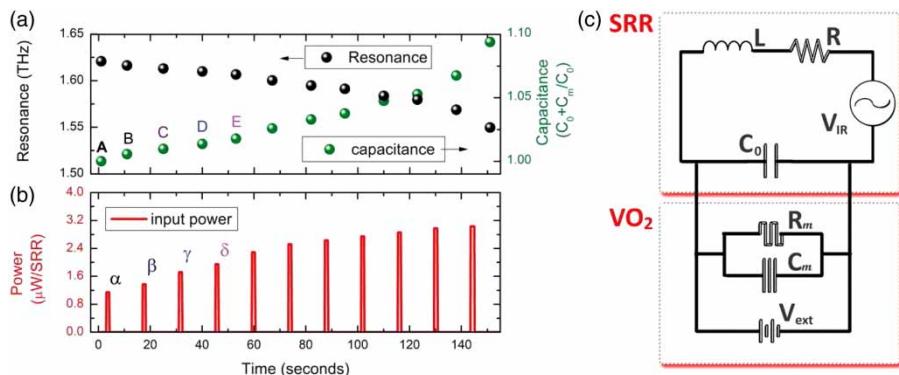


Figure 45. Electrical tuning of a metamaterial: (a) Modification of resonance frequency and capacitance by electrical pulses of increasing power (b). (c) Equivalent circuit model in which split-ring resonator (SRR) is described by traditional circuit elements L , R and C_0 , and vanadium dioxide material is represented by symbols of memristor R_m and memcapacitor C_m . From T. Driscoll *et al.*, Science, 325, pp. 1518–1521, 2009 [15]. Reprinted with permission from AAAS.

resonator deposited on vanadium dioxide involves both memristive R_m and memcapacitive C_m elements (Figure 45). As already anticipated, memristive and memcapacitive properties co-exist very often, and in the metamaterial configuration [15] they play together an important role in the device operation.

4.4. Spontaneously polarized medium memcapacitive systems

4.4.1. Ferroelectric memcapacitive systems

Another interesting concept is the use of ferroelectric materials [177–179] as the dielectric medium of a memory capacitor. Ferroelectric materials are composed of domains with a non-zero average electrical polarization. The polarization of ferroelectric materials shows hysteresis as a function of electric field, revealing two well-defined polarization states. These states are used in the ferroelectric random-access memory (RAM) technology [180] having functionality similar to Flash memory.

Experimentally, when ferroelectric materials are inserted into capacitor structures, a hysteretic C – V behavior is observed (see, e.g. [181–184]). In particular, in Figure 46, we plot the polarization-voltage and capacitance-voltage characteristics of metal-ferroelectric-metal capacitor Pt/PZT/Pt where PZT is $(\text{Pb}, \text{Zr})\text{TiO}_3$ [181]. In this plot, the C – V curve demonstrates the characteristic “butterfly”-shape related to ferroelectric material and can thus be characterized as a type II memcapacitive system (cf. Figure 2). In this experiment, the dielectric constant of the PZT film ranged from $\epsilon_r = 83\epsilon_0$ to $330\epsilon_0$, where ϵ_0 is the vacuum permittivity. The peak capacitance occurring at $\pm 2.5\text{ V}$ corresponds to the coercive field of the ferroelectric material.

4.5. Other memcapacitive systems

4.5.1. Metal-oxide-semiconductor capacitors with nanocrystals

Metal-oxide-semiconductor (MOS) structures with embedded nanocrystals (Figure 47(a)) have been much investigated recently [185–198]. These devices are promising candidates to replace floating-gate Flash memory. The latter, in fact, has long programming times and poor endurance. Many different materials such as Si [186–189, 193, 199], Ge [185, 188, 190, 191, 194, 195], SiGe [196, 198], Au [200] and Ag [192] have been considered as candidates for the nanocrystals that

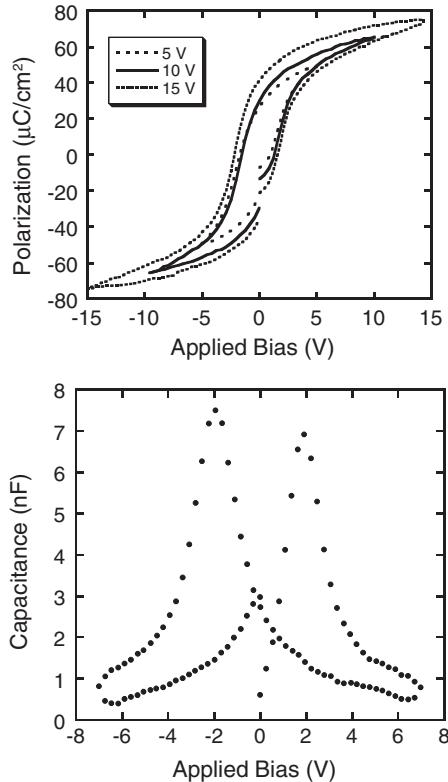


Figure 46. Ferroelectric behaviour of Pt/PZT/Pt thin-film capacitors. Polarization-voltage and capacitance-voltage measurements are plotted. Reprinted figure with permission from E. Cagin *et al.*, Journal of Physics D: Applied Physics 40, p. 2430, 2007 [181]. Copyright © (2007) by the Institute of Physics.

store charge. Currently, Ge nanocrystals seem to be the most promising ones because of a better data retention due to the smaller bandgap compared to Si [195].

It is known that $C-V$ curves of usual MOS capacitors demonstrate a non-linear behavior [201] (see the “Virgin” line in Figure 47(c)). Nanocrystals added to a MOS structure (an actual Ge nanocrystal image is shown in Figure 47(b)) provide a mechanism controlling the displacement of the $C-V$ curve. When charge is transferred to nanocrystals, the $C-V$ curve shifts by the amount ΔV_{FB} determined according to [194,199]:

$$\Delta V_{FB} = \frac{-qnD}{\varepsilon_{ox}} \left(t_{CO} + \frac{1}{2} \frac{\varepsilon_{ox}}{\varepsilon_{Ge} t_{dot}} \right), \quad (96)$$

where q is the elementary charge, n the number of charges per nanocrystal, D the density of Ge nanocrystals, t_{CO} the control oxide thickness, t_{dot} the mean diameter of Ge nanocrystals and ε_{Ge} and ε_{ox} dielectric permittivities of Ge nanocrystals and oxide, respectively. Figure 47(c) demonstrates displacement of $C-V$ curves induced by positive and negative stress biases.

From the point of view of memory elements, the amount of transferred charge n plays the role of the state variable defining the capacitance $C(V, n)$. The dynamics of n can be described by a rate equation. However, the total equivalent scheme of such device should include a resistor in series with a capacitor as charge transfer to nanocrystals involves also dissipation processes. Indeed, such an equivalent resistor–capacitor circuit of MOS capacitors with nanocrystals was

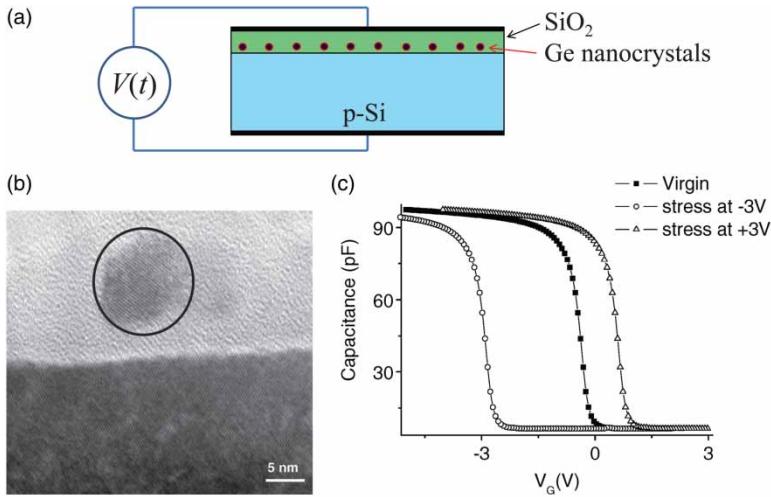


Figure 47. (a) Schematic of MOS capacitor with embedded germanium nanocrystals. (b) High-resolution transmission electron microscopy image of an isolated Ge nanocrystal with a mean size of 8.5 nm. (c) C - V curves measured after applying a stress bias. (b) and (c) are reprinted from Solid-State Electronics 50, M. Kanoun *et al.*, pp. 1310–1314, Copyright (2006) with permission from Elsevier [194].

recently discussed [202]. Therefore, MOS capacitors with nanocrystals do not manifest a purely memcapacitive behavior, although the memcapacitive component in these devices seems to be the dominant one. This is thus an example of a combined system as those discussed in Section 2.7.

5. Meminductive systems

We are now left to consider systems that show meminductive behavior. These are systems with inductance depending on the past dynamics and which can store energy. In this case, the energy stored may be a combination of magnetic energy and energy due to other degrees of freedom (e.g. elastic kinetic energy). Similar to the case of memcapacitive systems, memory effects in inductors can originate from a geometrical variation of their structure or be related to their permeability (see Figure 48). Although, at the present time, meminductors and meminductive systems are the least studied members of the family of circuit elements with memory, there are nonetheless several interesting examples of such devices, and owing to their practical importance, we expect that more will be discovered/designed in the future. Moreover, several SPICE models of meminductive systems have been suggested [203]. Below, we overview experimental realizations of meminductive systems based on the bimorph effect, introduce a model of an elastic meminductive system, and discuss some other possible realizations of these elements.

5.1. Geometrical meminductive systems

5.1.1. Bimorph meminductive systems

Similar to memcapacitive systems' realizations, the MEMS technology also provides an opportunity to fabricate devices based on an interplay of mechanical, electrical, magnetic and thermal properties. Several designs of inductors based on tunable MEMS that employ the bimorph effect [204] have been reported [205–207]. The bimorph effect refers to composite materials that show electrothermal actuation, namely they show reversible mechanical deformation under

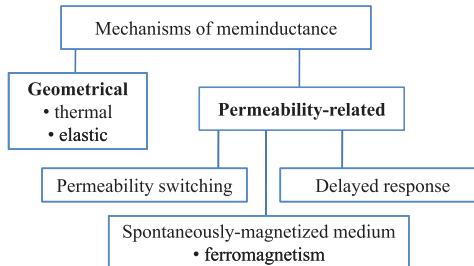


Figure 48. Classification scheme of meminductance mechanisms.

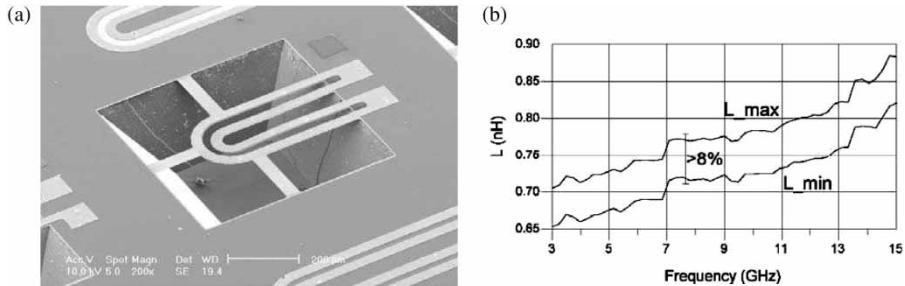


Figure 49. (a) An SEM image of a two-layer gold/silicon nitride meminductive system. The inner inductor deflects down as current heats the structure. (b) Inductance versus frequency curves showing a tuning range of 8%. Reprinted with permission from I. Zine-El-Abidine *et al.*, Proceedings of the 2004 International Conference on MEMS, NANO and Smart Systems (ICMENS'04) pp. 636–638, 2004 [206]. Copyright © (2004) by the IEEE.

electrothermal effects. The tunability of the inductors based on this effect is then achieved by the difference in thermal expansion coefficients of the two materials forming the inductor. When a voltage is applied to such a structure, its temperature changes due to heating and the structure deforms in a controllable manner. As a finite time is required for heating and cooling, the inductance is history-dependent. Therefore, such a device behaves as a *meminductive system*.

Two experimental designs of bimorph-effect-based meminductive system are shown in Figures 49(a) and 50(a). The first structure (Figure 49(a)) consists of two inductors (fabricated of gold/silicon nitride bilayer) connected in parallel. The outer loop inductor is fixed by nitride beams, while the inner inductor is free to move. The heating of the structure by current causes the inner inductor to deflect downward changing the structure's inductance. A variation of the inductance as much as 8% was reported [206]. A larger tuning range of 32% is achieved in the structure shown in Figure 50(a). Here, the meminductive system is made of an amorphous-silicon/aluminum (a-Si/Al) coil. Figure 50(a) shows that an applied dc voltage flattens the initial three-dimensional structure.

The modeling of such meminductive systems should be based on the heat transfer equation, similar to the case of thermistors (see Section 3.1). In the simplest case, we can assume that the device state is defined by a single temperature T , that is,

$$\phi(t) = L(T)I(t), \quad (97)$$

where $\phi(t)$ is the magnetic flux piercing the inductor, $I(t)$ the current that flows in it, and T satisfies

$$C_h \frac{dT}{dt} = RI^2 + \delta(T_{\text{env}} - T), \quad (98)$$

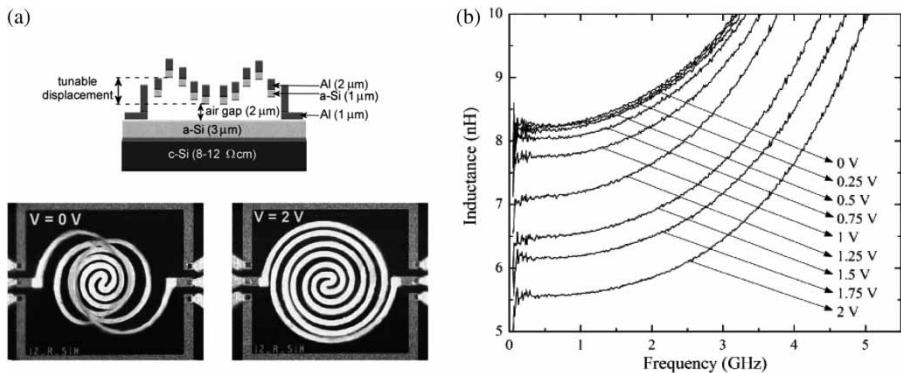


Figure 50. (a) Schematic cross-section and micrograph image of an a-Si/Al meminductive system and (b) its $L-f$ curves. In (a), one sees that the meminductive system is three dimensional at 0 V applied bias and completely flat at 2 V. An inductance tuning of 32% is reported for this structure. Reprinted with permission from S. Chang and S. Sivoththaman, IEEE Electron Device Letters 27, pp. 905–907, 2006 [207]. Copyright © (2006) by the IEEE.

Table 14. Bimorph meminductive system.

Physical system	Bimorph meminductive system
Internal state variable(s)	Temperature, $x = T$
Mathematical description	$\phi = L(x)I$ $\frac{dx}{dt} = C_h^{-1}RI^2 + C_h^{-1}\delta(T_{\text{env}} - x)$
System type	First-order current-controlled meminductive system

where C_h is the heat capacitance, δ is the dissipation constant of the device and T_{env} is the background (environment) temperature. It follows from Equations (97), (98) that meminductive systems based on the bimorph effect are first-order current-controlled meminductive systems. Moreover, since the state function (Equation (98)) and the response function (Equation (97)) are even functions of the current, these systems (under these simplified assumptions) should exhibit type II hysteresis loops under a periodic stimulus (see Figure 2). Table 14 summarizes properties of bimorph meminductive systems.

5.1.2. Elastic meminductive system

A model of meminductive system, based on an interplay of elastic forces with current-current interaction, can be found in Section 2.6.3.

5.2. Other meminductive systems

Having discussed geometry-based meminductive systems, we now turn to the other possible realizations that, as it was mentioned above, can be based on peculiarities in the permeability response. In particular, a meminductive behavior can be realized using the core material, with the response to the applied magnetic field depending on its history. As an example, we can think about ferromagnetic materials exhibiting a magnetic hysteresis such as iron or iron-based alloys. Such inductors can easily be realized in practice, and the desired orientation of the ferromagnetic core's easy axis with respect to the coil direction can be selected [208]. Moreover, a mathematical framework to model iron-core inductors is reported in [209]. As of now, however, a clear connection

of such inductors with the theory of memory elements has not been developed. In addition, memory effects in inductance (such as lagging) were revealed in the context of superconducting circuits [210]. An interesting, yet unexplored, direction is to employ field-induced ion motion in solid state electrolytes for non-volatile realizations of meminductive systems.

6. Other systems with memory

In this section we consider several systems with memory that cannot be categorized as pure memristive, memcapacitive or meminductive systems. Structural peculiarities of such devices (such as, for example, the presence of a third terminal or complex behavior) require a more involved description containing, in some cases, several basic circuit elements. For example, the equivalent structure of Josephson junctions considered below involves four different elements: resistor, capacitor, non-linear inductor and memristor. However, our goal here is not to provide a complete list of complex device structures with memory. Rather, we want to discuss some important examples that are presently investigated for practical applications and show the wide variety of systems where memory may occur. We also note that not all experimentally studied systems with memory can be in principle categorized according to the scheme presented in this review. The reason is simple: many experimental setups do not involve electrical connections. For example, in semiconductor spintronics [141], the dynamics of spin polarization decay is very often probed by the Faraday rotation technique that is based on the optical response of the system. Thus, many interesting memory phenomena, such as, for example, non-exponential relaxation of electron spins in heterostructures [211,212], or aging and slow relaxation of electron glasses [213] are not considered here.

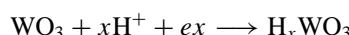
6.1. Three-terminal devices

6.1.1. Electrochemical cell “memistor”

A transistor-like three-terminal structure, which was named *memistor* (not to be confused with the term “memristor” we have employed so far), was designed by Widrow *et al.* [214,215] in the early 1960s for demonstration in neural networks. In Widrow’s memistor, the resistance between two of the terminals was controlled by the time integral of the current in the third terminal [214]. The particular realization of the memistor employed the phenomenon of “electroplating” whereby the amount of metal deposited on a resistive substrate is determined by the control current. In the first successful attempt, a memistor was realized using electroplating of copper from a copper sulfate–sulfuric acid bath upon an ordinary pencil lead [214].

6.1.2. Solid-state “memistor”

A solid-state realization of the memistor was reported by Thakoor *et al.* [216] in 1990. In the solid-state memistor device schematically shown in Figure 51(a), the programming voltage is applied to the gate electrode with respect to the two read electrodes positioned at the bottom of the structure. The read electrodes are separated by a layer of tungsten trioxide, WO_3 . The resistance of tungsten trioxide was varied due to a transfer of hydrogen ions H^+ from a thin film of hydroscopic chromium oxide Cr_2O_3 into the WO_3 active layer. It was suggested that a redox reaction (with x describing the amount of H^+ ions transferred to WO_3)



converting the WO_3 film into a conducting bronze during “turn-on” and the reverse reaction during “turn-off” is responsible for the variation of resistance [216]. The possibility of continuous analog

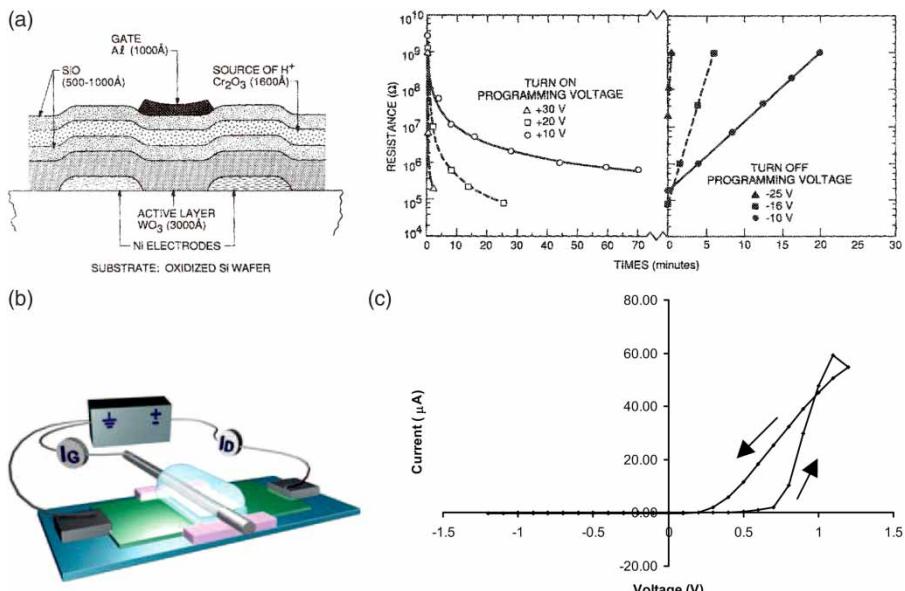


Figure 51. (a) Cross-section of a three-terminal WO_3 "memistor" device and its programming characteristics. Reprinted with permission from S. Thakoor *et al.*, Journal of Applied Physics 67, p. 3132, 1990 [216]. Copyright (1990), American Institute of Physics. (b) Schematic representation of polymeric transistor with memory connected to a battery and (c) its I - V characteristics. Reprinted with permission from T. Berzina *et al.*, Journal of Applied Physics 105, p. 124515, 2009 [217]. Copyright (2009), American Institute of Physics.

programming of resistance in a wide range of values from $\sim 10^5$ to $\sim 10^9 \Omega$ was demonstrated. Experimentally measured $R(t)$ curves under programming conditions (see Figure 51(a)) show a power-law relationship for the "turn-on" process and an exponential relationship for "turn-off" process [216]. Such a different form of "turn-on" and "turn-off" curves was related to a generated electromotive force that is in the same direction with the applied voltage in the "turn-off" process, and in the opposite direction during the "turn-on" one, thus facilitating and opposing ion transfer, respectively [216].

6.1.3. Polymeric transistor with memory

In several recent papers [217–220], a polymeric transistor with memory was investigated. Such a three-terminal device was used in a two-electrode configuration (the gate and source electrodes were short-circuited). The memristive properties of this system were clearly observed experimentally [217–220]. Here, for the purpose of clarity, we will use the name "transistor with memory" because of the three-terminal configuration.

The operation of polymeric transistors with memory is based on the possibility to reversibly change the conductivity of the conductive polymer emeraldin base polyaniline (PANI) between oxidized and reduced states using ion drift in a solid electrolyte (LiCl was used in initial studies [218]). The observed variation of conductivity was about two orders of magnitude [218] under bipolar operational conditions. In Figure 51(c), we show an example of I - V curve for a polymeric transistor with memory.

It is interesting that in such devices, the I - V shape is sensitive to electrolyte composition [220]. On this ground, an optimal electrolyte composition was determined [220]. Moreover, possible

applications of polymeric transistor with memory in adaptive networks mimicking, to some extent, the learning behavior of biological systems were suggested [221] (see also Section 7.2.1, where we discuss applications of three-terminal devices in neuromorphic circuits). Later, the same group has demonstrated a two-memristor circuit which shows synaptic plasticity and related the result to associative learning in a specific component of the *Limnea Stagnalis* neuron circuitry governing its feeding behavior [222] (reported at IEEE International Symposium on Circuits and Systems 2010, Paris, France).

6.2. Memristive components in Josephson junctions

In a realistic model of a Josephson junction [223], the latter is approximated by an equivalent scheme shown in Figure 52 involving a linear resistor R , linear capacitor C , non-linear inductor L and memristor M connected in parallel (this model is also discussed in [224]). In this scheme, the memristor takes into account a small current component due to interference among quasi-particle pairs [223]. The current through the memristor (we do not consider here the rest of the circuit since its modeling is standard, see, e.g. [225]) is given by [226,227]

$$I_M = G_0 \cos(k_0 \varphi) V, \quad (99)$$

where G_0 and k_0 are device-related constants [223], and φ is the superconducting phase difference across the junction.

Since, in the ac Josephson effect, the phase difference evolves according to (e is the electron charge)

$$\frac{d\varphi}{dt} = \frac{2eV}{\hbar}, \quad (100)$$

Equation (99) results in

$$I_M = G_0 \cos\left(\frac{2ek_0}{\hbar} \int_{-\infty}^t V(t') dt'\right) V, \quad (101)$$

which describes an ideal voltage-controlled memristor. We thus see that Josephson junctions contain a memristive component. This component is, however, generally small, and, in most cases, of practical interest, it can be neglected. Nevertheless, this example is important since the memristive component in Josephson junctions is a rare example of *ideal* memristor (see Table 15).

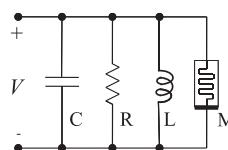


Figure 52. Equivalent scheme of Josephson junction involving resistor, capacitor, non-linear inductor and memristor [223].

Table 15. Memristive component in Josephson junctions.

Physical system	Josephson junction
Internal state variable(s)	Phase difference, $x = \varphi$
Mathematical description	$I = G_0 \cos\left(\frac{2ek_0}{\hbar} \int_{-\infty}^t V(t') dt'\right) V$
System type	Voltage-controlled memristor

7. Application of memory elements

There are several already well-established applications of memory elements such as the use of thermistors or tunable capacitors employing MEMS. Here, we would like to focus on future potential applications. Such future applications of memory-circuit elements are envisioned in both digital and analog domains. These mostly concern memristive systems, while those involving memcapacitive and meminductive systems are still at an early stage, even though certain applications discussed below (e.g. biologically inspired circuits or logic) could be equally realized with these classes of systems.

In the digital domain, applications of memristive systems involve non-volatile solid-state memory, signal processing and programmable logic. Analog applications of memristive systems are based on the possibility to continuously vary their physical response and, therefore, on their ability to store more (theoretically infinite) information than in the digital regime. In this respect, these are related to analog signal processing, learning circuits, programmable analog circuits and neuromorphic circuits. Below we discuss such cases.

7.1. Digital applications

7.1.1. Digital memory

The digital binary non-volatile memory is the most straightforward and developed application of memristive systems. The current research efforts are primarily focussed on this technological direction [62,228–235]. It is expected that the resistive random access memory (ReRAM) may replace Flash memory [2] in some years. Physically, a bit of information can easily be encoded in the state assigning of the memristive system, for example, the low resistance state to 1 and the high-resistance state to 0. Moreover, the possibility of continuous variation of device's resistance offers an opportunity for a multi-state memory cell [236,237].

In Table 16, we compare some basic technical characteristics of NAND (not AND gate-type) Flash memory and nanoionic ReRAM [59]. Most of the demonstrated nanoionic ReRAM parameters are extracted from [76] that reports fabrication of 2-Mbit CBRAM utilizing 90 nm technology. In this architecture, each memory cell contains one transistor and one memristive junction based on formation/disruption of a conductive bridge formed by Ag atoms in a germanium selenide chalcogenide material. The main advantage of ReRAM over Flash memory is in the significantly shorter read/write times. In addition, ReRAM technology is suitable for higher integration density circuit architecture by using a stack of crossbar arrays. The drawbacks of ReRAM include a low read voltage and relatively a high write energy.

Table 16. Current and projected characteristics of NAND Flash memory and nanoionic ReRAM from the ITRS 2009 edition [59]. Here, F is the smallest lithographic dimension.

Property	NAND Flash		Nanoionic ReRAM	
Year/status	2009	2024	Demonstrated	Best projected
Feature size F (nm)	90	18	90	5–10
Cell area	$5F^2$	$5F^2$	$8F^2$	$8/5F^2$
Read time (ns)	50	8	<50	<10
Write/Erase time	1/0.1 ms	1/0.1 ms	5 ns/5 ns	<20 ns
Retention time (years)	>10	>10	>10	>10
Write cycles	>1E5	>1E5	>1E9	>1E16
Write operating voltage (V)	15	15	0.6/ – 0.2	<0.5
Read operating voltage (V)	2	1	0.15	<0.2
Write energy (J/bit)	>1E–14	>1E–15	5E–14	1E–15

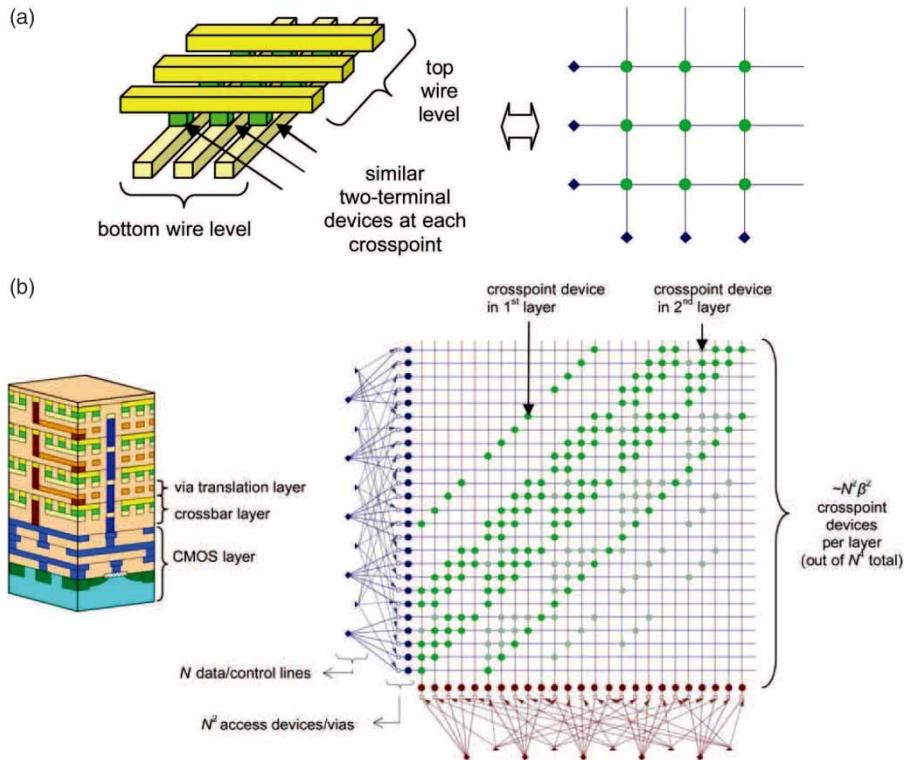


Figure 53. (a) Single crossbar array and its equivalent circuit representation. (b) Three-dimensional hybrid CMOS/crossbar circuit and its equivalent circuit diagram. We note that in this case each crossbar layer has a connectivity pattern different from that in (a). Reprinted with permission from D.B. Strukov and R.S. Williams, Proceedings of the National Academy of Sciences 106, pp. 20155–20158, 2009 [231]. Copyright © (2009) by PNAS.

A single crossbar array ReRAM architecture is called CMOL [238,239] (Cmos+MOlecular-scale devices) combining a single crossbar layer (see Figure 53(a)) with a conventional CMOS layer. In the recently suggested three-dimensional extension of CMOL technology [231], a single CMOS layer is located underneath multiple crossbar layers separated by translation layers (Figure 53(b)). In such an architecture, each memristive element can be accessed via a unique four-dimensional address (for a single crossbar layer, the address is two-dimensional) [231].

As we have noted in Section 3.2, the implementation of crossbar array memory may be complicated as a crossbar array represents a resistive network so that the current between any two selected word and bit lines can flow through many memristive devices. One of the approaches to overcome this problem is to use individual access devices such as diodes or transistors. Another approach was recently suggested by Wang *et al.* [240]. In order to write information into a specific cell, they propose to apply $V/2$ and $-V/2$ voltages to the corresponding word and bit lines, and zero voltage to all other lines. In this way, only the selected cell will be subjected to V voltage amplitude and all other cells will experience $\pm V/2$ or 0 bias. Assuming that the switching occurs when the applied voltage amplitude is above $V/2$, the change of only selected cell becomes possible. A disadvantage of this approach is that the current still will flow through all memristive elements connected to two selected lines dramatically increasing the power dissipation when utilizing many-element crossbar arrays.

A detailed overview of emergent storage memory technologies can be found in the review paper [241].

7.1.2. Logic

Another important application of memristive systems is in the field of digital logic circuits. On the one hand, memristive systems can serve as configuration bits and switches in a data-routing network, and on the other hand, they can be used to perform logic operations. In particular, Strukov and Likharev [242,243] have shown the potential of using CMOL circuits in the areas of field-programmable gate arrays (FPGAs) [242] and image processing [243]. The efficiency analysis shows that memristive FPGAs are much faster and more energy efficient in comparison with similar traditional devices based on CMOS technology [244]. Hybrid reconfigurable logic circuits [245], and logic circuits with a “self-programming” capability [246] (namely, with a capability of a circuit to reconfigure itself) were demonstrated. In both studies, titanium-dioxide thin-film memristive systems were used as basic device structures.

In stateful logic architecture, the “state” of the memristive system acts as both a logic gate and a latch (bistable circuit element capable of holding one bit of information). The concept of crossbar latch was discussed in [248] where a device storing a logic value, enabling logic value restoration and inversion was demonstrated. It was concluded that such functionality, in combination with resistor/diode logic gates, enables universal computing [248], namely given a description of any other computer or program and some data, it can perfectly emulate this second computer or program. Recently, Borghetti *et al.* have experimentally demonstrated a realization of material implication and NAND operation with memristive elements [249]. In addition, Lehtonen and Laiho [247,250] have analyzed how many additional memristive elements, in addition to memristive systems holding initial values, are needed to compute any Boolean function. Their conclusion is that two memristive systems are indeed enough to compute all Boolean functions [250].

To understand logic operations with memristive systems, let us consider a realization of material implication shown in Figure 54. In this circuit, voltages $|V_{cond}| < |V_{set}|$ are used in circuit operation, state 0 corresponds to the high-resistance state of memristive systems, and state 1 is the low-resistance state, and the memristive systems are connected to a load resistor. The circuit operation is based on the threshold-type behavior of experimentally realizable memristive systems (see, e.g. the equation for \dot{x} in Table 6). The calculation result is stored in m_2 .

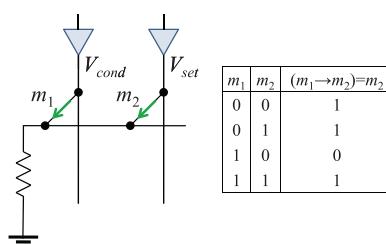


Figure 54. Material implication with memristive systems. State 0 (“false”) corresponds to the high-resistance state of memristive system, and state 1 (“true”) is the low-resistance state. The triangles indicate the external driver circuits that set the voltages V_{cond} and V_{set} . The memristive systems are connected to a load resistor. Memristance m_1 value does not change from its initial state during operation, while memristance m_2 changes according to the value of m_1 . The final result is stored in m_2 . All these are indicated by the symbol $(m_1 \rightarrow m_2) = m_2$, namely the material implication logic operation $(m_1 \rightarrow m_2)$ is stored (=) into m_2 . Reprinted with permission from E. Lehtonen and M. Laiho, Proceedings of the 2009 International Symposium of Nanoscale Architectures (NANOARCH’09) p. 33, 2009 [247]. Copyright © (2009) by the IEEE.

First of all, we note that the amplitudes of V_{cond} and V_{set} are selected in such a way that the voltage on m_1 never exceeds the threshold. Therefore, the state of m_1 remains unchanged. When m_1 is in the high-resistance state ($m_1=0$) and V_{cond} and V_{set} are applied, the voltage on m_2 exceeds the threshold leading to the transition of m_2 from 0 to 1. However, under the same conditions but with $m_1=1$, the voltage drop on m_2 is reduced and the transition of m_2 from 0 to 1 is prohibited. Symbolically, material implication operation can be expressed as

$$(m_1 \rightarrow m_2) = m_2, \quad (102)$$

namely the logic operation $m_1 \rightarrow m_2$ is stored in m_2 . Material implication, together with the possibility of reset (by changing polarity of V_{set}), is functionally complete, thus providing an opportunity to compute any Boolean function [247].

However, to the best of our knowledge, the actual sequences of operations to realize other logic gates were not reported anywhere in the literature. Therefore, below we provide the realization of the basic logic functions NOT, OR and AND. In these operations, an additional memristive element m_3 is used.

$$\text{NOT}(m_1) = m_2 : m_2 = 0; (m_1 \rightarrow m_2) = m_2, \quad (103)$$

$$\text{OR}(m_1, m_2) = m_2 : m_3 = 0; (m_1 \rightarrow m_3) = m_3; (m_3 \rightarrow m_2) = m_2, \quad (104)$$

$$\begin{aligned} \text{AND}(m_1, m_2) = m_2 : m_3 = 0; (m_2 \rightarrow m_3) = m_3; (m_1 \rightarrow m_3) = m_3; \\ m_2 = 0; (m_3 \rightarrow m_2) = m_2. \end{aligned} \quad (105)$$

Based on material implication, an algorithm for adding two numbers was suggested [247]. However, this operation requires a large number of steps. In order to overcome this deficiency, the present authors have suggested a modification of the circuit shown in Figure 54 by adding a memcapacitive element [251]. In such a configuration, “input” memristive systems can be distinguished from “output” ones. The operation of the modified circuit is based on charging the memcapacitive system through the input memristive system and discharging it through output ones. This protocol requires smaller number of steps to perform both main logic and arithmetic operations. In fact, the basic logic operations (NOT, AND and OR) as well as addition of two one-bit numbers were experimentally demonstrated using memristor emulators [251] (see also Section 7.2.5).

We would like to point out that several hybrid circuit layouts were patented that could perform these types of operations (see, e.g. [252,253]). We also note that, since memory-circuit elements are intrinsically analog devices (they acquire a continuous set of values within a certain range), they could also be used to generate “fuzzy logic” [254], namely non-Boolean logic operations, such as statements of the type (IF variable IS property THEN action), $m_1 > m_2$, etc. However, we are not aware of any experimental (or theoretical) work in this direction.

7.2. Analog applications

7.2.1. Neuromorphic circuits

Another potential exciting application of memristive systems – and, possibly, the most important among analog applications – is in neuromorphic circuits. Neuromorphic circuits are circuits that are designed to mimic the (human or animal) brain. In these circuits, memristive systems (and possibly also memcapacitive systems) can be used as synapses to provide connections between neurons and store information. As anticipated in Section 3.2.1, the small size of solid-state memristive systems is highly beneficial for this application since the density of memristive systems in a

chip can be of the same order of magnitude as the density of synapses in human brains ($\sim 10^{10}$ synapses/cm²) [255]. Therefore, using memristive systems, the fabrication of an artificial neural network of a size comparable to that of a biological brain becomes possible.

An important feature of biological synapses is the spike-timing-dependent plasticity (STDP) [256–259]. In fact, when a post-synaptic signal reaches the synapse *before* the action potential of the pre-synaptic neuron, the synapse shows long-term depression, namely its strength decreases (smaller connection between the neurons) depending on the time difference between the post-synaptic and the pre-synaptic signals. Conversely, when the post-synaptic action potential reaches the synapse *after* the pre-synaptic action potential, the synapse undergoes a long-time potentiation, namely the signal transmission between the two neurons increases in proportion to the time difference between the pre- and the post-synaptic signals. These general features of biological synapses can be implemented using different types of memristive systems [251]. We can distinguish three general approaches to STDP realization in artificial neural networks: using an overlap of asymmetric pulses [251,255,261], employing additional CMOS circuitry to track pulse timing [262], and utilizing higher-order memristive systems with intrinsic pulse-timing tracking capability [251].

A model of such a higher-order memristive system that is capable to track time separation between post- and pre-synaptic action potentials was suggested by the present authors in [251]. We provide the details of the model in Table 17, where, γ is a constant, V_t a threshold voltage, y_t a threshold value of the internal variable y , τ a constant defining the time window of STDP. It is assumed that short (e.g. approximately 1 ms width) pre- and post-synaptic square pulses of the same polarity are applied to the second-order memristive system. According to the equation for $R_M = x_1$, the memristance can change when $|y| \geq y_t$. The change of $y = x_2$ is described by an equation the right-hand side of which contains excitation terms involving θ -functions and a relaxation term $-y/\tau$. Therefore, after being excited, the decay of the variable y occurs with a decay constant τ . The particular combination of θ -functions in this equation defines the excitation rules: (i) the excitation is possible only when $|V| > V_t$ and (ii) the variable y excited by a certain polarity of the voltage applied to the memristive system (V is given by a difference of pre- and post-synaptic potentials) cannot be re-excited by a pulse of opposite polarity if $|y| > y_t$. We also note that the change in memristance described by the equations in Table 17 is constrained between R_{\min} and R_{\max} . These constraints are similar to those previously reported in Table 6.

Experimentally, several circuits showing neuromorphic behavior of different types and complexities were demonstrated [14,262–265]. These circuits were based on two- [14,262,263] and three-terminal [264–266] memristive devices. Jo *et al.* [262] have demonstrated a spike-timing-dependent plasticity using a crossbar array of Ag-based memristive synapses. In their architecture, CMOS elements were used to analyze timing of pre- and post-synaptic pulses in order to generate positive or negative memristive device programming pulses. In Figure 55, we show a comparison

Table 17. Memristive model of an artificial memristive synapse with timing-tracking capability [251]. All parameters are explained in the text.

Physical system	Artificial memristive synapse
Internal state variable(s)	Resistance and timing variable, $x_1 = R_M$, $x_2 = y$
Mathematical description	$I = x_1^{-1} V$ $\frac{dx_1}{dt} = \gamma[\theta(V - V_t)\theta(x_2 - y_t) + \theta(-V - V_t)\theta(-x_2 - y_t)]x_2\theta(x_1 - R_{\min})\theta(R_{\max} - x_1)$ $\frac{dx_2}{dt} = \frac{1}{\tau}[-V\theta(V - V_t)\theta(y_t - x_2) - V\theta(-V - V_t)\theta(x_2 + y_t) - x_2]$
System type	Second-order voltage-controlled memristive system

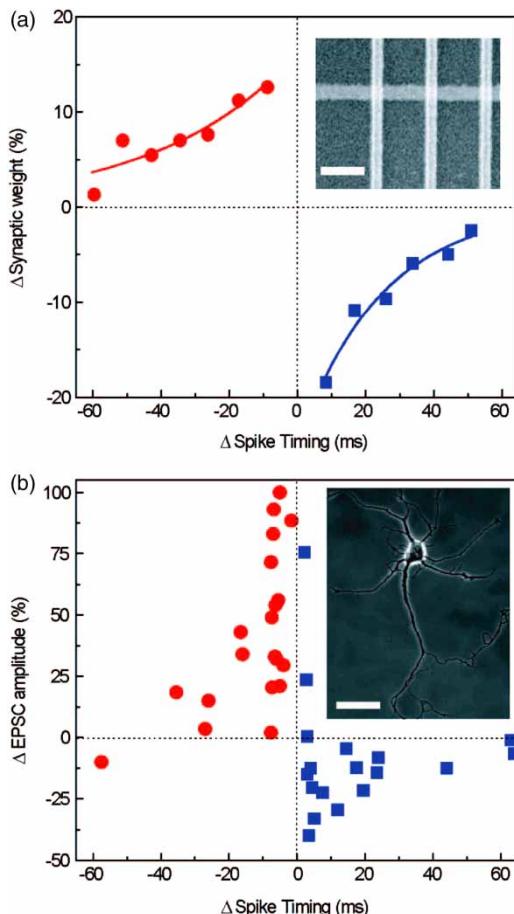


Figure 55. (a) Measured change in the synaptic weight versus spike separation. Inset: SEM image of the memristive crossbar array, scale bar is 300 nm. (b) Measured change in excitatory post-synaptic current of rat neurons after repetitive correlated spiking versus relative spiking timing. Inset: image of a hippocampal neuron (adapted by permission from Macmillan Publishers Ltd: Nature Protocols [259], Copyright © (2006)). Scale bar is 50 μ m. Reprinted with permission from S.H. Jo *et al.*, Nano Letters 10, pp. 1297–1301, 2010 [262]. Copyright (2010) American Chemical Society.

of STDP of artificial synapses with changes in excitatory post-synaptic current of rat hippocampal neurons [262]. Choi *et al.* [263] have built a crossbar array of $\text{GdO}_x/\text{Cu-doped MoO}_x$ memory and demonstrated a weight sum operation important for neural networks.

Three-terminal memristive devices employed in recent experiments [264,265] were of a transistor structure in which the gate electrode was typically used to induce resistance changes probed by a current through two other electrodes. Lai *et al.* [265] have demonstrated a synaptic transistor showing STDP. They have used a conventional MOS transistor structure with a conjugated polymer (MEH-PPV) layer and a layer of ionic conductor RbAg_4I_5 placed below the gate electrode. Peculiar features of their experiments are paired spikes composed of 1 ms positive and 1 ms negative voltage pulses. In Figure 56, an experimentally measured STDP of such synaptic devices is demonstrated. Alibart *et al.* [264] have fabricated a nanoparticle organic memory field-effect transistor (NOMFET) with memory response due to charging of gold nanoparticles embedded into a layer of pentacene thin film. Using this NOMFET, they have observed facilitating and depressing

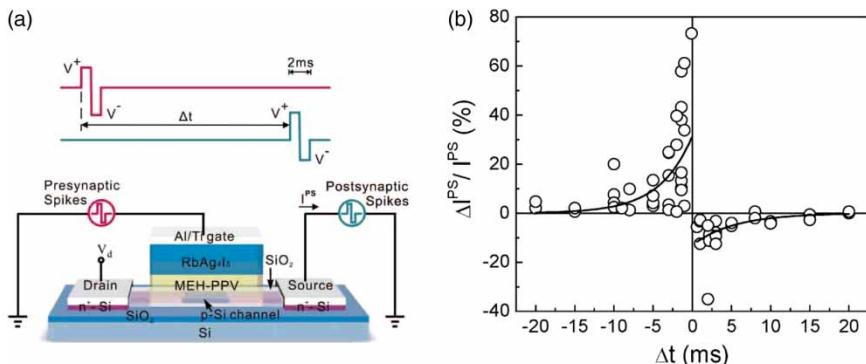


Figure 56. (a) Synaptic transistor structure. (b) The relative changes of the post-synaptic currents measured after application of 120 pairs of temporally correlated pre- and post-synaptic spikes. Q. Lai *et al.*, Advanced Materials, 2010, 20, p. 2448 [265]. Copyright © Wiley-VCH Verlag GmbH & Co. KGaA. Reproduced with permission.

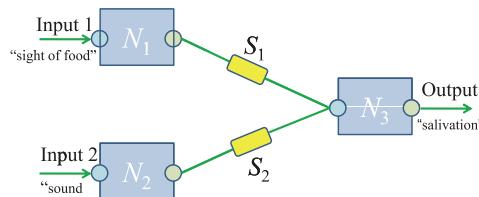


Figure 57. Artificial neural network for associative memory composed of three neurons (N_1 , N_2 and N_3) coupled by two memristive synapses (S_1 and S_2). The output signal is determined by input signals and strengths of synaptic connections which can be modified when learning takes place. Reprinted from Neural Networks 23, Y.V. Pershin and M. Di Ventra, p. 881, Copyright © (2010) with permission from Elsevier [14].

synaptic behavior. Possible drawbacks of this approach include charge leaking limiting retention time in the range of a few seconds to a few thousand of seconds and a high amplitude voltage (~ 50 V) needed for the circuit operation [264]. In a recent paper [266], a crossbar array architecture integrating optically gated carbon nanotubes was also suggested for neuromorphic applications.

Pershin and Di Ventra [14] have reported the experimental realization of a neural network based on memristor emulators (see Section 7.2.5 for their electronic scheme) demonstrating associative learning. The neural network used in that experimental study contains two memristive synapses and three neurons as shown in Figure 57. Associative memory is a fundamental property of the animal brain closely related to the so-called Pavlovian training [267] in which a particular response to a given stimulus develops. The most notable experiment of associative memory is that of a dog to which food is shown and, at the same time, the tone of a bell is rang so that, with time, the dog salivates at the ring of the bell only. In the electronic three-neuron network described in [14], two input neurons were responsible for the “sight of food” and “sound” events, while the output neuron generated a “salivation” command.

Figure 58 demonstrates experimental results of the neural network operation. The functioning of the electronic circuits is essentially based on pulse overlapping. When Input 1 is excited, the first neuron N_1 sends forward positive-polarity pulses that excite the third neuron N_3 which starts sending positive pulses in the forward direction and negative pulses backward. If, at the same time, the second neuron N_2 is also excited, the overlap of positive pulses from this second neuron and negative pulses from the third neuron over S_2 memristive synapse results in a voltage on S_2

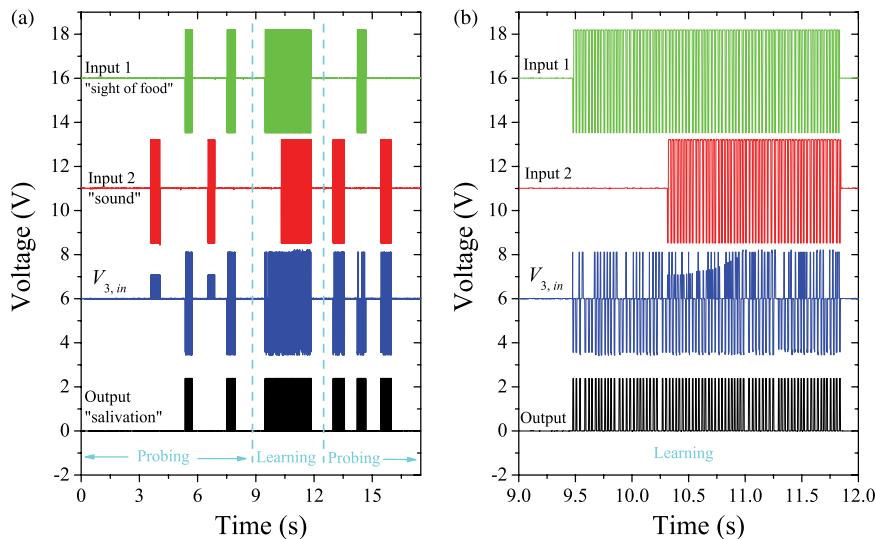


Figure 58. Development of associative memory. (a) Signal patterns in an electronic circuit corresponding to the neural network shown in Figure 57. Such a circuit employs electronic neurons and electronic synapses (memristor emulators) (see [14] for more details). At the initial moment of time, S_1 synapse is in a low-resistance state, while S_2 synapse is in a high-resistance state. Correspondingly, in the first probing phase, when Input 1 and Input 2 signals are applied without overlapping, the output signal develops only when Input 1 signal is applied. In the learning phase (see also (b) for more detailed picture), Input 1 and Input 2 signals are applied simultaneously. According to Hebbian rule, simultaneous firing of input neurons leads to development of a connection, which, in the present case, is a transition of the second synapse S_2 from high- to low-resistance state. This transition is clearly seen as a growth of certain pulses in the signal $V_{3,in}$ (voltage at the input of third (output) neuron) in the time interval from 10.25 to 11 s in (b). In the subsequent probing phase, we observe that “firing” of any input neuron results in the “firing” of output neuron, and thus an associative memory realization has been achieved. The curves in (a) and (b) were displaced for clarity. Reprinted from Neural Networks 23, Y.V. Pershin and M. Di Ventra, p. 881, Copyright © (2010) with permission from Elsevier [14].

exceeding its threshold. In this way, the S_2 resistance decreases, or, in other words, an association develops.

If we return to Figure 58 again, it clearly shows that, if one starts with an untrained state of the synapse connecting the input “sound” neuron and output neuron and exposes the neural network to “sight of food” and “sound” signals simultaneously, then an association between “food” and “sound” develops and an output signal is generated when only the “sound” input signal is applied. This is exactly the associative memory behavior discussed above.

7.2.2. Quantum computing with memory-circuit elements

Memcapacitive and meminductive systems may find useful applications in electronic circuits with superconducting qubits [268,269]. Since typical superconducting qubit circuits involve usual capacitors and inductors [268,269], certain memcapacitive and meminductive elements are ideal for such circuits. What are the advantages of using memory elements in superconducting qubit circuits? One of many possible applications is *field-programmable quantum computing* that was recently discussed by the present authors [251]. The idea is to replace capacitive (inductive) elements that provide coupling between different qubits by non-dissipative memcapacitive

(meminductive) elements and introduce additional voltage sources to control the state of these memory elements. In this way, the coupling strength between qubits can be selected. If we consider N simultaneously interacting qubits, then a variation of coupling between two of them will result in absolutely different interaction Hamiltonians, thus leading to a different system evolution. Quantum computation algorithms will thus benefit from such novel quantum hardware functionality because of the many (practically infinite) interaction schemes that can be implemented within a single circuit architecture [251]. We would like to note, however, that for such application, we envision memcapacitive and meminductive elements that are non-dissipative (at least within certain time scales), so that they do not introduce additional qubit relaxation/decoherence.

It might be well to point out that Josephson junctions coupled with nanomechanical resonators were studied in the past [270–274]. For example, it was shown in [270] that a nanomechanical resonator consisting of a piezoelectric crystal sandwiched between split metal electrodes can be used to provide coupling between phase qubits. Such a resonator has signatures of a memcapacitive system in which elastic vibrations play an important role. However, the coupling provided by the resonator is of a constant strength [270] and, therefore, it cannot be directly used for the field-programmable quantum computing idea discussed above.

7.2.3. Learning circuits

Quite generally, a “learning circuit” is an electronic circuit whose response at a given time adapts according to signals applied to the circuit at previous moments of time [92]. All three memory-circuit elements are ideal components for such a circuit since they provide non-volatile information storage and compatibility (as time-dependent devices) with other circuit elements. The present authors have recently suggested [92] a learning circuit which mimics adaptive behavior of a slime mold *Physarum polycephalum* from the group of amoebozoa. This work was inspired by recent experimental observations on this unicellular organism [275]. These experiments have shown that when *P. polycephalum* is exposed to a pattern of periodic environment changes (of temperature and humidity), it “learns” and adapts its behavior in anticipation of the next stimulus to come. We have shown [92] that such behavior can be described by the response of a simple electronic circuit as that shown in Figure 59(a). The circuit is composed of an LC contour and a memristive system in parallel with the capacitor. The memristive system was described by the equations presented in table 6 that was introduced in Section 3.2.4. This model takes into account the non-linear memristance rate of change defined by two parameters α and β (see also Figure 59(a)).

Figure 59(b) represents simulation results of the response of the circuit. When a periodic signal is applied to the learning circuit, the voltage across the capacitor significantly changes and can exceed the threshold voltage of the memristive system. This leads to an increase in the resistance of the memristive system and, consequently, in a smaller damping of the LC contour. Therefore, the LC contour oscillations are maintained for a longer period of time in analogy with the same type of behavior observed when the amoeba is subject to periodic environment changes.

Very recently, an electronic circuit [276] having a close similarity to the learning circuit in Figure 59(a) was experimentally implemented. In this circuit, a vanadium dioxide memristive system was placed into an LC contour. It was demonstrated that the application of specific frequency signals sharpens the quality factor of its resonant response, and thus the circuit “learns” according to the input waveform.

7.2.4. Programmable analog circuits

In programmable analog circuits, memristive systems that operate under threshold conditions (as those described in the previous section) can be used as digital potentiometers [106]. The main

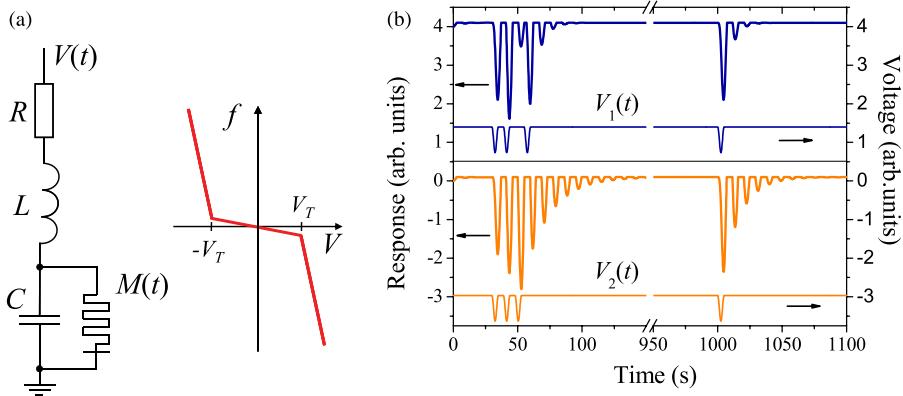


Figure 59. (a) Schematic representation of the learning circuit and sketch of the selected rate function f . The learning circuit contains four two-terminal circuit elements: resistor R , inductor L , capacitor C and memristive system M . The function f responsible for memristive system dynamics depends on the voltage applied to the system according to $f(V) = -\beta V + 0.5(\beta - \alpha)(|V + V_T| - |V - V_T|)$, where α and β are positive constants and V_T is a threshold voltage. (b) Modeling of the circuit response. This plot demonstrates that stronger and long-lasting responses for both spontaneous in-phase slowdown and spontaneous in-phase slowdown after one disappearance of the stimulus [275] are observed only when the circuit was previously “trained” by a periodic sequence of three equally spaced pulses as present in $V_2(t)$. The applied voltage $V_1(t)$ is irregular and thus the three first pulses do not “train” the circuit (see [92] for more details). The lines were displaced vertically for clarity. Reprinted figure with permission from Y.V. Pershin *et al.*, Physical Review E 80, p. 021926, 2009 [92] Copyright © (2009) by the American Physical Society.

idea is to apply small-amplitude voltages to memristive systems when they are used as analog circuit elements, and high amplitude voltage pulses for the purpose of resistance programming. Since the state of memristive system appreciably changes only when the voltage applied to it exceeds a certain threshold [104], its resistance is constant in the analog mode of operation, and changes by discrete values with each voltage pulse. Using this idea, several programmable analog circuits demonstrating memristive system-based programming of threshold, gain and frequency were demonstrated by these authors [106].

7.2.5. Emulators of memristive, memcapacitive and meminductive systems

All of the above-mentioned programmable analog circuits were built using a memristor emulator [106] which is schematically shown in Figure 60(a). It consists of a microcontroller-controlled digital potentiometer with resistance calculated by the microcontroller using equations of a current-controlled or voltage-controlled memristive system. For these calculations, the value of the voltage applied to the scheme is provided by an analog-to-digital converter. Since virtually almost any set of memristive system equations can be pre-programmed, the memristor emulator offers a unique opportunity to simulate memristive behavior in electronic circuits.

Moreover, the present authors have suggested that specific circuits with memristive systems can emulate an effective memcapacitive and meminductive behavior [107]. The architecture of such circuits (see Figure 60(b) and (c)) is based on the gyrator scheme. In both memcapacitive system and meminductive system emulators, memory properties of the memristor emulator described above are effectively transferred to an effective memcapacitive and meminductive response.

For instance, let us consider the circuit of memcapacitive system emulator depicted in Figure 60(b). In this scheme, since the operational amplifier keeps nearly equal voltages at its

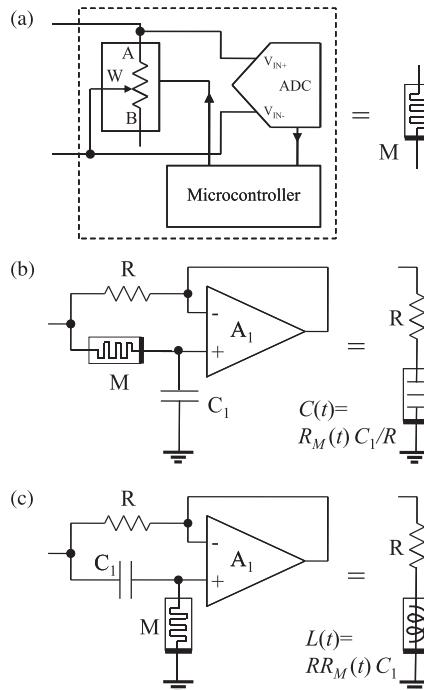


Figure 60. Circuits simulating (a) memristive system, (b) memcapacitive system and (c) meminductive system. Their approximate equivalent circuits are shown on the right. Reprinted with permission from Y.V. Pershin and M. Di Ventra, Electronics Letters 46, pp. 517–518, 2010 [107]. Copyright © (2010) by the IET.

positive and negative inputs, the voltage on the capacitor C_1 is applied to the right terminal of R . Therefore, we can think that an effective capacitor with a time-dependent capacitance $C(t)$ is connected to the right terminal of R , so that the relation $RC(t) = R_M(t)C_1$ holds.

Let us assume that a voltage-controlled memristive system is used in the memcapacitive system emulator. Then, equations describing the effective memcapacitor are given by

$$C(t) = \frac{R_M(V - V_C, x, t)C_1}{R} \quad (106)$$

$$\frac{dV_C}{dt} = \frac{1}{C_1} \frac{V - V_C}{R_M(V - V_C, x, t)}, \quad (107)$$

$$\frac{dx}{dt} = f(V - V_C, x, t), \quad (108)$$

where V is the applied voltage and V_C the voltage on the capacitor C_1 . In Equations (106)–(108), V_C acts as an additional state variable of the effective memcapacitive system. In fact, this is not surprising since the capacitor C_1 (in Figure 60(b)) stores information in the form of charge. Consequently, the order of the effective voltage-controlled memcapacitive system exceeds the order of the memristive system by one. The operation of the meminductive system emulator in Figure 60(c) can be understood in a similar manner. These emulators also show an interesting connection between the three memory elements. However, we need to stress that since the memcapacitive system and meminductive system emulators involve an extra resistance, they do not behave as pure memcapacitive or meminductive systems.

Biolek and Biolkova [277] have suggested a different scheme (mutator) transforming memristive behavior into memcapacitive one. Their approach uses two operational transimpedance amplifiers operating as the current conveyors. However, their suggested scheme responds as a *grounded* memcapacitive system although without an additional resistance R as that shown in the equivalent scheme in Figure 60(b).

Recently, floating emulators of memcapacitive and meminductive systems were proposed [278]. The circuits of these emulators are based on second-generation current conveyors and involve either four single-output or two dual-output current conveyors. The idea of the circuits is again to transform memristive behavior into a memcapacitive or meminductive one. Such floating emulators can be used in electronic circuits where any two voltages can be applied to a memcapacitive or meminductive device. It was shown in [278] that if the memristive element is described by

$$I_M = [R_M(x, V_M, t)]^{-1} V_M, \quad (109)$$

$$\frac{dx}{dt} = f(x, V_M, t), \quad (110)$$

then the equations governing an effective memcapacitive system (emulated by the proposed circuits) can be written as

$$Q = \frac{L}{RR_M(x, (V_1 - V_2), t)}(V_1 - V_2) \equiv C(x, (V_1 - V_2), t)(V_1 - V_2), \quad (111)$$

$$\frac{dx}{dt} = f(x, (V_1 - V_2), t) \quad (112)$$

and the equations of an effective meminductive system are given by

$$I = \frac{1}{CRR_M(x, \phi/RC, t)}\phi \equiv [L(x, \phi, t)]^{-1}\phi, \quad (113)$$

$$\frac{dx}{dt} = f(x, \phi/RC, t) \quad (114)$$

where V_1 and V_2 are voltages applied to the emulator, the phase ϕ is given by $\phi(t) = \int_0^t (V_1(t') - V_2(t')) dt'$, and L , C , R denote, respectively, inductance, capacitance and resistance of corresponding linear (traditional) circuit elements.

7.2.6. Other circuits

There are a few other memristive system-based analog circuits discussed in the literature [279–281]. In particular, an interesting method of using memristive systems as passive electromagnetic switches was suggested and analyzed by Bray and Werner [281]. Way and Benderli [280] have simulated and analyzed an architecture of an amplitude-modulation circuit. A circuit element combining diode and memory resistance properties, the *switchable rectifier*, was proposed and built by Shima *et al.* [279]. Their device based on Pt/TiO_x/Pt structure demonstrates a reproducible switching. Such a circuit element can find useful applications in both analog and digital domains.

Moreover, several authors have investigated chaotic circuits with memristors [282–287]. For the most part modified Chua's oscillators [288,289] were considered [282,283,285,286]. In such an approach, the active nonlinear resistance element, Chua's diode [289], is replaced by an *active* memristor (as we show in Figure 61) and novel features in chaotic behavior are observed [282,283,285,286]. An active memristor is the one for which Equation (30) is not satisfied. In fact, one such

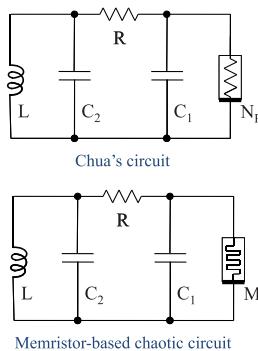


Figure 61. Original Chua circuit and chaotic memristive circuit using an *active* memristor. Reprinted with permission from B. Muthuswamy and P.P. Kokate, IETE Technical Review 26, pp. 417–429, 2009 [283]. Copyright © (2009) by The IETE.

circuit was implemented experimentally [290]. We have, however, recently shown that chaotic behavior does not require active memristors and even a single memristive system driven by an ac voltage can manifest chaos [291]. Moreover, chaos is observed when an ac voltage is applied to the bistable membrane memcapacitive system considered in Section 4.1.2 [171]. Apart from interesting fundamental studies of non-linear systems, the field of applications of such circuits includes secure communications with chaos [283].

8. Conclusions and outlook

In this review, we have shown that memory effects are ubiquitous in complex materials and nanoscale systems. This memory manifests itself under several physical properties – related to charge, spin and structural dynamics – which, however, can be generally categorized as memristive, memcapacitive and meminductive, or a combination of these. The advantage of these elements is based on a combination of a history-dependent behavior with properties of basic circuit elements – such as resistors, capacitors or inductors. The realization of this link between the underlying physical properties that lead to memory and their description in terms of memory-circuit elements opens up unprecedented opportunities in both fundamental science and applications, since it guides the discovery of novel functionalities, inspires new concepts and connections between apparently diverse fields, and in certain cases, it also allows a reconsideration of old concepts from a totally new perspective.

We have provided a large set of examples of systems where these memory effects are observed or expected. Clearly, due to the necessary space limitations of this review, we are far from having exhausted all possible physical systems and devices that show these features. Indeed, as we have also emphasized in this review, we firmly think that due to the continued miniaturization of devices, many more systems will be discovered that show memory. This confidence is supported by the physical fact that the change of state of electrons and ions is not instantaneous, rather it generally depends on the past dynamics.

We have also discussed many applications, ranging from information storage and programmable circuits to learning circuits and biologically inspired systems. In some cases, we also expect that the cost of certain practical implementations of these elements should be relatively low in view of their simple structure. It is thus not too unlikely that some of the systems we have discussed in this review may develop into commercially available products in the coming years.

and find their own niche of applications. We therefore anticipate that novel exciting applications will be developed with beneficial impact not only for technology, but also for fundamental science.

Acknowledgements

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