

## PART 3

### ① MIPS ENCODING

①.1 srl \$t3, \$t4, 10

INSTRUCTION CODING FORMAT : R-TYPE

OPCODE (6 BITS)	rs (5 bits)	rt (5 bits)	rd (5 bits)	SHAMT (5 bits)	FUNCTION (6 bits)
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srl rd, rt, shamt

OPCODE: 000000 (OPCODE FOR R-TYPE INSTRUCTIONS IS ALWAYS ZERO)

rs: 00000 (UNUSED FIELDS CODED WITH ALL 0 BITS)

rt: \$t4 = 12.

\$t0=8; \$t1=9; \$t2=10; \$t3=11; \$t4=12

rd: \$t3 = 11

SHAMT: 10

FUNCTION: 2 (FROM MIPS REFERENCE DATA CARD)

DECIMAL TO BINARY CONVERSIONS:

rt:  

$$\begin{array}{r} 12 \\ \hline 1 & 2 \\ \times & \quad 6 & 1 & 2 \\ \hline 0 & 3 & 1 & 2 \\ \times & \quad 1 & \leftarrow & 1 \end{array}$$

$$12_{10} = 1100_2$$

rd:  

$$\begin{array}{r} 11 \\ \hline 1 & 2 \\ \times & \quad 5 & 1 & 2 \\ \hline 1 & 0 & 2 & 1 & 2 \\ \times & \quad 1 & \leftarrow & 1 & \leftarrow \end{array}$$

$$11_{10} = 1011_2$$

SHAMT:  

$$\begin{array}{r} 10 \\ \hline 0 & 5 \\ \times & \quad 1 & 2 \\ \hline 0 & 2 & 1 & 2 \\ \times & \quad 1 & \leftarrow & 1 & \leftarrow \end{array}$$

$$10_{10} = 1010_2$$

FUNCTION:  

$$\begin{array}{r} 2 \\ \hline 0 & 4 & 1 \\ \times & \quad 2 \\ \hline 2_{10} = 10_2 \end{array}$$

BIN TO HEX

REPLACING BINARY NUMBERS ON THIS FIELD:

OPCODE	rs	rt	rd	SHAMT	FUNCTION
000000	00000	01100	01011	01010	000010
0x0	0x0	0x0	0xC	0x5	0xA

$$0000 = 0x0$$

$$0001 = 0x1$$

$$0010 = 0x2$$

$$0011 = 0x3$$

$$0100 = 0x4$$

$$0101 = 0x5$$

$$0110 = 0x6$$

$$0111 = 0x7$$

$$1000 = 0x8$$

$$1001 = 0x9$$

$$1010 = 0xA$$

$$1011 = 0xB$$

$$1100 = 0xC$$

$$1101 = 0xD$$

$$1110 = 0xE$$

$$1111 = 0xF$$

FIELDS WITH DECIMAL VALUES

OPCODE	rs	rt	rd	SHAMT	FUNCTION
0	0	12	11	10	2

MACHINE CODE: 0x000C5A82



1.2 lw \$t0, 32(\$s1)

INSTRUCTION CODING FORMAT : I-TYPE

OPCODE (6 bits)	rs (5 bits)	rt (5 bits)	IMMEDIATE (16 bits)
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lw rt, IMMEDIATE(rs)

OPCODE : 0x23 (FROM MIPS REFERENCE DATA CARD) 0010 0011

rs : \$s1 = 17      \$s0 = 16 ; \$t0 = 17

rt : \$t0 = 8

IMMEDIATE : 32

DECIMAL TO BINARY CONVERSIONS:

rs :

$$\begin{array}{r} 17 \mid 2 \\ \downarrow R \\ 8 \mid 2 \\ \downarrow R \\ 0 \mid 4 \mid 2 \\ \downarrow R \\ 0 \mid 2 \mid 12 \\ \downarrow R \\ 0 \mid 2 \mid 1 \end{array}$$

$$17_{10} = 10001_2$$

rt:

$$\begin{array}{r} 8 \mid 2 \\ \downarrow R \\ 0 \mid 4 \mid 2 \\ \downarrow R \\ 0 \mid 2 \mid 12 \\ \downarrow R \\ 0 \mid 2 \mid 1 \end{array}$$

$$8_{10} = 1000_2$$

IMMEDIATE: 32

$$\begin{array}{r} 32 \mid 2 \\ \downarrow R \\ 0 \mid 16 \mid 2 \\ \downarrow R \\ 0 \mid 8 \mid 2 \\ \downarrow R \\ 0 \mid 4 \mid 2 \\ \downarrow R \\ 0 \mid 2 \mid 2 \\ \downarrow R \\ 0 \mid 2 \mid 1 \end{array}$$

$$32_{10} = 100000_2$$

REPLACING BINARY NUMBERS ON THIS FIELD:

OPCODE	rs	rt	IMMEDIATE
100011	10001	01000	000000000000100000
0x8	0xE	0x2	0x8 0x0 0x0 0x2 0x0

OPCODE BINARY TO DECIMAL CONVERSION:

$$100011_2 = 1 \times 2^5 + 0 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 32 + 0 + 0 + 0 + 2 + 1 = 35$$

FIELDS WITH DECIMAL VALUES:

OPCODE	rs	rt	IMMEDIATE
35	17	8	32

MACHINE CODE: 0x8E280020



## ② MIPS DECODING

2.1  $\$x_{AE} \$09 \$020$

\* WHAT IS THE OPCODE (IN ASSEMBLY) OF THIS INSTRUCTION?

$$\$x_A = 1010_2$$

$$\$x_E = 1110_2$$

$$\$x_{AE} = \underbrace{1010}_{\text{OPCODE}} \underbrace{1110}_2$$

$$101011_2 = \$x_{2B}$$

ACCORDING TO THE MIPS REFERENCE DATA CARD THE OPCODE IN ASSEMBLY FOR  $\$x_{2B}$  IS SW

\* WHAT TYPE (I/J/R) IS THIS INSTRUCTION?

ACCORDING TO THE MIPS REFERENCE DATA CARD THE INSTRUCTION TYPE IS I-TYPE

\* WHICH REGISTERS ARE READ/UPDATED IN EXECUTING THIS INSTRUCTION? YOU CAN USE EITHER ASSEMBLY NAMES OR REGISTER NUMBERS IN YOUR ANSWER.

$$\$x_{AE} \$09 \$020 = 101011000001001000000000100000_2$$

I-TYPE INSTRUCTION FIELDS:

OPCODE (6 bits)	rs (5 bits)	rt (5 bits)	IMMEDIATE (16 bits)
101011	10000	01001	00000000000100000

## BINARY TO DECIMAL CONVERSIONS:

$$rs: 100000_2 = 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 0 \times 2^0 = 16 + 0 + 0 + 0 + 0 \\ = 16_{10}$$

$$rt: 010001_2 = 0 \times 2^4 + 1 \times 2^3 + 0 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 = 0 + 8 + 0 + 0 + 1 \\ = 9_{10}$$

REGISTERS USED: \$9 OR \$t3, AND \$16 OR \$s0

\* WHAT IS THE ADDRESS OF THE NEXT INSTRUCTION WE WILL FETCH AND EXECUTE? IF THE INSTRUCTION IS A CONDITIONAL BRANCH, GIVE TWO POSSIBLE ADDRESSES. GIVE THE ANSWER AS A HEXADECIMAL VALUE AND SHOW THE ADDRESS CALCULATION STEPS TO GET FULL CREDIT.

ASSUMING THE MIPS INSTRUCTION IS AT ADDRESS

0x 00800100

NEXT INSTRUCTION ADDRESS:

$$0x 00800100 + 0x 4 = 0x 00800104$$

2.2  $0x52530011$

\* WHAT IS THE OPCODE (IN ASSEMBLY) OF THIS INSTRUCTION?

$$0x1 = 0001_2$$

$$0x2 = 0010_2$$

$$0x12 = \underbrace{000100}_\text{OPCODE}0_2$$

$$\underbrace{000100}_2 = 0x4$$

$$0x4$$

ACCORDING TO THE MIPS REFERENCE DATA CARD THE OPCODE IN ASSEMBLY FOR  $0x4$  IS  $beg$

\* WHAT TYPE (I/J/R) IS THIS INSTRUCTION?

ACCORDING TO THE MIPS REFERENCE DATA CARD THE INSTRUCTION TYPE IS I-TYPE

\* WHICH REGISTERS ARE READ/UPDATED IN EXECUTING THIS INSTRUCTION? YOU CAN USE EITHER ASSEMBLY NAMES OR REGISTER NUMBERS IN YOUR ANSWER

$$0x52530011 = 000100100101001100000000000010001$$

I-TYPE INSTRUCTION FIELDS:

OPCODE (6 bits)	rs (5 bits)	rt (5 bits)	IMMEDIATE (16 bits)
000100	10010	10011	00000000000010001

BINARY TO DECIMAL CONVERSIONS:

$$rs: 10010_2 = 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 0 \times 2^0 = 16 + 0 + 0 + 2 + 0 \\ = 18_{10}$$

$$rt: 10011_2 = 1 \times 2^4 + 0 \times 2^3 + 0 \times 2^2 + 1 \times 2^1 + 1 \times 2^0 = 16 + 0 + 0 + 2 + 1 \\ = 19_{10}$$

$$\$50 = 16 ; \$51 = 17 ; \$52 = 18 ; \$53 = 19$$

REGISTERS USED: \$18 OR \$52, AND \$19 OR \$53

\* WHAT IS THE ADDRESS OF THE NEXT INSTRUCTION WE WILL FETCH AND EXECUTE? IF THE INSTRUCTION IS A CONDITIONAL BRANCH, GIVE TWO POSSIBLE ADDRESSES. GIVE THE ANSWER AS A HEXADECIMAL VALUE AND SHOW THE ADDRESS CALCULATION STEPS TO GET FULL CREDIT.

$$PC = 0x00800100$$

ADDRESS AFTER FALSE CASE:

$$\text{NewAddr} = PC + 4 = 0x00800100 + 0x4 = 0x00800104$$

ADDRESS AFTER TRUE CASE:

$$\text{IMMEDIATE: } 0000000000010001_2 = 0x0000000000010001$$

$$\begin{aligned}\text{NewAddr} &= (PC + 4) + 4 * \text{IMMEDIATE} \\ &= (0x00800100 + 0x04) + 0x04 * 0x11 \\ &= 0x00800104 + 0x44\end{aligned}$$

$$\begin{array}{r} 0x00800104 \\ + 0x44 \\ \hline 0x00800148 \end{array} \rightarrow \text{New Addr}$$

THE TWO POSSIBLE ADDRESSES ARE:

$$0x00800104 \text{ AND } 0x00800148$$

2.3  $\text{0x0800AABB}$

\* WHAT IS THE OPCODE (IN ASSEMBLY) OF THIS INSTRUCTION?

$$\text{0x0} = 0000_2$$

$$\text{0x8} = 1000_2$$

$$\text{0x08} = \underbrace{00001000}_\text{OPCODE}_2$$

$$00001000_2 = 0x2$$

ACCORDING TO THE MIPS REFERENCE DATA CARD THE OPCODE IN ASSEMBLY FOR  $0x2$  IS ~~j~~  $\text{j}$

\* WHAT TYPE (I/J/R) IS THIS INSTRUCTION?

ACCORDING TO THE MIPS REFERENCE DATA CARD THE INSTRUCTION TYPE IS J-TYPE

\* WHICH REGISTERS ARE READ/UPDATED IN EXECUTING THIS INSTRUCTION?

THIS INSTRUCTION DO NOT READ OR UPDATE ANY REGISTER.

\* WHAT IS THE ADDRESS OF THE NEXT INSTRUCTION WE WILL FETCH AND EXECUTION?

J INSTRUCTION FORMAT:

OPCODE (6 bits)	ADDRESS (26 bits)
000010	000000000001010101010111011

$$\text{0x0800AABB} = 0000100000000000010101010111011$$

OPERATION OF JUMP INSTRUCTION:  $\text{PC} = \text{Jump Addr}$

$$\text{JumpAddr} = \{ \text{PC} + 4[31:28], \text{ADDRESS}, 2'6 \emptyset \}$$

$$\text{PC} + 4 = \text{0x00800100} + \text{0x04} = \text{0x00800104}$$

$$\text{PC} + 4[31:28] = 0000_2$$

ADDRESS = 00000000001010101010111011

$$2^6 \phi = \phi\phi$$

Jump Addr = {000000000000000000101010101011101100}  
0x0 0x0 0x0 0x2 0xA 0xA 0xE 0xC

THE ADDRESS OF THE NEXT INSTRUCTION IS :

0x0002AAEC

③ CONSIDER THE FOLLOWING MIPS CODE

LOOP: sll \$t2, \$0, \$t1  
      beq \$t2, \$0, DONE  
      addi \$t1, \$t1, -2  
      addi \$s2, \$s2, 1  
      j LOOP

DONE:

ASSUMING THAT \$t1=20 AND \$s2=0 INITIALLY

① WHAT IS THE FINAL VALUE OF \$s2 ?

THE LOOP FINISH WHEN \$t1==0 , THAT HAPPENS WHEN  
\$t1 = 20-2\*(10) , (FROM addi \$t1, \$t1, -2) ← THIS LINE MUST  
BE REPEATED 10 TIMES TO ACHIEVE \$t1==0 , ALSO THE  
LINE addi \$s2, \$s2, 1 REPEATS 10 TIMES , SO THE FINAL  
VALUE OF \$s2 IS TEN (10)

② HOW MANY MIPS INSTRUCTIONS WILL BE EXECUTED FOR THE GIVEN  
SEQUENCE ? FROM THE FIRST QUESTION , THE 5 INSTRUCTIONS  
INSIDE THE LOOP ARE REPEATED 10 TIMES EACH ONE , PLUS ONE  
MORE TIME FOR THE TWO FIRST INSTRUCTIONS (50+2) WHEN \$t1==0  
THEN \$t2 BECOMES ZERO , THE CONDITION IS TRUE AND THE JUMP TO  
DONE LABEL IS EXECUTED FINISHING THE SEQUENCE . THE ANSWER IS 52

④

TRANSLATE FUNCTION FOO INTO MIPS ASSEMBLY LANGUAGE.  
YOU MUST FOLLOW MIPS REGISTER USAGE CONVENTIONS FOR  
FUNCTION CALLS/RETURNS AS DISCUSSED IN CLASS. ASSUME THE  
FUNCTION DECLARATION OF BAR IS "INT BAR(INT X);", AND A  
LABEL BAR MARKS THE STARTING POINT OF ITS FUNCTION BODY.  
YOU CAN ASSUME THAT FUNCTION BAR FOLLOWS THE SAME MIPS  
CONVENTIONS BUT DO NOT NEED TO IMPLEMENT IT.

```
void foo(int *vals){  
    while (bar(*vals) != 0){  
        vals++;  
    }  
}
```

# MIPS:

```
FOO:   ADDI $SP,$SP,-32    # MAKING SPACE ON THE STACK  
       SW $RA,28($SP)    # STORING $RA ON THE STACK  
       SW $SO,24($SP)    # STORING $SO ON THE STACK  
       ADDU $SO,$0,$A0    # COPYING $A0 (FOO ARGUMENT) TO $SO  
WHILE:  LW $A0,($SO)    # LOADING THE CONTENT OF $SO ADDRESS ON $A0  
       JAL BAR          # CALL TO BAR FUNCTION WITH $A0=*VALS AS ARGUMENT  
       BEQ $V0,$0,FOOEND  # WHILE (BAR(*VALS)) != 0  
       ADDI $SO,$SO,4      # VALS++; INCREMENT ADDRESS TO NEXT INT  
       J WHILE           # JUMP TO WHILE LABEL TO REPEAT  
FOOEND: LW $SO,24($SP)  # READ FROM STACK AND STORE TO $SO  
       LW $RA,28($SP)  # READ FROM STACK AND STORE TO $RA  
       ADDI $SP,$SP,32    # RESTORE $SP VALUE BEFORE FOO CALL  
       JR $RA            # JUMP TO INSTRUCTION NEXT TO FOO CALL
```