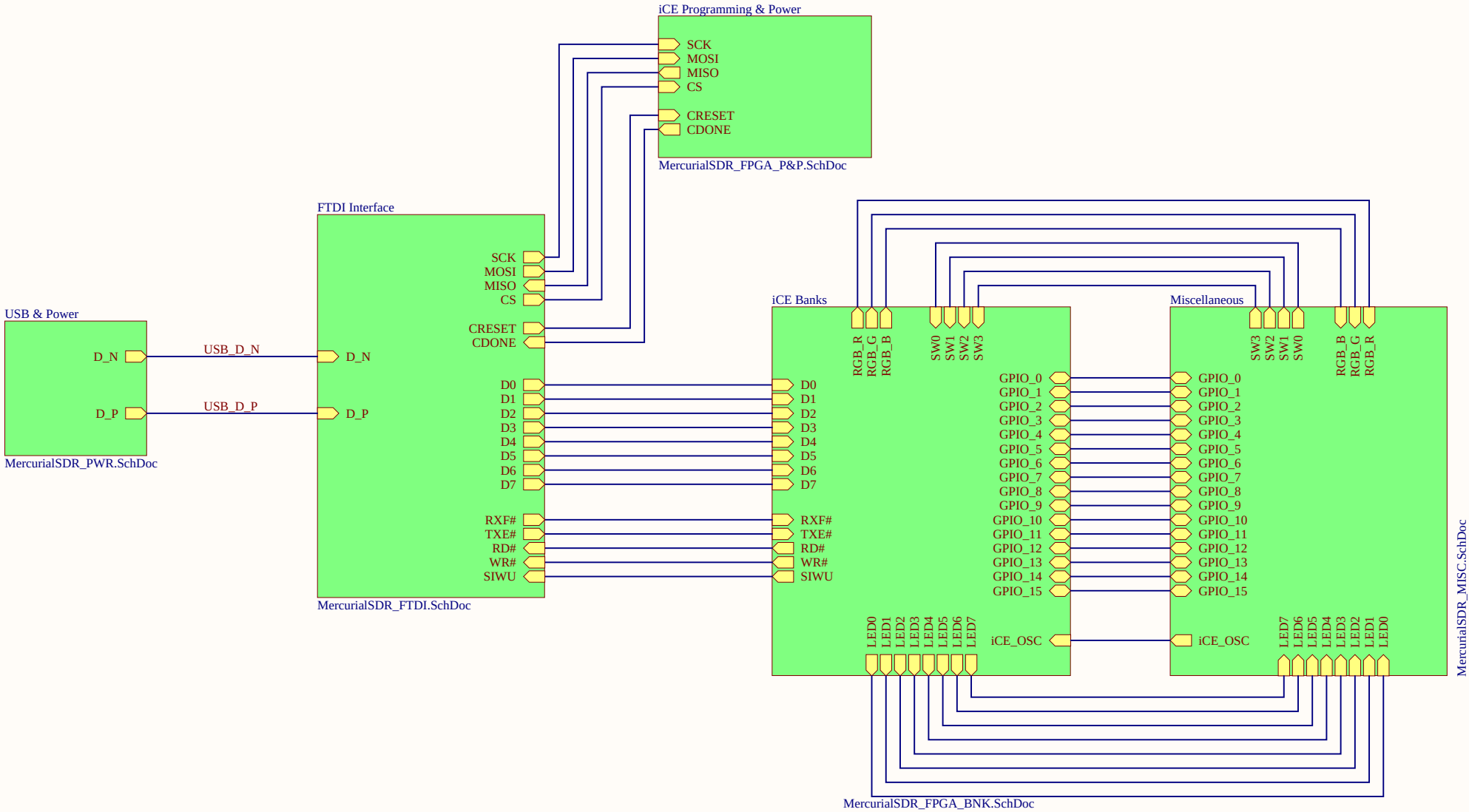
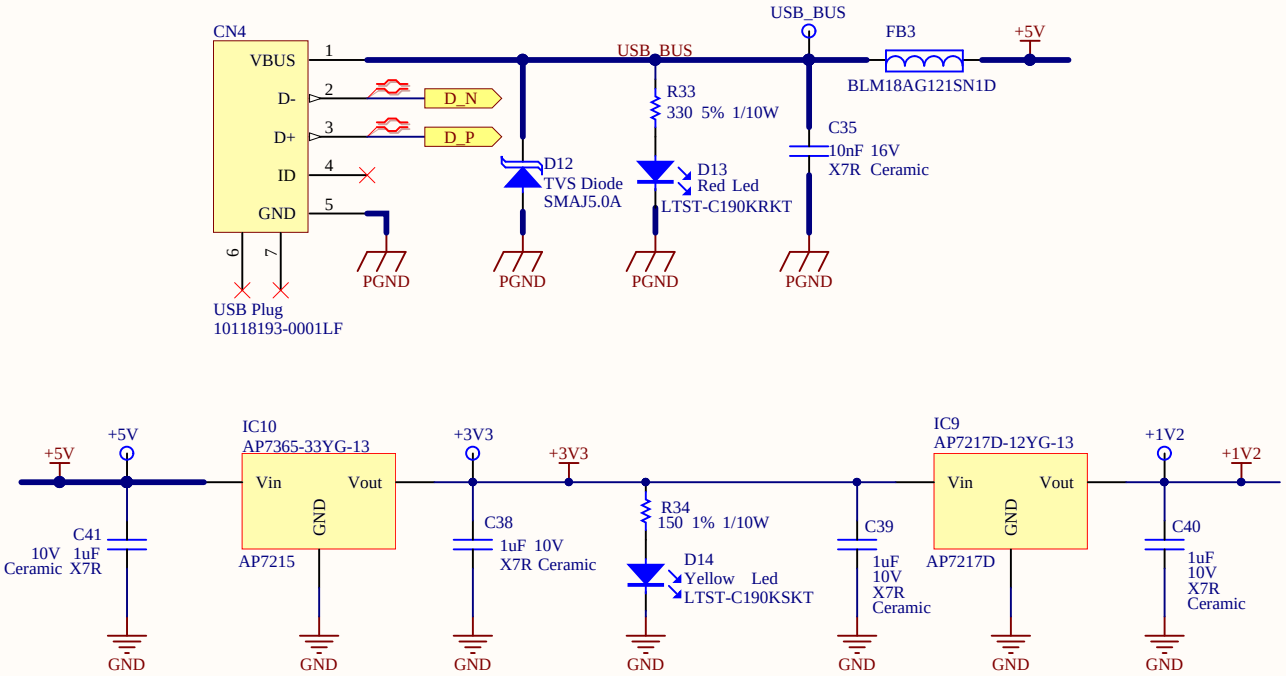


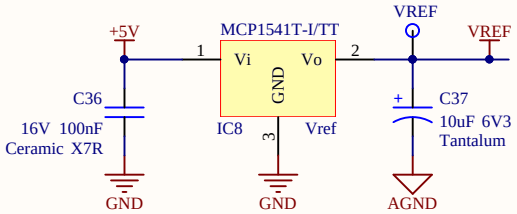
Title: MercurialSDR - Block Diagram		
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 1 of 6	
File: C:\Users\..\MercurialSDR_BLK.SchDoc	Drawn By: Andres Hojnadel	

Power Stage

USB to +3V3 and +1V2



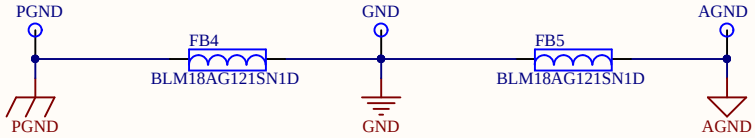
Reference Voltage



This is a precision voltage reference for DAC (IC1).

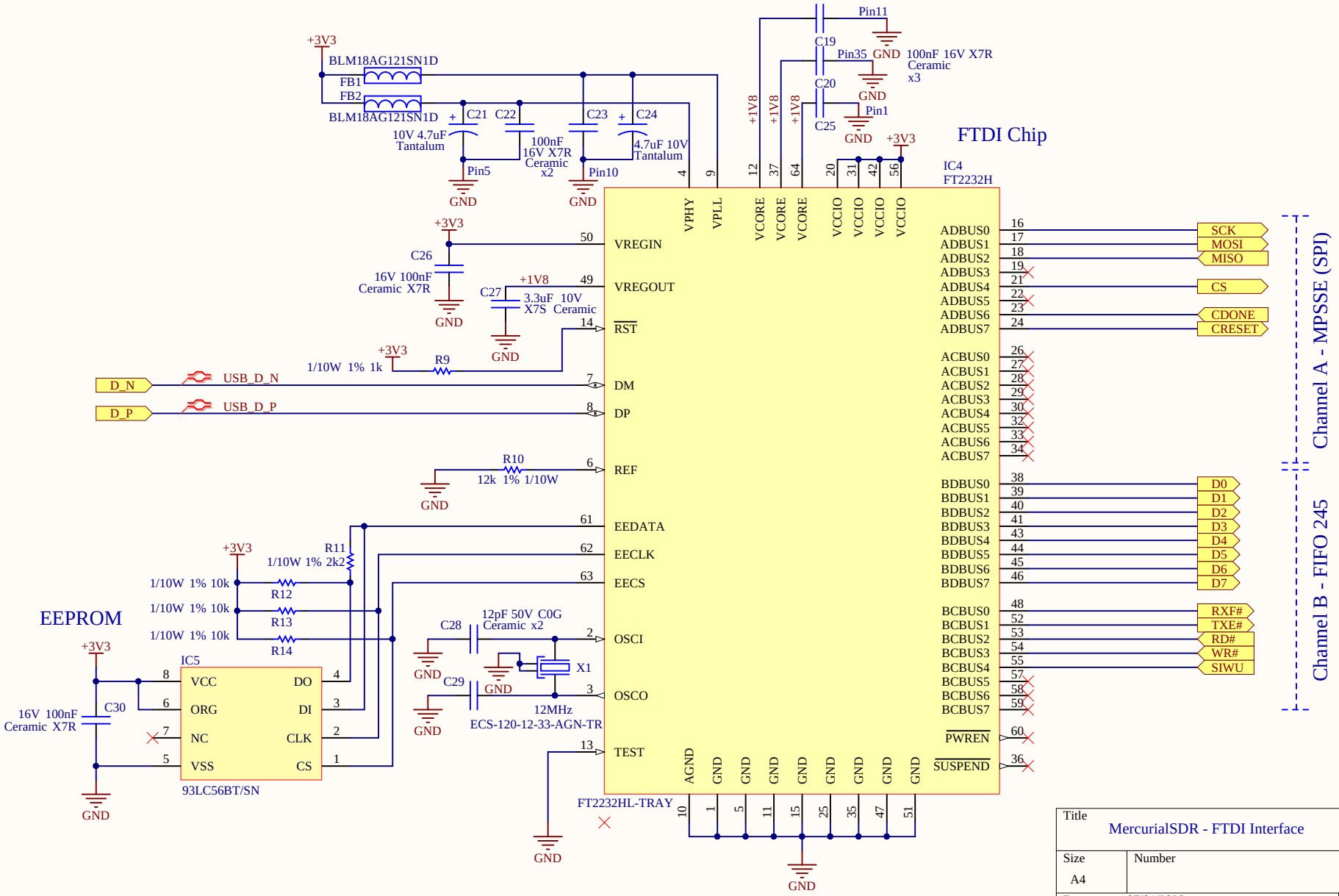
Them must be close.

Ground Connections



Title: MercurialSDR - Power Stage		
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 2 of 6	
File: C:\Users\..\MercurialSDR_PWR.SchDoc	Drawn By: Andres Hojnadel	

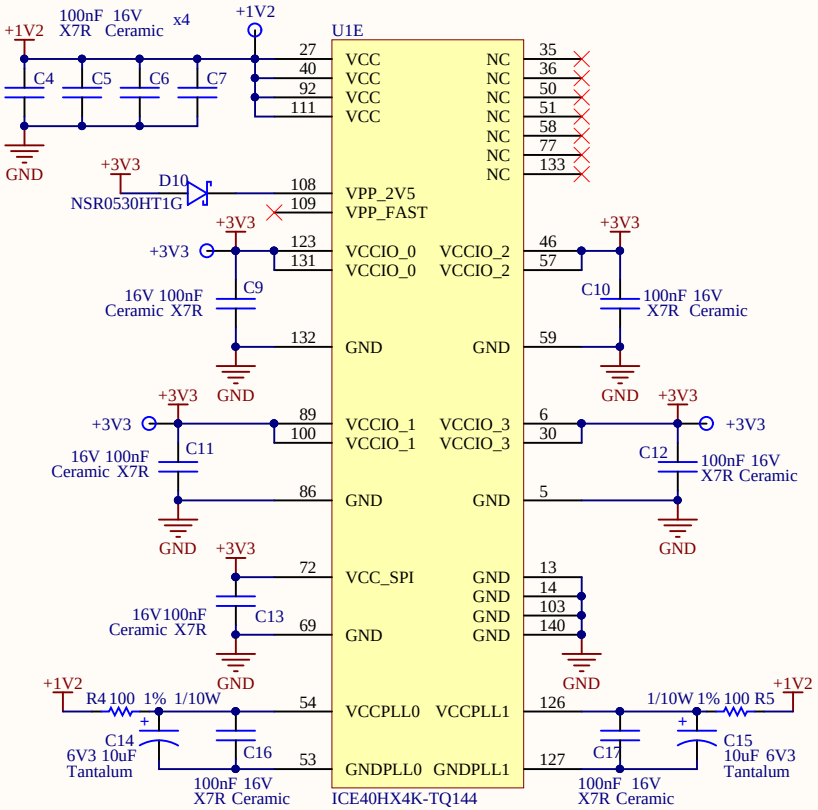
FTDI Interface



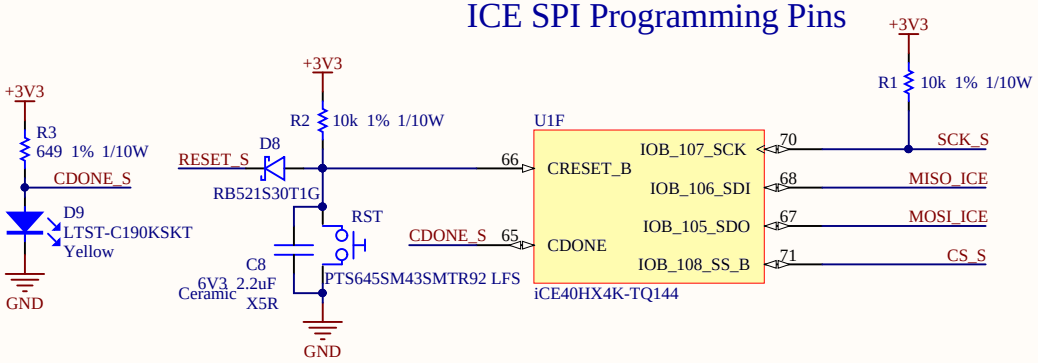
Title	MercurialSDR - FTDI Interface	
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 3 of 6	
File: C:\Users\..\MercurialSDR_FTDI.SchDoc	Drawn By: Andres Hojnadel	

ICE Programming & Power

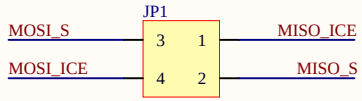
iCE Power



ICE SPI Programming Pins



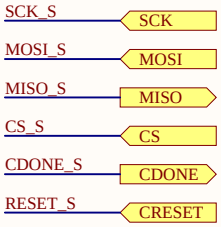
ICE/Flash programming selection



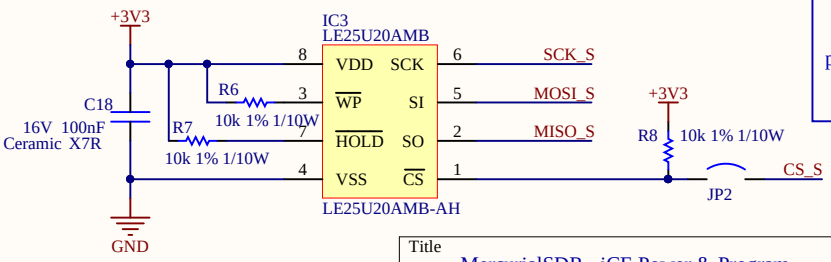
For programming ICE: shunt 1-3 & 2-4

For programming Flash: shunt 1-2 & 3-4

FTDI Ports



Flash Memory

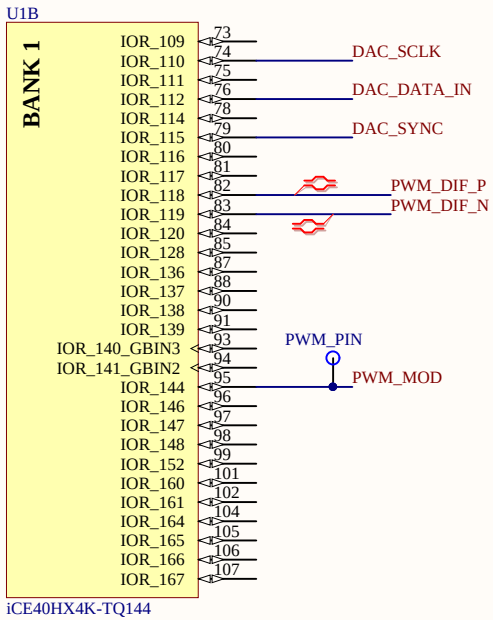


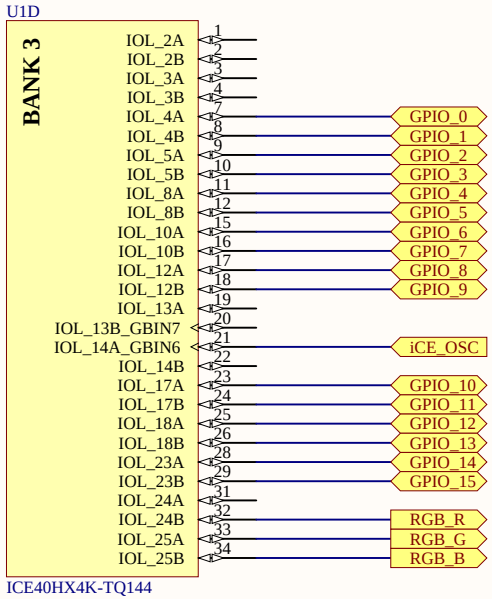
Remove JP2 only for programming ICE

Shunt JP2 for Flash programming or normal operation

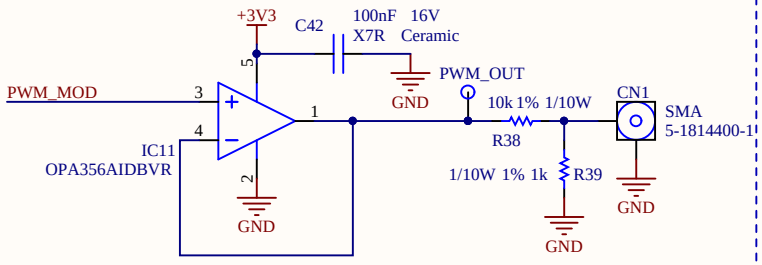
Title: MercurialSDR - iCE Power & Program.		
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 4 of 6	
File: C:\Users\..\MercurialSDR_FPGA_P&P.SchDoc	Drawn By: Andres Hojnadel	

FPGA Banks

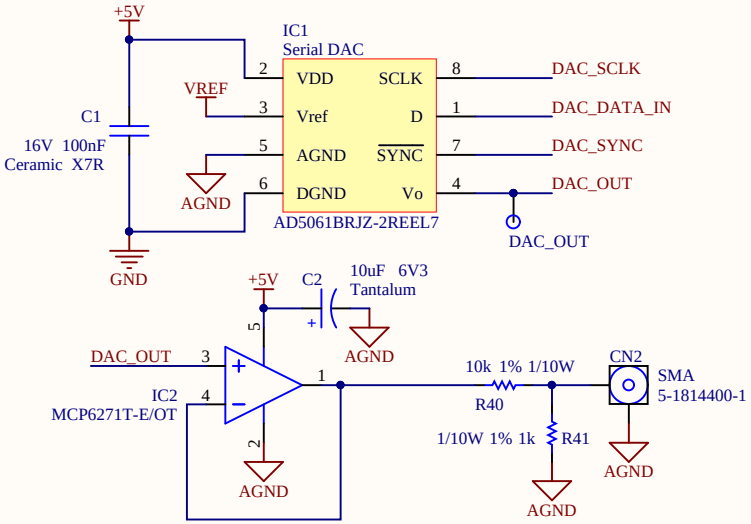




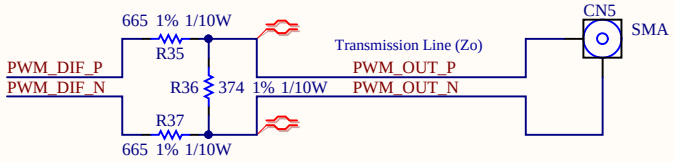
One-Pin-RF Single Ended Output



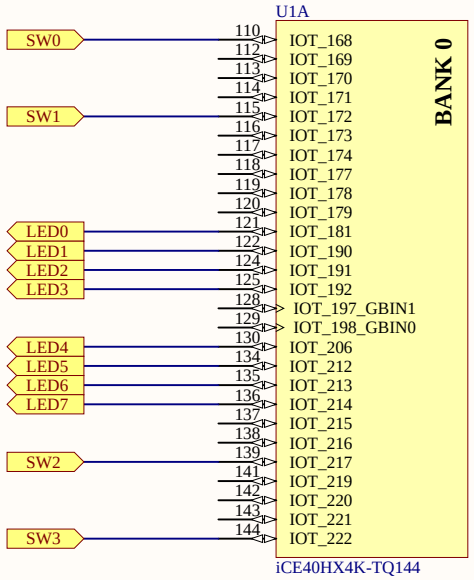
PAM Output

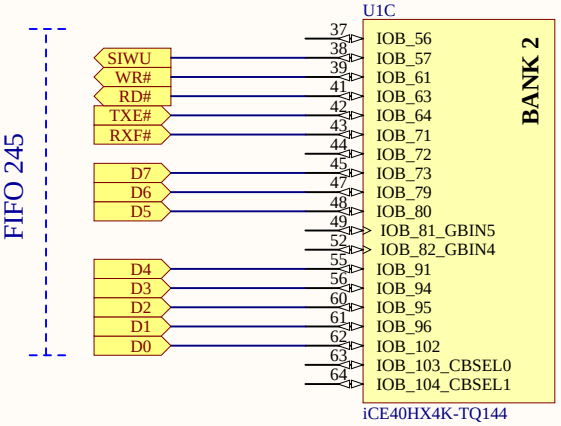


One-Pin-RF Differencial Output



The resistors network must be close to the FPGA differential output pins



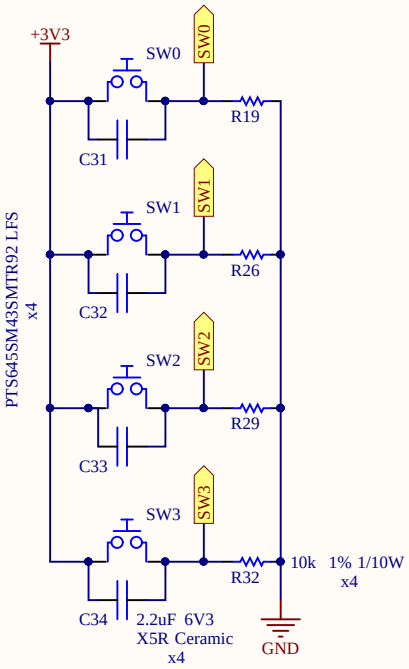


Title: MercurialSDR - iCE Banks		
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 5 of 6	
File: C:\Users\..\MercurialSDR_FPGA_BNK.SchDoc	Drawn By: Andres Hojnadel	

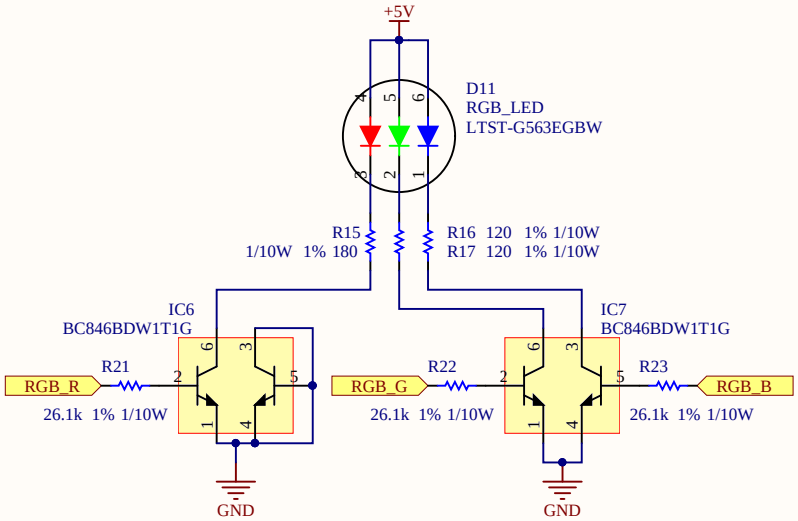
GND

Miscellaneous

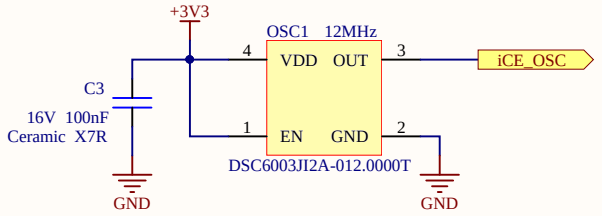
Buttons



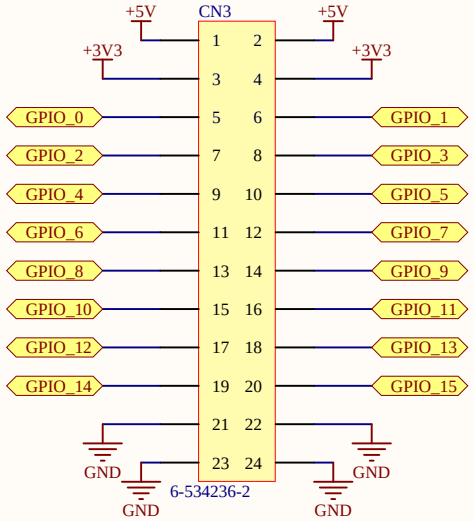
RGB Led



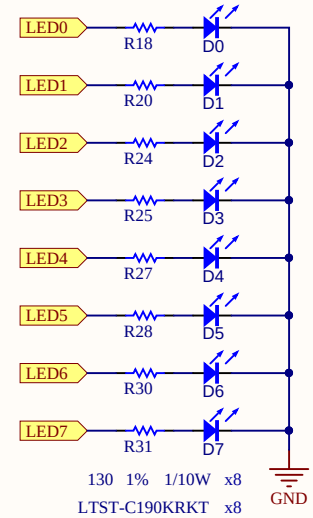
iCE Oscillator



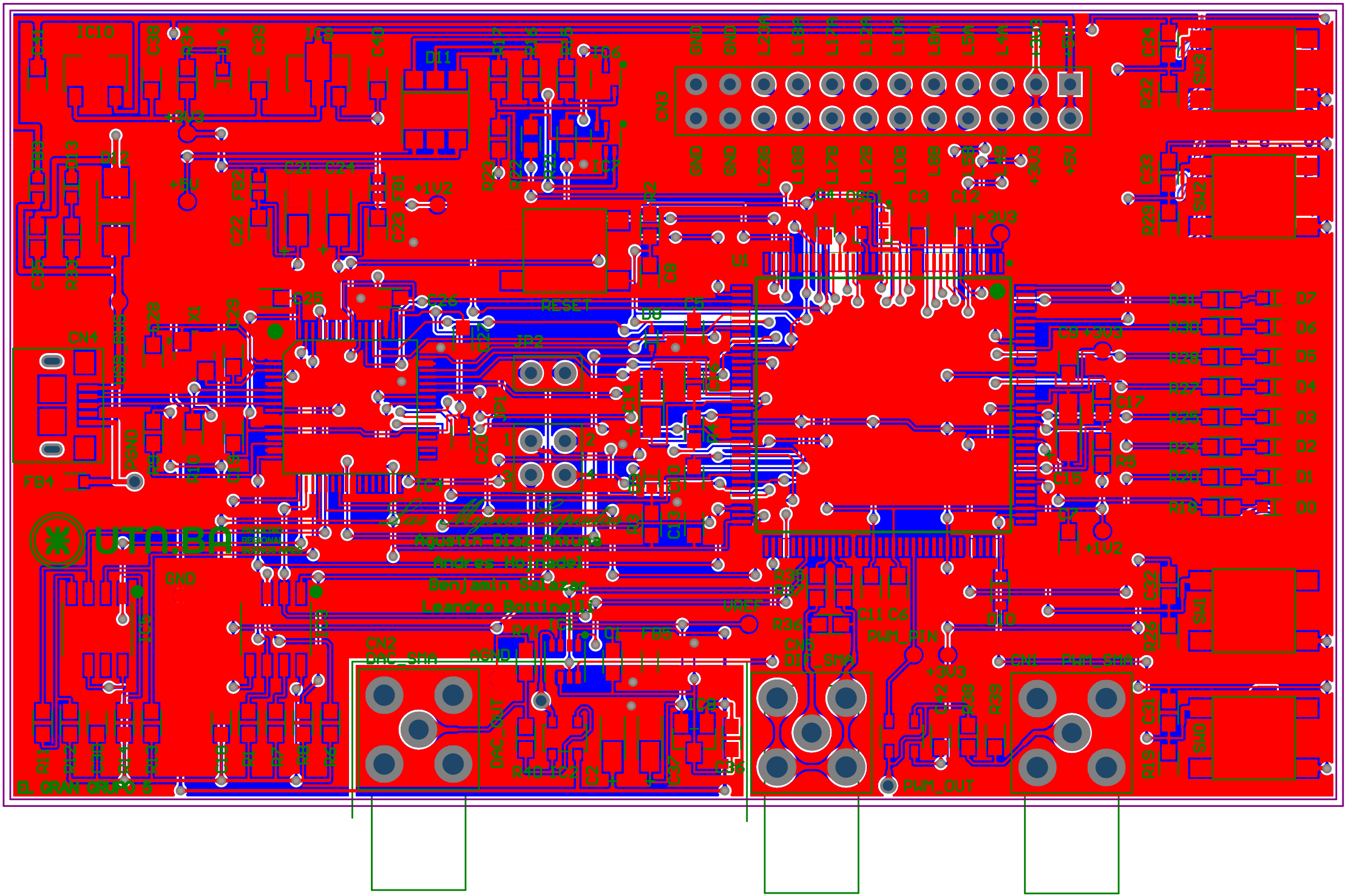
GPIO Ports



8-Led Array



Title: MercurialSDR - Miscellaneous		
Size: A4	Number:	Revision: Rev2.0
Date: 07/01/2020	Sheet 6 of 6	
File: C:\Users\..\MercurialSDR_MISC.SchDoc	Drawn By: Andres Hojnadel	


Agustín Díaz Arturia
Andres Hojmodel
Benjamin Salazar
Leandro Bottinelli
EL GRAN GRUPO 5
PWM_PIN
PWM_OUT
DAC_SMA
PWM_SMA
RESET
PGND
AGND
+3V3
+1V2