Introduction to Hardware Design
Basic Digital Logic: Solutions

Profs. Sundeep Rangan, Siddharth Garg

1. *Propagation delay*: A signal x has time-value change points

$$(10, 0), (20, 4), (30, 2)$$

   where the time is in nanoseconds. The signal is passed through a circuit that produces $y = 2x + 1$ with a propagation delay of 3 ns. What are the time-value change points of y? Use x for unknown values.

2. *Critical path*: Consider the following SystemVerilog code:

```
always_ff @(posedge clk) begin
    x1 <= 3*x1>>2 - 5*x>>3 + 7;
    x2 <= 3*x1>>2 +  2;
end
```

   Here `3*x>>2` denotes multiplication by 3 followed by a right shift by 2 bits (division by 4). Assume that:

   - Each multiplication with shift takes 4 ns.
   - Each addition or subtraction takes 2 ns.
   - Registers have zero delay.

   What is the critical path delay of this circuit?

3. *Sequential updates*: Consider the following SystemVerilog code:

```
always_ff @(posedge clk) begin
    x <= x + v;
    if (x > 30) begin
        v <= -10;
    end else if (x < 0) begin
        v <= 10;
    end
end
```

   Starting from $(x, v) = (15, 10)$, what are the values of (x, v) for the next 5 clock cycles?

4. *Splitting paths over multiple cycles*: Consider the following SystemVerilog code:

```
always_comb begin
    act_in = w1*xreg+b1;
    if (act_in > 0) begin
        a = act_in;
    end else begin
        a = 0;
```

```
    end
    xsq = xreg*xreg>>4;
    y = xsq + w2*a + b2;
end
always_ff @(posedge clk) begin
    xreg <= x;
end
```

where `>>4` denotes a right shift by 4 bits (division by 16). So, the code registers the input `x` into `xreg` on each clock cycle, and produces the output `y` in a single clock cycle based on the registered value. The circuit is to be syntheized with components:

- Multiplication with shift: 4 ns
- Addition or subtraction: 2 ns
- Logic to compute $\max\{0, u\}$: 1 ns
- Registers: zero delay

Assume that w_1, b_1, w_2, and b_2 are constants.

(a) Draw a block diagram of the circuit showing an implementation of the circuit. If this is being auto-graded, you do not need to submit the diagram. But, I will include it in the solutions.

(b) What is the critical path delay of this circuit?

(c) Rewrite the code to operate over two clock cycles instead of one to minimize the critical path delay. What is the critical path delay of the new circuit?

5. *Exponent* Suppose we wish to implement the function

$$y = x^i,$$

with an integer exponent $i \in \{0, 1, 2, 3\}$. The input x and output y are signed short integers – do not worry about overflow. Write a SystemVerilog module that computes y. The output should always be 2 cycles after the input, even if $i = 0, 1$ or 2. Use only one multiplication in each clock cycle.

Hint: This problem is a bit harder. You will need to use delay lines to store the input x and exponent i.