NC State University

Department of Electrical and Computer Engineering

ECE 463/563: Fall 2018 (Rotenberg)

Project #3: Dynamic Instruction Scheduling

by

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NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

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(sign by typing your name)

Course number: _____563_____
(463 or 563 ?)

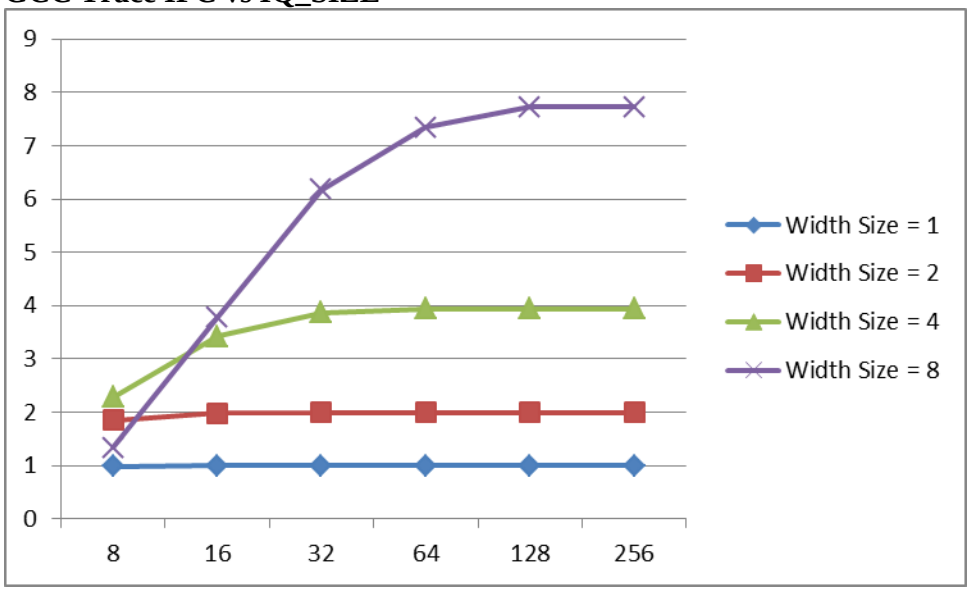
1) Large ROB, effect of IQ_SIZE

ROBSIZE: 512 entries

a. GCC trace

	WIDTH			
IQsize	**1**	**2**	**4**	**8**
8	**0.99**	1.85	2.28	1.33
16	1	**1.98**	3.43	3.78
32	1	1.99	**3.87**	6.17
64	1	1.99	3.94	**7.34**
128	1	1.99	3.94	7.73
256	1	1.99	3.94	7.73

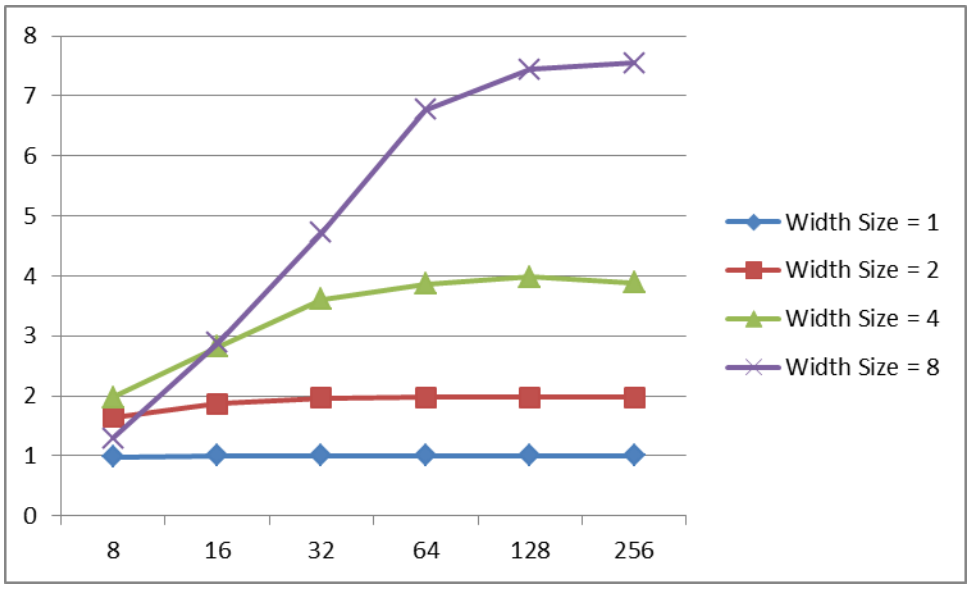
GCC Trace IPC vs IQ_SIZE



b. PERL trace

	WIDTH			
IQsize	**1**	**2**	**4**	**8**
8	**0.98**	1.64	1.98	1.29
16	1	1.87	2.82	2.88
32	1	**1.97**	3.61	4.72
64	1	1.98	**3.87**	6.77
128	1	1.98	3.98	**7.44**
256	1	1.98	3.89	7.55

PERL Trace IPC vs IQ_SIZE



"Optimized IQ_SIZE per WIDTH"
Minimum IQ_SIZE that still achieves within 5% of the IPC of the largest IQ_SIZE

	WIDTH			
Trace/Benchmark	**1**	**2**	**4**	**8**
GCC	8	16	32	64
PERL	8	32	64	128

The value of IPC which is within 5% of the best IPC for the highest IQsize = 256 is chosen. It gives the highest value for the IPC, as with so large IQsize it does not act as a bottleneck to processor performance.

Discussion:

The goal of a superscalar processor is to achieve an IPC that is close to WIDTH (which is the peak theoretical IPC of the processor). Given this goal, what is the relationship between WIDTH and IQ_SIZE? Explain.

Ans: For a fixed IQsize, the IPC increases as the WIDTH is increased. The number of instructions in the pipeline in each stage is determined by the WIDTH. Thus, greater the width greater the number of instructions retiring. The exception to this general observation is when the IQsize is almost equal to the width. In this case, the Dispatch stage is stalled more often since it cannot issue WIDTH number of instructions unless IQ

has WIDTH number of free entries in it. IQsize = width shows the high reduction in IPC which can be observed in the graph for width= 8, IQsize = 8, where the IPC for WIDTH = 8 turns out to be lesser than width = 2, 4 with IQsize = 8.With an increase in IQsize, it does not become a hardware bottleneck and thus leads to fewer stalls in the pipeline. But, with a sufficiently sized IQ, the IPC begins to level up as IQsize is no longer the performance bottleneck for the pipeline. It can be observed in IQsize greater than 64

Do some benchmarks show higher or lower IPC than other benchmarks, for the same microarchitecture configuration? Why might this be the case?

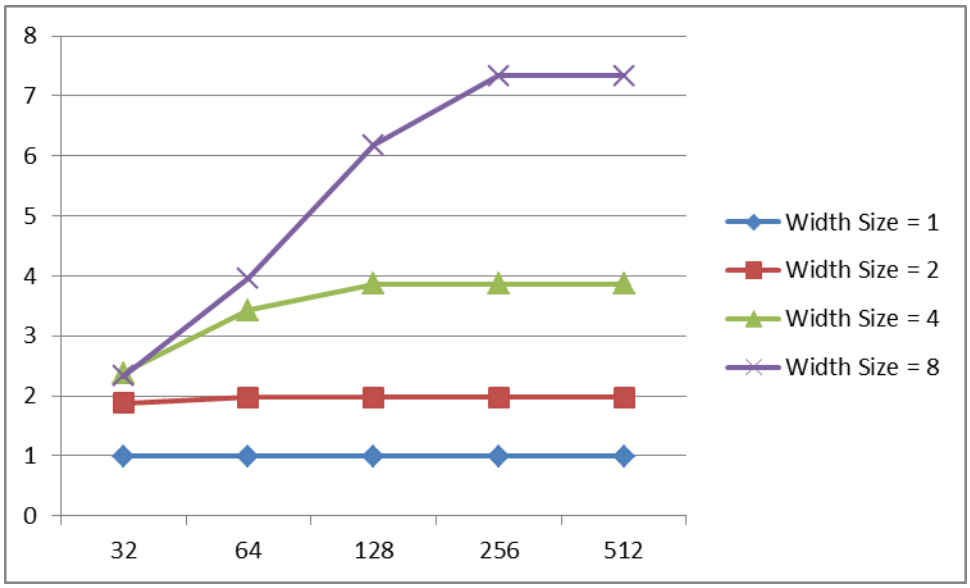
Ans:
On comparing GCC trace and Perl trace, we can see that they follow similar trends. However, the values of IPC for the GCC trace are a bit higher than those for the Perl trace. The benchmark instruction trace affects the IPC depending upon the number of RAW and WAR hazards in the pipeline. Perl trace has more hazards in the instruction sequence compared to the GCC trace. Also, the number of high latency instructions in the Perl trace might be higher than GCC.

2) Effect of varying ROB_SIZE, using the optimal IQ_SIZE values

GCC TRACE

ROB Size	1	2	4	8
32	0.99	1.88	2.38	2.33
64	0.99	1.98	3.43	3.96
128	0.99	1.98	3.87	6.18
256	0.99	1.98	3.87	7.34
512	0.99	1.98	3.87	7.34

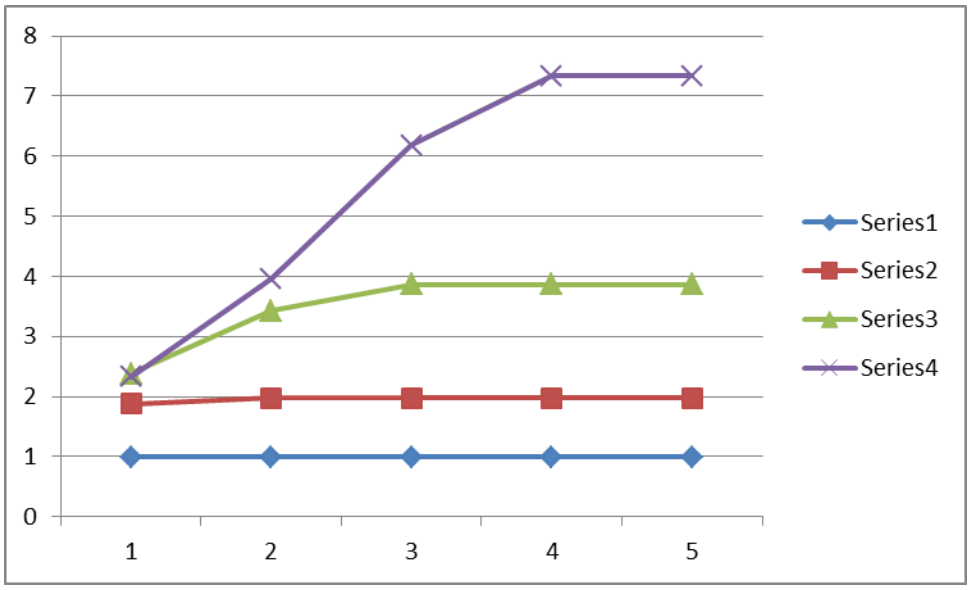
GCC Trace IPC vs WIDTH



PERL TRACE

ROB Size	1	2	4	8
32	0.98	1.79	2.19	2.18
64	0.98	1.97	3.16	3.51
128	0.98	1.97	3.83	5.36
256	0.98	1.97	3.87	7.05
512	0.98	1.97	3.87	7.44

PERL Trace IPC vs WIDTH



Observation:

From graph, as the ROB_SIZE is increased keeping the WIDTH constant, the IPC increases. This is because with increase in ROB_SIZE, it no longer continues to be a hardware resource bottleneck. With a sufficiently sized ROB, the IPC begins to level off since ROB_SIZE no longer remains a performance determining factor. ROB_SIZE of 128, 256 or 512 entries show the leveling off. With constant ROB size and width increasing IPC goes on increasing.

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