Test Report for LBNL 4k x 4k CCD #127298-14-4

Date: Mar 20, 2009
Tested by: William F. Kolbe

1. *Operating parameters*

All tests were conducted in thermal vacuum at 140K. The CCD was read out at 70 kpix/sec, with the voltages optimized as follows:

High and low clock levels are given for exposure, readout, erase and purge, and the DC voltages for the output gate (OG), reset voltage (VR), output transistor drain (VDD) and substrate bias voltage (VSUB) are also given. Clock widths are overlap times per phase. Total pixel time includes 2 x 5.2 μs integration time plus settling times. Output gate settings were determined by measuring charge injection threshold values at the specified Vsub and adding 0.6V to each to achieve proper operation at well depth of 150,000 e^-. Note: also N+ currently is filtered with a 1.0 μf capacitor and 3 MΩ resistor to ground.

Signal	Type	Exposure/Readout		Erase		Purge		t width
		VL	VH	VL	VH	VL	VH	(μsec)
V1	ck	-3	5	9	9	-9	-9	20
V2	ck	-3	5	9	9	-9	-9	20
V3	ck	-3	5	9	9	-9	-9	20
FS1	ck	-3	5	9	9	-9	-9	20
FS2	ck	-3	5	9	9	-9	-9	20
FS3	ck	-3	5	9	9	-9	-9	20
TG	ck	-3	5	-3	5	-3	5	20
H1	ck	-4	6	-4	6	-4	6	0.16
H2	ck	-4	6	-4	6	-4	6	0.16
H3	ck	-4	6	-4	6	-4	6	0.16
SW	ck	-5	5	-5	5	-5	5	0.5
RG	ck	0	-6	0	-6	0	-6	0.16
				- U1 -				
OG	dc	2.7		2.7		2.7		
VR	dc	-12.5		-12.5		-12.5		
VDD	dc	-22		-22		-22		
				- U2 -				
OG	dc	2.7		2.7		2.7		
VR	dc	-12.5		-12.5		-12.5		
VDD	dc	-22		-22		-22		
				- L1 -				
OG	dc	2.7		2.7		2.7		
VR	dc	-12.5		-12.5		-12.5		
VDD	dc	-22		-22		-22		
				- L2 -				
OG	dc	2.7		2.7		2.7		
VR	dc	-12.5		-12.5		-12.5		
VDD	dc	-22		-22		-22		
VSUB	dc	+50		ramp		+50		
N+	float							
P+	dc	0		0		0		

2. Output transistor characteristics

The CCD has four output transistors. Each transistor was characterized for gain and noise using an ^{55}Fe x-ray source to deposit a known signal, corresponding to approximately 1570 e- at 140K. (Note that the value of 1620 e- per 5.9 keV x-ray that is often used is valid only at room temperature.) To obtain the total deposited charge for each incident x-ray, 3x3 pixels were summed. The noise was determined by measuring the rms spread of the overscan, and correcting by the measured gain. The results for our system are summarized in the following table:

Transistor	Gain (ADU/e-)	Noise (e-)
U1(LL)	1.569	3.0
U2(UL)	1.450	3.1
L1(LR)	1.566	2.9
L2(UR)	1.499	3.3

.

3. Full Well and Linearity

The CCD was exposed to flat field illumination for successively greater exposure times to measure linearity and determine the pixel charge capacity at full well. The following figures show the average flat field in ADU vs exposure time for each of the four quadrants. From this data we determine the full well capacity to be greater than 150,000 e- and the linearity to be within 1% up to this value. Note: the gain was reduced by a factor of 4.75 from values in the above table to cover the desired range of signal levels within the 16 bit range of the adc.

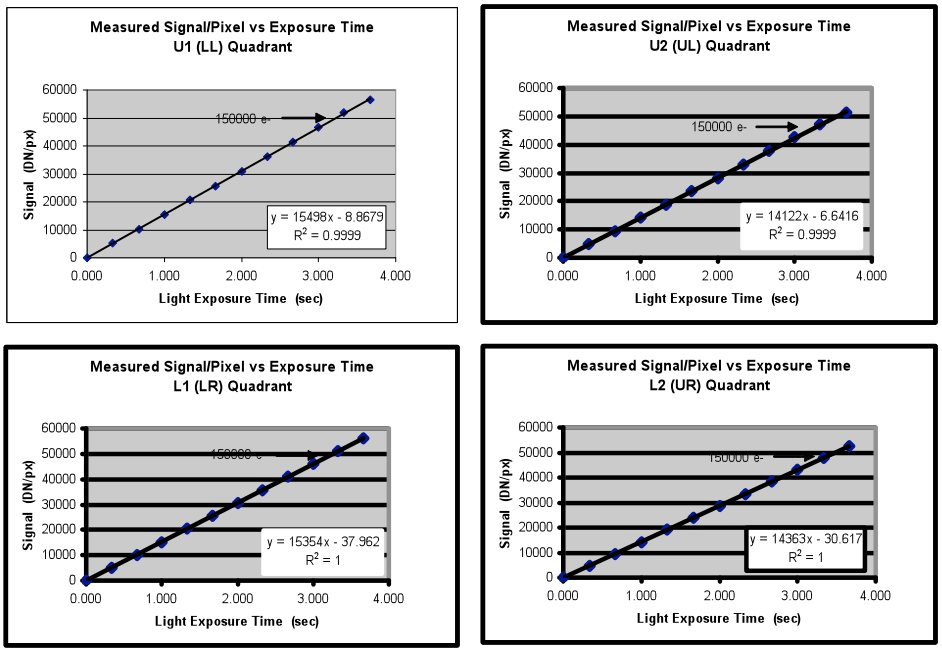


Figure 1 Linearity of each of the 4 quadrants.

4. Dark Current

Dark current was measured by taking a series of 6 1800 sec darks and median combining them to eliminate cosmic rays. A representative half-hour dark image is shown below. The measured dark current was 0.7 e-/px-hr.

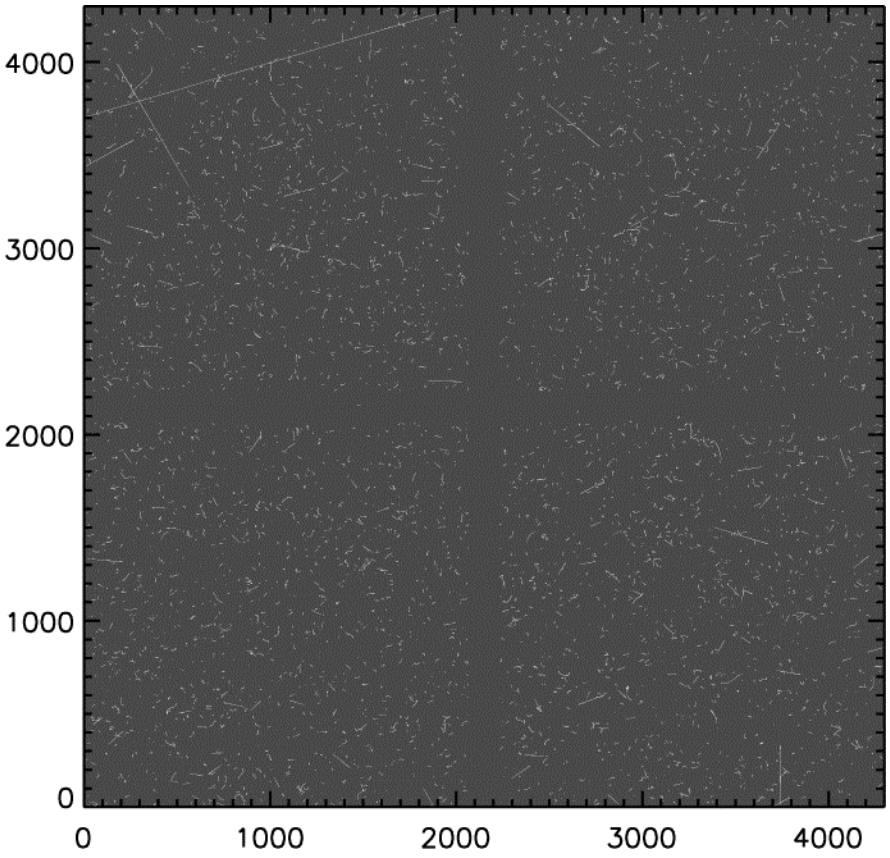


Figure 2 Dark current image (1800 second exposure).

5. Parallel and Serial CTE

A flat field image taken with this device shows that it images well with no serious artifacts. Visible circular arcs (~1.5% amplitude) are believed to be caused by small variations in conductivity during crystal growth. Two small glue voids can be seen in quads LL and LR. To quantify the charge transfer efficiency, we use two independent techniques, as described below.

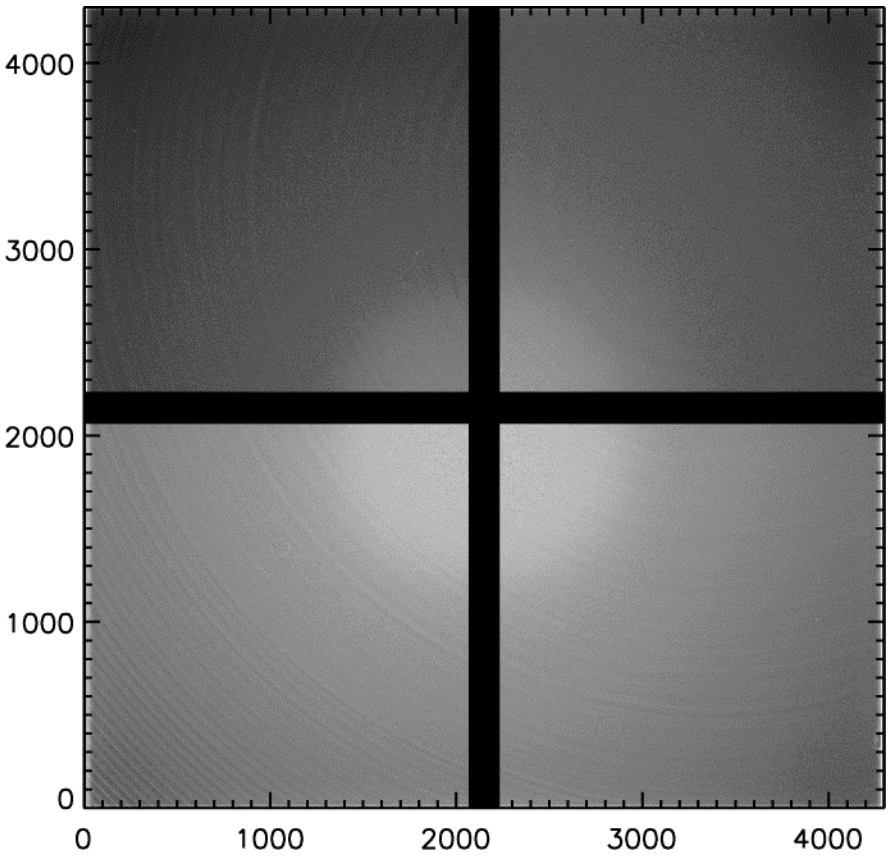


Fig. 3 Flatfield image produced by illumination at 500 nm. The illumination was not uniform but was somewhat brighter in the central region. Note: the image includes overscan columns and rows.

Charge transfer efficiency determination is complicated in a thick, fully-depleted back-illuminated CCD by the effects of lateral charge diffusion, which results in charge sharing between pixels of the localized charge deposited by incident x-rays from an ^{55}Fe x-ray source. We have developed a technique to deal with this in which we create larger pixels with 2x2 binning, and then make the usual stacking plot of measured x-ray energy vs pixel row or column number, fitting the slope to determine the CTE. The only caveat with this technique is that the measured CTI is 2 times the intrinsic CTI because charge appearing in an adjacent binned pixel has shifted twice.

The table below summarizes the measured parallel and serial CTE for each quadrant after the correcting for the 2x2 binning. All data were taken at 140K and 70 kpix/sec readout speed. Uncertainty of CTE measurement is fairly large and estimated to be about +/- 0.000020.

Transistor	Binned Serial CTE	Binned Parallel CTE	EPER Parallel CTE
U1	0.999999	0.999999	0.999999
U2	0.999995	0.999999	0.999999
L1	0.999999	0.999999	0.999999
L2	0.999999	0.999999	0.999999

As a cross-check to the binned x-ray technique, we use the extended pixel edge response (EPER) technique which determines CTE by examining the sharpness of the edges of flat field images. The EPER method we use takes advantage of the independence of the FS and V parallel clocks and delayed clocking to produce an edge in the middle of each quadrant of the CCD. Figure 4 below shows such a flatfield image with gaps midway in each quadrant suitable for EPER analysis.

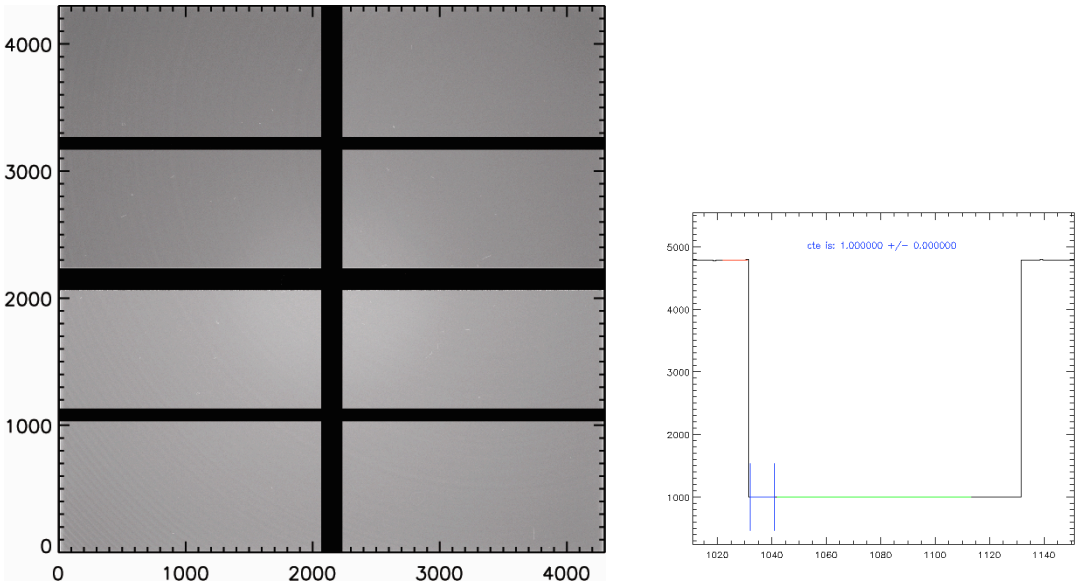


Fig. 4 Flatfield image with 100 pixel gaps in each quadrant and column plot for L1(LL) quadrant showing the region where the EPER technique is applied.

Please note: In all measurements, light is collected in two phases in order to minimize fixed pattern noise. Because of the way our readout electronics is wired, this means that the two parallel clocks at the very center of the CCD are both held in barrier phase during integration. As a result, when read out, an increase in the neighboring pixels on each side of the center is observed. This artifact could be eliminated by a modification of the wiring and clocking software.

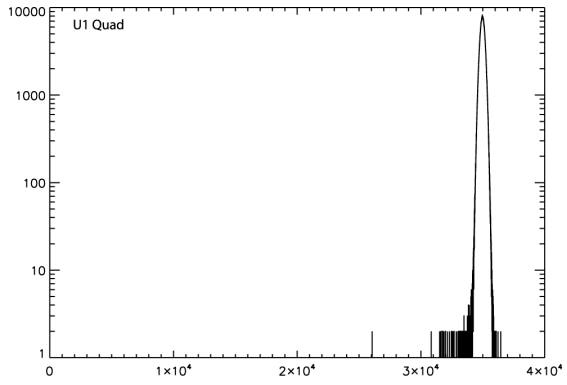
6. Pocket Pumping to Detect Traps

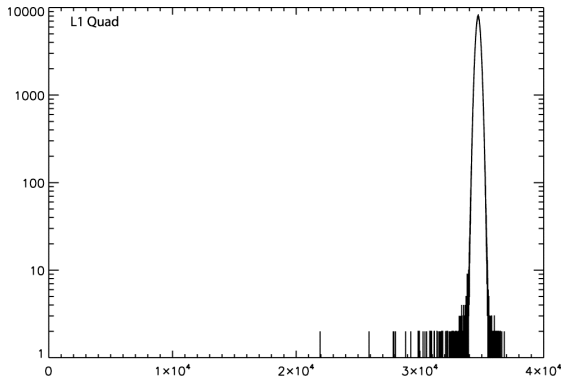
Traps in the silicon that cause poor CTE can be directly detected through the method of pocket pumping. We have performed pocket pumping on this device and determined the number and location of traps. Pocket pumping was performed by exposing the CCD to a flat field of ~2000 e- and then shifting the charge back and forth by one pixel 120,000 times. This causes charge to build up in pixels associated with traps and be depleted from neighboring pixels. Since the shift rate and other operational conditions are the same as during readout, the pumping magnifies the influence of the traps by a large factor. For a depletion of 50% or 1000 e-, the effective trap depth per cycle is 1000/120000 = 0.0083 e-. This device had a total of 303 traps with a depth of at least 50%, or an average 1.95E-5 traps per pixel. Note: In normal readout only forward traps should contribute.

Observed Traps with Depth 50% or more			
Quadrant	**Forward Traps**	**Reverse Traps**	**Trap Density**
U1 (LL)	59	23	2.11E-05
L1 (LR)	59	18	1.98E-05
U2 (UL)	44	39	2.14E-05
L2 (UR)	33	28	1.57E-05

7. Cosmetic Quality

The cosmetic quality of this device was determined by examining co-added median combined flats and darks. Hot/dark pixels were defined as pixels with at least 20% excess/less charge than the local median. A total of 0 hot pixels and 5 dark pixels were identified. These are shown for each quadrant of the image in the log histogram plots shown below for each quadrant. In the graphs, log(histogram+1) is plotted to make the events more visible. No blocked columns and no hot columns were observed in any quadrant.





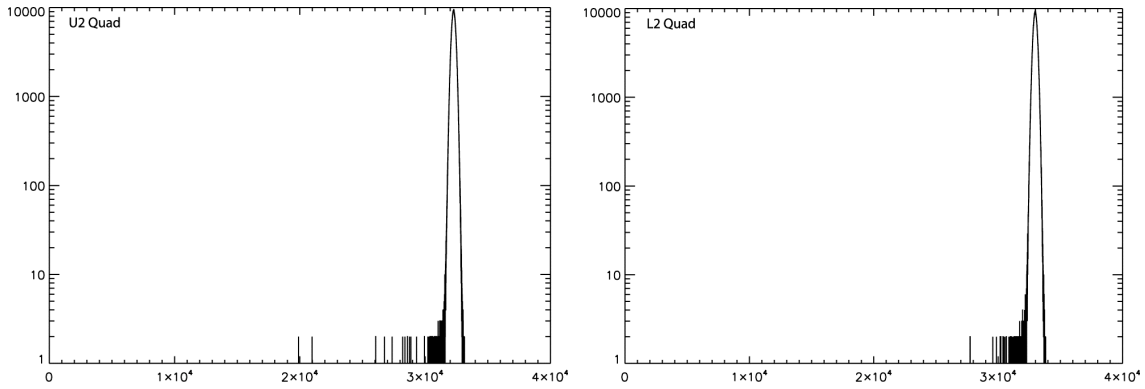


Figure 5 Histograms showing hot and dark pixels above and below the main peak for each quadrant of a flatfield image of 35000 adu.