4k x 2k and 4k x 4k CCD Technical Manual

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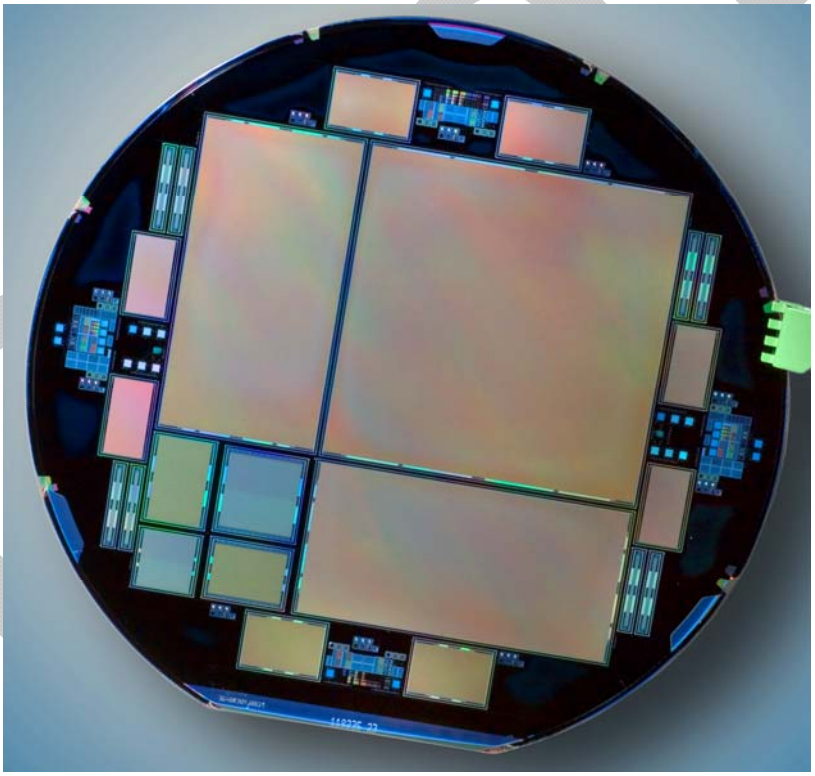

Table of Contents

1 CCD description

Figure 1 is a cartoon of the CCD. The pixel field is 2040 x 4114 or 4128 x 4114 cells, parallel by serial, aka, rows by columns. The pixel size is 15 μm.

The imaging area is split top and bottom into two parallel registers, which are in turn split into image areas and storage areas. All four areas, whether image or storage, can be used for accumulating image charge; the names are historical. All four areas are electrically continuous; charge can be shifted in either direction across or away from any of the boundaries. The imaging areas are driven three clock phases, V1-3, the frame store areas are driven by its three clock phases, FS1-3, and terminated with transfer gates TG.

There are two serial register structures, each half of each register has its own clocks. The serial registers are electrically continuous; charge can be shifted in either direction across or away from the boundary. At the start of the serial registers are 7 extended pixels. Each of the four half-registers has an independent set of five clocks – three-phase H1-3, summering well SW, and reset gate RG – and an output source follower and reset transistor.

Figure 2 show the details of the order of the clocks within the CCD. Refer to Figure 1 for the mapping of pad locations and names to these phases.

2 Signal naming convention

1. CCD halves along the pixel columns are labeled 1 and 2. Half 2 is tagged with a pair of 4-square symbols in the pad area.
2. Each half is divided into U and L.
3. CCD readout quadrants are labeled U1, U2, L1, and L2.
4. Clock phases are labeled 1, 2, and 3.
5. Labeling: p=1, 2, or 3 for clock phases; h=U or L to denote halves; c=1 or 2 to denote sectors within halves.

3 Signal descriptions

3.1 Parallel clocks

3.1.1 Vp_ hc

1. Parallel registers clocks (a.k.a., vertical clocks) for pixel rows farthest from serial register.
2. The three phases have identical voltage swings.
3. Vp_Uc and Vp_Lc are bussed together within the CCD.

3.1.2 FSp_hc

1. Parallel registers clocks (a.k.a., vertical clocks) for pixel rows closest to serial register.
2. The three phases have identical voltage swings.
3. FSp_Uc and FSp_Lc are bussed together within the CCD.

3.1.3 TG_hc

1. Parallel register to serial register transfer gate clocks.
2. Top and bottom clocks have identical voltage swings.
3. TG_Uc and TG_Lc are bussed together within the CCD.

3.2 Serial clocks

3.2.1 Hn_hc

1. Serial clocks for four quadrants of serial readout register (a.k.a., horizontal clocks).
2. The three phases have identical voltage swings.

3.2.2 SW_hc

1. Serial register to summing well transfer clock.
2. The four instances have identical voltage swings.

3.2.3 RG_hc

1. Floating diffusion capacitor reset gate clock.
2. The four instances can have identical voltage swings.

3.3 Bias voltages

3.3.1 OG_hc

1. summing well / floating diffusion Isolation gate (DC).

3.3.2 VR_hc

1. Floating diffusion capacitor reset reference voltage (DC).

3.3.3 VDD_hc

1. Readout source follower transistors drain voltage (DC).
2. 1 μF, 25V capacitor to P+.

3.3.4 VOUT_hc

1. Readout source follower transistors sources – output signal.
2. 20 kΩ load resistor to P+.
3. 1 μF, 25V capacitor to signal processing.
4. Sensitivity is ~3.5 μV/e for I_{ds}=0.6 mA and V_{ds}=6V and 4 μs signal integration.

3.3.5 P+_hc

1. p+ guard ring contact (DC).
2. Four instances are bussed together within the CCD.
3. By convention, this node is 0V; all other voltages are referenced to this.

3.3.6 N+_h and N+_hc

1. n+ channel stop implant contacts (floating).
2. The six instances are bussed together within the CCD.
3. 100 nF, 50V capacitor to P+.

3.3.7 VSUB_hc

1. Substrate depletion voltage (DC).
2. The four instances are bussed together within the CCD.
3. 100 nF, 100V capacitor to P+.
4. Nominal operating voltage is +80V.

4 Sensitivity and source follower noise

The sensitivity of the output stage is 3.5 μV/e.

The noise voltage spectrum is shown in Figure 3 for i_{DS}=600 μA and V_{ds}=5 V. A good approximation is 1 μV at 1 Hz for 1/*f* noise and 15 nV/√Hz for white noise.

5 Signal AC and DC requirements

Table 1 lists the nominal operating voltages for the CCD in its different modes of operation. Also given are rise-fall times, clock widths, and approximate capacitances. The last three columns parameterize the noise susceptibility of the CCD. The “max noise” column is the amplitude of a sine wave at frequency “worst freq” that increases the readnoise by 1 electron (~3.5 μV). The “max 20MHz noise” column is the sine wave amplitude at 20 MHz that increases the readnoise by 1 electron.

Figure 4 shows the suggested wiring of discrete components to the CCD. To the best of our knowledge, none of the parts need be mounted at the CCD within the cryostat.

6 Binning

The serial register can accommodate the binning of three parallel pixels. The summing well can accommodate the binning of three serial pixels.

7 Clocking

7.1 Parallel clocking

Figure 5 shows a parallel clocking sequence. Charge accumulation occurs in the low voltage phase of the gates.

7.2 Serial clocking

Figure 6 shows a serial clocking sequence. Charge accumulation occurs in the low voltage phase of the gates.

8 Modes of operation

Figure 7 shows that the serial register can be read in one of three ways, split read, read left, and read right. Split read is the nominal mode since this minimizes the overall readout time. There is a fourth mode that is sometimes used where all the clock phases are low so that the serial register is a simple conducting channel. This can be used for erase and purge modes described below.

Figure 8 shows readout of the entire CCD. The corresponding clock pairs of V1-3 and FS1-3 are clocked identically, TG broadside loads the serial register, the serial register halves then clock out a lines worth of pixels.

Figure 8 shows readout of the storage region only. V1-3 and FS1-3 are clocked, TG broadside loads the serial register, the serial register halves then clock out a lines worth of pixels.

Figure 9 shows readout of the storage area. The corresponding clock pairs of V1-3 and FS1-3 are clocked, TG broadside load the serial register, the serial register is put in "conducting" mode, H1-3 and SW are in accumulate mode and the RG the reset transistor is turned on with RG.

9 Procedures unique to LBNL CCDs

9.1 Erase Procedure

When CCDs are first turned on or subjected to strong, saturating illumination, residual "ghost" images or high dark current signals are produced. These are caused by the emptying of dielectric interface traps at the Si/SiO2 interface by the excess hole carriers produced by saturation. These traps then refill slowly at the low operating temperature by releasing holes into the wells in a process extending over many hours.
Figure 10.

These effects can be eliminated by an "erase" procedure in which the traps are quickly refilled with electrons. The current recommended procedure is as follows: Lower Vsub to 0 V in a controlled, linear manner. Increase all the parallel clocks to a value high enough to produce inversion, typically 3 – 5 V above barrier phase. After a brief delay (fraction of a second) ramp Vsub back to normal operating voltage. We use a linear ramp rate of about 75 V/s. When Vsub > ~10 V restore the parallel clocks to normal values. Figure 11 shows an example waveform and parallel clocking sequence generated during an erase. Further details are given in the Karcher web page.

9.2 E-Purge Procedure

In CCDs lacking the structure interconnecting the channel stop implants, the individual channel stops become isolated electrically as Vsub is increased. In this case it is possible for the channel stops to be left in different charged states after a low temperature power-up or an erase procedure. The result is that images produced are found to have irregular baselines and a very noisy (fixed pattern) appearance.

This situation can be rectified by the following "e-purge" procedure: During the idle-mode prior to acquisition of an image set all the parallel clocks to a strong accumulation potential of -8 V and hold them there for a fraction of a second before restoring normal operation. During this procedure do NOT ramp or change Vsub. Once this procedure is completed, multiple clean, low-noise images can be acquired. (Note that the e-purge procedure is necessary for the 4k X 4k and 4k X 2k 4-corner readout CCDs but is not needed for other devices which have a mystery structure.)

10 Die parameters

Table 2 and Table 3 list the locations of the center of wirebond pads relative pad VSUB_L2. Table 4 and Table 5 list ideal die corners relative to pad VSUB_L2. Table 6

and Table 7 give the ideal die size. To accommodate dicing tolerances, 75 µm should be added to the overall dimensions.

NB, if wire-bonding to the die, *do not* contact the metal ring adjacent to the VSUB pads; bond to the center of the 100 x 200 µm^2 pads.

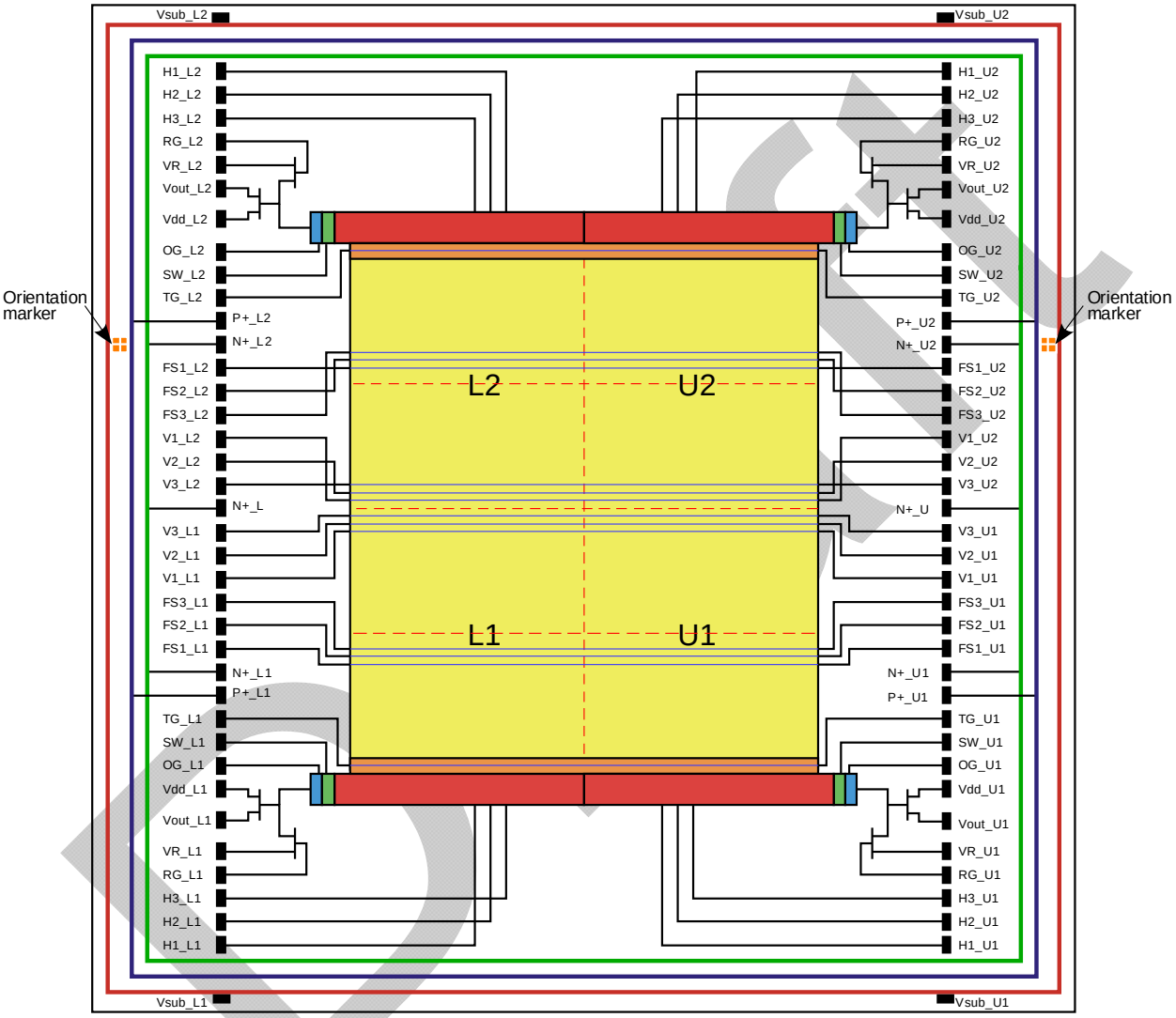

Figure 1. CCD pads and signals. This is a frontside view. Serial channels are continuous and can be read at either end or both. Parallel channels are continuous and can be read at either end or both.

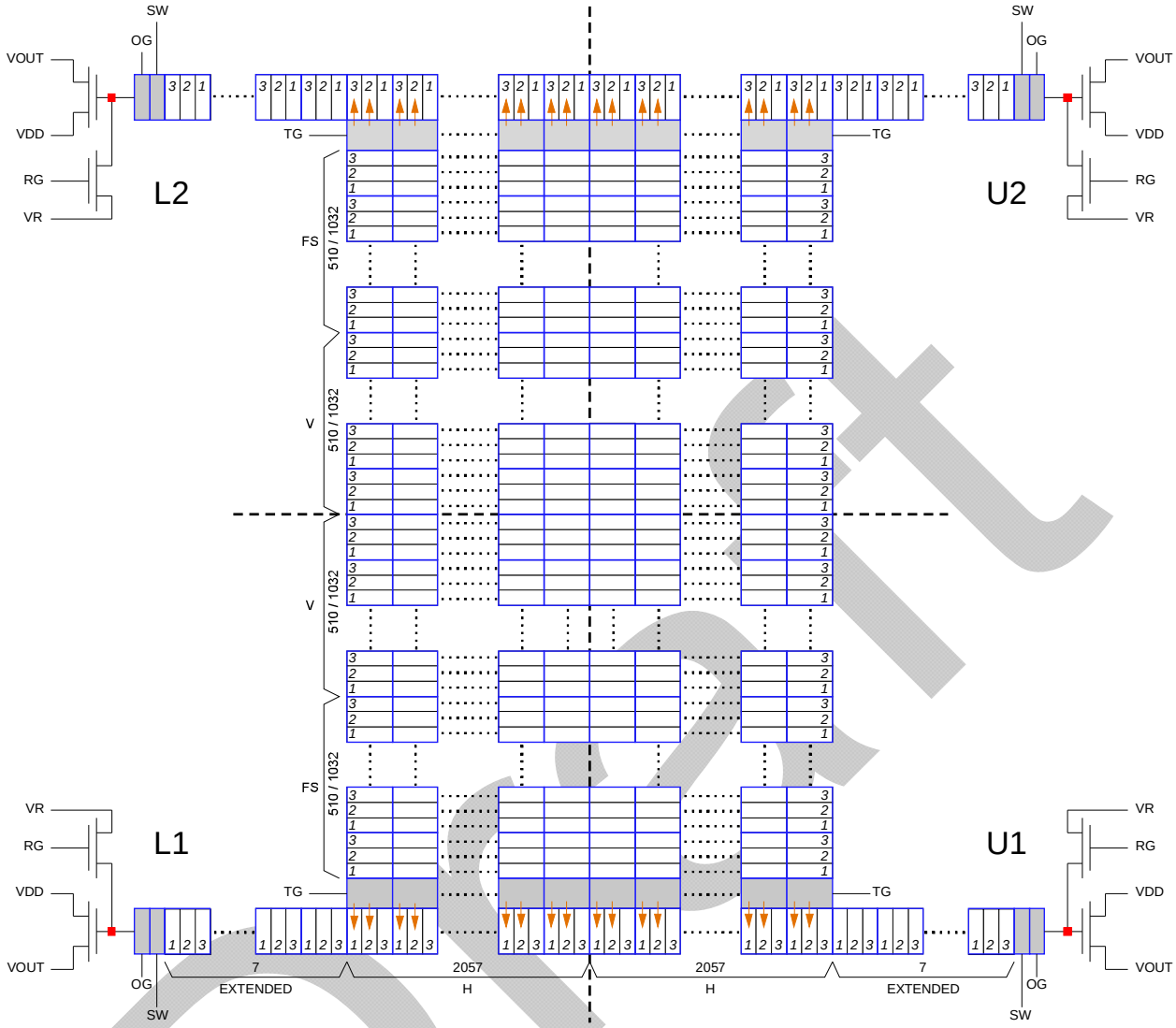

Figure 2. Details of serial and parallel register clock ordering This is a frontside view. Note that the symmetry in the clocking order is diagonal, not left to right.

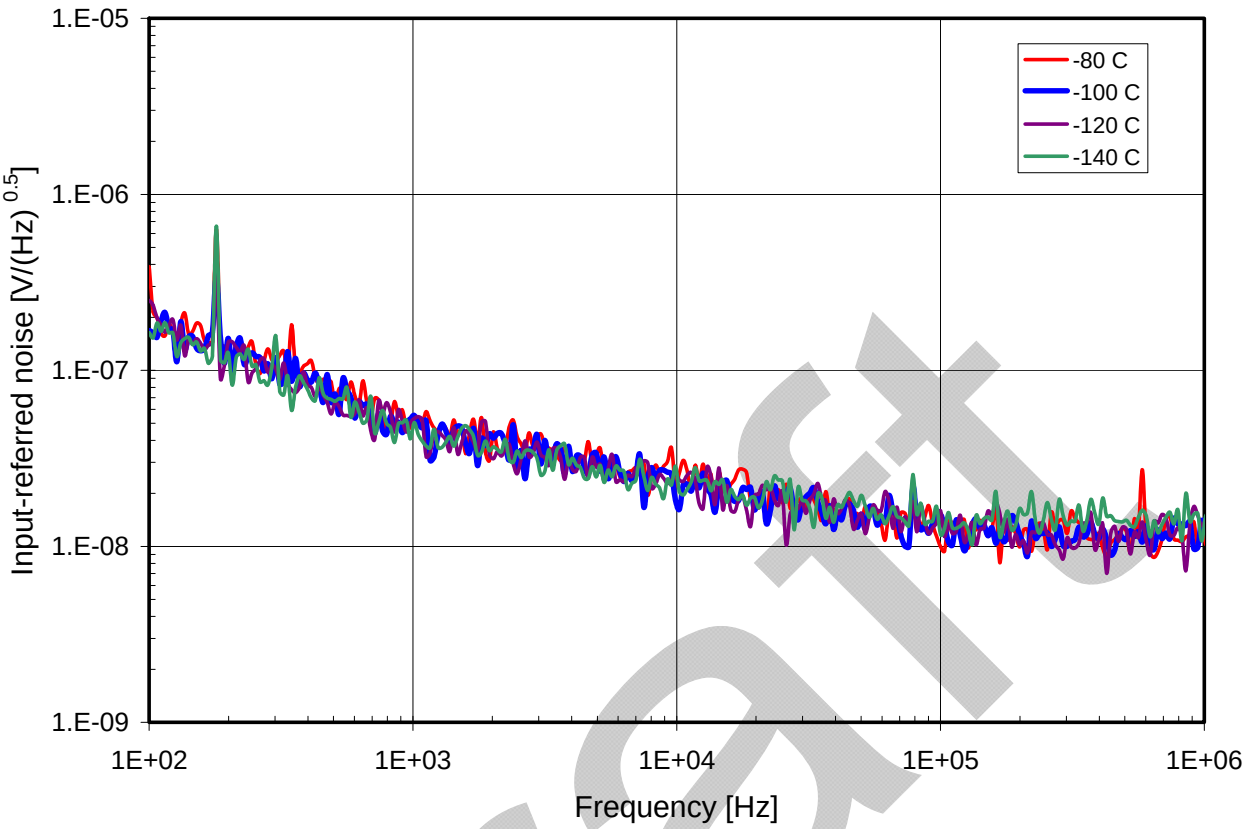

Figure 3. Noise voltage spectra for the output source follower transistor for several temperatures. The transistor was biased at i_{DS} = 600 µA and V_{ds} = 5 V.

Table 1. CCD operating voltages and AC parametersp

Signal	# of copies	Type	Exposure VL	Exposure VH	Readout VL	Readout VH	Erase VL	Erase VH	Purge VL	Purge VH	Adj. Range VL	Adj. Range VH	t width (µsec)	I	max noise (uV)	worst freq (kHz)	max 20MHz noise (mV)
V1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	12
V2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	12
V3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	12
FS1	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	9.5
FS2	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	9.5
FS3	2	ck	-3	5	-3	5	9	9	-9	-9	-5	15	50		70	400	9.5
TG	2	ck	-3	5	-3	5	-4	6	-4	6	-5	10	50		80	700	11
H1	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5		200	100	13
H2	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5		200	100	13
H3	4	ck	-4	6	-4	6	-4	6	-4	6	-5	10	0.5		200	100	13
SW	4	ck	-5	5	-5	5	-5	5	-5	5	-8	8	0.5		250	100	6.2
RG	4	ck	-6	0	-6	0	-6	0	-6	-6	-8	0	0.15		45	100	1.5
OG	4	dc	2.2		2.2		2.2		2.2		0	5			37	150	1.5
VR	4	dc	-12.5		-12.5		-12.5		-12.5		-15	0			420	150	1.5
VDD	4	dc	-22		-22		-22		-22		-25	0		<1 mA	12	150	2.4
VOUT	4	ac															
VSUB	1	dc	+80		+80		0		0		0	100		<1 µA	50	150	2.6
N+	3	float															
P+	1	dc	0		0		0		0		0						

Signal	4kx4k Cap	4kx4k Cap	
V1-V2	65000	65000	nF
V2-V3	65000	65000	nF
V3-V1	65000	65000	nF
FS1-FS2	65000	65000	nF
FS2-F3	65000	65000	nF
FS3-FS1	65000	65000	nF
FS3-TG	300	300	pF

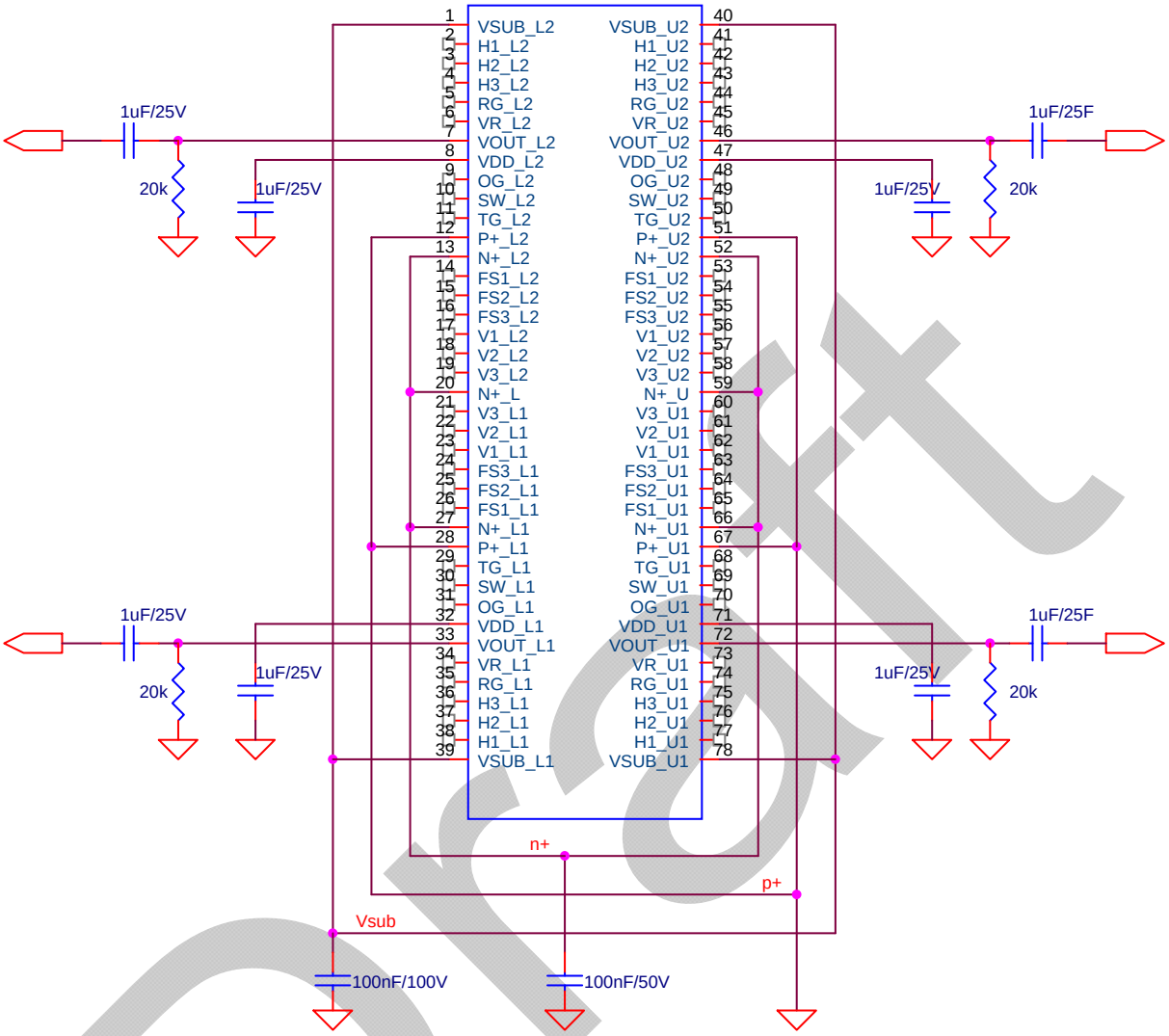

Figure 4. Suggested discrete component wiring to the CCD.

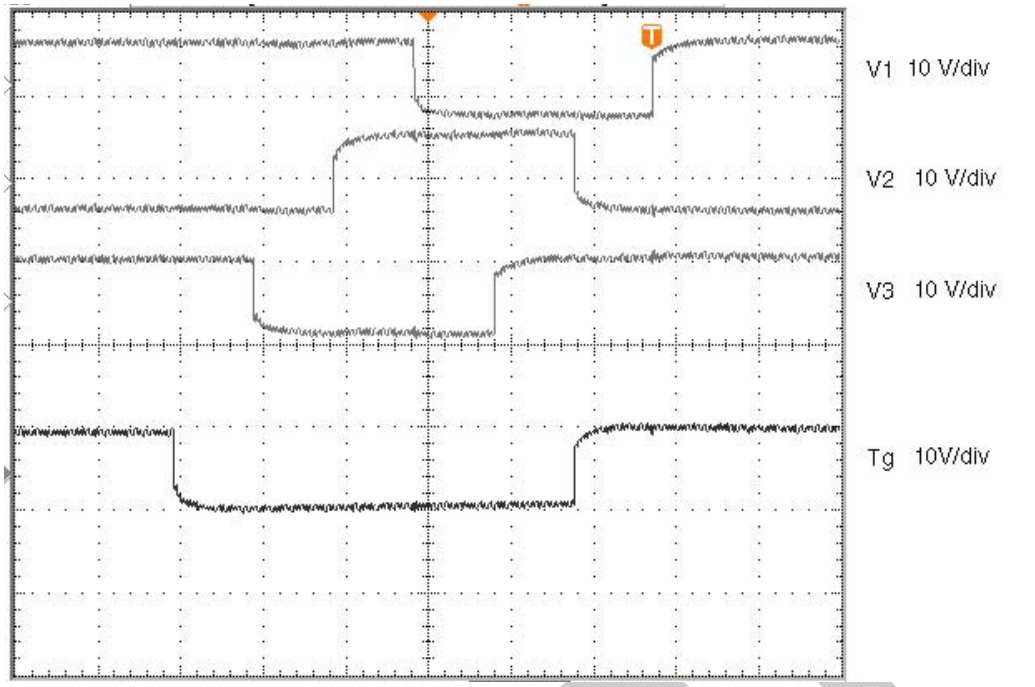

Figure 5. Parallel clocking example. The barrier phase occurs when a clock is high; the accumulation phase occurs when a clock is low.

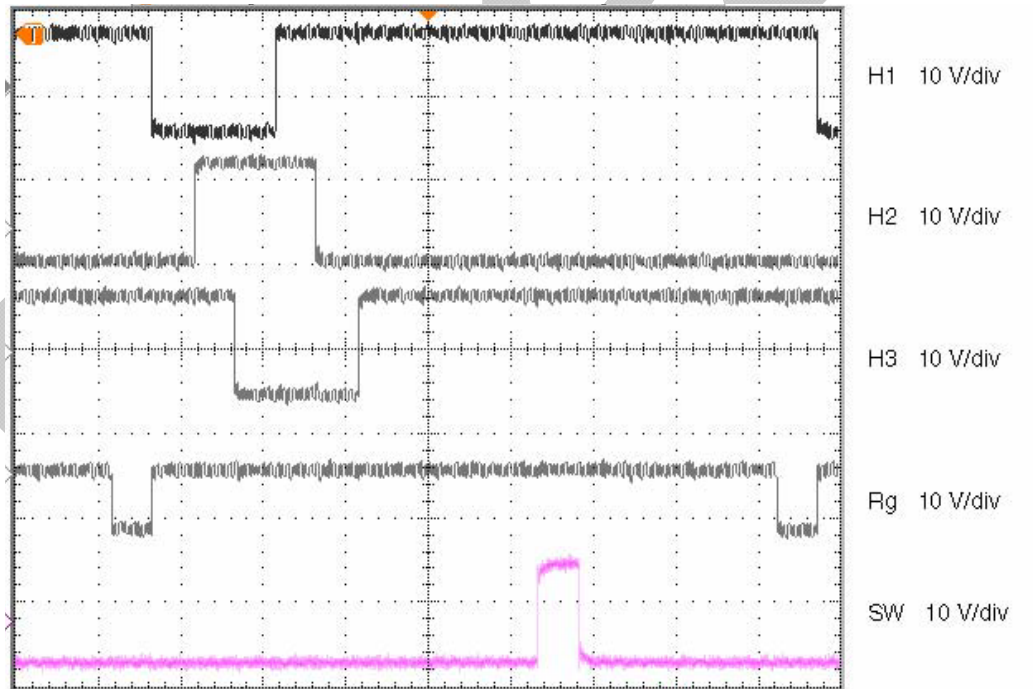

Figure 6. Serial clocking example. The barrier phase occurs when a clock is high; the accumulation phase occurs when a clock is low.

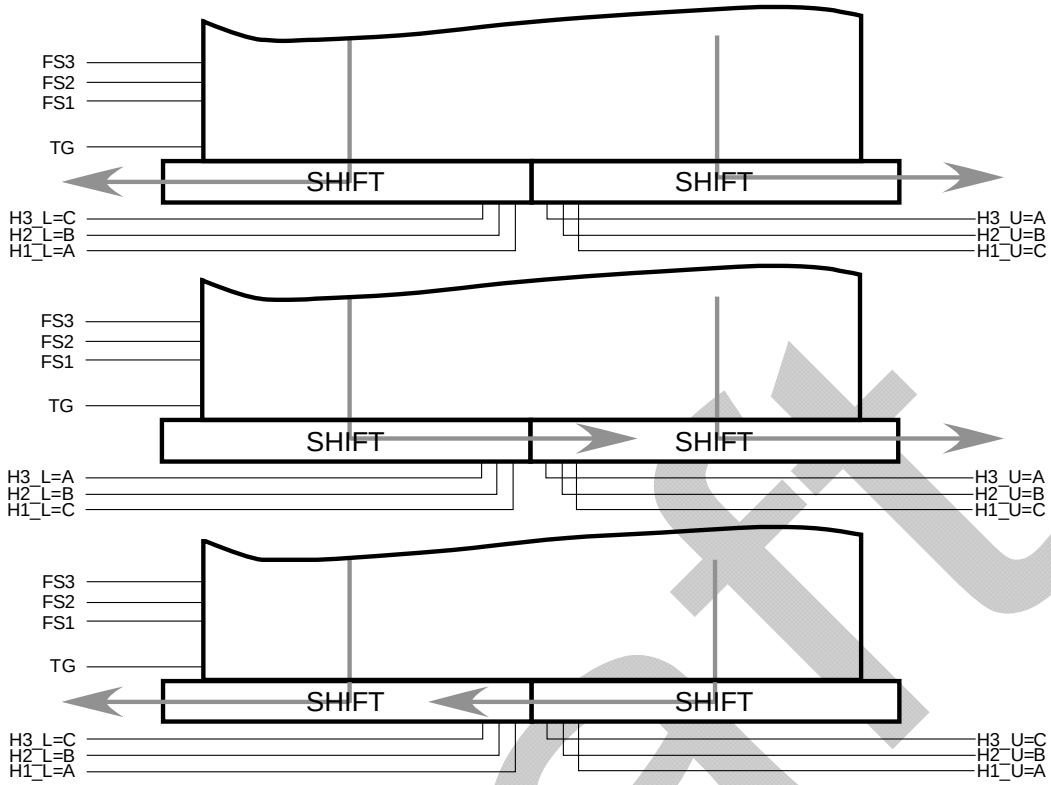

Figure 7. Operating modes of one of the CCD serial registers. Top, the normal of operations is a split read where half of the pixels are shifted to each of the two output structures. Middle, all pixels are shifted to the right output structure. Bottom, all pixels are shifted to the left output structure. The different modes are accomplished by manipulating the first and third clock phases at each end of the serial register.

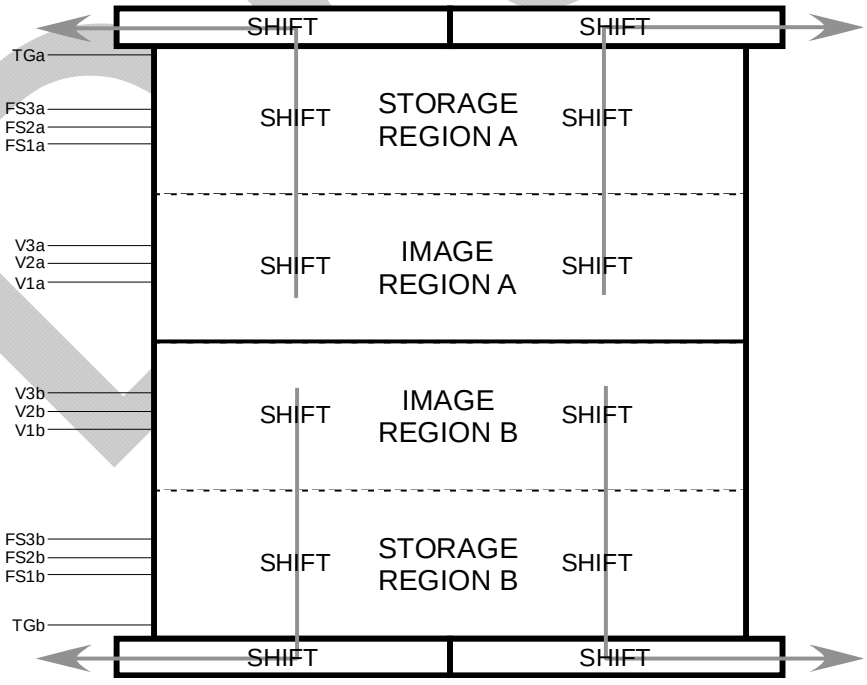

Figure 8. Imager CCD full four corner readout mode. The V and FS clocks are cycled together. The serial register is active between line transfers with reset gate resetting the sense node per pixel.

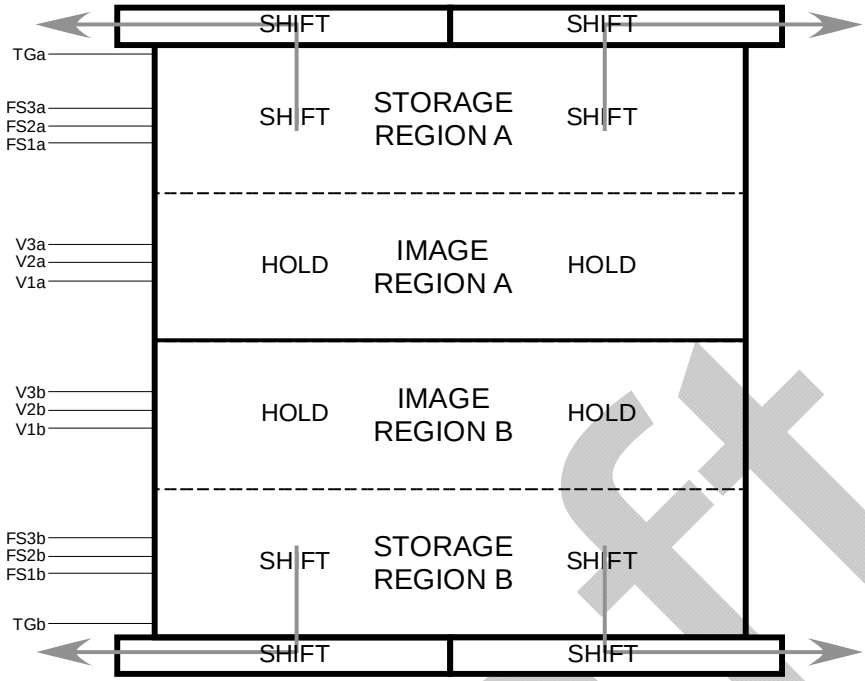

Figure 9. Imager CCD four-corner frame store read out mode. V clocks are quiescent while FS and associated TG transfer lines to the serial register. The serial register operates in standard readout mode.

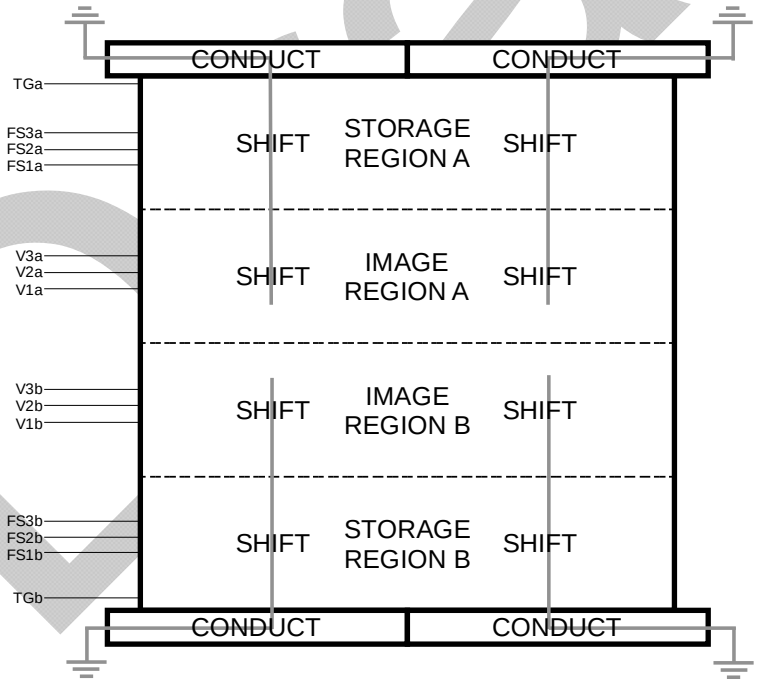

Figure 10. Imager CCD four-corner image area to frame store transfer. The serial register is put into conductive mode where all charge is drained through the reset transistor. V and FS clocks and TG are cycle together.

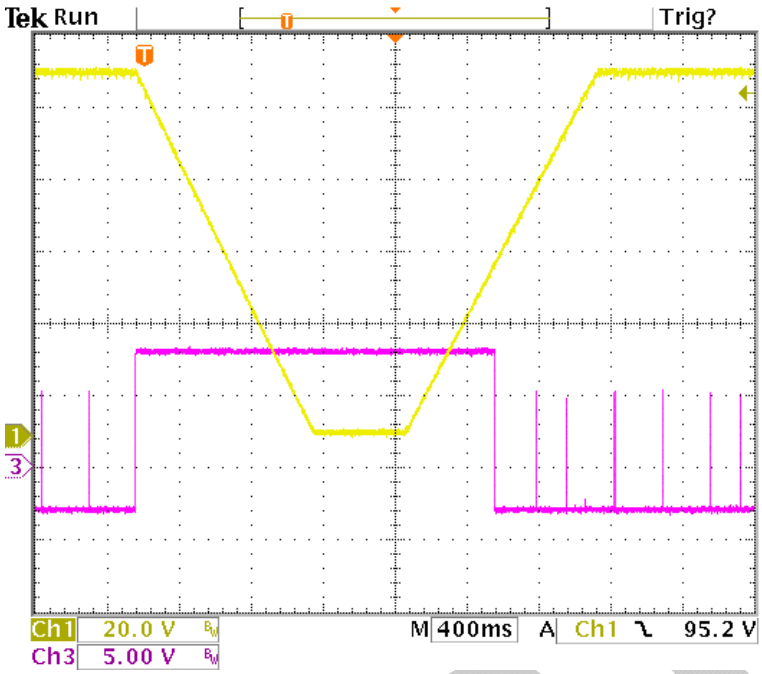

Figure 11. Example waveform illustrating the erase sequence. The yellow trace (a) shows the linear ramping of Vsub and the magenta trace (b) shows one of the parallel clocks changed from normal operation to a constant +8 V during the erase.

Table 2. 4k x 2k pad location relative to VSUB_L2 pad. Units are in mm.

Pad	X	Y
VSUB_L2	0.000	0.000
H1_L2	0.809	0.000
H2_L2	1.209	0.000
H3_L2	1.609	0.000
RG_L2	2.009	0.000
VR_L2	2.409	0.000
VOUT_L2	2.809	0.000
VDD_L2	3.209	0.000
OG_L2	3.609	0.000
SW_L2	4.009	0.000
TG_L2	4.409	0.000
P+_L2	4.809	0.000
N+2_L2	5.209	0.000
FS1_L2	7.970	0.000
FS2_L2	8.370	0.000
FS3_L2	8.770	0.000
V1_L2	14.874	0.000
V2_L2	15.274	0.000
V3_L2	15.674	0.000
N+_L	16.090	0.000
V3_L1	16.505	0.000
V2_L1	16.906	0.000
V1_L1	17.305	0.000
FS3_L1	23.409	0.000
FS2_L1	23.809	0.000
FS1_L1	24.209	0.000
N+2_L1	26.970	0.000
P+_L1	27.370	0.000
TG_L1	27.770	0.000
SW_L1	28.170	0.000
OG_L1	28.570	0.000
VDD_L1	28.970	0.000
VOUT_L1	29.370	0.000
VR_L1	29.770	0.000
RG_L1	30.170	0.000
H3_L1	30.570	0.000
H2_L1	30.970	0.000
H1_L1	31.370	0.000
VSUB_L1	32.179	0.000

Pad	X	Y
VSUB_U2	0.000	62.401
H1_U2	0.809	62.401
H2_U2	1.209	62.401
H3_U2	1.609	62.401
RG_U2	2.009	62.401
VR_U2	2.409	62.401
VOUT_U2	2.809	62.401
VDD_U2	3.209	62.401
OG_U2	3.609	62.401
SW_U2	4.009	62.401
TG_U2	4.409	62.401
P+_U2	4.809	62.401
N+2_U2	5.209	62.401
FS1_U2	7.970	62.401
FS2_U2	8.370	62.401
FS3_U2	8.770	62.401
V1_U2	14.874	62.401
V2_U2	15.274	62.401
V3_U2	15.674	62.401
N+_U2	16.090	62.401
V3_U1	16.505	62.401
V2_U1	16.906	62.401
V1_U1	17.305	62.401
FS3_U1	23.409	62.401
FS2_U1	23.809	62.401
FS1_U1	24.209	62.401
N+2_U1	26.970	62.401
P+_U1	27.370	62.401
TG_U1	27.770	62.401
SW_U1	28.170	62.401
OG_U1	28.570	62.401
VDD_U1	28.970	62.401
VOUT_U1	29.370	62.401
VR_U1	29.770	62.401
RG_U1	30.170	62.401
H3_U1	30.570	62.401
H2_U1	30.970	62.401
H1_U1	31.370	62.401
VSUB_U1	32.179	62.401

Table 3. 4k x 4k pad location relative to VSUB_L2 pad. Units are in mm.

Pad	X	Y	Pad	X	Y
VSUB_L2	0.000	0.000	VSUB_U2	0.000	62.401
H1_L2	0.809	0.000	H1_U2	0.809	62.401
H2_L2	1.209	0.000	H2_U2	1.209	62.401
H3_L2	1.609	0.000	H3_U2	1.609	62.401
RG_L2	2.009	0.000	RG_U2	2.009	62.401
VR_L2	2.409	0.000	VR_U2	2.409	62.401
VOUT_L2	2.809	0.000	VOUT_U2	2.809	62.401
VDD_L2	3.209	0.000	VDD_U2	3.209	62.401
OG_L2	3.609	0.000	OG_U2	3.609	62.401
SW_L2	4.009	0.000	SW_U2	4.009	62.401
TG_L2	4.409	0.000	TG_U2	4.409	62.401
P+_L2	4.809	0.000	P+_U2	4.809	62.401
N+2_L2	5.209	0.000	N+2_U2	5.209	62.401
FS1_L2	15.800	0.000	FS1_U2	15.800	62.401
FS2_L2	16.200	0.000	FS2_U2	16.200	62.401
FS3_L2	16.600	0.000	FS3_U2	16.600	62.401
V1_L2	30.534	0.000	V1_U2	30.534	62.401
V2_L2	30.933	0.000	V2_U2	30.933	62.401
V3_L2	31.334	0.000	V3_U2	31.334	62.401
N+_L	31.750	0.000	N+_U2	31.750	62.401
V3_L1	32.166	0.000	V3_U1	32.166	62.401
V2_L1	32.566	0.000	V2_U1	32.566	62.401
V1_L1	32.965	0.000	V1_U1	32.965	62.401
FS3_L1	46.899	0.000	FS3_U1	46.899	62.401
FS2_L1	47.299	0.000	FS2_U1	47.299	62.401
FS1_L1	47.699	0.000	FS1_U1	47.699	62.401
N+2_L1	58.290	0.000	N+2_U1	58.290	62.401
P+_L1	58.690	0.000	P+_U1	58.690	62.401
TG_L1	59.090	0.000	TG_U1	59.090	62.401
SW_L1	59.490	0.000	SW_U1	59.490	62.401
OG_L1	59.890	0.000	OG_U1	59.890	62.401
VDD_L1	60.290	0.000	VDD_U1	60.290	62.401
VOUT_L1	60.690	0.000	VOUT_U1	60.690	62.401
VR_L1	61.090	0.000	VR_U1	61.090	62.401
RG_L1	61.490	0.000	RG_U1	61.490	62.401
H3_L1	61.890	0.000	H3_U1	61.890	62.401
H2_L1	62.290	0.000	H2_U1	62.290	62.401
H1_L1	62.690	0.000	H1_U1	62.690	62.401
VSUB_L1	63.499	0.000	VSUB_U1	63.499	62.401

Table 4. 4k x 2k die corners relative to center of VSUB_L2 pad. Units are mm.

Corner	X	Y
VSUB_L2	-0.213	-0.946
VSUB_L1	32.392	-0.946
VSUB_U1	32.392	63.346
VSUB_U2	-0.213	63.346

Table 5. 4k x 4k die corners relative to center of VSUB_L2 pad. Units are mm.

Corner	X	Y
VSUB_L2	-0.213	-0.946
VSUB_L1	63.711	-0.946
VSUB_U1	63.711	63.346
VSUB_U2	-0.213	63.346

Table 6. 4k x 2k die dimensions in mm.

Die	X	Y
	32.605	64.292

Table 7. 4k x 4k die dimensions in mm.

Die	X	Y
	63.924	64.292