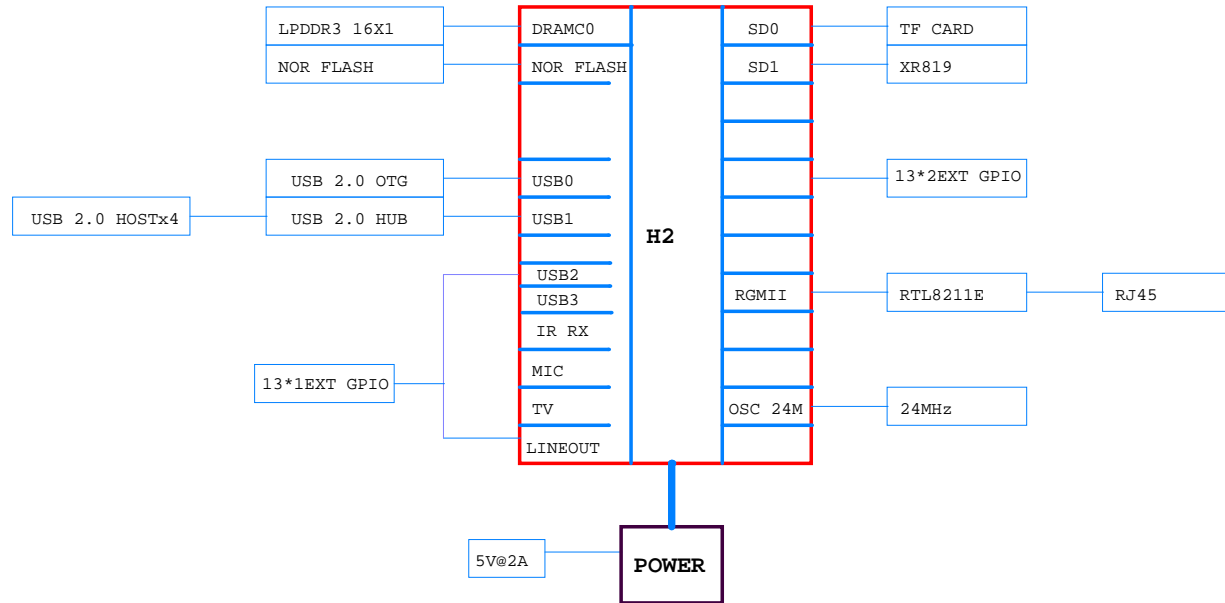


REVISION HISTORY

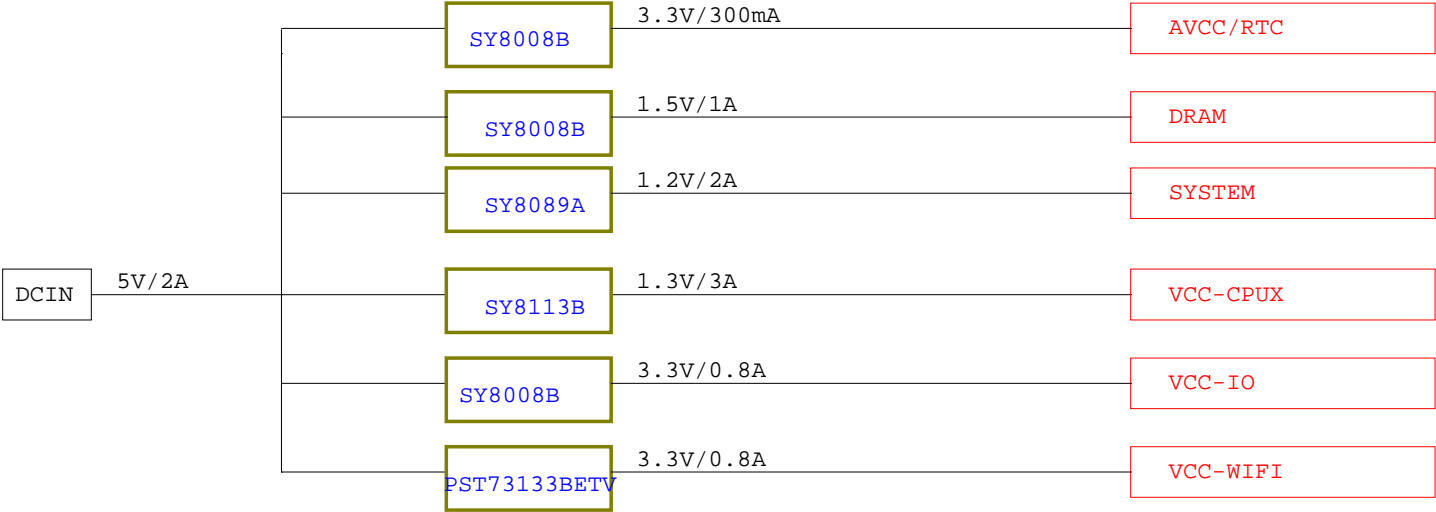
Schematics Index:

Revision	Description	Date	Drawn	Checked
Ver 1.0	Initial	2016-09-05		
1、主控晶振和匹配电容（WIFI）？ 2、POE供电				
Ver 1.1				
1、去掉WIFI部分π型滤波 2、串口调试更改为3pin 3、bom默认无POE供电（需要选择）				

BLOCK



POWER TREE



GPIO ASSIGNMENT

PIN	Define	CFG	Function
PA0	RMS/DRVVBUS0	3/1	JTAG /USB
PA1	TCK/DRVVBUS1	3/1	
PA2	TDO/WPS	3/1	
PA3	TDI	3	UART
PA4	JART-TX	3	
PA5	JART-RX	3	
PA6	NC	7	
PA7	NC	7	
PA8	NC	7	
PA9	NC	7	
PA10	NC	7	
PA11	NC	7	
PA12	NC	7	
PA13	NC	7	
PA14	NC	7	
PA15	STATUS-LED	1	LED
PA16	MUTE	1	AV
PA17	SPDIF-OUT	2	SPDIF
PA18	NC	7	
PA19	NC	7	
PA20	NC	7	
PA21	NC	7	

PIN	Define	CFG	Function
PC0	NWE	2/3	NAND /eMMC /NOR
PC1	NALE	2/3	
PC2	NCLE	2/3	
PC3	NCE1	2/3	
PC4	NCE0	2	
PC5	NRE	2/3	
PC6	NRB0	2/3	
PC7	NRB1	2	
PC8	NDQ0	2/3	
PC9	NDQ1	2/3	
PC10	NDQ2	2/3	
PC11	NDQ3	2/3	
PC12	NDQ4	2/3	
PC13	NDQ5	2/3	
PC14	NDQ6	2/3	
PC15	NDQ7	2/3	
PC16	NDQS	2/3	

PIN	Define	CFG	Function
PD0	NC	7	
PD1	NC	7	
PD2	NC	7	
PD3	NC	7	
PD4	NC	7	
PD5	NC	7	
PD6	NC	7	
PD7	NC	7	
PD8	NC	7	
PD9	NC	7	
PD10	NC	7	
PD11	NC	7	
PD12	NC	7	
PD13	NC	7	
PD14	NC	7	
PD15	NC	7	
PD16	NC	7	
PD17	NC	7	

PIN	Define	CFG	Function
PE0	NC	7	
PE1	NC	7	
PE2	NC	7	
PE3	NC	7	
PE4	NC	7	
PE5	NC	7	
PE6	NC	7	
PE7	NC	7	
PE8	NC	7	
PE9	NC	7	
PE10	NC	7	
PE11	NC	7	
PE12	NC	7	
PE13	NC	7	
PE14	NC	7	
PE15	NC	7	

PIN	Define	CFG	Function
PF0	D1	2	CARD0
PF1	D0	2	
PF2	CLK	2	
PF3	CMD	2	
PF4	D3	2	
PF5	D2	2	
PF6	DET	0	

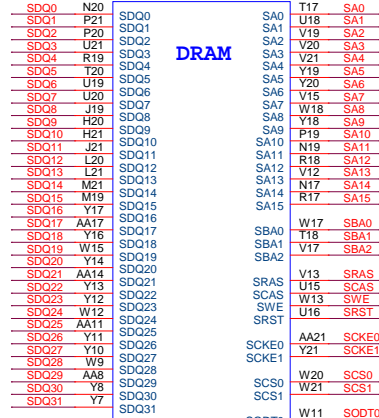
PIN	Define	CFG	Function
PG0	NC	7	
PG1	NC	7	
PG2	NC	7	
PG3	NC	7	
PG4	NC	7	
PG5	NC	7	
PG6	NC	7	
PG7	NC	7	
PG8	NC	7	
PG9	NC	7	
PG10	NC	7	
PG11	NC	7	
PG12	NC	7	
PG13	NC	7	

PIN	Define	CFG	Function
PL0	TWI	2	TWI
PL1	TWI	2	
PL2	USB0-DRVVBUS	1	USB
PL3	USB1-DRVVBUS	1	
PL4	RECOVERY	0	KEY
PL5	VCC-IO-EN	1	IO-EN
PL6	NC	7	WIFI-EN
PL7	WIFI-EN	7	
PL8	PWR-STB	1	
PL9	PWR-DRAM	1	
PL10	PWR-LED	1	
PL11	IR-RX	2	

DDR3 16x2

U1A

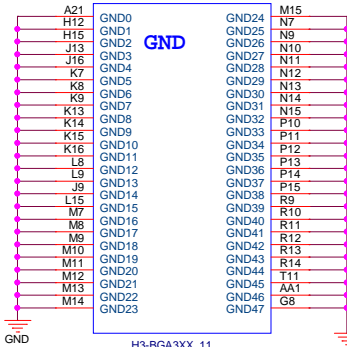
DRAM



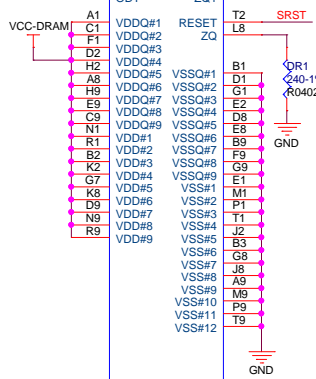
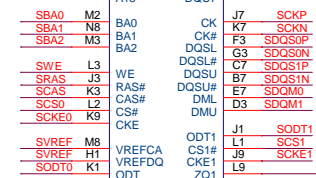
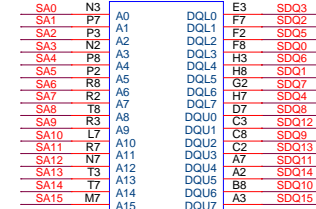
H3-BGA3XX_11

U11

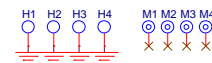
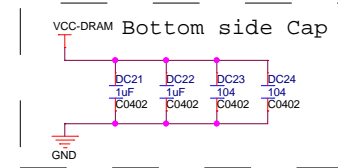
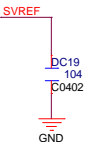
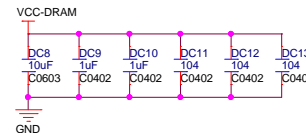
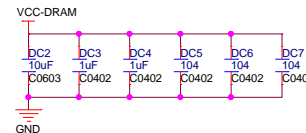
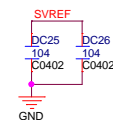
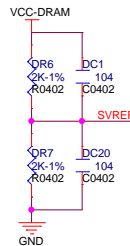
GND



H3-BGA3XX_11



DU1
DDR3-FBGA96
FBGA96C80P9X13



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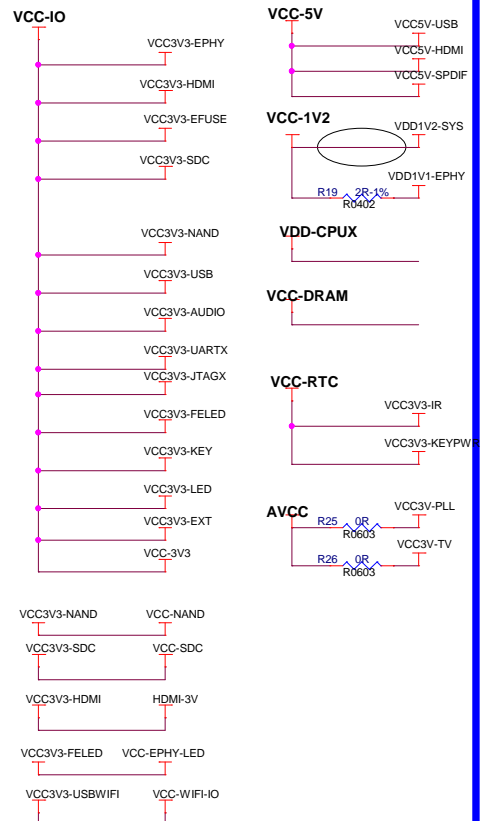
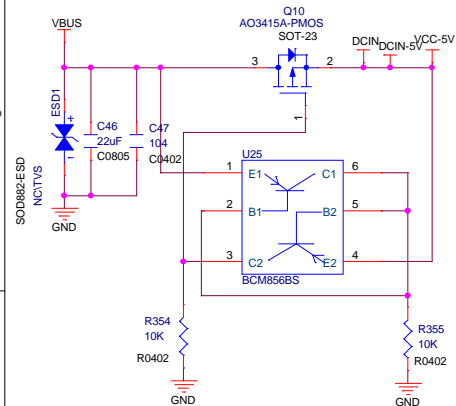
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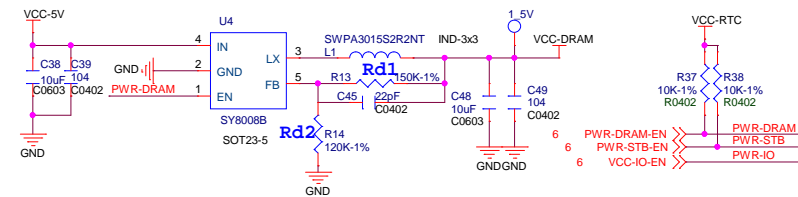
	PWRON/WORK	STANDBY	PWROFF
PWR-STB	1	0	0
PWR-DRAM	1	1	0

DCIN

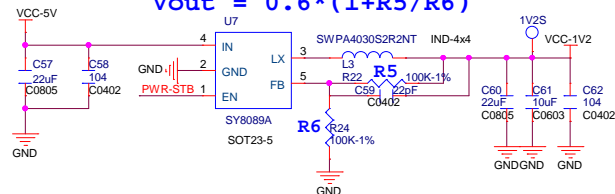


POWER

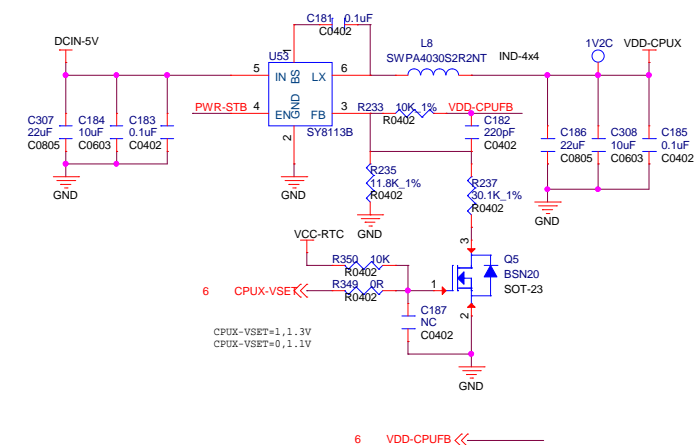
Vout = 0.6*(1+Rd1/Rd2)
VDRAM=1.5V/1A,R2=100K-1%
VDRAM=1.35V/1A,R2=120K-1%



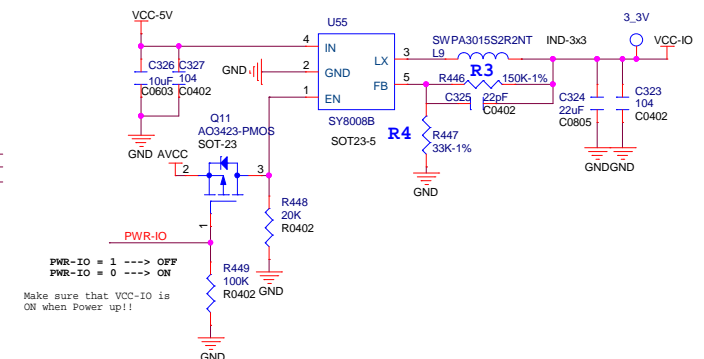
SYSTEM 1.2V/2A
Vout = $0.6 \cdot (1 + R5/R6)$



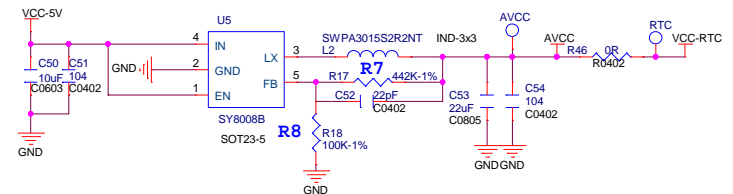
CPUX 1.1V/1.3V/3A
 $V_{out} = 0.6 * (1 + R1/R2)$



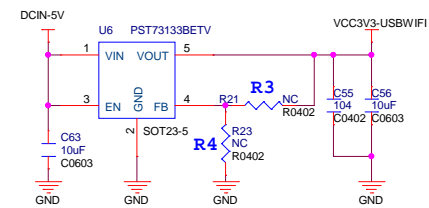
VCCIO 3.3V/1A



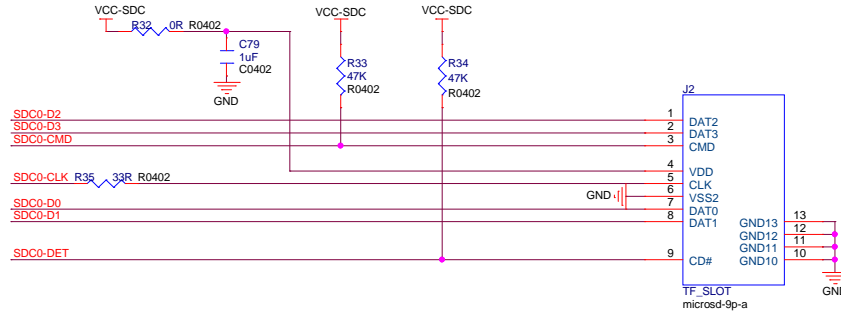
AVCC 3.3V/1A



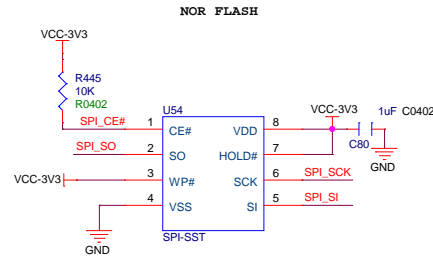
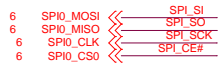
WIFI Power 3.3V/300mA



eMMC



NOR FLASH



USB

5

4

3

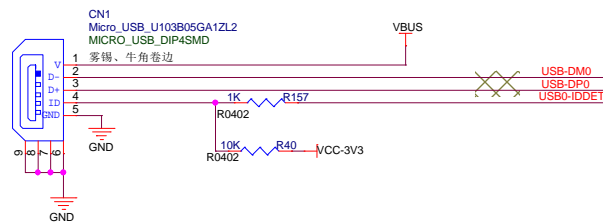
2

1

D

D

6 USB-DM0
6 USB-DP0
6 USB0-IDDET
6 USB0-DRVVBUS

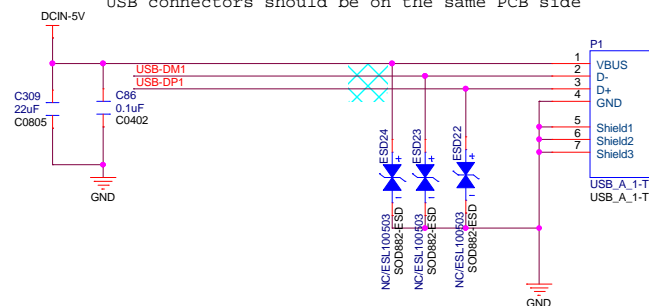


C

C

6 USB-DM1
6 USB-DP1
6 USB-DM1
6 USB-DP1

note: Make sure the routing between the ESD and the USB connectors should be on the same PCB side



B

B

A

A

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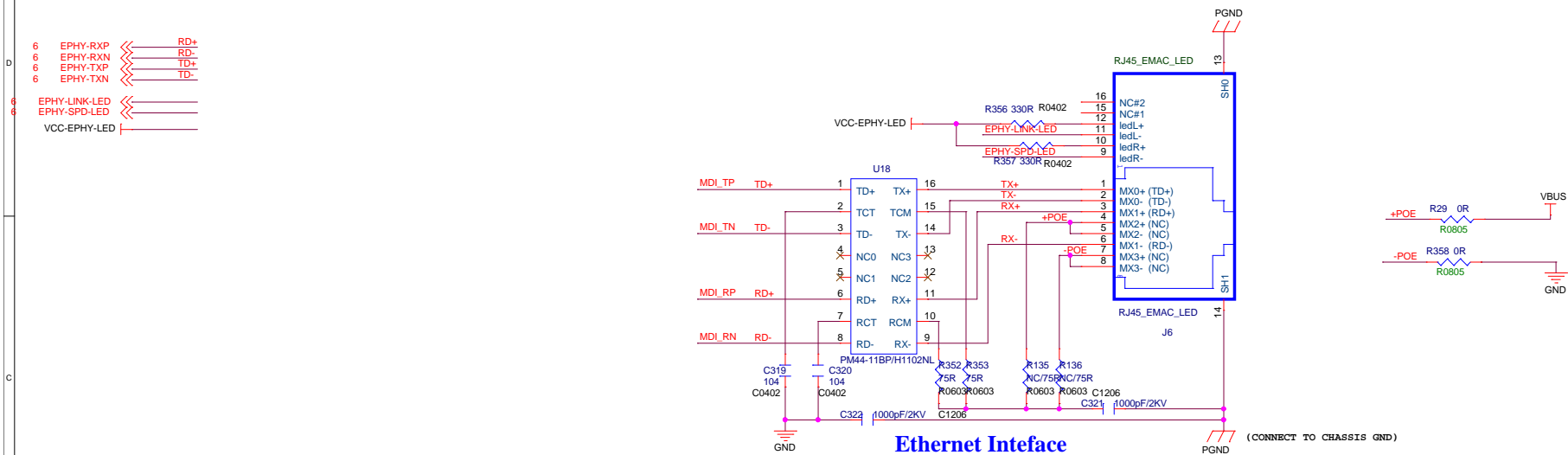
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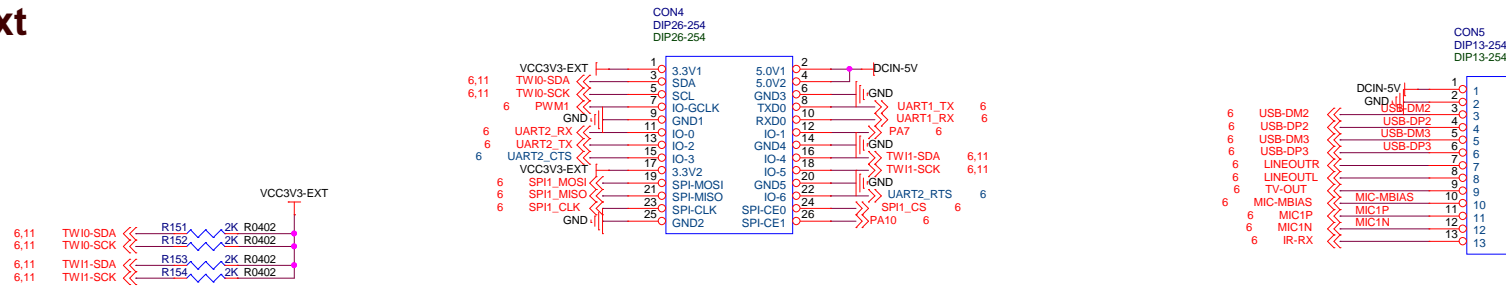
EMAC



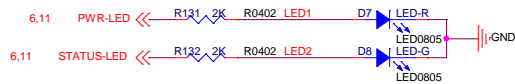
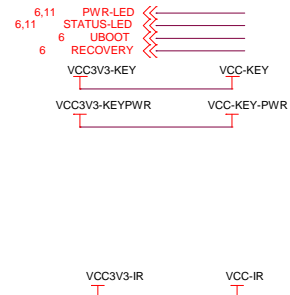
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Ext Port

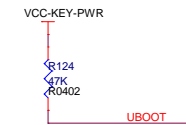
Ext



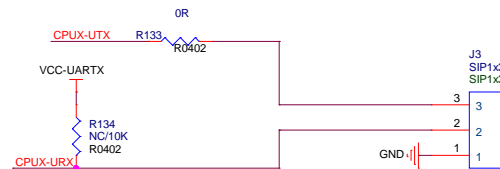
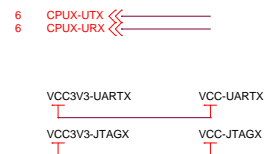
LED



KEY

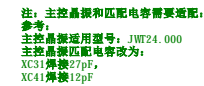


DEBUG



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