Stewart Dulaney CS 40 Section 4104 SID: 1545566

Assignment 1.5a

Problem 1.1	Fetch stage			Execute stage			
	Memory	CPU Regi	isters	Memory	CPU Register	15	
	300 300	5 300	PC	300 3005	301 PC		
	301 594		AC	301 5 9 40	7 0003 A	14	
	302 700	6 300	5 IR	302 7006	3005 I	R	
	Devices : Devices						
	940 000	2 005 000	3	940 0002	005 0003		
	941	006		941	006		
	Step 1 Step 2						
	Memory	CPU Regi	sters	Memory	CPU Registers		
	300 300	5 301	PC	300 3005	302 PC		
	301 5 9 4	0 000	3 AC	301 5940	0005 A	c	
	302 7 0 0	6 591	10 12	302 7006	5940 II	R	
	:	Device	c S	;	\$ 5940 II	1	
	940 000	2 005 000	03	940 0002			
	941	006		941	000		
	Step 3 Step 4						
	Memory	CPU Registe	ess	Memory	CPU Rgisters		
	300 3005	302 P	4 3	00 3005	303 PC		
	301 5940	0005	AC 3	501 5940	10005 A		
	302 7006	7006	IR 3	302 7006	7006 I	R	
	Devices			: Devices			
	940 0002	005 0003	3	2000 040	005 0003		
	941	006	a	941	006 0005		
	Step 5		1	Step 6			
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