Application Report
– Feb 2012

Memory Map in DM81xx DVR RDK

Video Surveillance Applications

The document discusses about the memory map implementation in DM816x and DM814x DVRRDK. DVRRDK allows different usecases for different platforms and hence a generic memory map might not be sufficient for all users. This document gives insight on different sections of the memory map that a user can change for their usecases.
It is expected that the user has gone through the DM81xx SoC architecture and MultiChannel FrameWork UserGuide to understand the hardware and software architecture/partitioning.

1. Memory Sections in DVRRDK Memory Map

DVRRDK has multiple memory map configurations supported based on the usage scenarios and available total memory on the platform. The total system memory is divided into various sub-systems/processors. The broad classification of the sections is listed below:

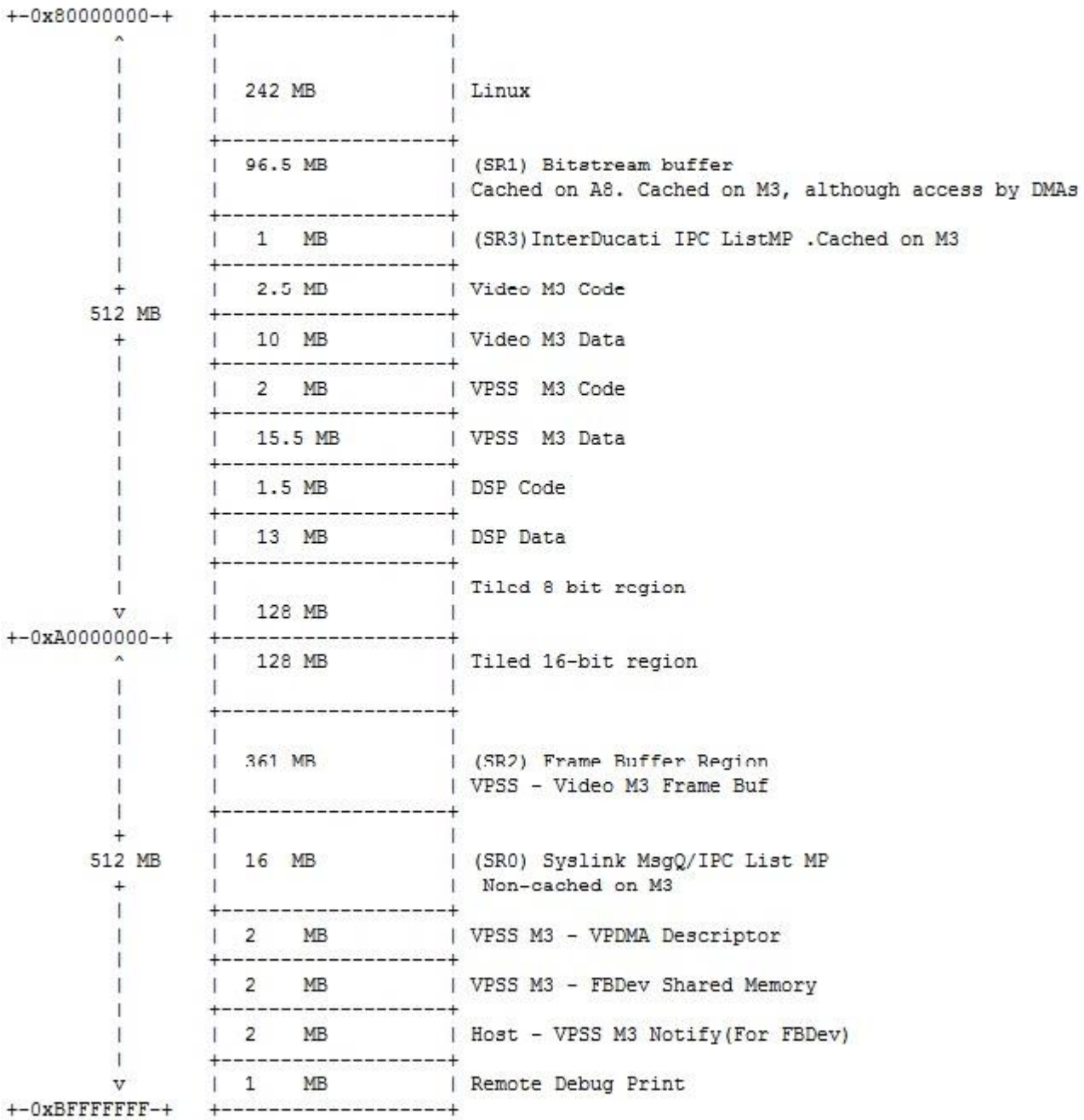
- **Linux Memory** – Single memory partition given to linux kernel memory manager
- **Shared Regions** – Different memory partitions that are shared across processors
  - **Bitstream Buffer (SR1)** – Shared Region 1. This shared region is meant to receive encoded bitstream from Video M3 processor to A8 processor, send bitstream from A8 to Video M3 for decoding and for sharing the buffers between A8 and DSP for Scene Change Detection algorithm results. This region is cached on A8.
  - **Frame Buffer (SR2)** – Shared Region 2. This shared region is used for allocating frame buffers for capturing video data, deinterlacing, scaling, displaying video frames. The shared region is accessible from A8, Video M3, VPSS M3 and DSP. **This is non-tiled region.**
  - **IPC MessageQ / ListMP (SR0) –** Shared Region 0. This shared region is used to allocate memory for datastructures needed for interprocessor communication. This shared region is not cached on any of the processor cores.
  - **IPC ListMP for M3 (InterDucati) (SR3) –** Shared Region 3. This shared region is currently not used but has been left in the memory map so that it can easily be used for M3-only IPC usage.
- **Slave Code and Data Section Memory**
  - **Video M3 Data Section** – Partition for data section of Video M3 executable binary

    - **Video M3 Code Section** – Partition for code section of Video M3 executable binary
    - **VPSS M3 Data Section** – Partition for data section of VPSS M3 executable binary
    - **VPSS M3 Code Section** – Partition for code section of VPSS M3 executable binary
    - **DSP Data Section** – Partition for data section of DSP executable binary
    - **DSP Code Section** – Partition for code section of DSP executable binary
- **Remote Debug Memory** – Memory section reserved and accessible from all processor cores to dump the debug print messages. Each processor core uses VPS_printf() to dump the debug messages on this memory region. Remote Debug Client running on A8 reads this memory region and prints the content on the (UART) console.
- **VPDMA Descriptors Memory** – Memory section used by VPSS M3 processor core. It is used by HDVPSS driver for its internal descriptor data structure.
- **Host VPSS Notify Shared Memory –** Memory section used by VPSS M3 processor core. It is used by HDVPSS driver for FBDev commands from A8 to M3. The base address of this section is used in the boot arguments under the name "`notifyk.vpssm3_sva`". This information is used by linux kernel for the FBDev driver.
- **FBDev Shared Memory –** Memory section for FBDev drivers on VPSS M3
- **Tiler Memory Region –** This is the memory region on the system memory that can have a Tiled view from different masters (like HDVPSS, HDVICP). Tiler region is divided into two regions – 8-bit Tiled region and 16-bit Tiled region. **If the tiler usage is disabled in the McFW, the memory allocator uses this region as extension of frame buffer region.** Tiler base address has to be 128MB aligned.

2. Memory Map Table on DM8168

2.1 System Memory – 1GB, Linux Memory – 256 MB (Default Memory Map Configuration)

Memory Map - 1GB DDR, upto 256MB DDR.



In the above memory map, the linux memory is configured to be 242MB, hence when using this default memory map, user need to set "`mem=242M`" in the boot arguments.

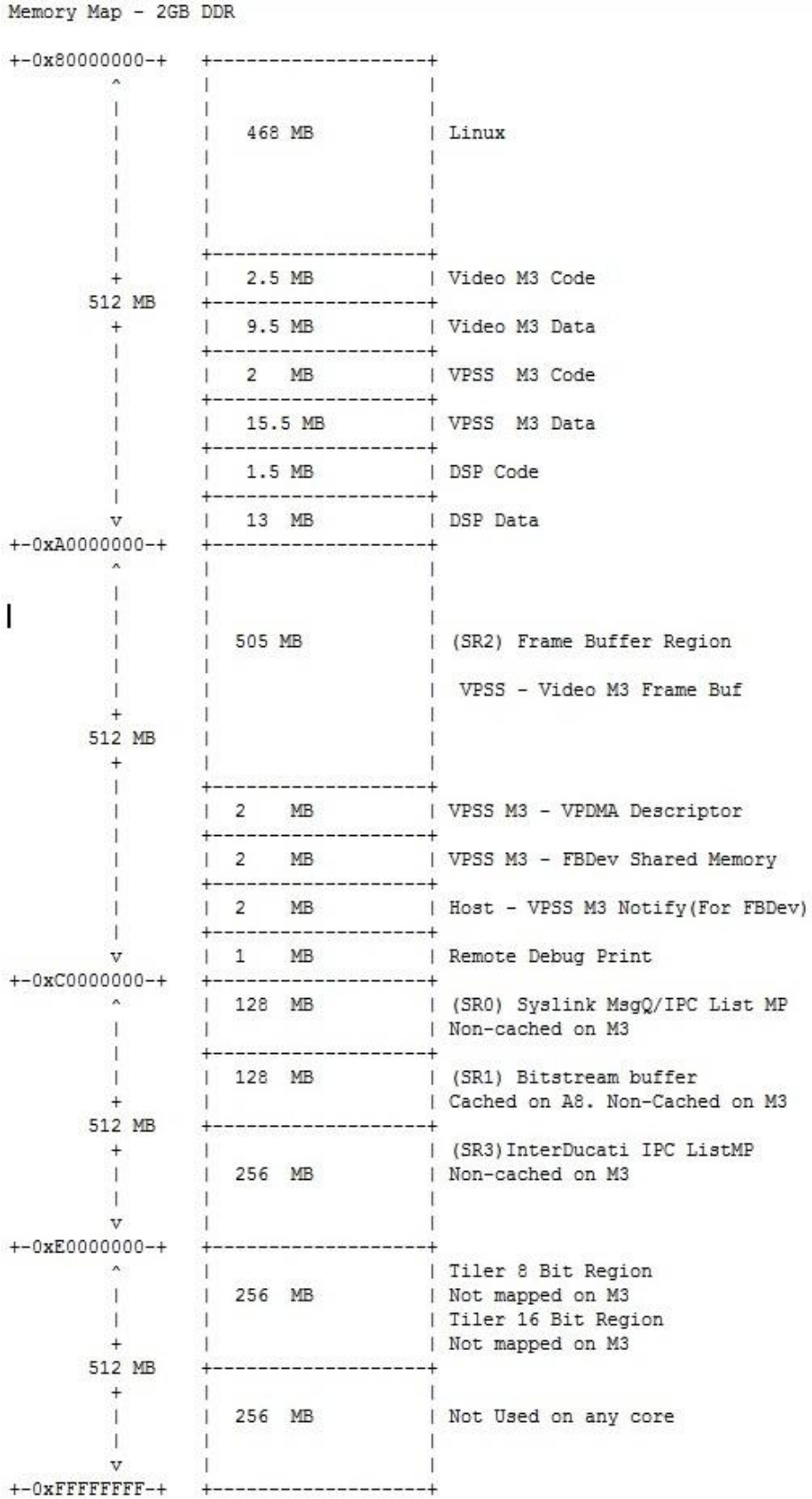
2.2 System Memory – 1GB, Linux Memory – 128 MB

```
Memory Map - 1GB DDR, upto 128MB DDR.


+-0x80000000-+   +--------------------+
             ^   |                    |
             |   |                    |
             |   |  116 MB            | Linux
             |   |                    |
             |   +--------------------+
             |   |  97   MB           | (SR1) Bitstream buffer
             |   |                    | Cached on A8. Cached on M3, although access by DMAs
             |   +--------------------+
             |   |   0.5 MB           | (SR3)InterDucati IPC ListMP .Cached on M3
             |   +--------------------+
             +   |   2.5 MB           | Video M3 Code
           512 MB+--------------------+
             +   |   9.5 MB           | Video M3 Data
             |   +--------------------+
             |   |   2   MB           | VPSS  M3 Code
             |   +--------------------+
             |   |   14.5 MB          | VPSS  M3 Data
             |   +--------------------+
             |   |   1   MB           | DSP Code
             |   +--------------------+
             |   |   13  MB           | DSP Data
             |   +--------------------+
             |   |                    | Tiled 8-bit region
             |   |   128 MB           |
             |   +--------------------+
             |   |   128 MB           | Tiled 16-bit region
             v   |                    |
+-0xA0000000-+   +--------------------+
             ^   |                    |
             |   |  489 MB            | (SR2) Frame Buffer Region
             |   |                    | VPSS - Video M3 Frame Buf
             |   |                    |
             |   +--------------------+
             |   |  16  MB            | (SR0) Syslink MsgQ/IPC List MP
             +   |                    |  Non-cached on M3
           512 MB+--------------------+
             |   |  2    MB           | VPSS M3 - VPDMA Descriptor
             |   +--------------------+
             |   |  2    MB           | VPSS M3 - FBDev Shared Memory
             |   +--------------------+
             |   |  2    MB           | Host - VPSS M3 Notify(For FBDev)
             |   +--------------------+
             v   |  1    MB           | Remote Debug Print
+-0xBFFFFFFF-+   +--------------------+
```

In the above memory map, the linux memory is configured to be 116MB, hence when using this default memory map, user need to set "`mem=116M`" in the boot arguments.

2.3 System Memory – 2GB, Linux Memory – less than 512 MB



3. Memory Map Table on DM814x

```
Memory Map - 512MB DDR

+--------------+
| 128MB        | Linux
|              |
|              |
+--------------+
| 46MB         | (SR1) Bitstream buffer (Cached)
|              |
+--------------+
| 2.5MB        | Video M3 code
+--------------+
| 17.5MB       | Video M3 data
+--------------+
| 2MB          | VPSS / DSS M3 code
+--------------+
| 14MB         | VPSS / DSS M3 data
+--------------+
| 2MB          | DSP code
+--------------+
| 14MB         | DSP data
+--------------+
| 96MB         | Tiler buffer
|              |
+--------------+
| 142MB        | SR(2) Frame buffer
|              |
|              |
|              | VPSS-VID M3 Frame buffer
|              |
|              |
|              |
|              |
|              |
+--------------+
| 4MB          | (SR0) Syslink MsgQ / IPC List MP (Non-cached)
+--------------+
| 2MB          | VPSS M3 - VPDMA descriptor
+--------------+
| 2MB          | VPSS M3 - FBDev
+--------------+
| 2MB          | Host - VPSS M3 Notify (for FBDev)
+--------------+
| 1MB          | Remote Printf
+--------------+
```

4. Software and Hardware Constraints To Consider For Deciding Memory Map

4.1 Hardware Constraints

- Video M3 and VPSS M3 cannot access any program memory above 0xA00000
- Video M3 and VPSS M3 cannot access any data memory above 0xE0000000
- AMMU in Video M3 and VPSS M3 handles large memory segments of size 512MB/32MB only and there can be 4 such segments. As one of the 512MB address range is used to access memory mapped registers, only 3 regions can be used to access DDR.

4.2 Software Constraints

- Current system allows 1GB of kernel virtual memory and 3 GB of userspace virtual memory split for linux. This means kernel can map a maximum of 1GB memory. This includes the memory in the boot arguments and any further mapping done for the shared regions.
- Current system does not use the feature of memory hole for system RAM. It can be enhanced and would be available in later releases. Users trying to change the linux memory configuration can refer to http://processors.wiki.ti.com/index.php/DM816x_AM389x_PSP_User_Guide#Setting_Memory_Holes_For_System_RAM
- The shared regions are statically defined in the build configuration. Any change in the build configuration needs to be done before re-compiling the source code.
- Frame Buffer Shared Region (SR2) is not mapped on A8 as it would take up lot of kernel virtual memory. User need to mmap the physical address in the application code to map the SR2 buffers on A8. This is needed for getting the frame buffers on A8 using IPCFramesOut/In link.
- Due to increased size of the bitstream buffers and other sections between 0x80000000 – 0xA00000, the size of available linux memory is reduced from 256MB or 128MB in the respective configurations of DM8168.

5. How To – Modify the Memory Map

The memory map of complete DVRRDK is controlled in **<DVR_RDK>/dvr_rdk/mcfw/src_bios6/cfg/ti81<x>x/config_<xxxx>.bld**

In this build configuration file, size of each section can be reconfigured. For example, in `config_1G_256M.bld`, DSP code size and DSP data size section can be changed by modifying the following entries.

```
DSP_CODE_SIZE              = 1*MB + 1*MB/2;
DSP_DATA_SIZE              = 13*MB;
```

The base addresses of each section are incremented based on the base address of previous section and the size of the previous section. For example, if sections are created in the numerical order, base address of Section 2 is calculated as below:

<Start Addr of Sect 2> = <Start Addr of Sec 1> + <Size of Sect 1>

To modify the memory map, user needs to consider the following:

- Refer to the hardware limitations and software limitations in section 4.
  - This means Video M3 and VPSS M3 code has to reside in the first 512MB of the physical DDR memory. We assume one-to-one mapping of AMMU virtual address to physical address.
- A section of minimum 2MB need to be reserved for Syslink-Notify support in linux kernel. Linux kernel uses this memory to communicate with VPSS M3 in DVR RDK. Any

change in address for this section requires an update of bootargs for "**notifyk.vpssm3_sva**" boot parameter

- The other sections like "Remote Debug", "HDVPSS Shared Memory" are read directly from the build configuration file and updated in **<DVR_RDK>/dvr_rdk/bin/ti81<x>x/env.sh**
- Change in the linux memory size in build configuration file has to be reflected in the boot arguments of the linux kernel using "mem=<SIZE>M" entry.
- Tiler address has to start with 128MB alignment.
- Consider the overall buffer requirement for the specific usecase before modifying the Frame Buffer or BitsBuffer section sizes. The details of memory requirement for each usecase are available in **<DVR_RDK>/dvr_rdk/docs/RDK_MemAnalysis.xls**

5.1 How To – Change Memory Section Sizes for Additional Linux Memory

The current default memory map on DM814x (512MB physical memory and 128MB Linux memory) is optimized for the memory buffers required for 4D1 or 8CIF or 16CIF DVR implementations.
Similarly, the current default memory map on DM8168 (1GB physical memory and 242MB Linux memory) is optimized for the memory buffers required for 16D1 DVR implementations. (Refer to the specification of each usecase in **<DVR_RDK>/dvr_rdk/docs/usecases/)**

If user wants to increase the linux memory further, there are a few options available. For example on DM8168, user can

- Move the DSP code and data section to lower 512MB region (after 0xA0000000), still ensuring the Tiler 16-bit section start address is not modified (due to 128MB alignment constraint).
  - Reduce either the frame buffer region (SR2) or SR0 or both, to accommodate the DSP Code and Data section
- Reduce the BitsBuffer Shared Region(SR1) if the bitrate for each channel is known to be low. Current system allocates each buffer of WIDTHxHEIGHT for each encoded frame, which might not be needed by the encoder if the bitrate is low enough. This size can be changed in the following macro in **<DVR_RDK>/dvr_rdk/mcfw/src_bios6/links_m3video/codec_utils/utils_encdec.h**

```
/** @enum UTILS_ENCDEC_GET_BITBUF_SIZE
 *  @brief Macro that returns max size of encoded bitbuffer for a given
resolution
 */
#define UTILS_ENCDEC_GET_BITBUF_SIZE(width,height,bitrate,framerate)
\
                    ((width) * (height))
```

Note: If the encoder returns the bitstream size bigger than the allocated buffer size, then encoder link would return error.

If user wants to increase the linux memory in 2GB physical memory system on DM8168, there are a few options available.

- User can have two memory sections for linux memory. The steps to modify the boot arguments are listed in http://processors.wiki.ti.com/index.php/DM816x_AM389x_PSP_User_Guide#Setting_Memory_Holes_For_System_RAM
  - The last 256MB starting at 0xF0000000 can be used for second memory section for linux kernel. **The constraint is that linux has only 1GB of the kernel virtual space.**